WP11.2
28 nm update from CPPM

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3st AIDAinnova annual meeting
WP11.2 : Exploratory study of advanced CMOS (28 nm)
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Outline

- Introduction : the context of the activity
- 28 nm chip design
- Analog FE pixel simulations
- Preliminary test results
- Current status and perspectives

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Introduction

R&D around **hybrid pixels** for **future upgrades and future colliders** with the 28nm CMOS technology

- The **radiation tolerance** of the 28nm process up to 1-2 Grad
- **Time measurement** with a resolution better than 50ps
- Small pixel size -> **25µm × 25µm**

Context

- RD53 collaboration shows a strong interest in these developments for the future upgrades of ATLAS and CMS trackers
- The project is part of the R&D project DEPHY and can be extended to the other IN2P3 labs interested in the 28 nm process
- This work is done in relation to the **CERN R&D Program** on Technologies for **Future Experiments**
- CPPM is a member of two working groups within the DRD (ECFA) projects
  - WG 7.3a (4D and 5D techniques) to develop front ends with **high temporal resolution**
  - WG 7.4b (Advanced and hardened CMOS nodes) to study the **effects of radiation** on highly advanced processes

28 nm chip design

R&D on hybrid pixels

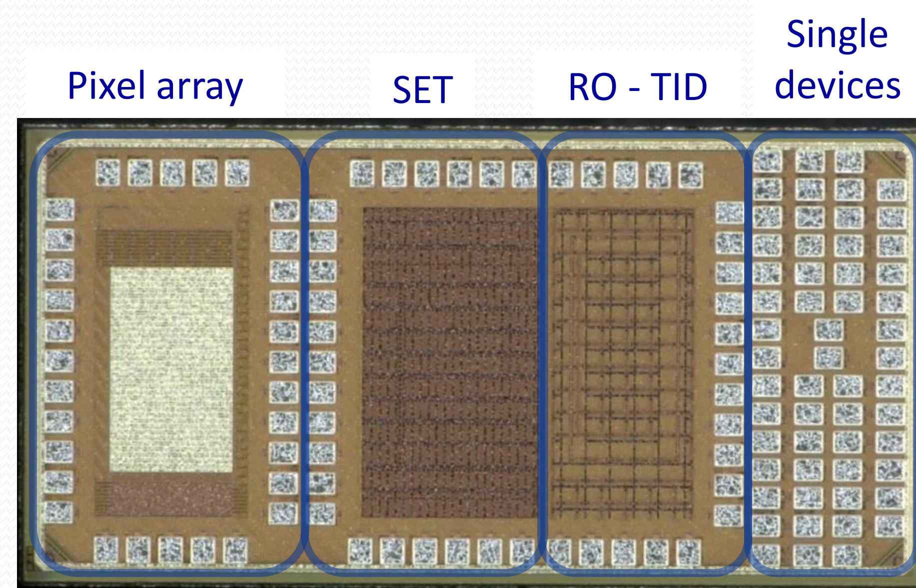
- Process qualification in terms of performance for analog, low-power and low-noise circuits
- Architecture studies
- Fast charge amplifier array

Study of Single Event Effects (SEE)

- Measure the **SET cross-section**
- Measure the **SET pulse width** with a good resolution < 20 ps
- Measure the effect of the std cell size

TID tests and qualification

- Compatibility with typical dose levels for future projects
- 28 nm process device qualification
- **Gate delay** evolution with TID and the effect of the std cell size
- TID Effects modeling → Analog and digital simulations with TID effects



Mini@sics of 2×1 mm2 received June 2023, consisting of 4 main blocks

- Analog pixel array (25×25 µm2) with Fast charge amplifiers for high time resolution
- SET test structures
- Ring Oscillators for TID tests on digital standard cells
- Test structures for TID tolerance studies

Fast amplifier design

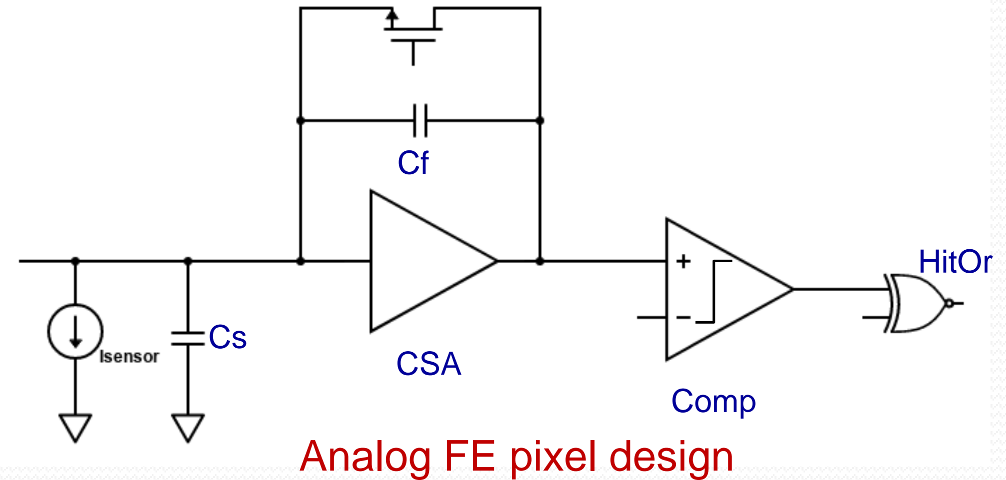
Study the limits to **time resolution** in the analog front-end designed with the **28 nm CMOS** process

- Effects of the Current bias, power supply, Bandwidth, Noise …

Design and test a **pixel array of 36 × 12 cells** where only the analog part is considered and implemented

The time resolution of a detector:

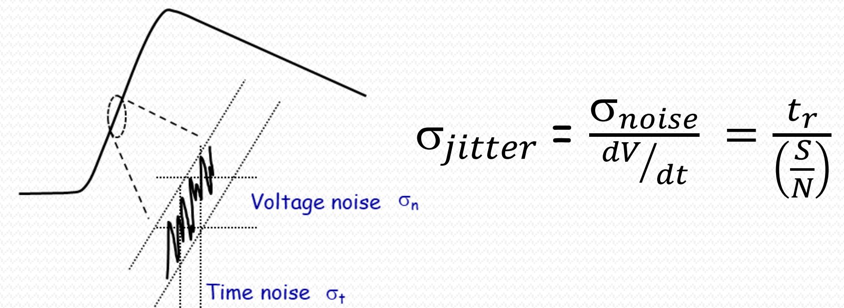
$$\sigma^2_{total} = \sigma^2_{jitter} + \sigma^2_{timewalk} + \sigma^2_{Landau} + \sigma^2_{TDC}$$



Analog FE pixel design

Minimizing the front-end jitter corresponds to :

- Low RMS noise of the charge amplifier (CSA)
- High output voltage
- Small rise time → High bandwidth



$$\sigma_{jitter} = \frac{\sigma_{noise}}{dV/dt} = \frac{t_r}{\left(\frac{S}{N}\right)}$$

Analog FE pixel prototype

For each pixel :

- The charge amplifier current bias can be set in the range of 2µA-20µA
- MOM capacitance connected to each preamplifier input -> test for different input capacitance values

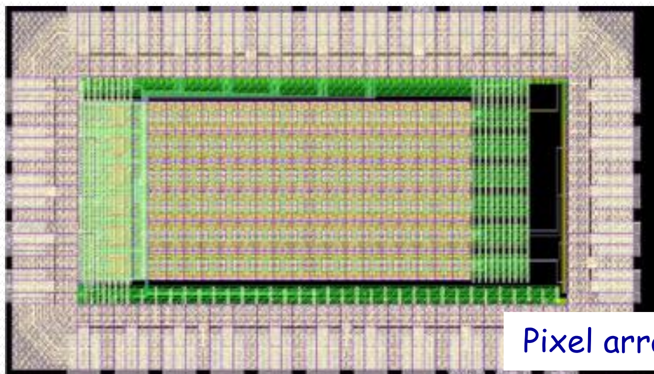
Large bandwidth buffers (> 1GHz) implemented and connected for a few pixels for direct jitter measurement

Simulations for I_{CSA} = 5 µA

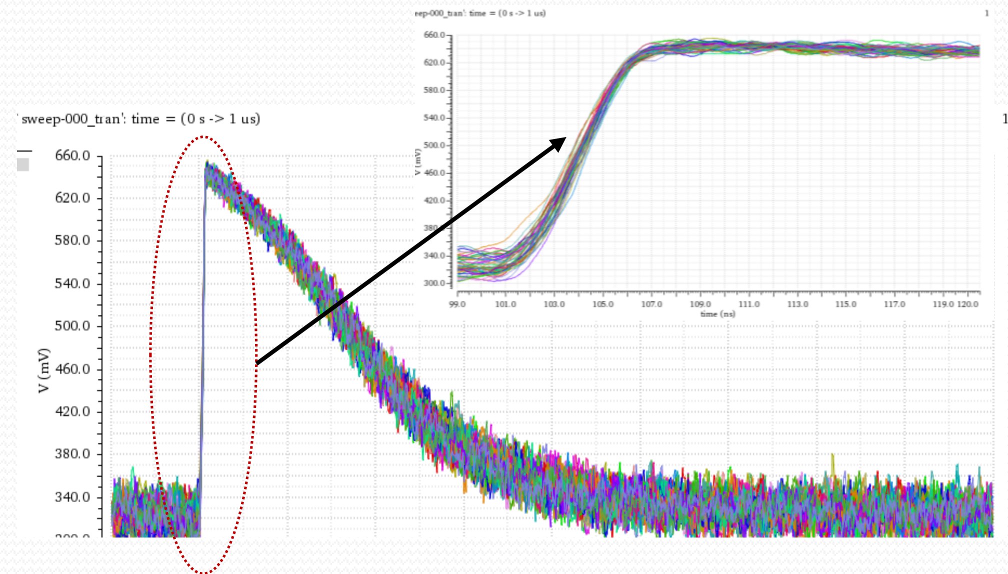
- dV/dt = 100 mV/ns
- RMS noise = 97 e- RMS for Cin = 100fF
- Jitter < 100 ps RMS for input charge > 4 ke-
- Jitter < 40 ps RMS for charge > 10 ke-

Each pixel contains : CSA + Discriminator + 6 bit DAC

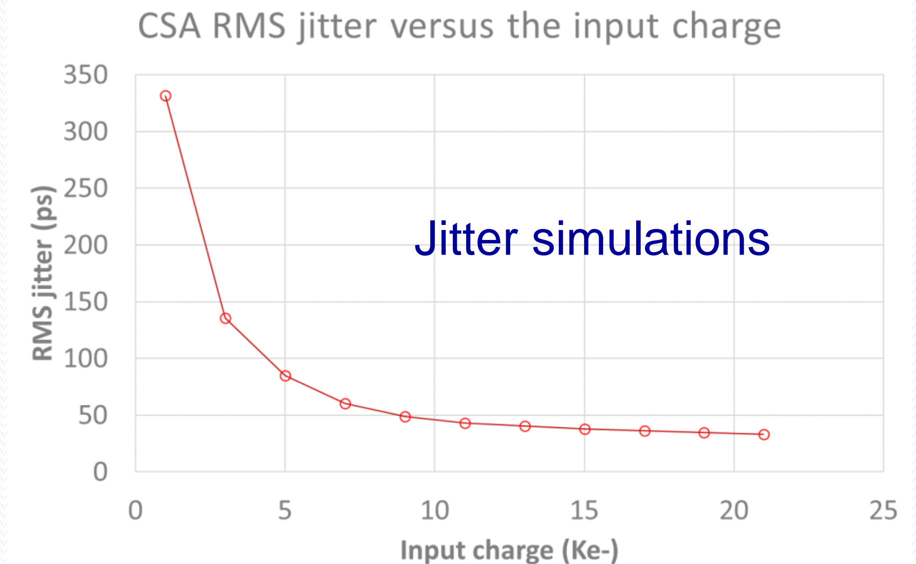
- Size : 20 µm × 12 µm



Pixel array of 36 × 12 pixels



50 superimposed transient noise simulations



Prototypes 28nm sur PCB

Pixel_28nm

SET_28nm

RO_28nm

Preliminary results

The pixel array prototype is working properly

- The 3456 registers can be configured correctly
- The test pixel output signal is consistent with simulations
- intensive testing under way

Ring oscillators

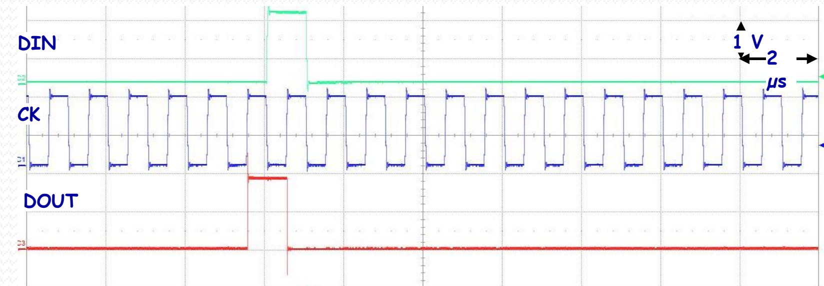
- Minor configuration issue but should not prevent testing of the various blocks

SET block

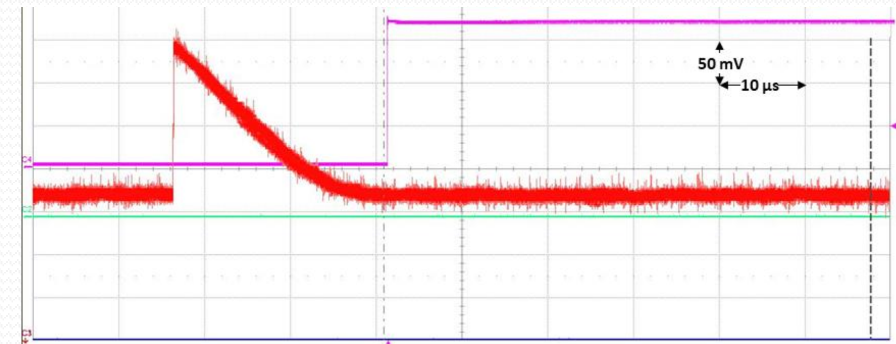
- To be tested soon

Devices characterization

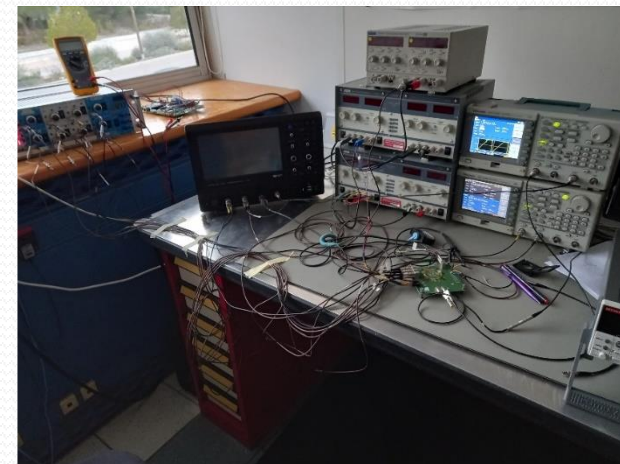
- waiting for the PCB with wire bonded block



Configuration SR chip Pixel_28nm (EN_INJ = '1' pixel 36)



Sortie CSA pixel 36



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Conclusion and perspectives

28nm prototype test boards received the beginning of 2024

- Testing has just started and first results are quite promising
- 4 chips to be tested and characterized
- Existing test-setup based on a beagle-bone board to be used

Continuation of the project

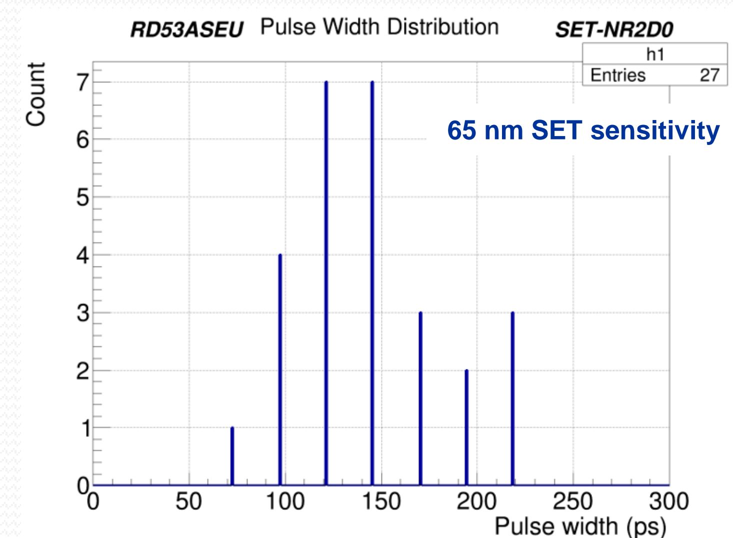
- The project is part of the IN2P3 R&D DEPHY project
- Functional tests to be done in Q2 2024
- Irradiation tests (TID and SEE) in Q3-Q4 2024
- A new 28 nm design focused on pixel array with the possibility to be bump bonded with sensor array
  - Use of CERN PDK makes the design more manageable
  - Prototype submission scheduled for Q4 2024

Other Slides

SEE/SET Testing

- The SEE mitigation is a major challenge for the next generation of pixel chips because of the luminosity increase
- SET propagation through combinatorial logic and generate SEU in memories, FIFO and state machines …
- SET sensitivity increases with process advance and with speed

- SET test structures implemented in the prototype chip will allow characterizing the 28nm CMOS process for SET tolerance

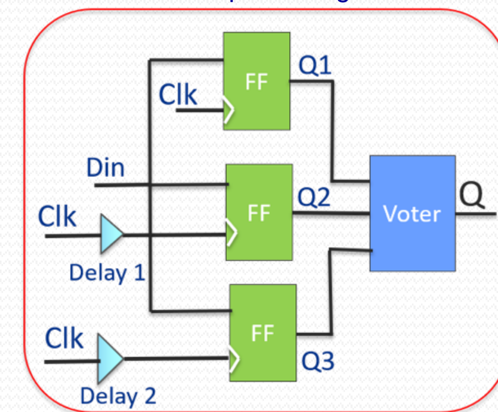


Objectives :

- Measure the SET cross-section
- Measure the SET pulse with a **good resolution < 20 ps**
- Measure the effect of the std cell size

Allows for example to define the delay to be imposed for the triplication with time mitigation

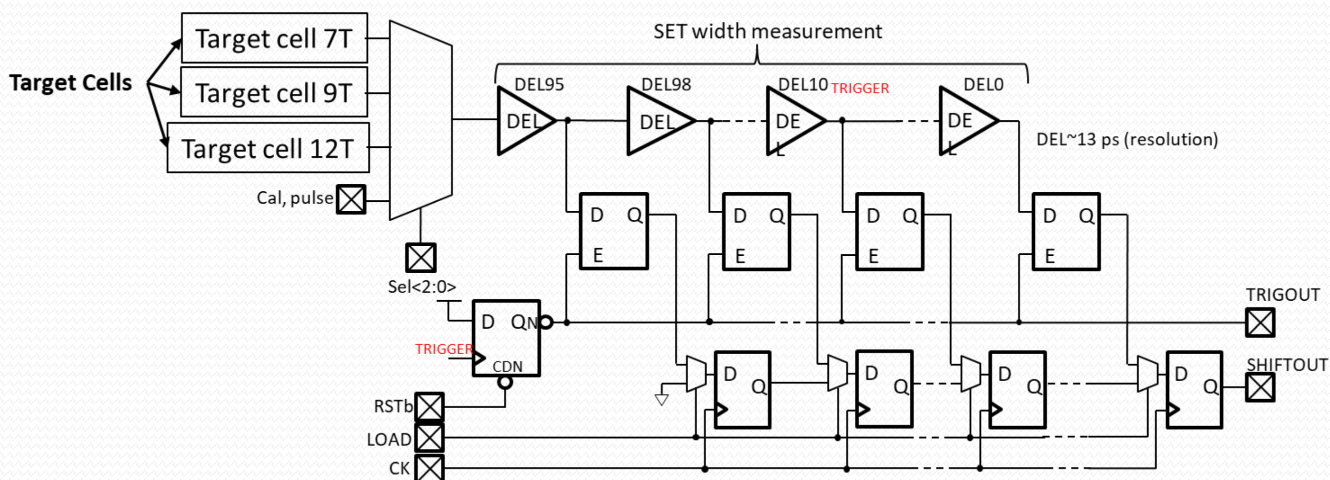
SEU tolerant design with temporal Mitigation

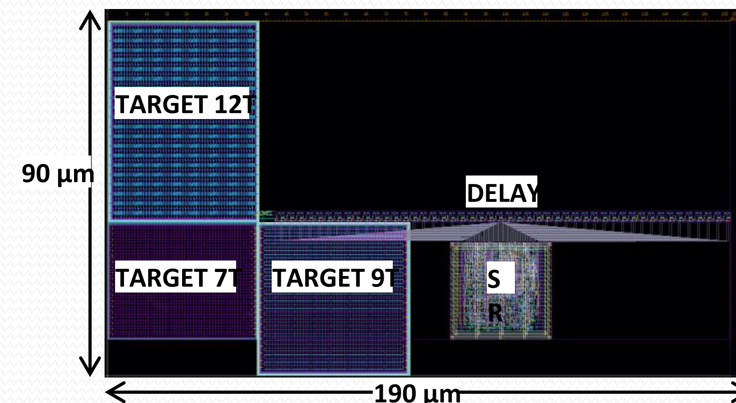


SET Bloc design

Designer : Denis Fougeron

SET sub-bloc synoptic





Layout example for INVD4 cell

Each sub-bloc contains

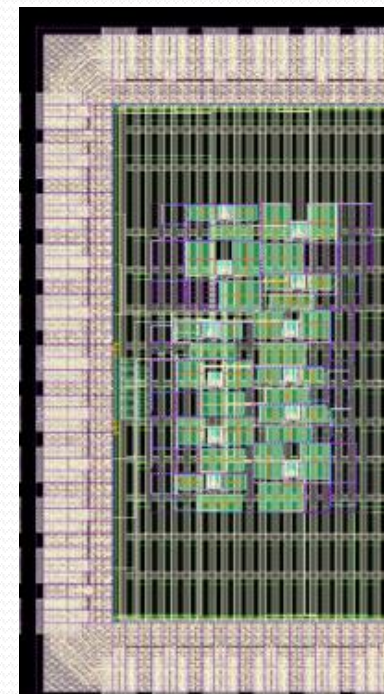
- 3 target cells made up of thousands of basic cells + 1 calibration input
- Circuit for SET width measurement 96 delay cells (13ps/cell) -> from a few ps to 1 ns
- Shift register to send the data to the output when a trigger signal occurs

31 SET sub blocs

- 24 uses SVT target cells (7T, 9T, 12T) -> **Effect of the cell size**
- 7 uses LVT or HVT target cells -> Effect of **the device options**

The whole bloc contains 6 inputs / 13 outputs

In addition to SET testing, this constitutes a sub-block of the TDC required in the pixel front end



Ring Oscillator Design

Designer : Eva Joly

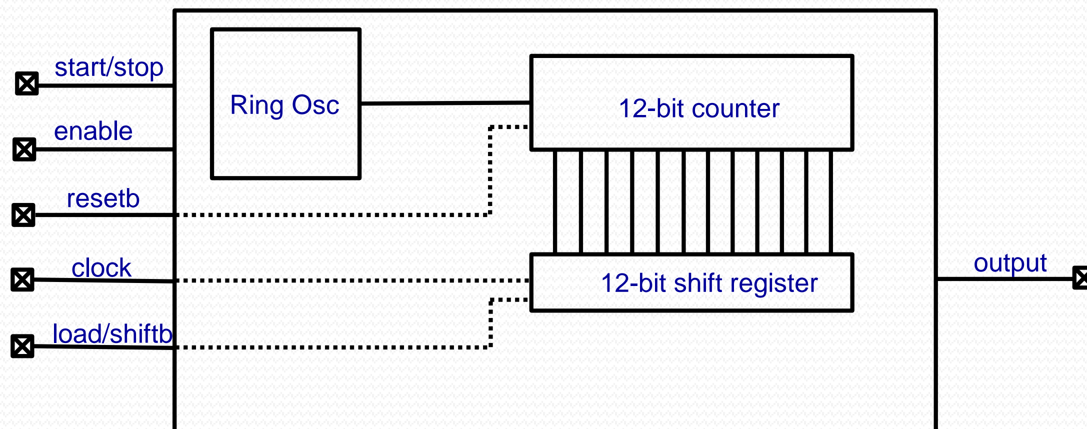
Study the **effect of TID** on the performances of **digital standard cells**

- Timing of combinatorial cells
- Leakage currents and static power

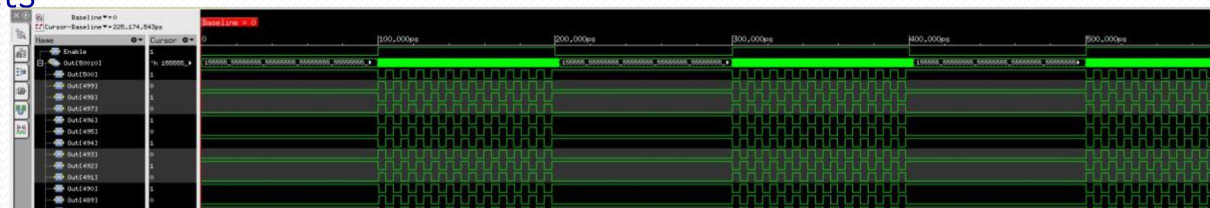
96 ROsc sub-bloc

- Cell size (7T, 9T,12T) -> **cell size** effects
- Driving (D0, D2, D4) -> **cell driving** effects
- SVT, LVT, HVT -> **device threshold** effects

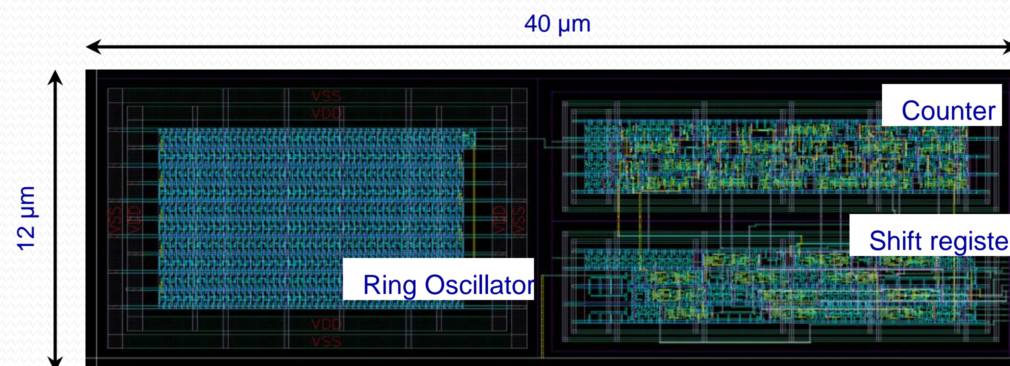
Design based on the **digital flow**



ROsc sub-bloc synoptic



Basic cells	Frequency (MHz)
INVD0	154
INVD2	222
NAND0	118
NAND2	143
NOR0	111
NOR2	139



Simulation

Manual layout

Synthesis