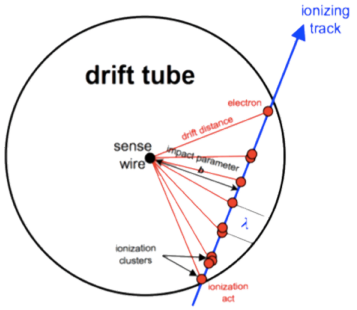
Task 7.4.1
A 4-channel electronics board for Cluster Counting

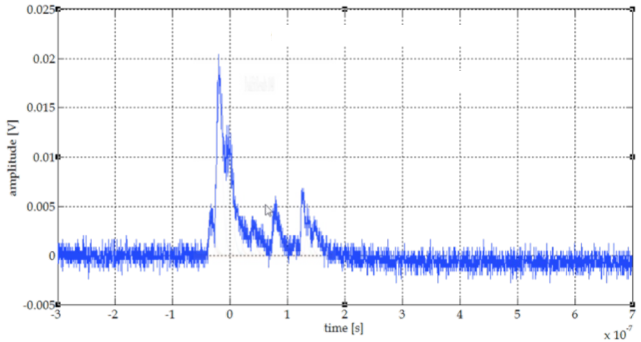
F. Grancagnolo
INFN-Lecce

3rd Annual Meeting - Catania, 18-21 March, 2024

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement No 101004761.

Cluster Counting pills





Single out, in every recorded detector signal, the **isolated structures** related to the arrival on the anode wire of the **electrons belonging to a single ionization act.**

Determine, in the signal, the **ordered sequence of the electron arrival times**:

$$\left\{t_j^{el}\right\} \qquad j = 1, n_{el}$$

based on the **the average time separation between consecutive clusters** and on the **time spread due to diffusion**, as a function of the drift time, **define** the **probability function**, that the ***j*th electron** belongs to the ***i*th cluster**:

$$P(j,i) \qquad j = 1, n_{el}, \quad i = 1, N_{cl}$$

then **derive** the most probable **time ordered sequence of the ionization clusters:**

$$\left\{t_i^{cl}\right\} \qquad i = 1, N_{cl}$$

the total **number of clusters:** N_{cl} and the average **cluster population:** n_{el}/N_{cl}

Cluster Counting PID

$$\frac{\sigma_{dE/dx}}{(dE/dx)} = 0.41 \cdot n^{-0.43} \cdot \left(L_{track}[m] \cdot P[atm]\right)^{-0.32}$$

from *Walenta parameterization (1980)*

versus

$$\frac{\sigma_{dN_{cl}/dx}}{(dN_{cl}/dx)} = \left(\delta_{cl} \cdot L_{track}\right)^{-1/2}$$

from *Poisson distribution*

dE/dx

truncated mean cut (70-80%)

***n* = 112** and a **2m track** at **1 atm** give

dN$_{cl}$/dx

δ_{cl} = 12.5/cm for He/iC$_4$H$_{10}$=90/10 and a **2m track** give

σ ≈ 4.3% ⟷ for the IDEA Drift Chamber ⟷ **σ ≈ 2.0%**

Cluster Timing technique

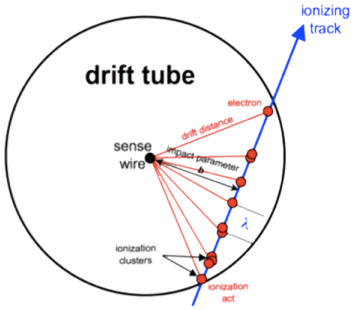
For any given first cluster (FC) drift time, the **cluster timing technique** exploits the time distribution of all successive clusters to determine hit by hit, the most probable **impact parameter**, by using statistical (**MPS**) or **ML techniques**, thus reducing the **bias** and improving the average **spatial resolution** with respect to that obtainable with the FC method alone:

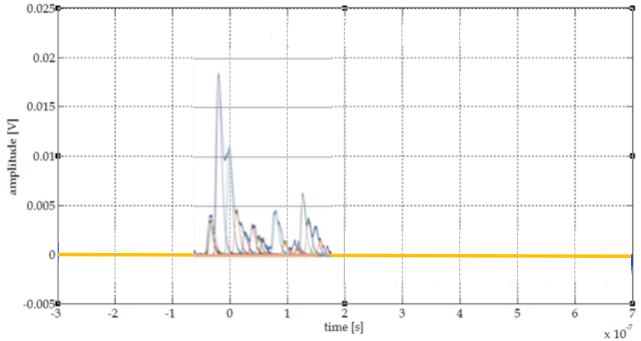
over a 1 cm drift cell, **spatial resolution** may improve by ≳ 20%
down to ≲ 80 μm.

Fringe benefits of the **cluster timing** technique are:

- **event time stamping (at the level of ≈ 1 ns);**
- **improvements on longitudinal resolution both by charge division and by time difference;**
- **possibility of defining a track multiplicity and even a momentum selected trigger**

Cluster Counting pills





Single out, in every recorded detector signal, the **isolated structures** related to the arrival on the anode wire of the **electrons belonging to a single ionization act.**

Determine, in the signal, the **ordered sequence of the electron arrival times**:

$$\left\{t_j^{el}\right\} \qquad j = 1, n_{el}$$

based on the **the average time separation between consecutive clusters** and on the **time spread due to diffusion**, as a function of the drift time, **define** the **probability function**, that the ***j*th electron** belongs to the ***i*th cluster**:

$$P(j,i) \qquad j = 1, n_{el}, \quad i = 1, N_{cl}$$

then **derive** the most probable **time ordered sequence of the ionization clusters:**

$$\left\{t_i^{cl}\right\} \qquad i = 1, N_{cl}$$

the total **number of clusters:** N_{cl} and the average **cluster population:** n_{el}/N_{cl}

Cluster Counting PID

$$\frac{\sigma_{dE/dx}}{(dE/dx)} = 0.41 \cdot n^{-0.43} \cdot \left(L_{track}[m] \cdot P[atm]\right)^{-0.32}$$

from *Walenta parameterization (1980)*

versus

$$\frac{\sigma_{dN_{cl}/dx}}{(dN_{cl}/dx)} = \left(\delta_{cl} \cdot L_{track}\right)^{-1/2}$$

from *Poisson distribution*

dE/dx

truncated mean cut (70-80%)

***n* = 112** and a **2m track** at **1 atm** give

dN$_{cl}$/dx

δ_{cl} = 12.5/cm for He/iC$_4$H$_{10}$=90/10 and a **2m track** give

σ ≈ 4.3% ⟷ for the IDEA Drift Chamber ⟷ **σ ≈ 2.0%**

Cluster Timing technique

For any given first cluster (FC) drift time, the **cluster timing technique** exploits the time distribution of all successive clusters to determine hit by hit, the most probable **impact parameter**, by using statistical (**MPS**) or **ML techniques**, thus reducing the **bias** and improving the average **spatial resolution** with respect to that obtainable with the FC method alone:

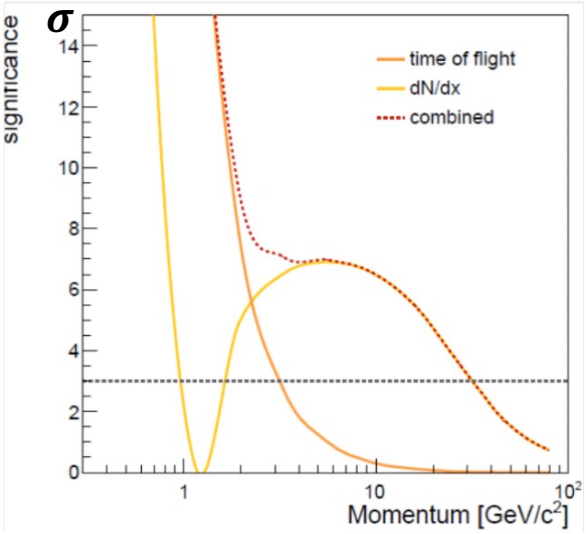
over a 1 cm drift cell, **spatial resolution** may improve by ≳ 20%
down to ≲ 80 μm.

Fringe benefits of the **cluster timing** technique are:

- **event time stamping (at the level of ≈ 1 ns);**
- **improvements on longitudinal resolution both by charge division and by time difference;**
- **possibility of defining a track multiplicity and even a momentum selected trigger**

Motivations for the proposal

IDEA drift chamber expected π/K separation (DELPHES simulation)



Cluster counting recipe:

high front-end bandwidth (**∼ 1 GHz**)
S/N ratio ≧ 8
high sampling rate (**≳ 2 GSa/s**)
≧ 12 bit

PROBLEM

For the IDEA drift chamber, however, given:

- > 56,000 active cells, readout at both ends;
- 1.5 cm drift length, max drift time: ∼500 ns;
- Z → hadrons trigger rate: ∼100 KHz;
- charged tracks multiplicity: 20 tracks/hadronic event;
- average of 130 hit cells/track;
- Digitization: 12 bits at 2 Gsa/s:

20 track/event × 130 cell/track/side × 2 side × 10^5 event/s × 5×10^{-7} s/cell × 2×10^9 byte/s =

= 0.5 TB/s

plus $\gamma\gamma$, Bhabha, beam background, noise, …

⟹ Transfer rate at Z-pole ≳ **1 TB/s!**

some data reduction is mandatory!

SOLUTION

A possible solution consists in transferring, for each hit drift cell, only the minimal information relevant to the application of the cluster timing/counting techniques, i.e.: **amplitude** and **arrival time** of each peak associated with each individual ionization electron, instead of the full digitized **signal waveform**:

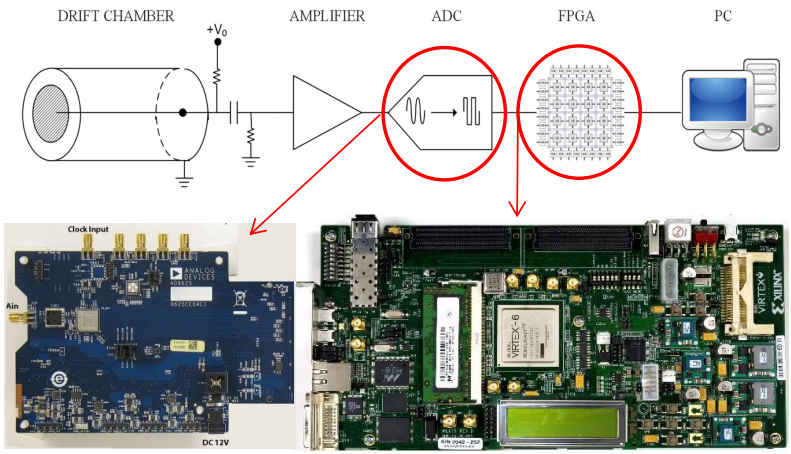
20 track/event × 130 cell/track/side × 2 side × 10^5 event/s × 30 peaks/cell × 2 byte/peak =

= 30 GB/s

This can be accomplished with the use of simple algorithms on a **FPGA** for the real time pre-processing of the digitized data generated by the drift chamber.
Moreover, background and noise can easily be filtered out by the same algorithm.

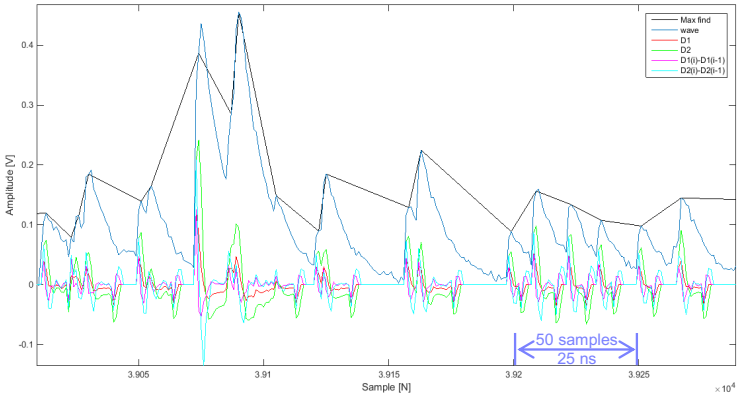
Motivations for the proposal

Single channel implemented solution



A fast readout algorithm (**CluTim**) for identifying, in the digitized drift chamber signals, the individual ionization peaks and recording their time and amplitude was developed as a **VHDL/Verilog** code implemented on a **Virtex 6 FPGA**, allowing for a maximum input/output clock switching frequency of **710 MHz**. The hardware setup included also a 12-bit monolithic **pipeline sampling ADC** at conversion rates of up to **2.0 GSPS**.

The **CluTim** algorithm*



Portion of the input signal, values of the auxiliary functions and found peaks.

At the start of the signal acquisition and processing procedures, a counter is set to provide the timing information.

A peak at the i-th bin is defined by relating its amplitude to those of a number n of preceding and successive bins, with n function of the rise and fall times of the single electron signal.

The amplitude and time of a found peak are then sent to a pipeline memory which is continuously filled as new peaks are found. When a trigger signal occurs at time t_0, the reading procedure is enabled and the data relative to the found peaks in the $[t_0, t_0 + t_{max}]$ time interval, where t_{max} is the maximum drift time, are transferred to an external device

At 1.5 LSB threshold
70% efficiency with
1.1 fake peak rate

* G. Chiarello, C. Chiri, G. Cocciolo, A. Corvaglia, F. Grancagnolo, M. Panareo, A. Pepino and G. Tassielli
The Use of FPGA in Drift Chambers for High Energy Physics Experiments, ISBN 978-953-51-3208-0, *2017 JINST 12 C03056*

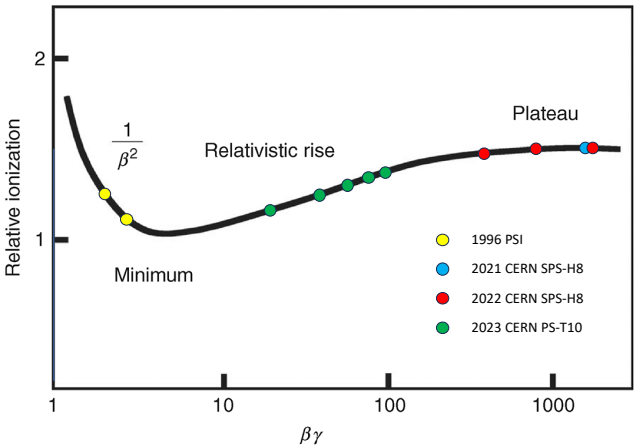
Objectives of the Task 7.4.1

- The application of the Cluster Counting/Timing (CC/T) technique in real time has the advantage of **reducing the amount of data transfer and of data storage**. The objective of the proposal is to be able to implement, on a single FPGA, CC/T algorithms (with high peak finding efficiency) for the parallel preprocessing of as many channels as possible (4, at this stage) to **reduce cost and complexity** of the system and to gain **flexibility in determining the proximity correlations** between hit cells for **track segment finding** and for **triggering purposes**.
- This strategy is being accomplished with **FPGAs for the real time analysis** of the data generated by the drift chamber and successively digitized by an ADC.
- Three different approaches to the **CC/T algorithms**:
  - **DERIV,** based on the first and second derivative of the digitized signal function.
  - **RTA**, based on a bin-by-bin matching of the signal waveform with a normalized search template.
  - **ML** techniques based on RNN, GNN and Domain Adaptation with Optimal Transport.

  are being implemented on different **hardware configurations**:
  - **(ADC32RF45 or LMH6522) + FPGA KCU105**
  - **CAEN digitizer VX2751**
  - **NALU Scientific ASoCv3 and HDSoCv1**
  - **PYNQ based solution for ML algorithms**
- Test-bed for all hardware configurations with the different algorithms is a **beam test campaign** aimed at establishing the performance of the **cluster counting/timing technique**.

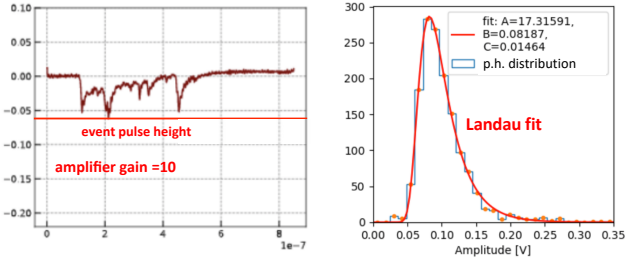
Beam test campaign

Muon beam test campaign

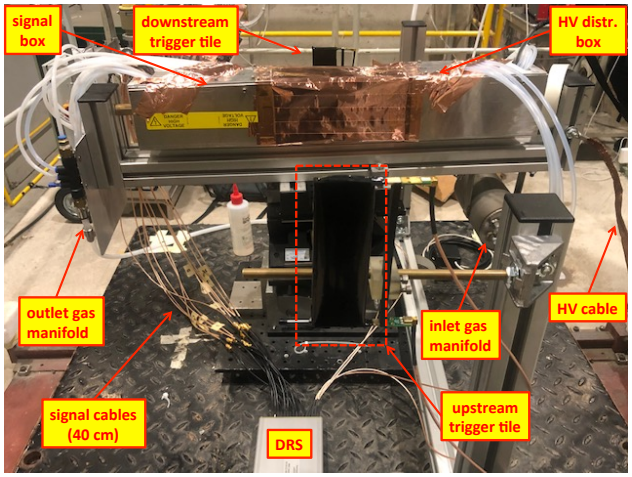


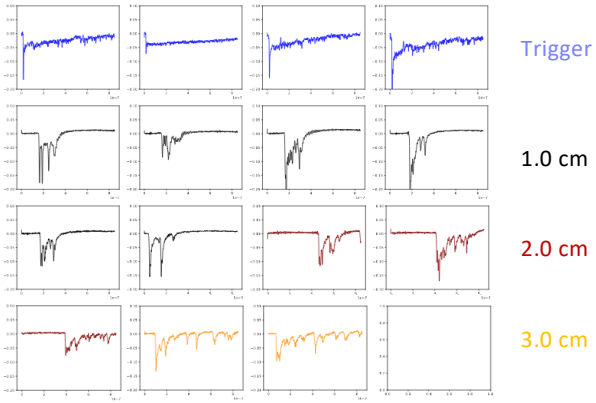
The explored βγ values extend over the region of interest for PID at the future lepton colliders.

Single electron pulse height

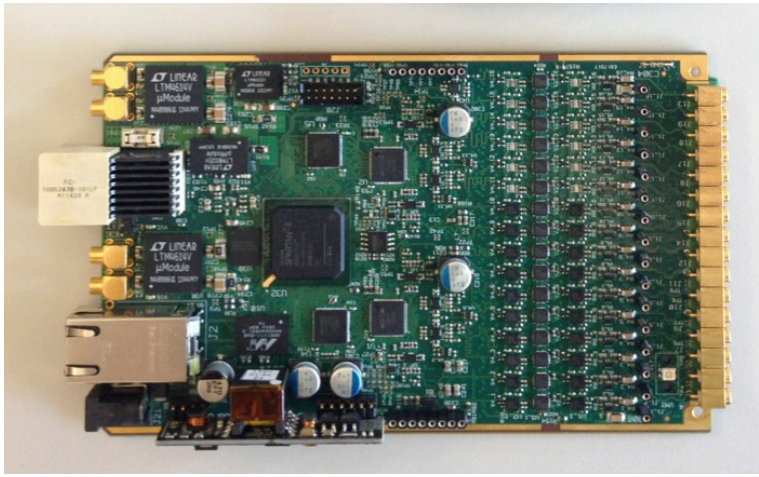


Test setup at CERN

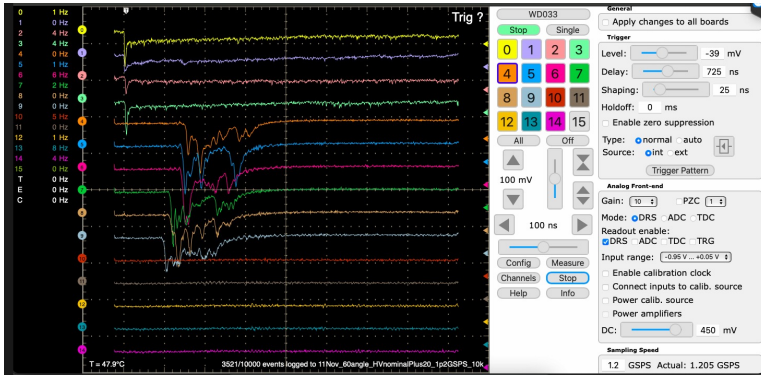




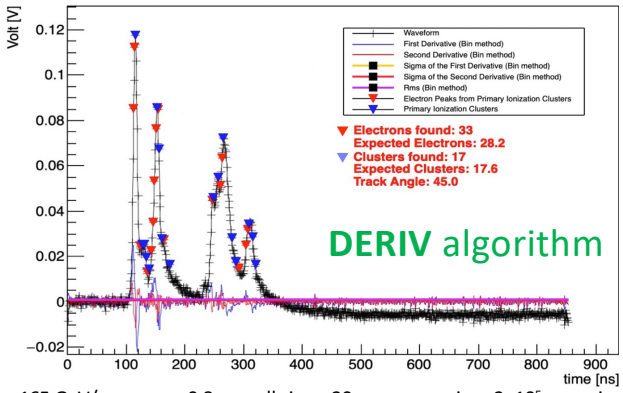
The hearth of the acquisition system



Wave Dream Board (courtesy of MEG2)

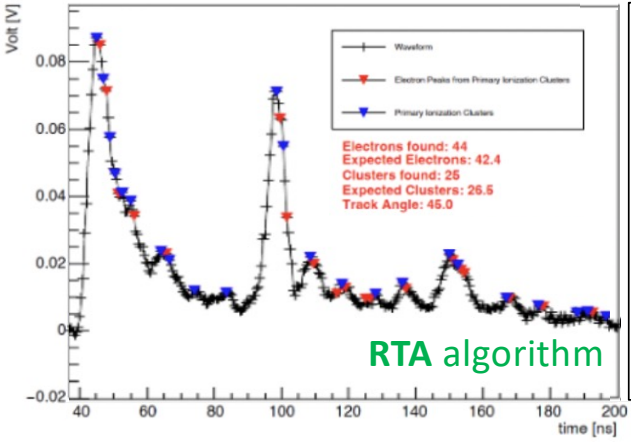


Peak finding algorithms

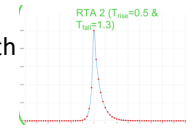


Compute the first and second derivative over a pre-defined number of bins and compare them to thresholds in terms of a r.m.s. value, where. r.m.s. is a measurements of the noise level in a control region of the waveform.

165 GeV/c muons – 0.8 cm cell size – 20 μm sense wire - 2×10^5 gas gain – 90% He/10% iC_4H_{10} (m.i.p.: 12 clusters/cm) - 45° track angle –12 bits at 1.2 Gsa/s



Define a digitized pulse template with raising and falling exponentials.

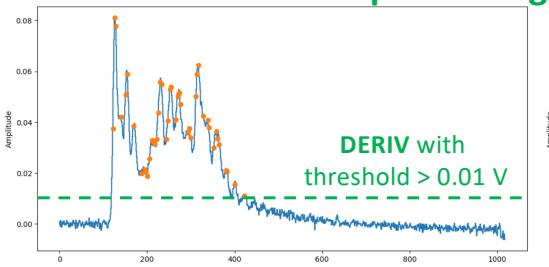


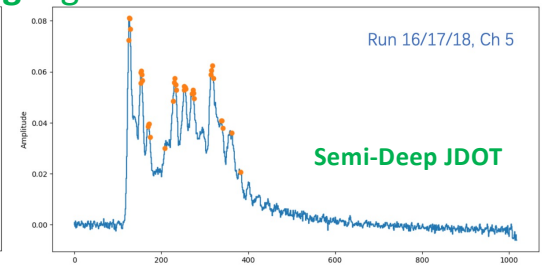
Scan the data waveform by comparing it to the template, normalized to the amplitude, and construct a χ^2. If above threshold, subtract the found peak from the waveform and iterate until no new peaks are found.

same as above except 80% He/20% iC_4H_{10} (m.i.p.: 18 clusters/cm)

Deep Learning algorithm

Test beam data



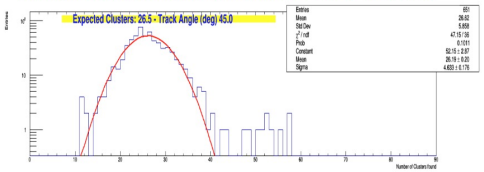


Supervised Learning:
Peak finding with **Long-Short Term Memory** (**LSTM** RNN-based)
Clusterization with **Dynamic Graph CNN** (**DGCNN** GNN-based)

Experimental data application:
Domain Adaptation (**DA**) with **Deep Joint Distribution Optimal Transport** (**DeepJDOT**)
Semi-supervised DeepJDOT

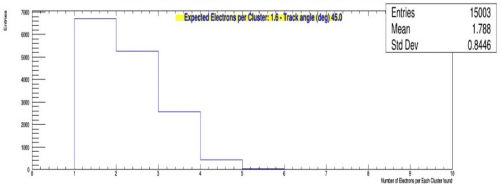
Beam test results

Poissonian distribution for the number of clusters



mean = 26.62 r.m.s. = 5.86

Electrons per cluster distribution

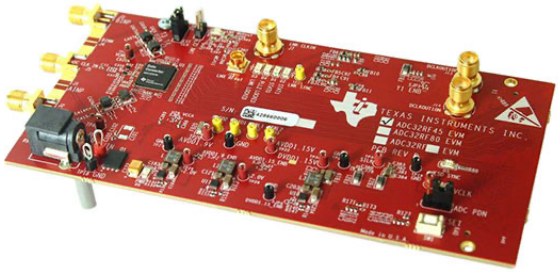


1.8 e^-/cluster

Expected number of clusters: Cluster density × cell size × relativistic rise w.r.t. m.i.p. × 1/cos(track angle)
Expected number of electrons: expected number of clusters × average cluster population

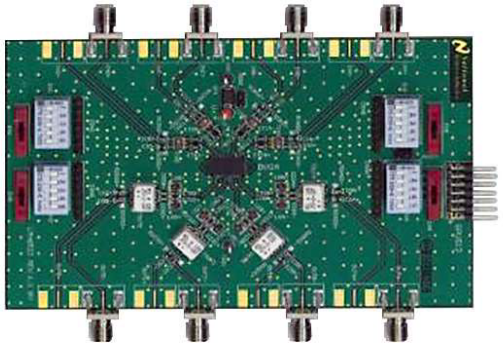
Hardware Configurations

ADC (ADC32RF45 or LMH6522) + FPGA KCU105



2 x 2-ch ADC32RF45

OR

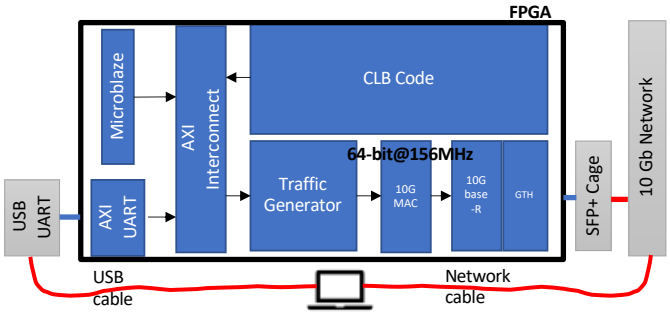


1 x 4-ch LMH6522

+

AMD Kintex UltraScale FPGA KCU105

- The code for the single channel in the old framework has been translated to the new Xilinx framework
- The communication between the FPGA and the ADCs has been carried out and simulations of timing and power consumption have been completed
- The code for using the 10Gb standard SFP + connections has been developed and tested
- The integration between the CC/T algorithm block is being completed



CAEN VX2751

We have been provided by **CAEN** with the digitizer **VX2740** (a lower performance version of **VX2751**, better suited for the **CC/T** algorithm and not yet released)

We have been performed tests with the **open FPGA SCICompiler** software:

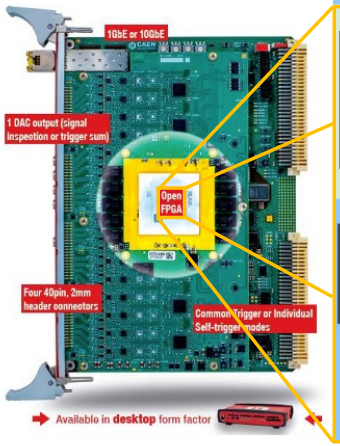
- program very simple to use with GPIO cards
- electrical circuits easily created and converted into VHDL
- very simplified code/circuit debugging thanks to the available tools

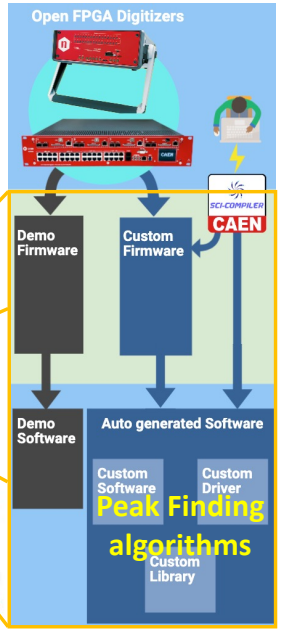
Model	# channels	MS/s	# bit	Applications
x2740	64	125	16	64 MCAs for high channel density spectroscopy Good fit for Neutrino and Dark Matter exp.
x2745 Advanced version of x2740	64	125	16	Variable gain input stage Designed for Si detectors readout
x2725/x2730	32	250/500	14	Medium-fast detectors Sub-ns timing combined with high energy resolution Optimal trade off between cost and performances
x2751	16	1000	14	Ultra-fast detectors (diamond, MPCs, SiPMs) with ps timing applications Potential upgrade to higher sampling rate
x2724	32	125	16	Spectroscopy & MCA Advanced Front-End (gain, shaping, AC/DC coupling ...) Semiconductor detector (HPGe, Clover, SDD ,...) Typically connected to charge Sensitive Preamplifier

VX2740: the first of a kind

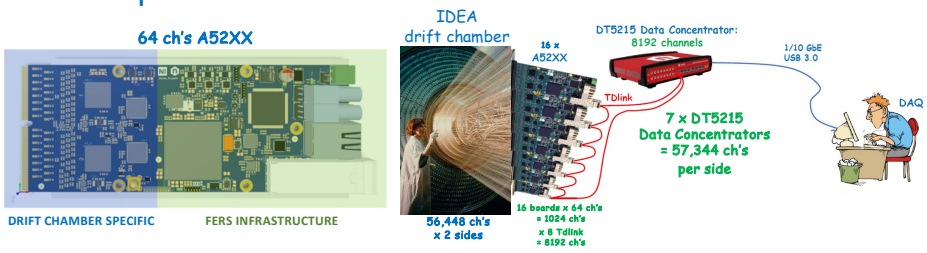
64 channel, 125 MS/s, 16 - bit waveform digitizer

- High channel density spectroscopy
- Good fit for Neutrino and Dark Matter experiment
- **Open FPGA**: SCI-Compiler tool for beginners or advanced firmware template
- Four 40-pin, 2 mm header connectors with DIFF or SE inputs
- **1 GbE, 10 GbE, USB 3.0** and CONET 2.0 (optional) connectivity
- Common Trigger (waveforms) or Individual Self-trigger modes
- **DPP options**: PHA, QDC, PSD, CFD
- Advanced Waveform Readout modes: ZLE, DAW
- DT2740, 64 channels in Desktop form factor





We are also exploiting the possibility of implementing the **CAEN FERS-5200** platform* using the **Citiroc-1A** chip, with **proper FE ASIC and digitizer**, as a modular and scalable platform for the high-density readout of a large volume drift chamber instrumented with cluster counting/timing techniques.

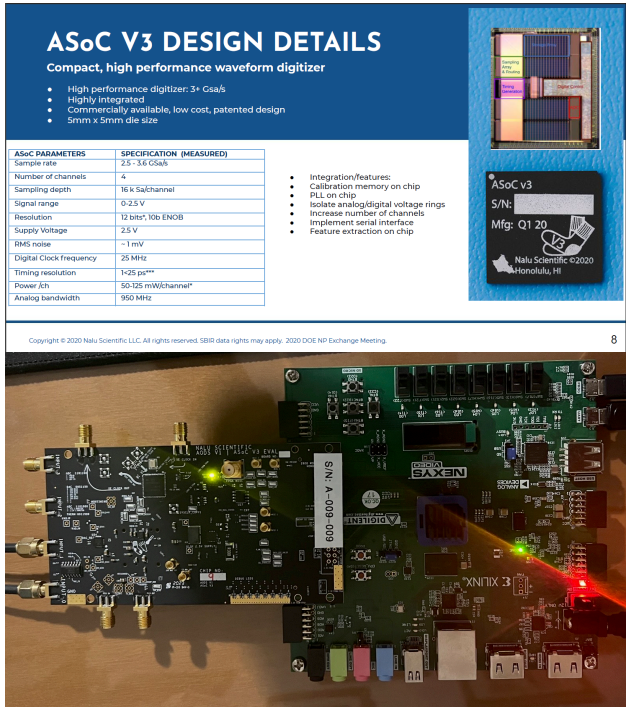


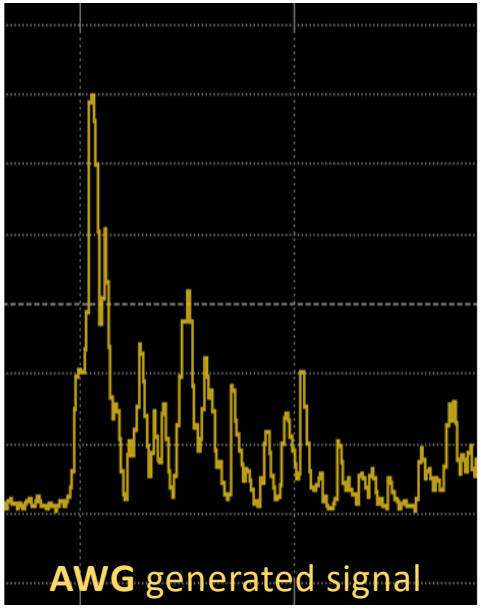
* M.Venaruzzo, A. Abba, C. Tintori, and Y. Venturini, *FERS-5200: a distributed Front-End Readout System for multidetector arrays* , arXiv:2010.15688v1 [physics.ins-det] 29 Oct 2020

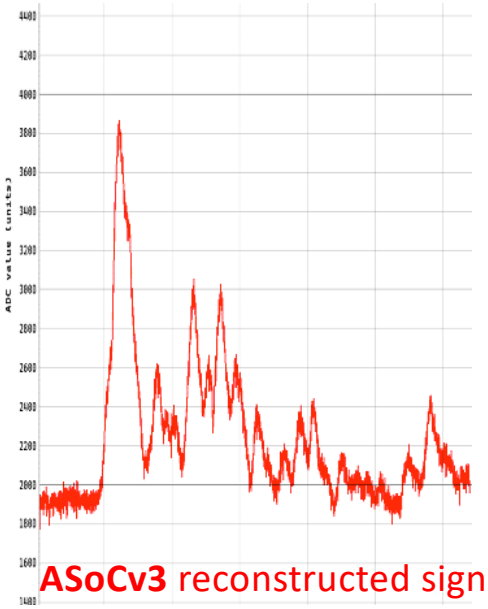
Naluscientifc ASoCv3

Naluscientific 4-ch **ASoCv3** evaluation board tested with a pulse generator

Aim was to connect the ASoCv3 board to drift tubes implementing the peak finding algorithms. However, issues related to the expiration of the temporary importation of the NALU chip forced the restitution of the ASoCv3 evaluation board to the company, before being able to test the full chain: drift tube – pre-amplifier – AsoCv3 board and to assess the performance on real data of this proposed solution which, however, still represent a valid alternative, worth to be kept under consideration.







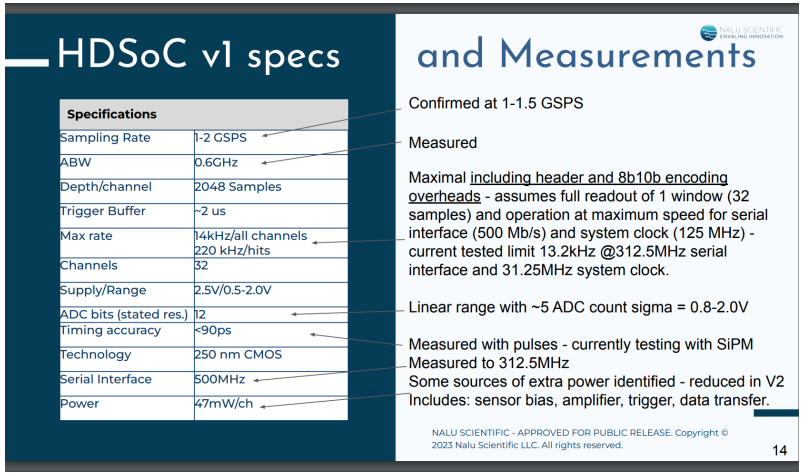
ASoCv3 reconstructed signal

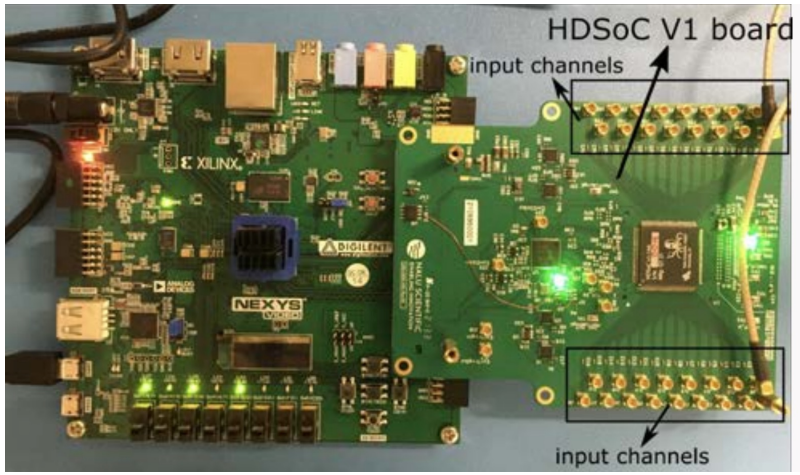
(clear analog bandwidth and noise limitations visible)

Naluscientifc HDSoCv1

HDSoC is a novel streaming readout capable, waveform- sampling ASIC:

- Low Cost, low power, scalable
- Works with a variety of sensors arrays: GEMS, TPCs, SiPMs, MA/PMTs, MCP PMTs
- Tracking and PID
- Portable radiation imaging systems
- Compact, high-efficiency neutron scatter cameras for non-proliferation national security missions.

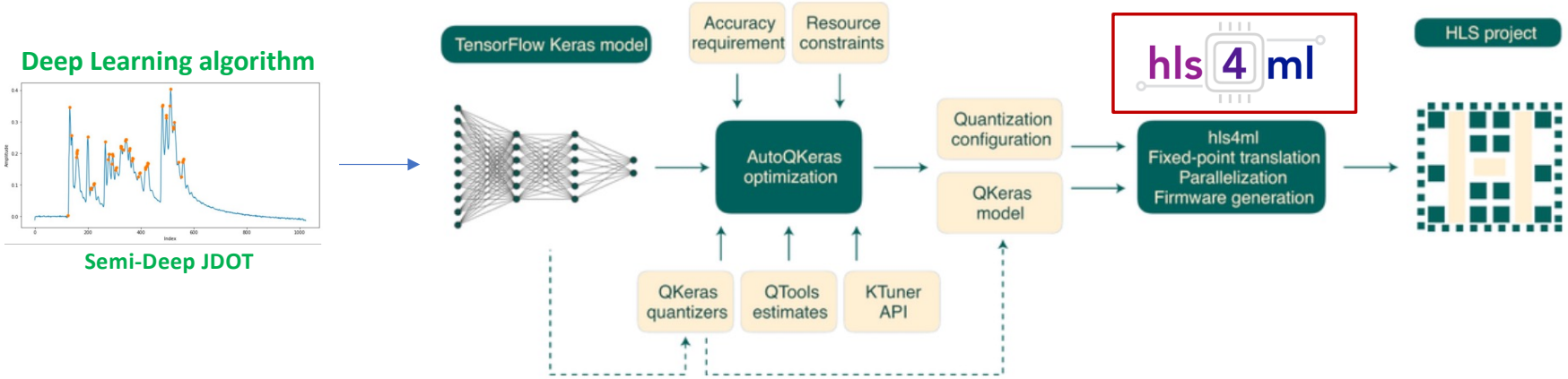




- Received with a 32 ch's **HDSoCv1 evaluation board**, thanks to CAEN Technologies, US branch of CAEN (distributor for Naluscientific).
- NEXYS interface cards procured.
- Currently under bench test.
- Aim is to test the setup at the next beam test scheduled in July at CERN PS-T10.

Implementing ML algorithms on FPGA

The first step required for the implementation of **neural networks** on FPGAs is the conversion of the high-level code used for the creation of the network (**QKeras**) into a **High-Level Synthesis** (**HLS**). To accomplish this task, the **hls4ml** package will used.



Use **PYNQ**, an open-source project for *Adaptive Computing* platforms to create high performance applications with:

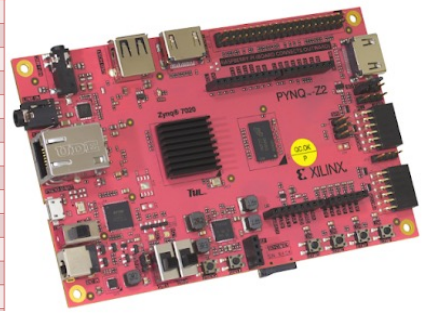
- parallel hardware execution
- real-time signal processing
- high bandwidth IO
- low latency control

XILINX PYNQ

TUL PYNQ-Z2

Product Specification	
Part number	1M1-M000127DEV
EAN	TUL PYNQ-Z2 | 4713436170785
Processor:	Dual-Core ARM Cortex-A9
FPGA:	1.3M reconfigurable gates
Memory:	512MB DDR3 / 128Mbit FLASH
Storage:	Micro SD card slot
Video:	HDMI In / HDMI Out
Audio:	HP+Mic, Line in, ADAU1761 AUDIO codec
Network:	10/100/1000 Ethernet
Expansion:	USB Host connected to ARM PS
Interfaces GPIO:	Arduino Shield connector, Raspberry Pi connector, 2 Pmod ports
Other I/O:	6 User LEDs, 4 Push-buttons, 2 Slide Switches
Dimensions:	87mm x 140mm

Photos of Product



- Hardware procured
- Deep neural network algorithm based on Semi-Deep JDOT fully developed and tested in off-line analysis
- Design of quantized versions (QKeras) of model and
- Firmware generation to be started

Milestones and deliverables

Milestones

- month 36: 4-ch system board (ADC + FPGA) engineered
  (March 2024)

- month 46: board completed
  (January 2025)

Deliverables

- month 46: board tested under particle beams (written report)
  (January 2025)

Milestones and deliverables

Milestones

- month 36: 4-ch system board (ADC + FPGA) engineered
  (March 2024)
  Fulfilled: we have developed and presented 5 possible solutions, although we have not yet outlined a comparative table among them

- month 46: board completed
  (January 2025)
  we are confident that this milestone **will be completed in time**

Deliverables

- month 46: board tested under particle beams (written report)
  (January 2025)
  some of the proposed solutions will undergo a beam test this summer at CERN PS-T10 and thereafter a **written report will be released**