# Task 7.2.2 - Shower development in SDHCAL

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***UE participants***

Belgium: Ghent → Vrije Universiteit Brussel
France: CNRS-IP2I, CNRS-LPC, CNRS-OMEGA
Spain: CIEMAT

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China: SJTU - Shanghai Jiao Tong University
South Korea: GWNU - Gangneung–Wonju National University
& SNUBH- Seoul National University Bundang Hospital

# Introduction – The SDHCAL concept



**SDHCAL** - **S**emi-**D**igital **H**adronic **CAL**orimeter

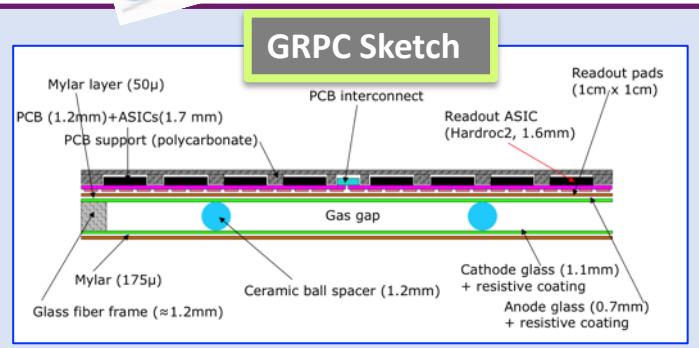
A sampling hadronic calorimeter under development at CALICE Collaboration intended to be used with PFA reconstruction techniques. ( ➔ High Granularity is a must)
One of the proposed options for the *ILD (International Large Detector) at the ILC (International Linear Collider)* and for and *CEPC (Circular Electron Positron Collider)* detectors

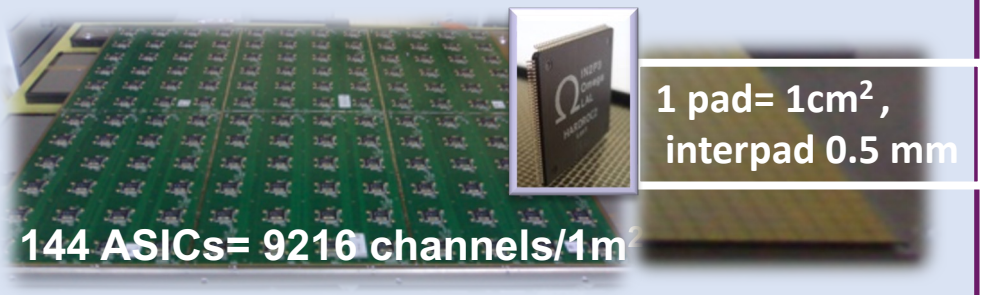
*Sampling calorimeter:* ***Absorber: Stainless Steel +*** ***Detector: Glass Resistive plate Chambers***

***Detector***: **GRPC (Glass Resistive Plate Chambers)** operating in **avalanche mode**

**1x1 cm$^2$ pads. Semi-Digital Readout**, 2bits **- 3 thresholds**
➔ It counts **how many** and **which pads** have a **signal larger than one of the 3 thresholds**

**Embedded electronics:**
**PCB** separated from the GRPC by a mylar layer (50µm).
➔ Bottom: **1x1cm2 pads**
➔ Top: **HARDROC** (**HA**dronic **R**pc **R**ead**O**ut **C**hip) & related connections
**Power-pulsed electronics:** In **stand-by during dead time** in between ILC Collisions or spills in beam tests



# SDHCAL at AIDAInnova – Task 7.2.2

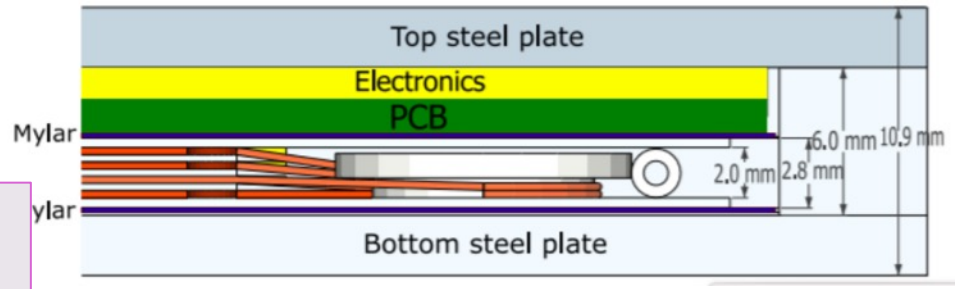


**General goal**: Extending the Semi-Digital Hadronic CALorimeter (SDHCAL) to include timing information (100 - 200ps resolution) for a **5D-calorimetry (space, amplitude & timing)**

**Implementation**: **Build small multi-gap RPC (MRPC)** equipped with a **new version of electronics** with **timing capabilities** to prove the final performance

The use of MRPC will improve the intrinsic timing of the detector but **electronic on the previous SDHCAL 1m3 prototype** has not high resolution timing capabilities.

➔ Readout Chip **HARDROC3**. Time Stamping=**200ns**




For AIDAInnova developments

Using **PETIROC (~50ps)** as first step before a future new ASIC

Also some chamber tests using NINO

# THIS TALK PRESENTS THE ADVANCES SINCE LAST YEAR REPORT AT 2ND AIDAINNOVA MEETING IN VALENCIA

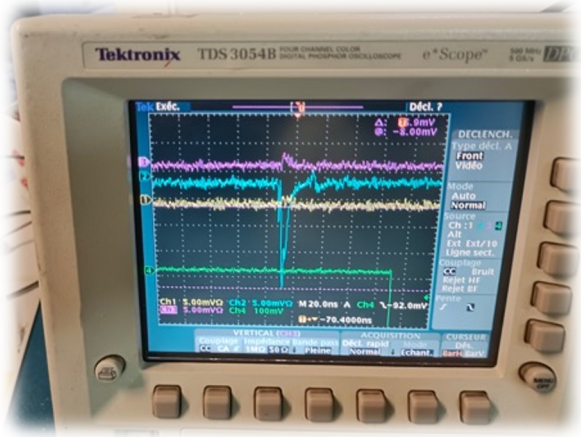
Previous report is available at:

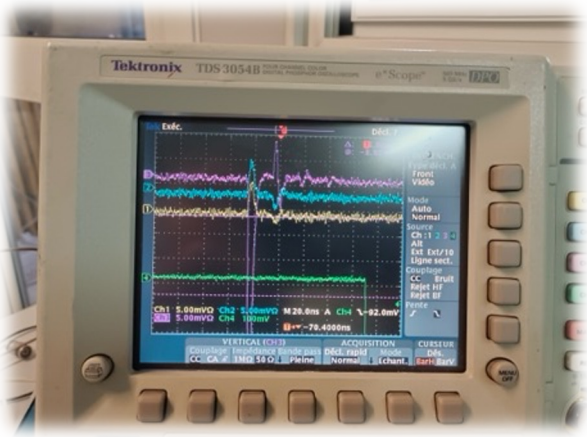
https://indico.cern.ch/event/1191719/contributions/5315264/attachments/2634658/4557670/AIDAInnova_SDHCAL_AnnualApr23.pdf

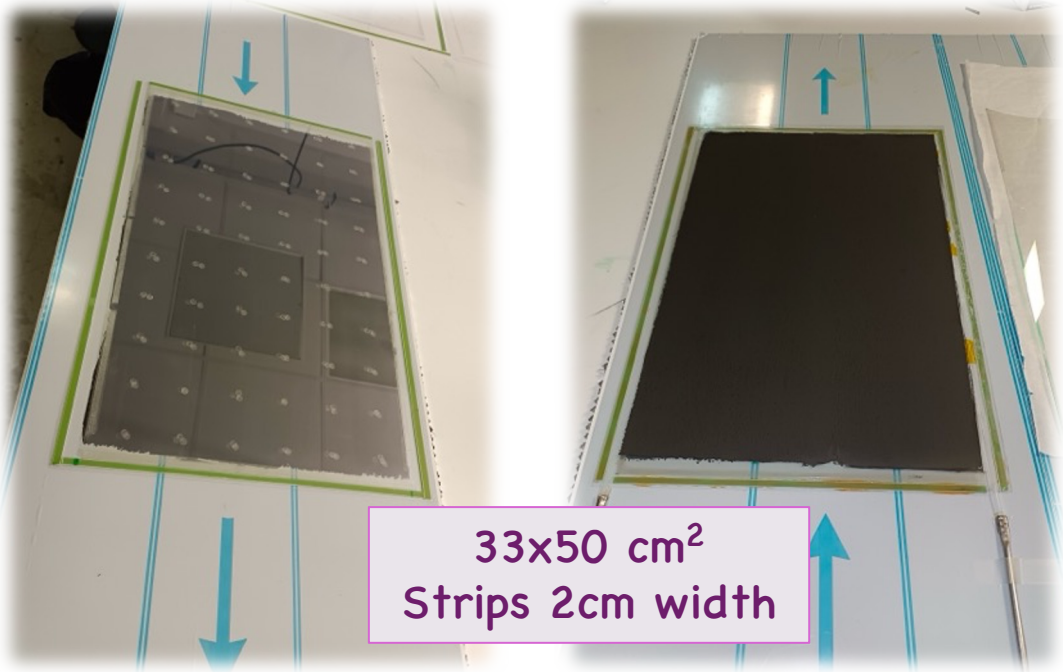
# Chamber tests ongoing @ Lyon








## ABOUT ELECTRONICS FOR SMALL CHAMBERS

**Design finalized**

48x35 cm2 ASU - 1.5 X 1.5 cm2
and the associated readout electronics.

**Production**

Pending to solve some budgetary problems

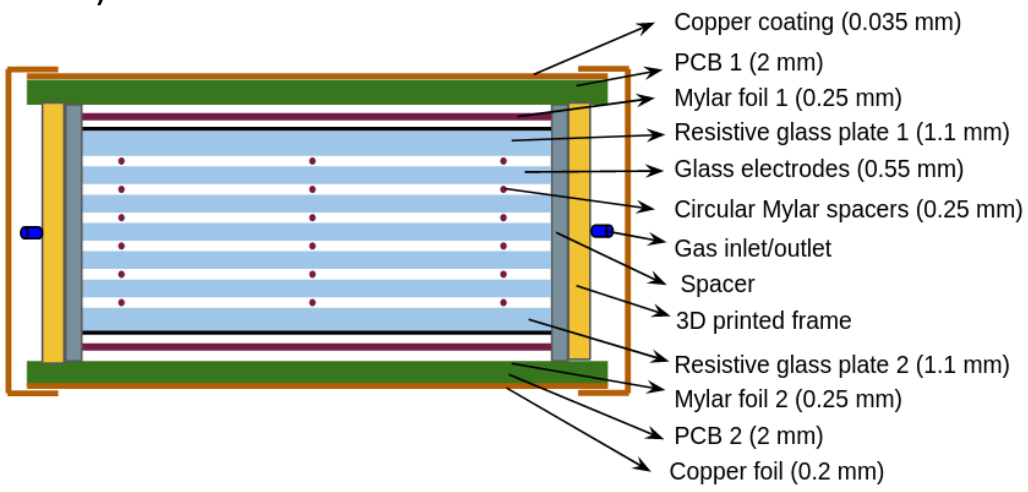
# New GRPC chambers since April 2023

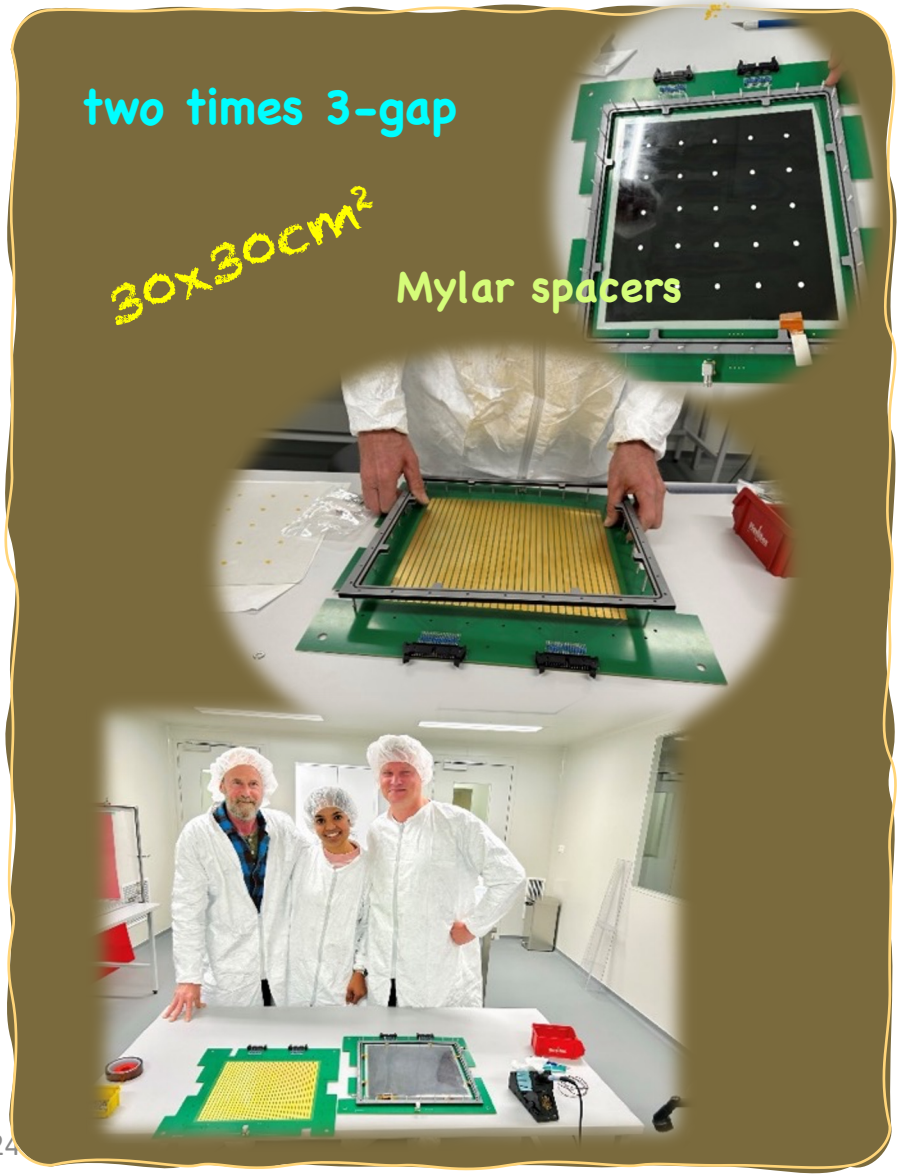


General design aims:

- Gas-tight, low volume
- No gluing which allows re-opening and disassembling chamber in case of issues
- Easily adaptable in terms of readout board
- Time resolution of O(<100ps)

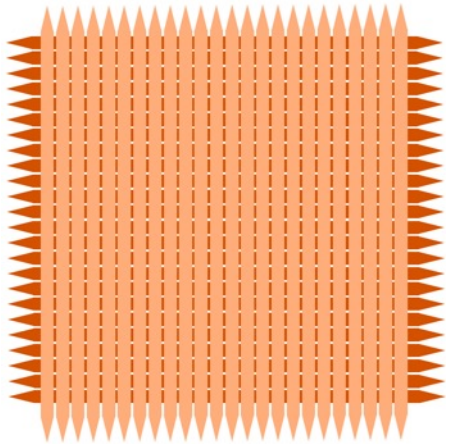
→ Gas volume contained inside gas-tight metallic frame, sandwiched between 2 Printed Circuit Boards containing strip pattern, connection to readout electronics and services (HV, T-H sensors)



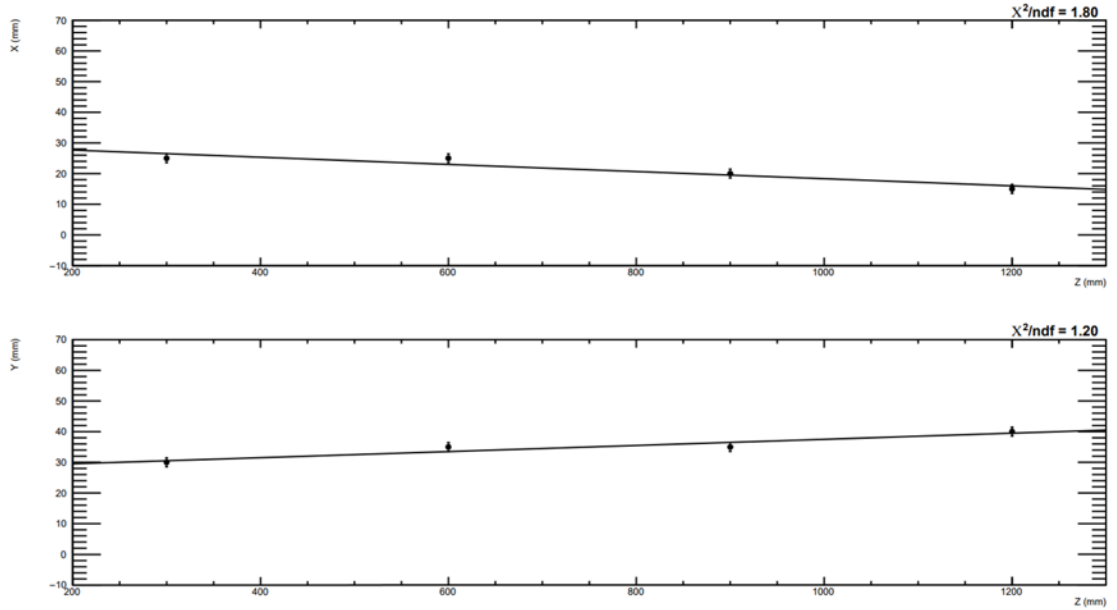



# Beam test at CERN/PS-T10 – High resistivity chambers October 2023



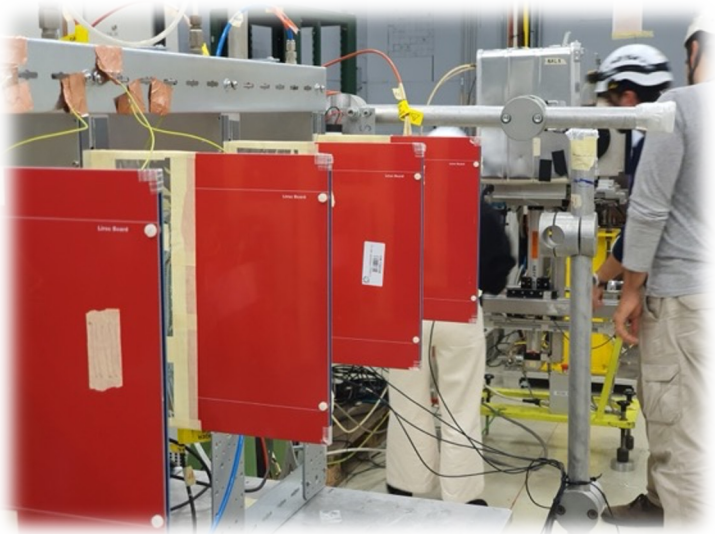


New design of chambers with perpendicular strips on both sides of the chamber




Test most focused on tracking than in high rate capabilities

4 MRPCs (high resistivity glass)



## New test beam foreseen for June 2024

Plans to

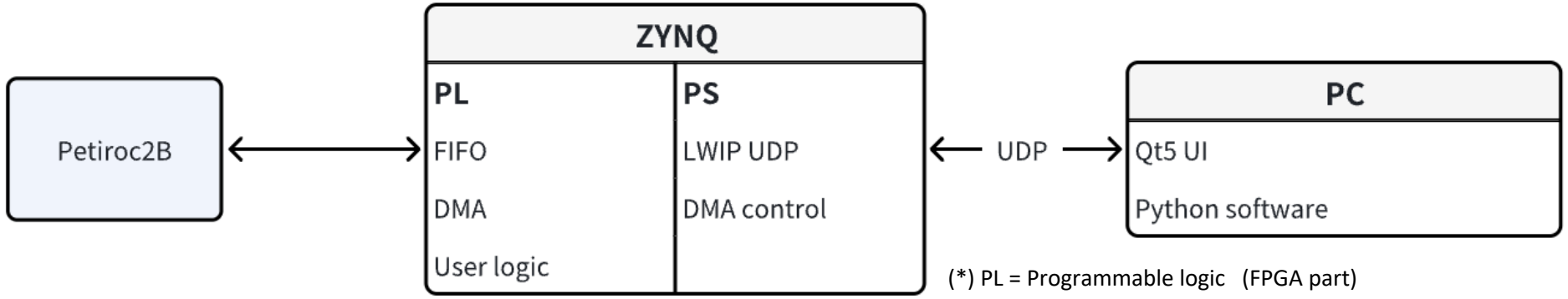
- improve the structure of the readout strips to see higher signal
- Use TOT (Time-over-Threshold) of adjacent strips to improve spatial resolution



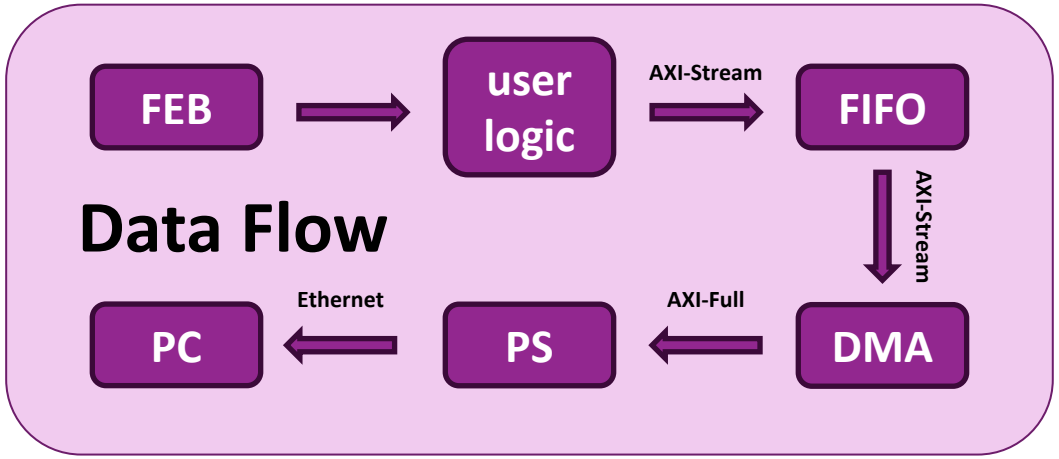
*Overlaps with Task 7.2.1*

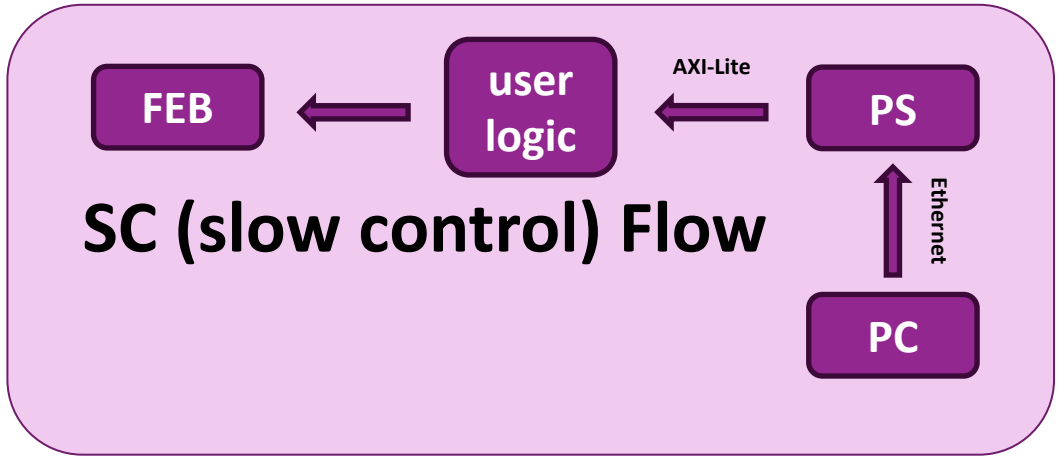
# DAQ diagram based on ZYNQ (to be used with small – 16 x 16 cm$^2$ - GRPC prototypes)





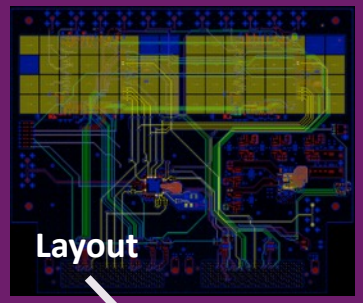

(*) PL = Programmable logic (FPGA part)
(*) PS = Processor system (Process part)
(*) DMA= Direct memory access
(*) LWIP UDP -> data transmission protocols



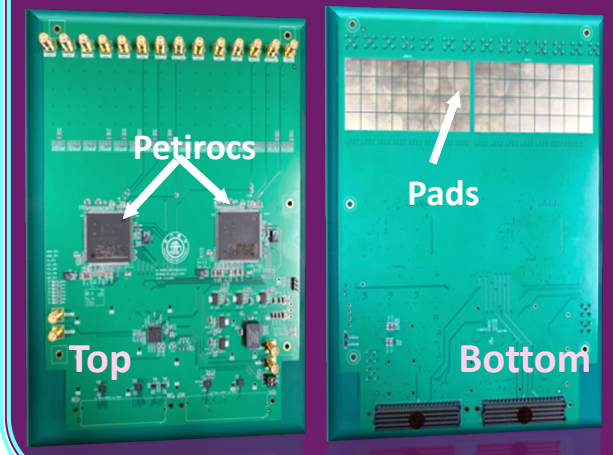
# DAQ Tests Setup





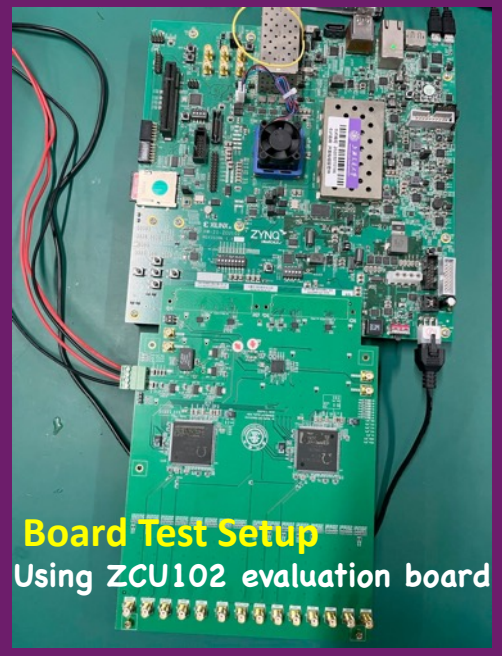

Hosting **2 Petiroc ASICs**
to readout 64 **1cm x 1cm pads**
for **16x16 cm²** detector

**Board (version2)**

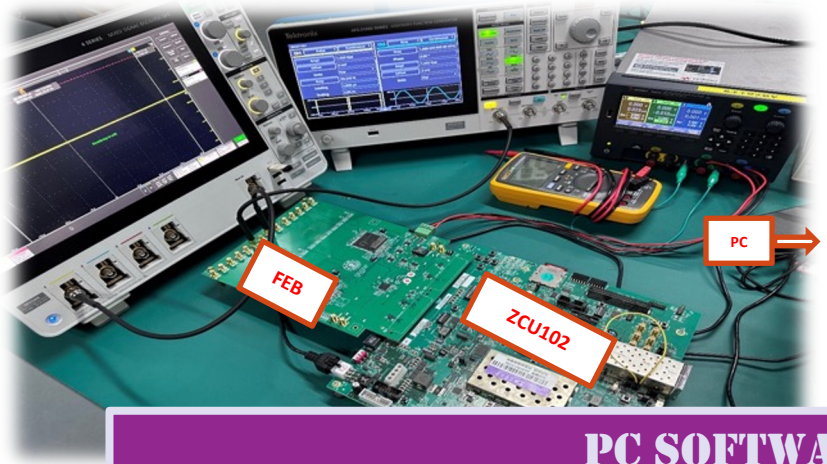









**Prototype of high-resolution timing system**

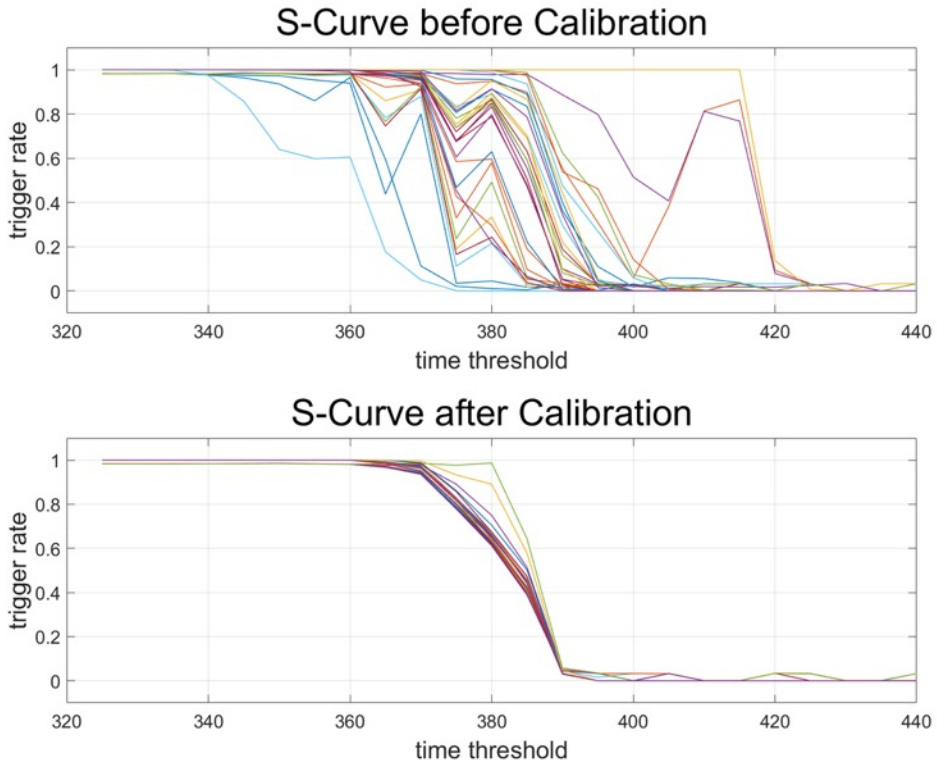


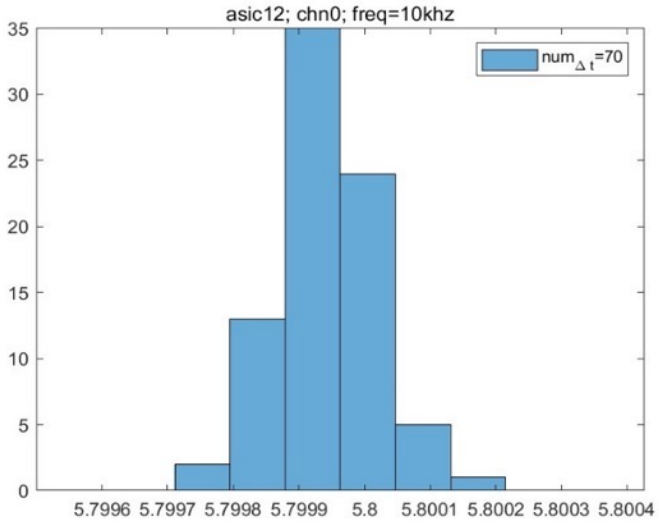

## PC SOFTWARE

- Main settings
  - Control masks, thresholds, etc.
- EN/PP
  - Control other binary configurations (ON/OFF)
- Calibration
  - Control individual DACs and offer S-curve drawing and calibration function
- Slow Control
  - For slow controls in user logic in FPGA
- Data Transmission
  - For sending, receiving and ethernet connecting

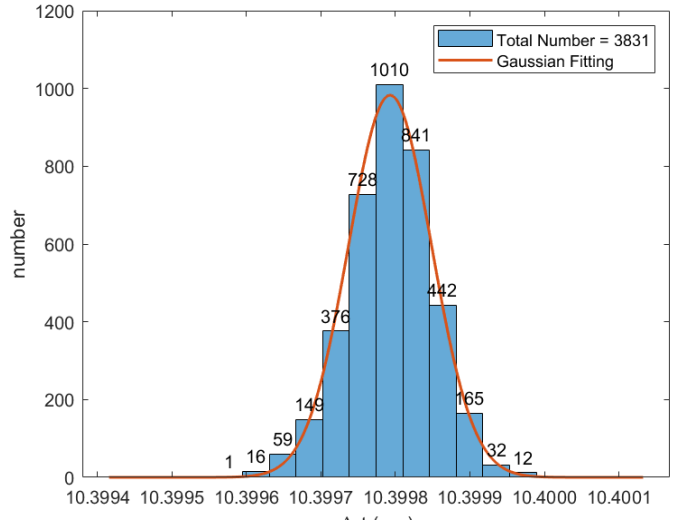
# DAQ Tests

## CALIBRATION




Timing performance tests using ILA
(std is 53.6ps, **70** instances)



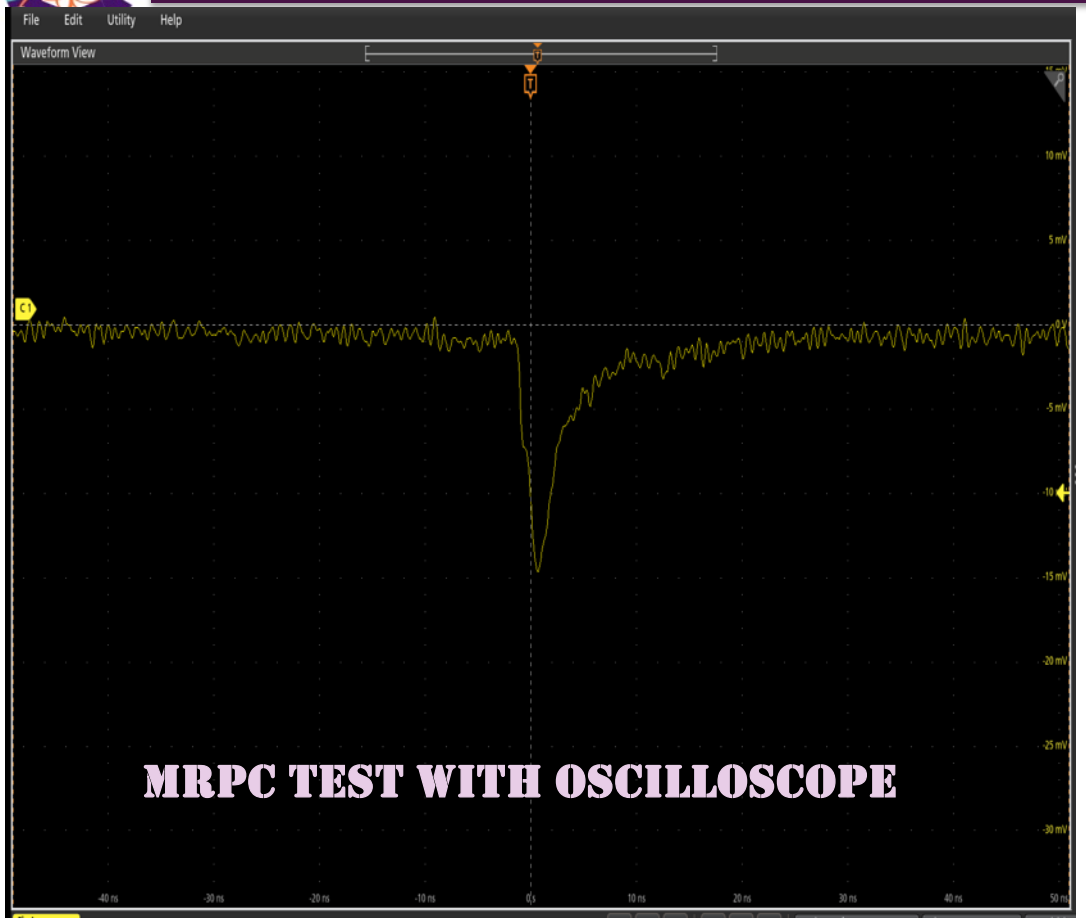

Timing performance tests using ethernet
(std is 56ps, **3831** instances)

**Ethernet communication developed.**
**It allows to receive much more data, compared to using ILA.**

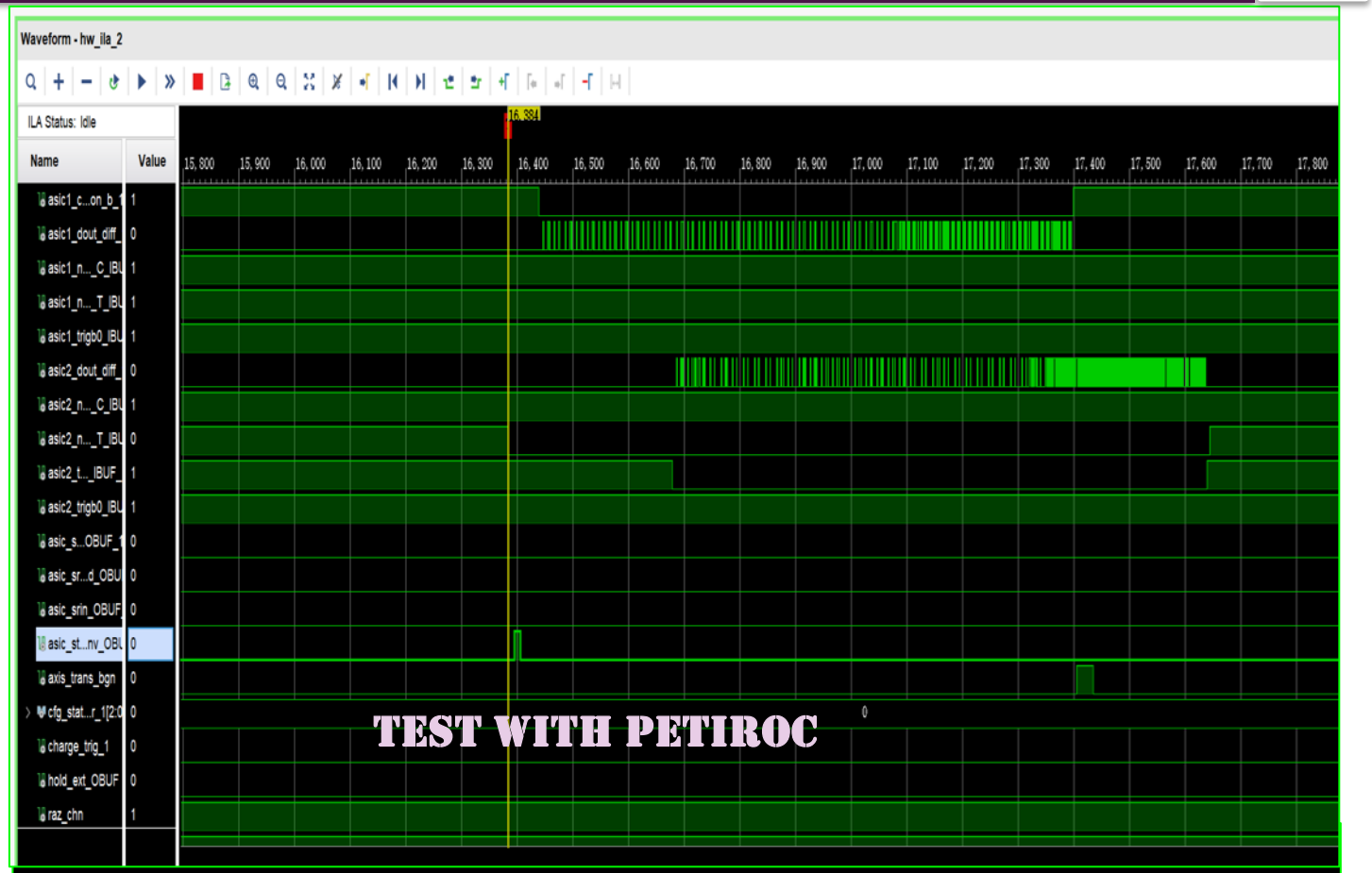
(*) ILA Integrated Logic Analyzer

# m-GRPC + electronics tests





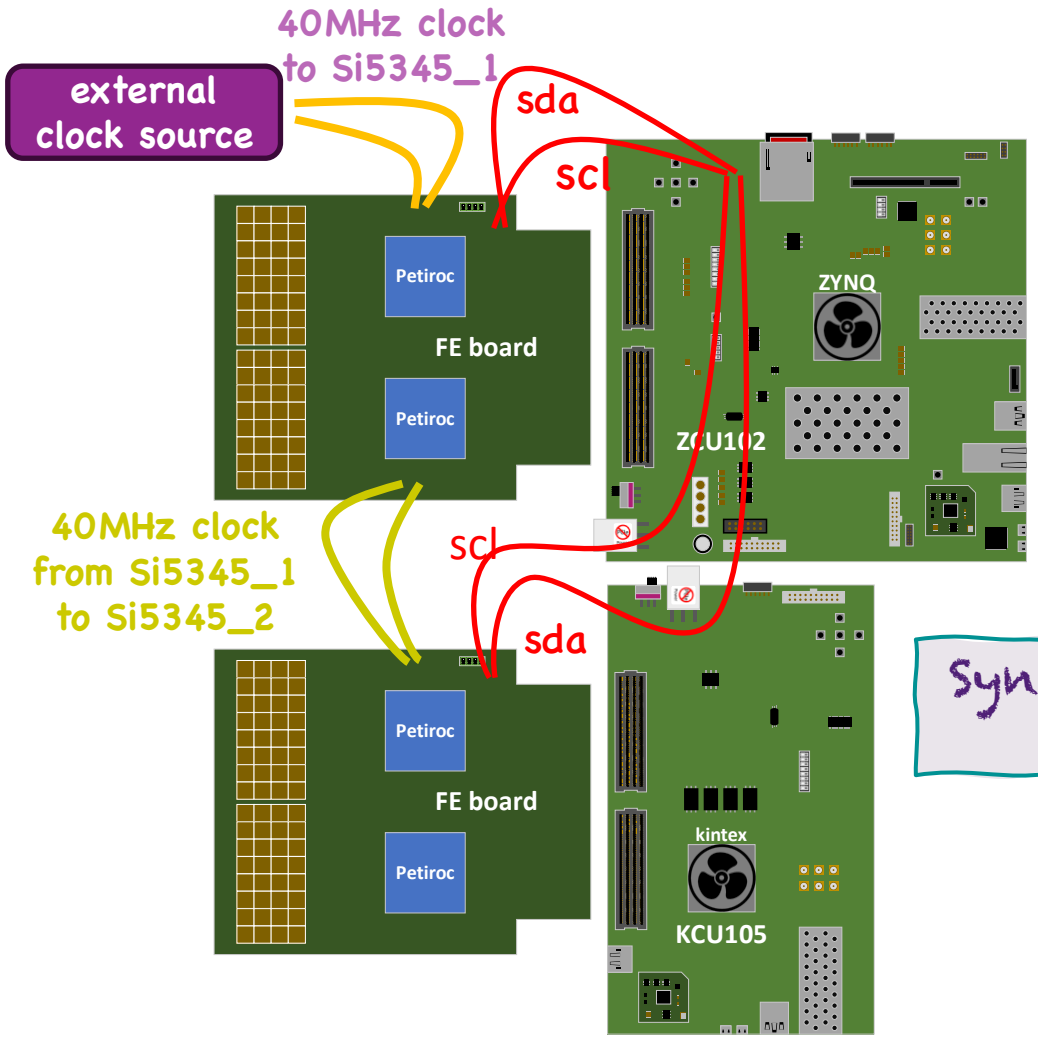

voltage 7500V
detector 10cm x 20cm copper panel
result Signals could be obtained and the signal characteristics were consistent with muons.

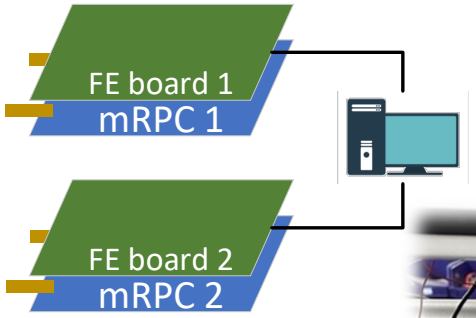



voltage 7500V
detector FE board with 2x32 1cm x 1cm copper pads
result Petiroc could be triggered by the mRPC,
if and only if mRPC voltage was turned on.

# mGRPC cosmic tests

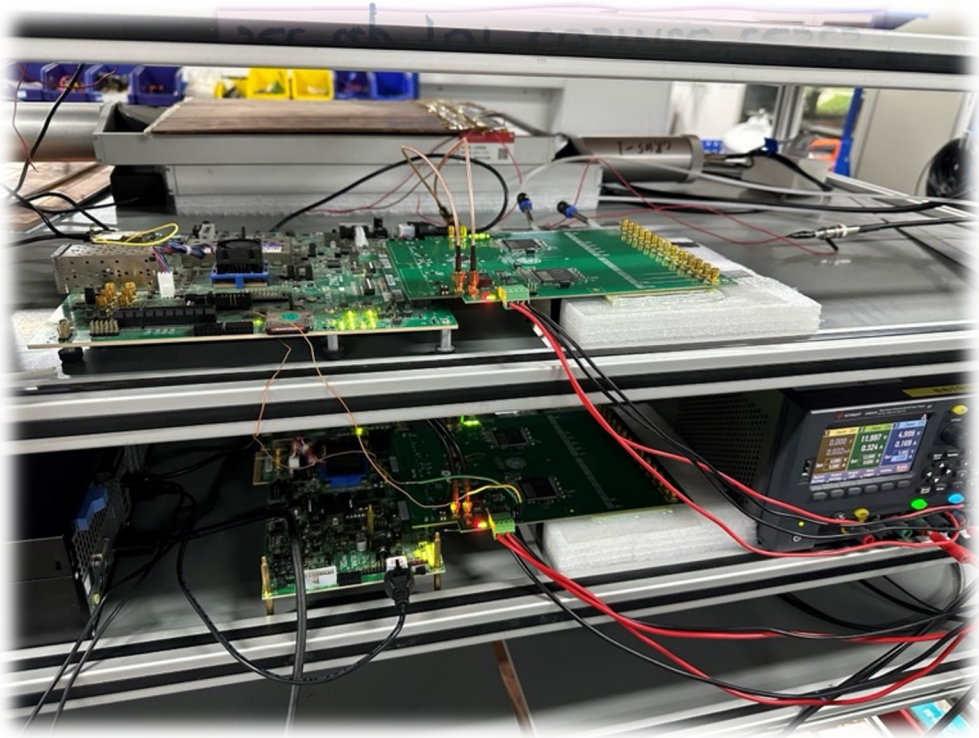





Synchronization Done

Set up for cosmic tests



*Under final development*

# Questions