WP3: Test beam and DAQ infrastructure

M. Stanitzki (DESY) and M. Wing (UCL)

AIDAinnova 3rd Annual Meeting , Catania

20 March 2024

Tasks and task leaders

- Task 3.1 Management
  - ➡️ Marcel Stanitzki (DESY), Matthew Wing (UCL)
- Task 3.2 Upgrading the EUDET-style beam telescope infrastructure (DESY, CERN, CNRS-IPHC)
  - ➡️ Adrian Herkert (DESY)
- Task 3.3 Sub-ns timing capabilities for the EUDET-style telescopes (NWO-I/Nikhef, UNIVBRIS, CSIC-IFCA, DESY, UCL, USC)
  - ➡️ Martin van Beuzekom (Nikhef), David Cussans (Bristol)
- Task 3.4 Development of DAQ software for next generation beam tests (UCL, DESY, UOS)
  - ➡️ Lennart Huth (DESY)
- Task 3.5 Development of common DAQ hardware (CERN, DESY, SRS)
  - ➡️ Dominik Dannheim (CERN)

News

- Task leaders Meeting in January 2024
  - Touch base on Status of the many upcoming deliverables
  - https://indico.cern.ch/event/1376333
- Parallel Session this morning
  - Limited WP3 attendance in person, many remote
  - Restrictions on travel take their toll

Milestones

MS #	Milestone name	Lead beneficiary	Due Date (in months)	Means of verification
MS8	Telescopes upgraded with ALPIDE sensor	12 - DESY	**Delayed** 27	New telescope in test-beam facilities (Task 3.2)
MS9	Timepix4 timing layer in telescopes	23 - NWO-I/Nikhef	**Delayed** 36	Upgraded telescope in all beamlines (Task 3.3)
MS10	Monitoring software developed	39 - UCL	30	**Use in beam tests (Task 3.4)**
MS11	Common readout boards designed	1 - CERN	23	**Prototype developed (Task 3.5)**

Deliverables

D #	Deliverable name	Lead beneficiary	Type		Due Date (in months)
D3.1	**Common cold box delivered**	**1 – CERN**	**Report**	**Was MIA Update this morning**	**39**
D3.2	New TLU produced	38 – UNIVBRIS	Demonstrator	**Delayed**	39
D3.4	New software developments available for use	39 – UCL	Report		39
D3.5	Common readout boards delivered	1 - CERN	Report		**42**

Some comments

- Details also in Highlight slides
- MS8 WP3.2 → delays because "doing the right thing"
  - A open, long-term supportable solution for the ALPIDE Telescopes
  - Development took longer, but we are convinced the long-term gains justify the delays
- MS9 is in principle in reach, needs a bit longer, "justification for delay" being written
- No real show stoppers in either
- D3.1 – WP Management has received no updates
- D3.2 - will be delayed by approx 6 month - tbc

WP Highlights

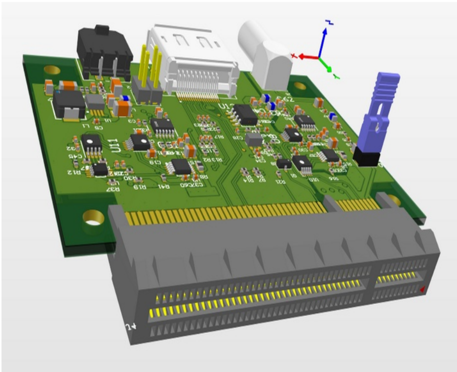
WP3.2 Beam Telescopes
Status of MIMOSA telescopes

- DESY
  - The two remaining telescopes running like clock-work
- CERN
  - Keep getting reports from user's that infrastructure is slowly decaying and not enough effort is allocated to keep them running
- Why do we care ?
  - We are running very low on MIMOSA26 sensor plane spares
  - There was also a strong push from parts of AIDAInnova to keep MIMOSA26 running as long as possible -> superior point resolution

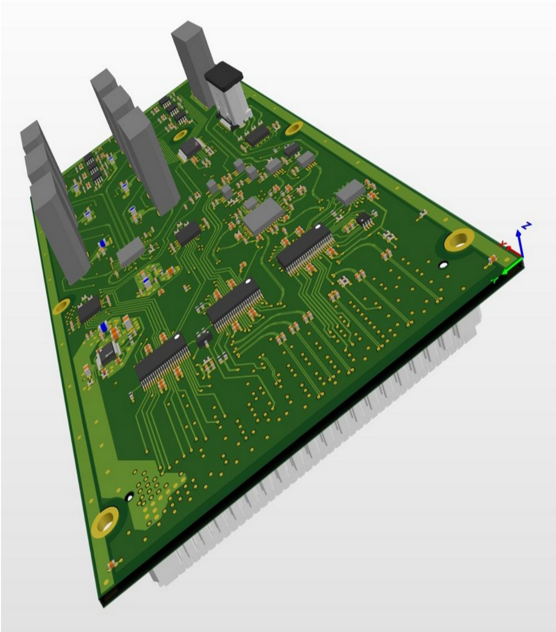
WP3.2 Beam Telescopes

- Milestone was officially delayed by 6 months due to
  - Issues with “mass” production based on first prototype (which is in user operation at DESY and performs excellently)
  - Component shortages
  - No long-term support guaranteed
- New prototype being developed, this time in-house at DESY to avoid issues of first design and being fully open-source
- Based as much as possible on components used also in other common infrastructure projects (mostly Caribou DAQ system, see WP3.5)
  - New expected delivery date (end of 2023) was calculated too tightly
  - Manpower currently limited
  - Still constant progress being made (see next slide), only slower than expected

WP3.2 Final ALPIDE System



- 1 Enclustra system-on-module (SoM) + base board
  - Commercial product used also for Caribou;
  - flexibility in choice of exact model as long as pin-compatible,
  - several at hand at DESY for development phase
- 6 ALPIDE sensors on ALICE chipboards
  - DESY got end-user license; 60 paid,
  - 30 expected to be delivered within the coming weeks
- 6 chipboard interface cards
  - Design finished; to be submitted very soon
- 1 adapter card to interface 6 telescope layers with 1 SoM
  - Design finished; to be submitted very soon
- Software (based on Caribou's PEARY) and firmware
  - Work in progress



WP3.2 Beam Telescopes MS8 and D3.3

- MS8: Telescopes upgraded with ALPIDE sensor
  - Already delayed
- As soon as 2nd prototype is tested and working (expected for summer 2024):
  - Milestone report on both prototypes
  - Production of as many copies as requested
- D3.3: Telescopes upgraded with new layers (due in month 46)
  - "Telescopes upgraded and available with precise timing layer and next generation sensors (Task 3.2, Task 3.3)"
  - A second upgrade with "a suitable next-generation sensor, to be developed within the CMOS DMAPS WP5", as considered in 'Description of work and role of partners', does not seem realistic in the mean time
- An ALPIDE-based beam telescope with an additional integrated timing layer is suitable as successor of the EUDET-type beam telescope
  - The goal is to deliver the best possible version of this

WP3.2 D3.1

- Deliverable
  - Two cold box adapted for use in the beam telescopes at DESY and CERN
  - Submitted an extension to EU of deliverable 30 June 2024
  - Schedule compatible with coldbox for June 2024 AIDAinnova testbeam @ CERN
    - Working to meet this deadline

29th September 2023

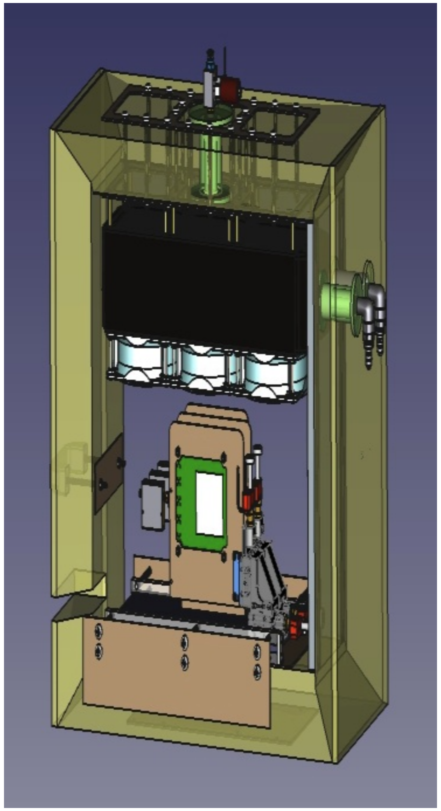
Delay on:	**D3.1 Common cold box delivered**
Delivery Date in Annex 1:	M30 (30th September 2023)
Expected Delivery Date:	30.06.2024

- Status of ongoing work
  - Collaboration ongoing with CERN (requirements), Univ. Zurich (design) and JCLab (manufacture)
  - Preliminary design (Vagelis Gkougkousis) in discussion

Slides as of this morning and shown as is
Not yet “digested” by Task and WP leads

WP3.2 D3.1

- Status of ongoing work
  - Finalising the design
  - Main features
    - Interior size min. 22cm x 34cm x 30 cm
    - x/y positioning by heavy duty linear stage, low precision
    - Control software for position, chiller and nitrogen/dry air low with eudaq option
    - Temperature <~-40°C with pre-cooling
    - Universal cable feedthroughs
  - Open points
    - Chiller type
    - Possibility for DUT rotation inside box
  - Final quotes and manufacturing to follow



Slides as of this morning and shown as is
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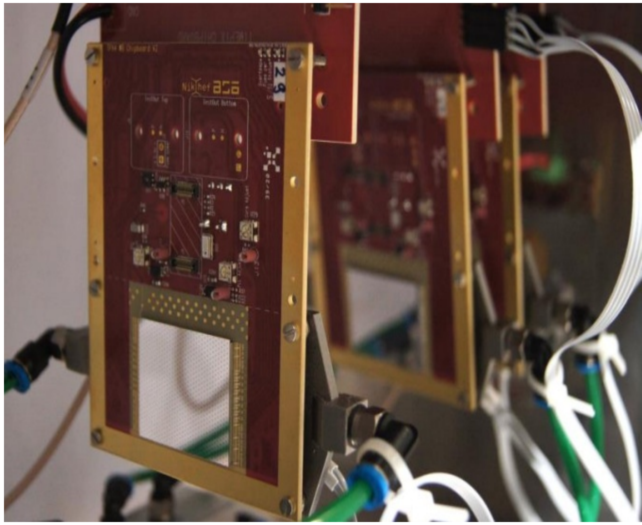
Task 3.3 Timepix4 timing layer

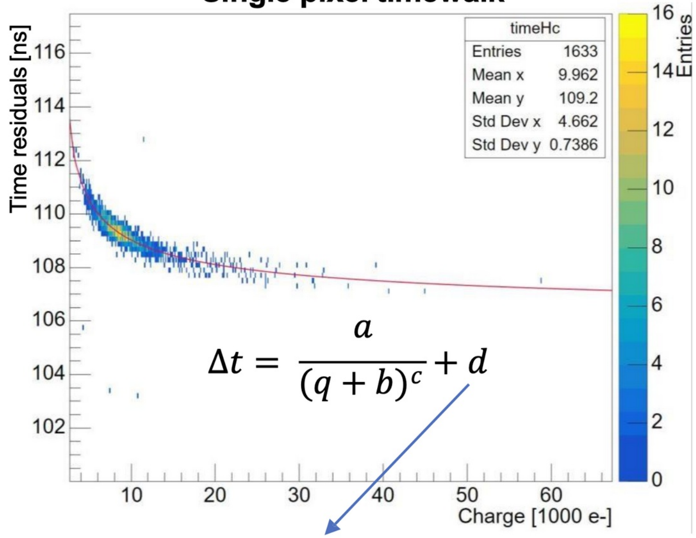
- Main objectives:
  - Sub-ns timing capabilities for the EUDET-style telescopes
  - 3.3.1: Integration of a TimePix4 plane into EUDAQ2 (NWO-I/Nikhef)
- Milestones:
  - *MS 9 [M36]:* Timepix4 timing layer in telescopes
    - Hardware
      - Extensive bench and beam tests with Timepix4 ASIC
      - SPIDR4 boards produced and tested
      - Timepix4 chipboard produced and tested
      - TLU compatibility to be checked
      - 2 TPX4 wafers, bump deposition ongoing at IZM (WP6)
      - Waiting for fast sensors from WP6
    - EUDAQ2 integration ongoing
      - With help from Uni. Hamburg and IFCA
    - Mechanical and cooling integration started

Timepix4v2 sensor assemblies at SPS beam test



Task 3.3 Timepix4 timing layer

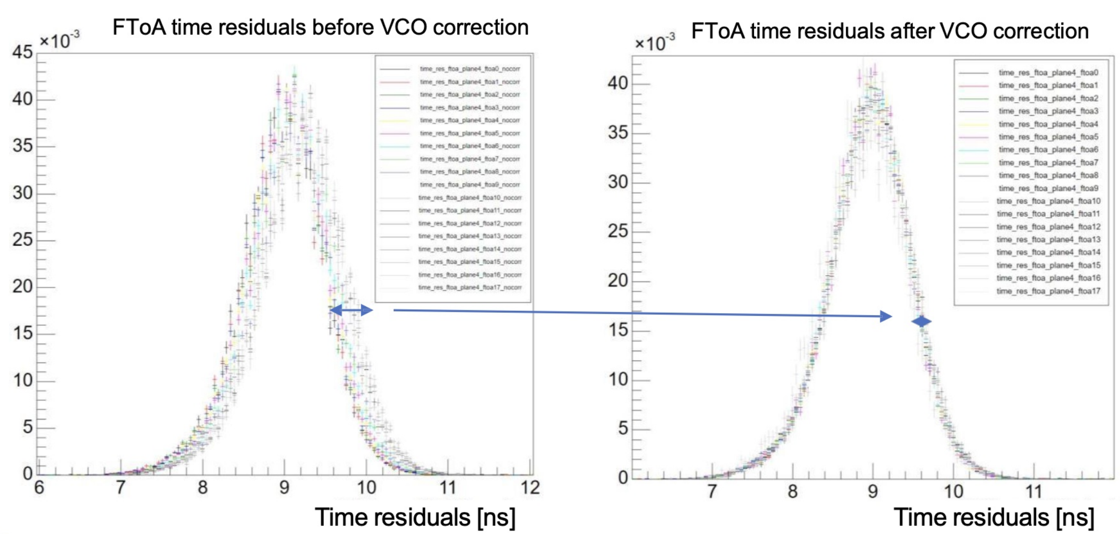
- Main results:
  - Four 100 and four 300 mm sensors on Timepix4v2 tested in telescope configuration at SPS
  - Stable operation, 10+ hours without reconfiguration
  - Achieved time resolution of 170 (best) – 185 (worst) ps for 100 µm planar sensors
    - Requires per pixel timewalk correction
    - And per superpixel calibration of Voltage Controlled Oscillator (VCO)
    - Time resolution is limited by planar sensor, faster sensors from WP6 in pipeline



$$\Delta t = \frac{a}{(q+b)^c} + d$$

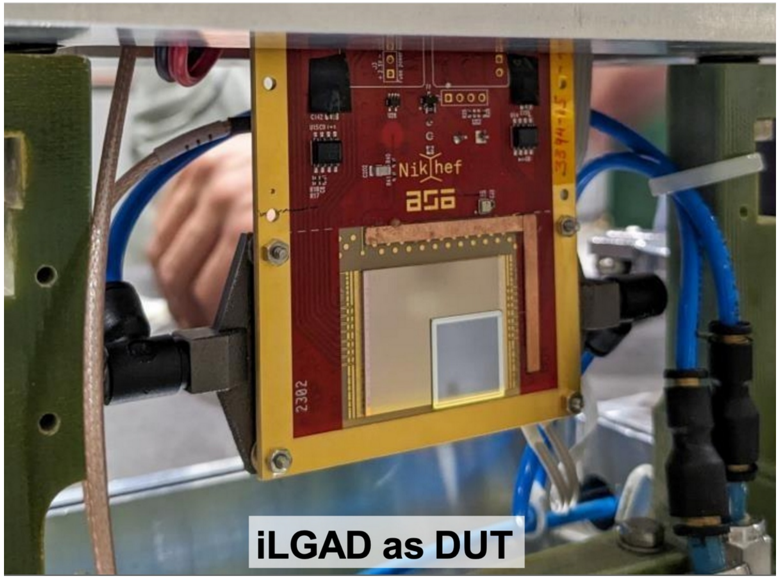
Timewalk correction includes per-pixel oscillator offset

Frequency variation of oscillators (VCO) across chip, corrected offline

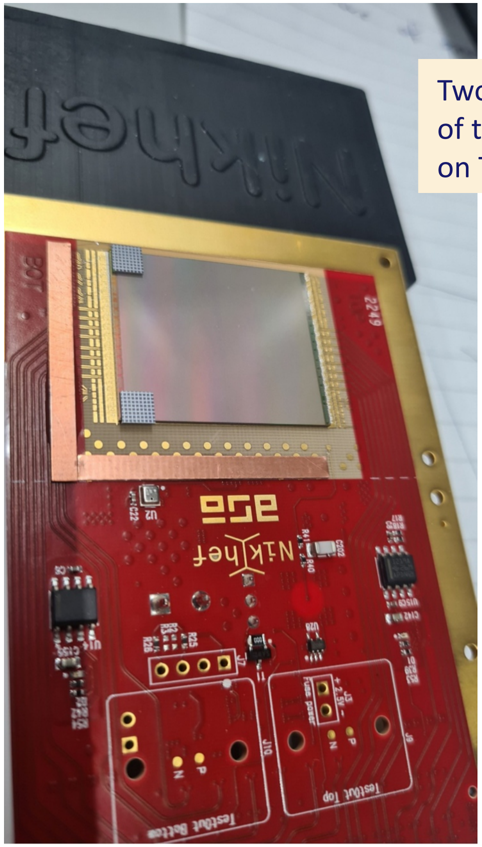


- Outlook:
  - Time resolution is limited by planar sensor, faster sensors from WP6 not yet available
  - Therefore using sensors from other projects, to gain experience with devices with gain
    - iLGAD from Glasgow group
    - Trench Isolated LGAD from RD50

256x256 pixel inverted LGAD on Timepix4

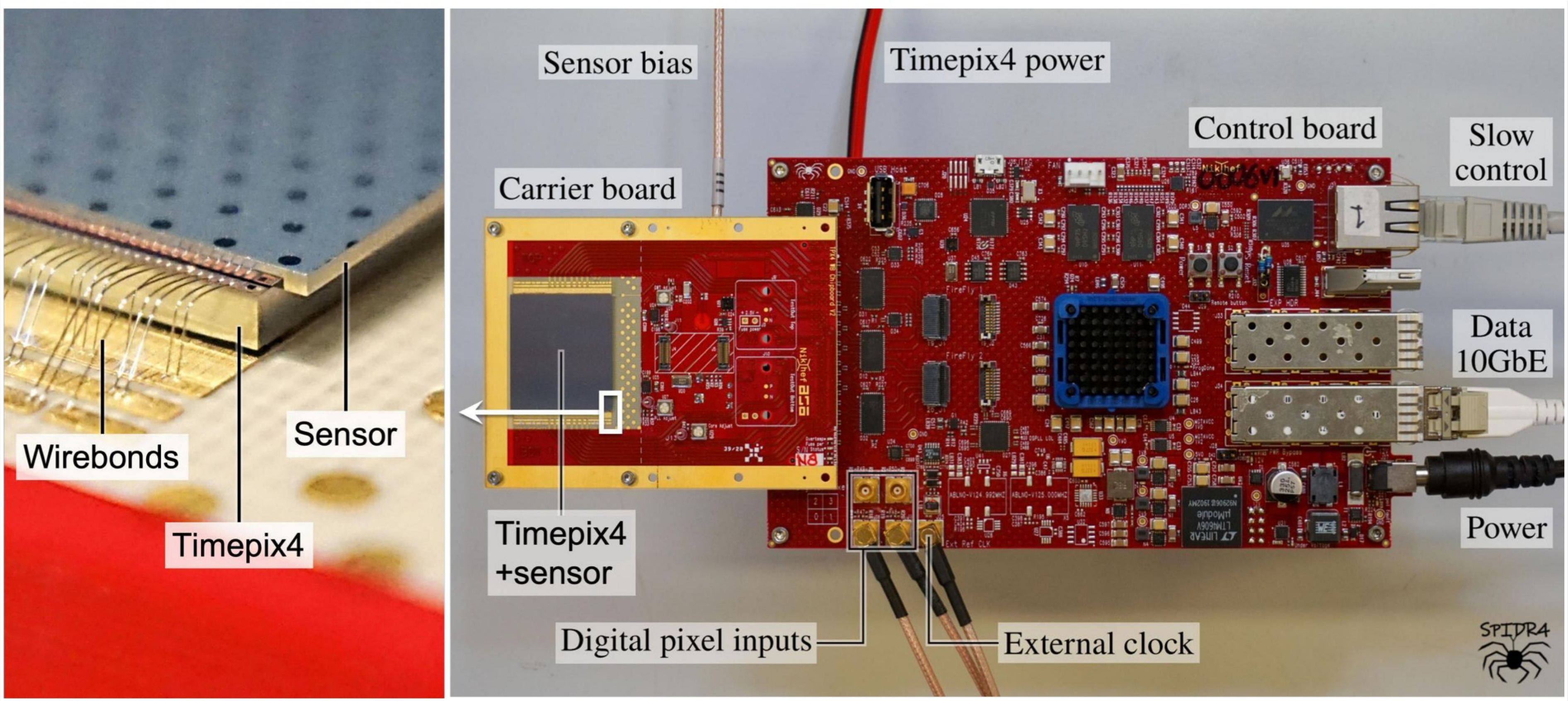


Two 55x55 pixel matrices of trench isolated LGAD on Timepix4



Task 3.3 Timepix4 timing layer

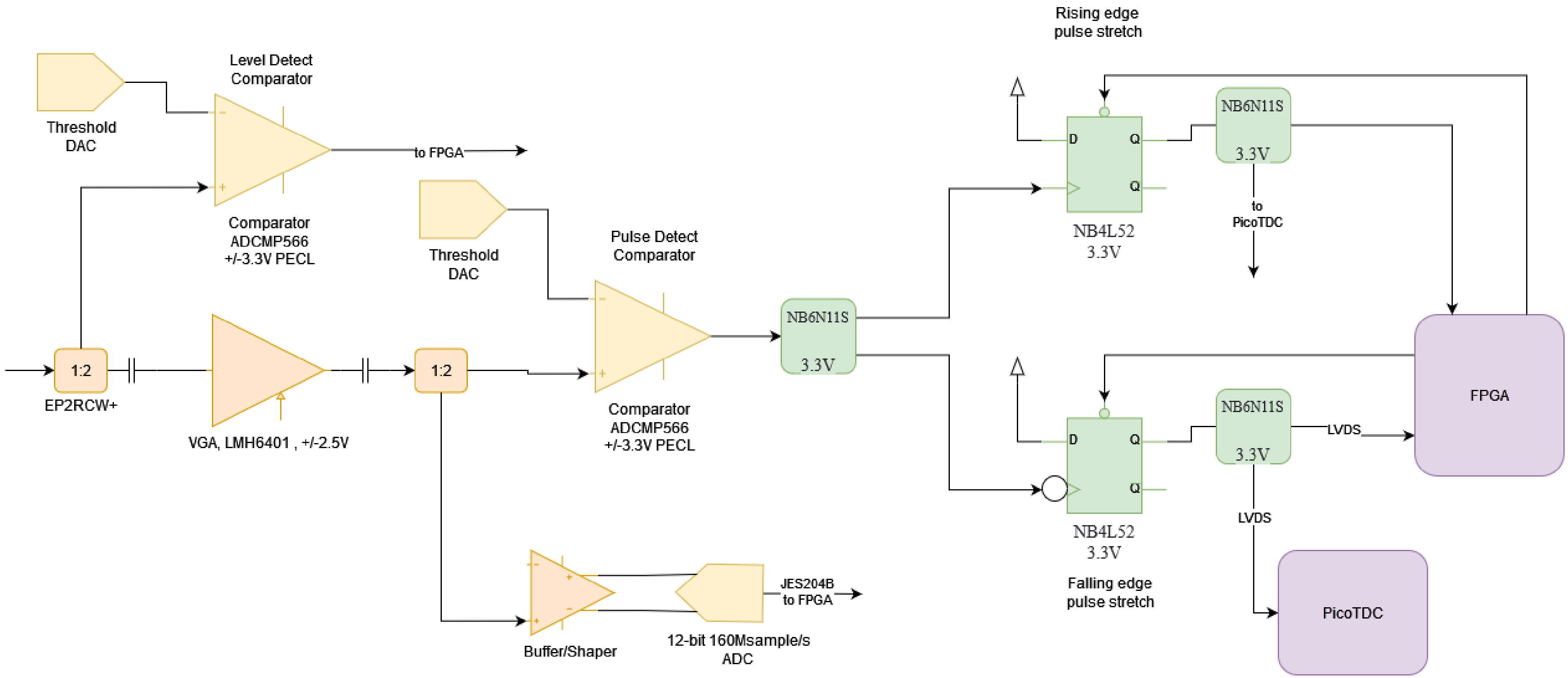
SPIDR4 readout



Task 3.3 Picosecond TLU

- Input structure design underway
  - Two discriminators
    - One DC coupled for level detection
    - One preceded by variable gain amplifier for accurate timing of low-level pulses
      - 160 MSample/s ADC for time-walk correction
      - Pulse stretching on both rising and falling edges.
- Schematic capture in progress
- Investigating two methods for time-stamping:
  - PicoTDC (default)
  - Carry-chain delay-line TDC in Xilinx Artix UltraScale+ FPGA
- Optimizing timing resolution for small amplitude fast rise signals.
  - Use case: single-anode MCP-PMT used as a timing detector
    - Cherenkov light produced in face-plate
    - Single photon timing jitter ~ 30 ps

Task 3.3 Picosecond TLU



Task 3.3 D3.2 Timeline

- Revised Timeline
  - By June, should have hardware prototypes of the front-end.
  - Prototype of full hardware ready by October 2024. May have firmware.
  - Enough testing done to allow production of more units by December
  - "production-ready" units tested Jan 25
  - Software and full integration (with EUDAQ2) will take longer. Hopefully by Jan 25
- With this D3.2 “New TLU delivered” moves to M46 (was M39)
- “Justification of Delay” being prepared

Task 3.3 TLU Availabiliy

- AIDA2020 TLU availability
  - It's in short supply, mass production has ended
  - Component availability is a real issue → Some components are not available anymore
  - Some Efforts to update design/layout to be able to remake small quantities
- Lessons learned
  - Don't let to much time pass between prototype and mass production
  - Have a Production Readyness Review
- Picosecond TLU Mass Production
  - Once we have a working prototype, prepare mass production
  - Call to user community → be generous, Making 30 or 60 is almost no difference in effort
  - Restarting production is ...

WP3.4 Common DAQ software MS 10 Achieved

MS10	Monitoring software developed	WP3	3.4	M30	30/09/2023	Achieved	Report

AIDAinnova

Published September 30, 2023 | Version v1

Project milestone | Open

Monitoring software developed

A. Loeschcke Centeno [1]

Show affiliations

Online monitoring tools have proven to be indispensable in test beam activities. As such, many test beam users implement their own monitoring tools tailored to their needs. The goal of work package 3 in the AIDAinnova project is to develop a common test beam and DAQ infrastructure. This encompasses the development of an online monitoring system which is implemented as part of the EUDAQ2 framework. In this document, we present the status of the development of such an online monitoring tool and demonstrate the ability to run the monitoring in different setups.

Files

AIDAinnova-MS10.pdf

Page: 1 of 14 Automatic Zoom

Grant Agreement No: 101004761

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Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

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AIDAinnova-MS10.pdf md5:1e4551ac33b828d0aa104a2366176b60	837.0 kB	Preview Download

Additional details

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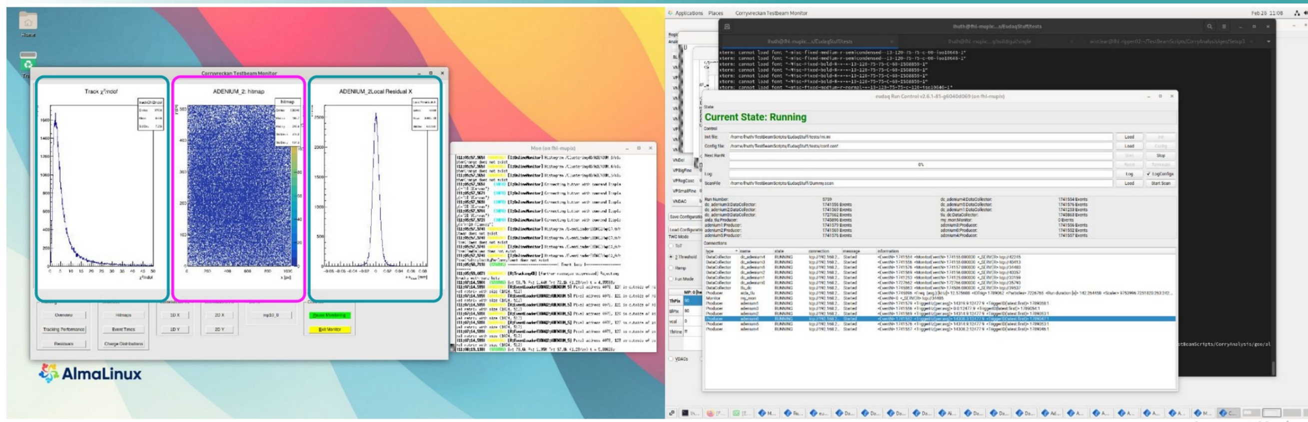
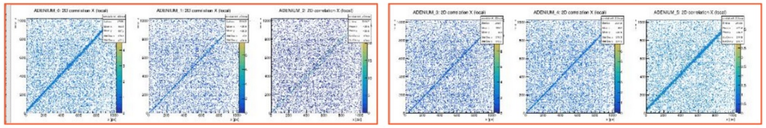
WP3.4 Common DAQ software Deliverable Status



courtesy: Lennart Huth



- Software already in use and tested
  - Telescope at DESY
  - AHCAL test beam
  - Dual Readout Monitoring
  - Working on deliverable report
- Implementing feature beyond the tasks objective now
  - Distributed file reading via XRootD

20 March 2024

Task 3.5.1 Common Caribou DAQ

- Caribou flexible DAQ system for silicon-detector testing (CERN, DESY)
  - Based on modular hardware, firmware and Peary software
  - Successfully used by several AIDAinnova / RD50 (DRD3) institutes for various pixel projects
  - AIDAinnova milestone and deliverables combined with VMM3 (slides 3, 4)
  - Support from EP R&D, RD50 (HW production) and BNL / Carleton / ORNL (HW design)
- **2023 achievements:**
  - Milestone: MS11 achieved – design of common readout boards
  - Device integration: 65 nm demonstrator chips APTS, DPTS, H2M (DESY/CERN) fully integrated in Caribou, including beam-telescope setups, several beam tests and published results
  - New features: implemented TDC in FPGA, used for picosecond timing of digital signals
  - Consolidation of firmware: New modular firmware architecture proposed and implemented, currently under test at CERN
  - New hardware revision: Carboard v1.5 (BNL): Re-spin of v1.4 with minimal changes (replacing obsolete components, bug fixes); prototype produced, validation at BNL and CERN ongoing

Task 3.5.1 Common Caribou DAQ

- **Plans for 2024:**
  - Deliverable D3.5 - common readout boards delivered:
    - prototype v1.5 produced by BNL, currently under validation at BNL, CERN (see previous slide)
    - Integration in Ultrascale+ FPGA platform as intermediate step towards new SoM platform
    - ~20 Carboard v1.5 to be produced (offers received, 8-10 weeks delivery), asking for DRD3 common-funds support
    - Backup: Carboard v1.4 (already delivered)
  - Carboard v2.0 (BNL, Carleton, ORNL):
    - Based on Ultrascale+ System-On-Module platform
    - design in progress @ BNL
    - final specifications by 4/2024, aiming for first prototypes in 2025
    - RD50/DRD3 common project for production of v2 Carboards (R. Palomo, Sevilla)
  - Consolidation of firmware, documentation, user support:
    - First use case for new firmware architecture: RD50 MPW sensors – Sevilla/CERN student project (J. Jiménez Sánchez)
    - New project web page: https://caribou-project.docs.cern.ch/
    - Will resume regular developer / user meetings in the coming weeks

Task 3.5.2 Common VMM3a DAQ

Development of the SRS/VMM3a common readout board to support gas detector R&D

Achievements in 2023 (driven by the needs of the gas detector community in RD51 and DRD1)

- **Distributed, large lever arm telescope (10-20m).** Relevant for future DRD1/GIF++ test beam campaigns at the CERN North Area.

→ Successful operation due to new powering scheme (PBX) [1]. Synchronization with 20 m long HDMI cables between beam telescope and DUT for HCAL application [2] was achieved [3].

- **Test beam operation and detector characterization.**

→ GEM-Detector prototype for AMBER, optimization of spatial resolution in triple-GEM detectors [3], GEM-TPC for MIXE experiment @ PSI [3].

- **Externally triggered readout.** Relevant for integration of the system in existing experiments' DAQ system and reduction of noise acquisition.

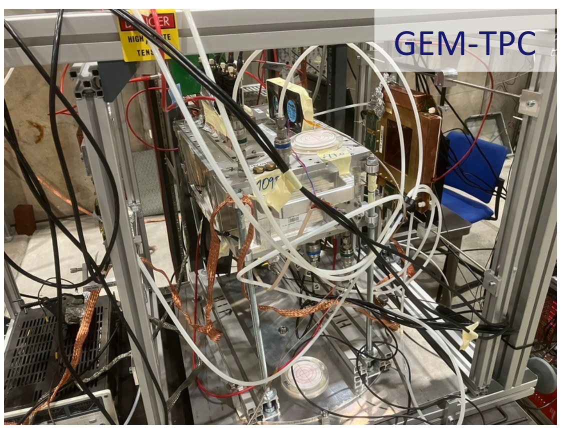
→ RD51/DRD1 colleagues from FRIB @ MSU implemented custom SRS triggered mode, as well as the ATLAS L0 mode of the VMM3a.

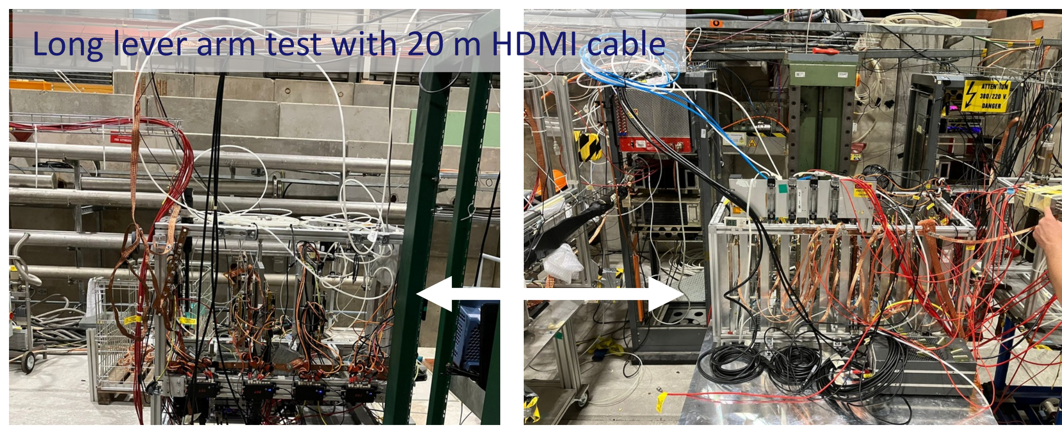
Task 3.5.2 Common VMM3a DAQ

Plans for 2024

- Performance evaluation of both triggered modes in the upcoming test beam campaigns.
- Continue detector characterization and optimization, including GEM-TPC.
- Hardware production for D3.5 started, expected delivery end of 2024.

Colleagues from TOTEM are working on integrating SRS (with APV25 front-end) in EUDAQ2 for consolidation of their test beam facility at the H8 beam line [4]





Summary and Conclusions

- WP2 is advancing reasonably well
  - Some deliverables are coming later – but we clearly understand why
  - Mainly not as much technical effort available as desired
- In WP3.2 there is a real danger of not achieving the “Common Cold Box” deliverable
  - Also the “decay” of the MIMOSA26 infrastructure is worrying
- All other milestones and deliverables are either on-track or already done
- Thanks to Adrian, Martin, David, Lennart and Dominik for providing material and slides