Third annual meeting

Catania 21 mar 2024

WP 11

Microelectronics

A. Rivetti (INFN) Ch de La Taille (CNRS)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

WP11 Objectives

- **Task 11.1. Coordination and Communication [CNRS+INFN]**

- **Task 11.2. Exploratory study of advanced CMOS (28 nm)**
  - INFN PV, AGH, CNRS CPPM, UBONN
  - Explore advanced 28 nm CMOS for future trackers AGH, CNRS CPPM
  - Design and test front-end prototypes INFN PV, UBONN

- **Task 11.3. Networking and ASICs for other WPs (65/130 nm)**
  - AGH, CNRS OMEGA, IP2I, DESY, INFN (BA, BO, PV, TO) Uni Heidelberg, WEEROC (industry)
  - Cold and timing ASICs in 65/130nm CMOS : CNRS OMEGA, IP2I
  - MPGD readout ASICs : INFN (BO, TO)
  - Silicon and SiPM readout ASICs for future colliders and timing applications : AGH, CNRS OMEGA, DESY, UniH, WEEROC

WP11 session : 18 mar 24

14:00	207 - introduction	*Angelo Rivetti et al.*
	208 - WP11.2 28 nm update from CPPM	*Mohsine Menouni*
	209 - WP11.2 28 nm update from INFN PV	*Luigi GAIONI et al.*
15:00	210 - WP11.2 28 nm update from AGH	*Marek Idzik*
	212 - WP11.2 28 nm update from U Bonn	*Mr Kennedy Caisley*
16:00	**Coffee break**	
	211 - WP11.3 130nm update from AGH	*Marek Idzik*
	214 - WP11.3 130nm update from CNRS/OMEGA	*Mr Damien Thienpont et al.*
	218 - WP11.3 130nm update from INFN/TO	*Andrea Di Salvo et al.*
17:00	219 - WP11.3 130nm update from WEEROC	*JULIEN FLEURY*

28 nm @CPPM [Moshine Menouni]

28 nm chip design

R&D on hybrid pixels

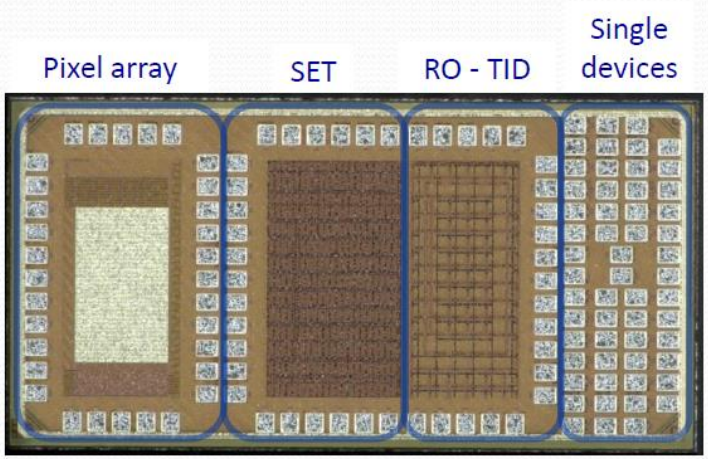
- Process qualification in terms of performance for analog, low-power and low-noise circuits
- Architecture studies
- Fast charge amplifier array

Study of Single Event Effects (SEE)

- Measure the SET cross-section
- Measure the SET pulse width with a good resolution < 20 ps
- Measure the effect of the std cell size

TID tests and qualification

- Compatibility with typical dose levels for future projects
- 28 nm process device qualification
- Gate delay evolution with TID and the effect of the std cell size
- TID Effects modeling → Analog and digital simulations with TID effects



Mini@sics of 2×1 mm2 received June 2024, consisting of 4 main blocks

- Analog pixel array (25×25 µm2) with Fast charge amplifiers for high time resolution
- SET test structures
- Ring Oscillators for TID tests on digital standard cells
- Test structures for TID tolerance studies

28 nm @CPPM [Moshine Menouni]

Conclusion and perspectives

28nm prototype test boards received the beginning of 2024

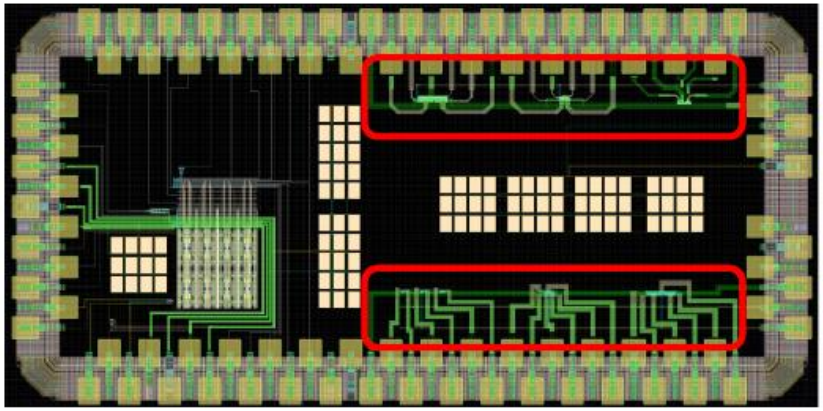
- Testing has just started and first results are quite promising
- 4 chips to be tested and characterized
- Existing test-setup based on a beagle-bone board to be used

Continuation of the project

- The project is part of the IN2P3 R&D DEPHY project
- Functional tests to be done in Q2 2024
- Irradiation tests (TID and SEE) in Q3-Q4 2024
- A new 28 nm design focused on pixel array with the possibility to be bump bonded with sensor array
  - Use of CERN PDK makes the design more manageable
  - Prototype submission scheduled for Q4 2024

Technology characterization

- 18 differently sized core, standard-threshold devices, both P-channel and N-channel in triple well
  - channel length: 30 nm, 60 nm and 180 nm
  - channel width: 100 um, 200 um and 600 um (finger width Wf = 2.5 um -> 40 , 80 and 240 fingers)



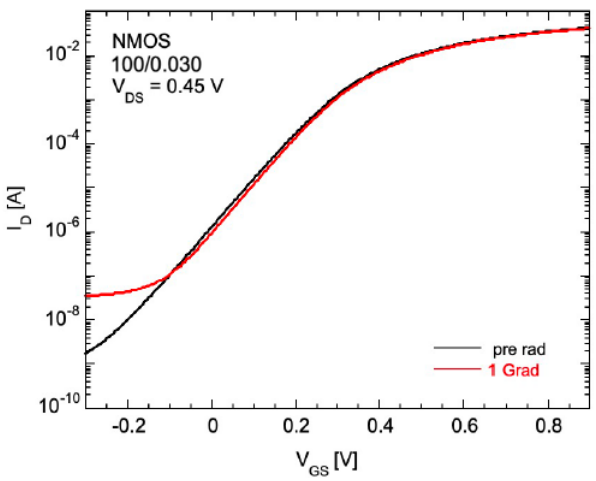
- **Static and signal parameters** measured with an Agilent B1500A Semiconductor Parameter Analyzer
- **Noise power spectral density** measurements carried out with an HP4395A Network/Spectrum Analyzer and a noise amplification system
  - Drain current in DUTs: from 50 µA to 500 µA → low power operation as in high density front-end circuits

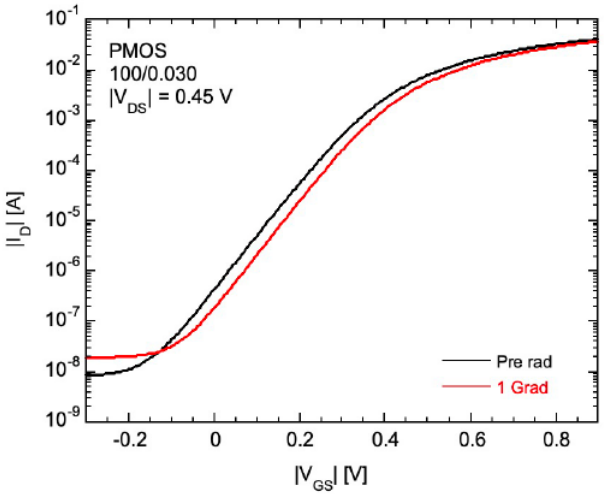
Ionizing radiation effects

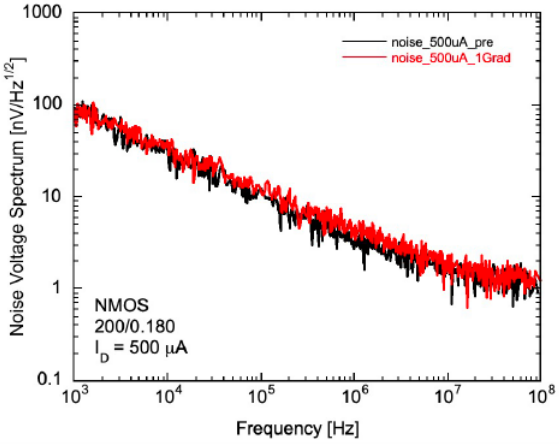
- Investigated devices **irradiated up to 1 Grad(SiO_2)** total dose with X-rays (5.5 Mrad/h dose rate)
- MOSFETs biased during irradiation in the **worst-case condition**
- Slight increase in drain leakage current after irradiation
- **Limited threshold voltage changes** (depending on MOS polarity and geometry)

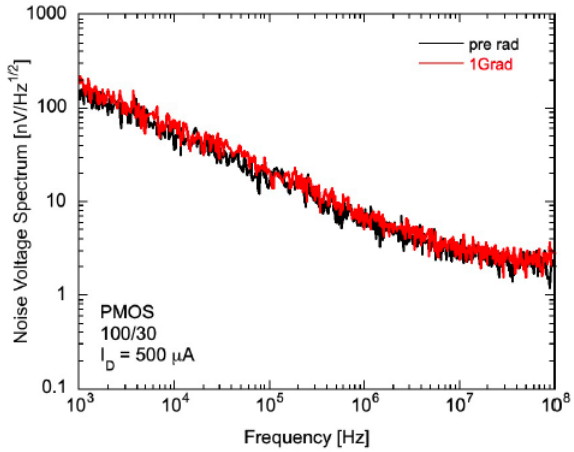
- Up to 1 Grad, NMOS and PMOS do not feature significant change in their **noise properties** after irradiation

Thanks to Serena Mattiazzo and Devis Pantano (INFN PD) for their valuable support during the irradiation campaign!









28 nm at AGH [Marek Idzik]

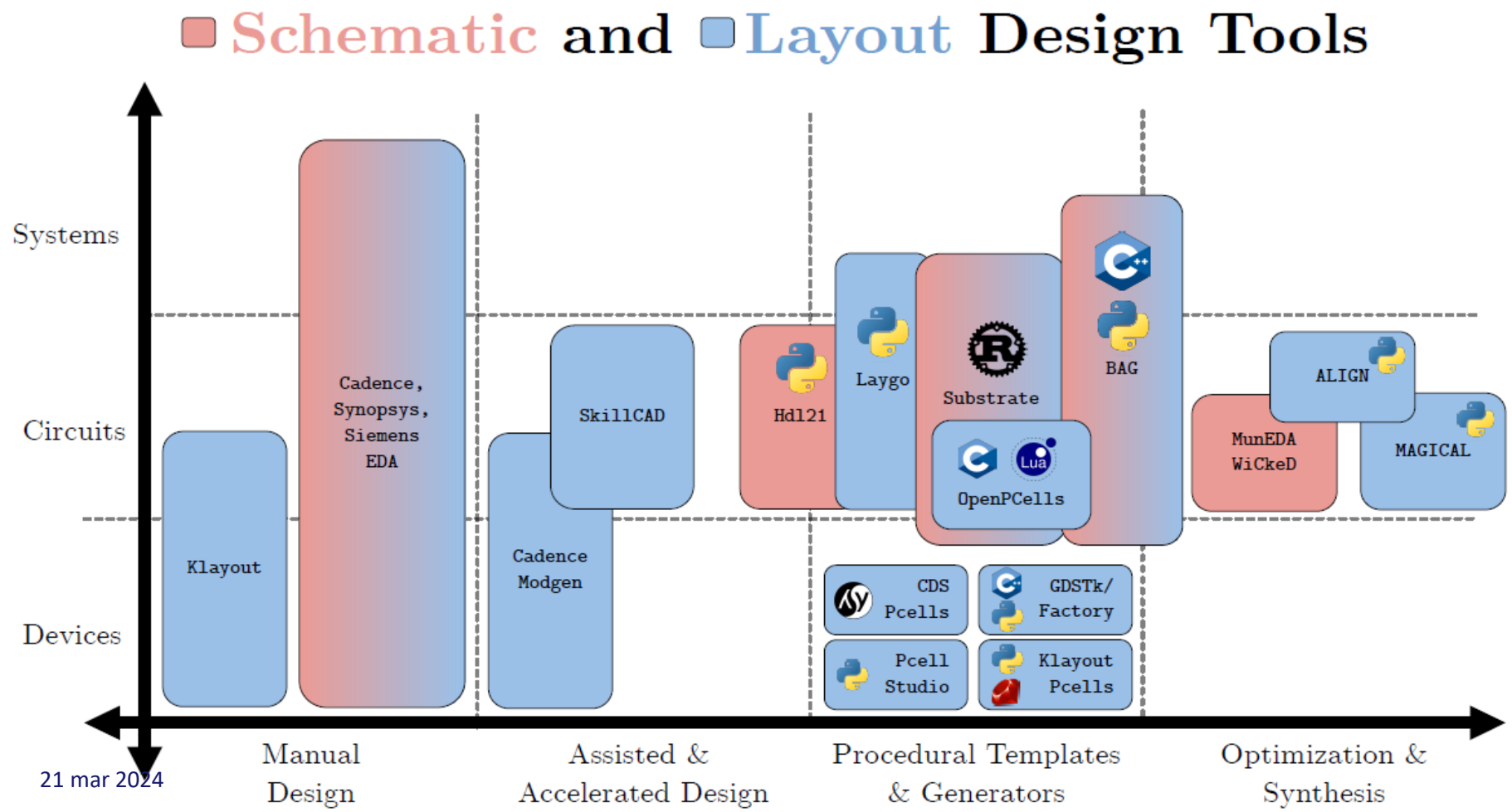
Simulation results of 10-bit SAR ADC Comparison to ADC prototypes in 130/65 nm

CMOS [nm]	Verification	Power @40MHz [uW]	Max fsample [MHz]	
130	Prototype ASIC	680	50	M. Firlej et al. JINST 18 P11013 (2023)
65	Prototype ASIC	440	50-60	M. Firlej et al. JINST 19 P01029 (2024)
65	Prototype ASIC	~550	80-90	M. Firlej et al. JINST 19 P01029 (2024)
28	Post-layout simulation	<150 ?	~180 ?	

- Post-layout simulations show a great improvement in power consumption and sampling frequency, compared to 130/65 nm
- How realistic the post-layout simulations are ?

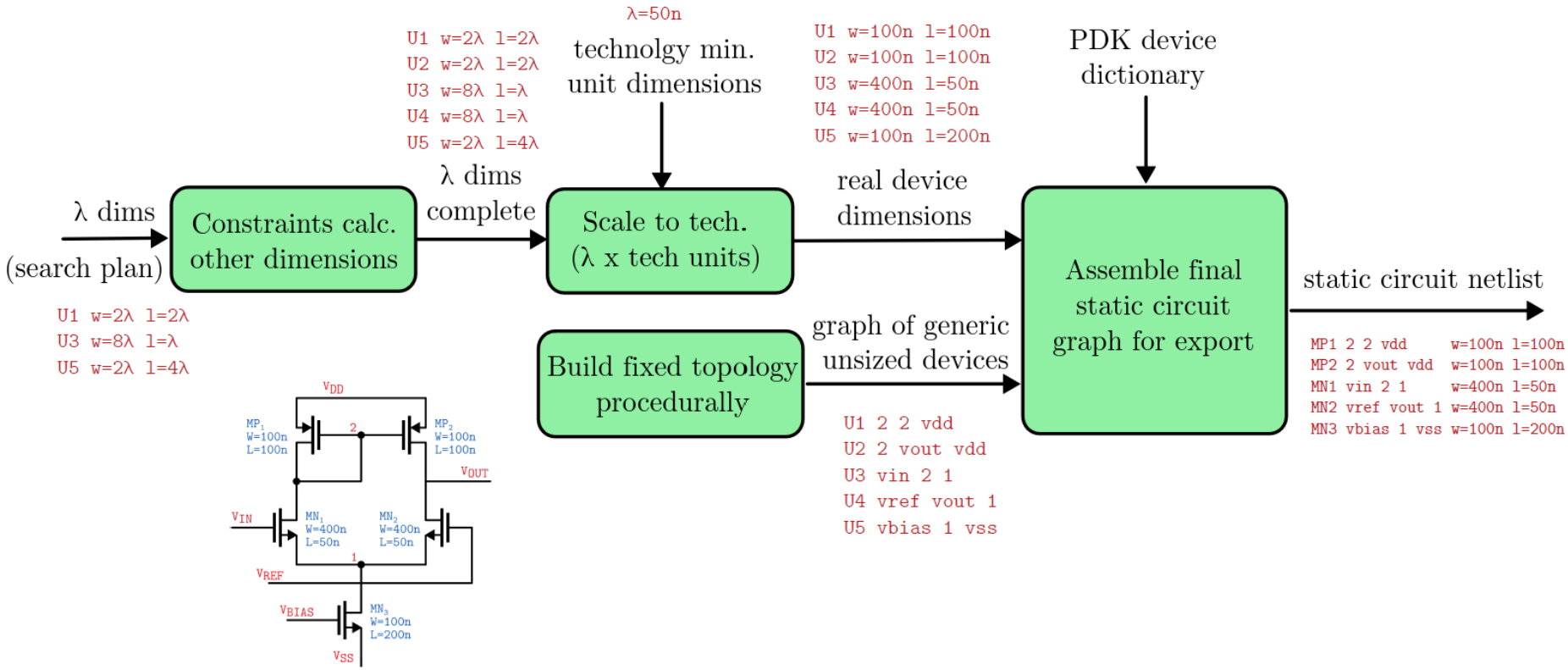
28 nm at UBonn [Kennedy Caisley]

- Mixed-signal parameterized cells in general-purpose programming languages
- “Why chip design should be software-driven”



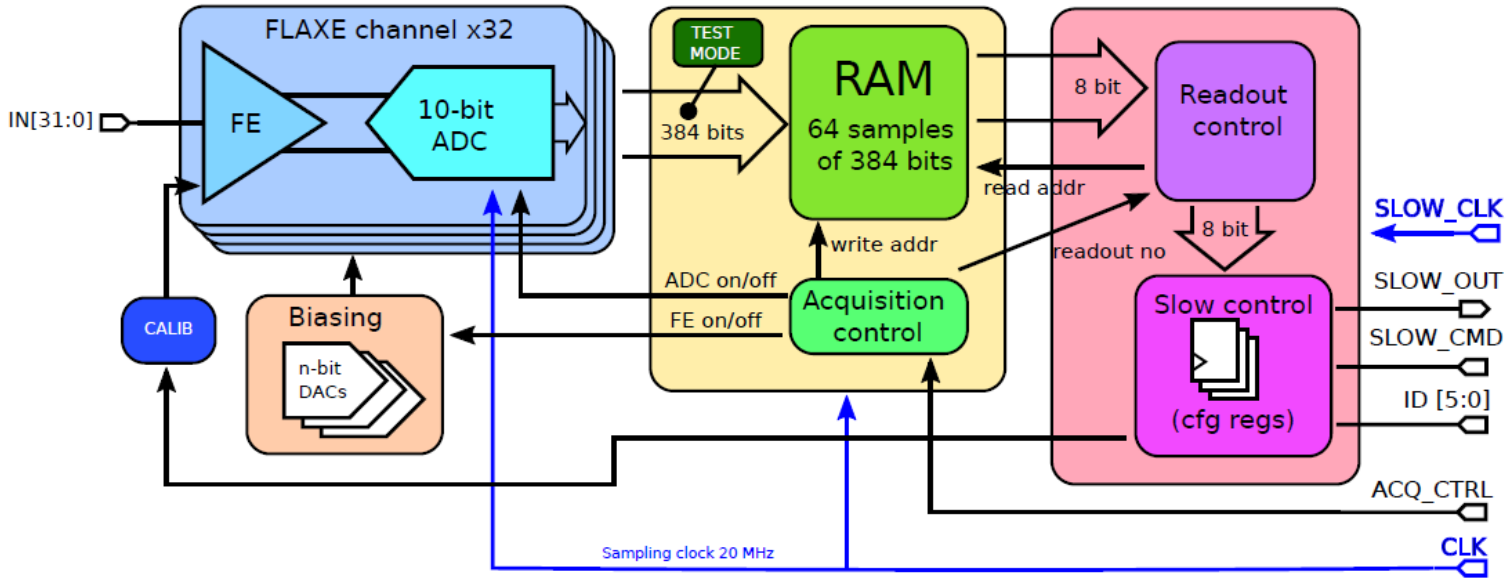
28 nm at UBonn [Kennedy Caisley]

What if we express this in code?



130 nm at AGH [Marek Idzik]

Activities in CMOS 130nm
FLAXE ASIC for ECAL-p in LUXE experiment

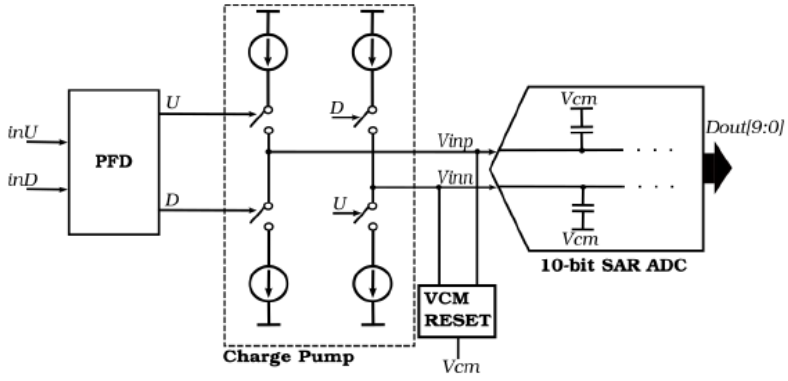


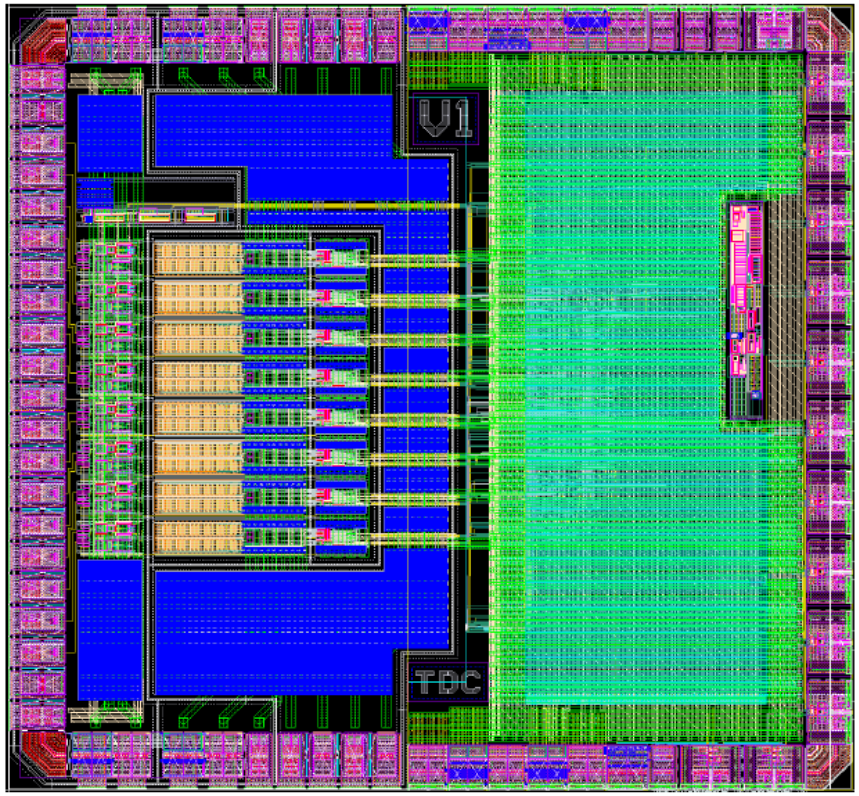
- FLAXE is a modified 32-channel FLAME in CMOS 130nm without high speed serialisers&transmitters – readout rate in LUXE ~10 Hz
- More than 1000 FLAXE chips were produced. Sent for dicing and packaging recently…

130 nm at AGH [Marek Idzik]

Activities in CMOS 130nm
R&D on precise TDC – TAC+ADC architecture

Single TDC channel





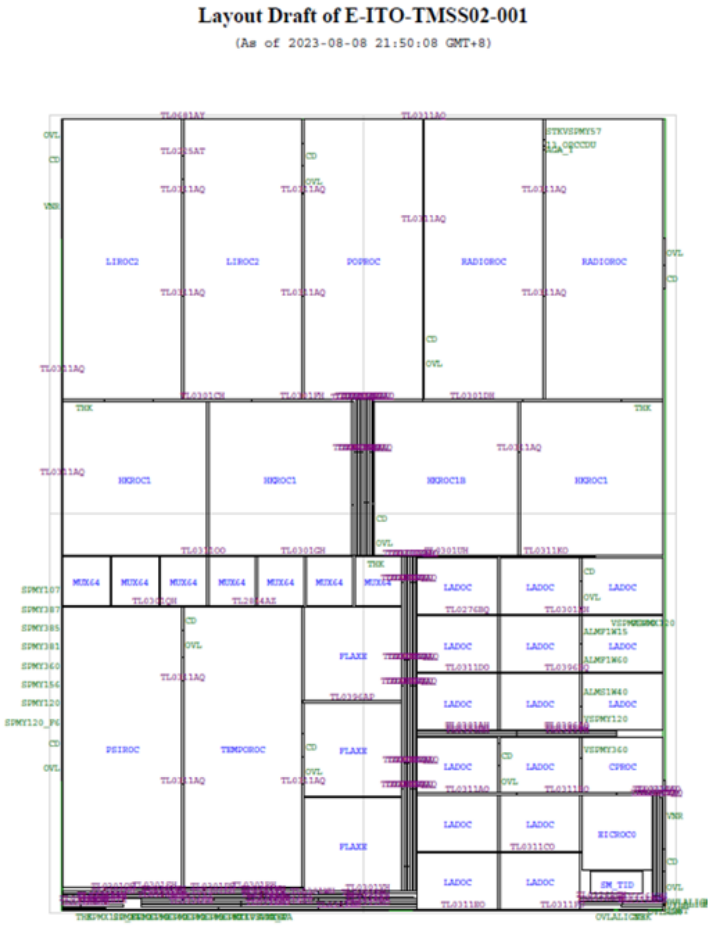
- New TAC-based TDC aiming at timing measurement precision of ~10ps, consuming ~1mW
- As ADC the existing 10-bit SAR is used
- 8-channel prototype TDC chip was fabricated in 2022

130 nm at OMEGA [Damien Thienpont]

Engineering run submitted in April 2023

- TSMC 130 nm
- 10 chips have been submitted
  - From OMEGA, AGH, IJCLAB, WEEROC
  - C4 (16 wafers) and WB (4 wafers), 90 chips/wafer
  - In fab at TSMC in November 2023 only!
    - Reticle completion , payment, …
  - Wafers received last month, presently in packaging
- HKROC1B, EICROC0 and CPROC

chip	x	y		lab
HKROC1B	5,96	6,16	C4	OMEGA
LADOC2B	3,243	2,142	WB	IJCLAB
LIROC2	11,244	4,919	C4	OMEGA
POPROC	11,244	4,919	C4	WEEROC
PSIROC	11,244	4,919	C4	WEEROC
RADIOROC2	11,244	4,919	C4	WEEROC
TEMPOROC2	11,244	4,919	C4	WEEROC
FLAXE	4,02	3,7	WB	AGH
EICROC0	2,89	3	WB	OMEGA
CPROC	3,243	2,142	WB	OMEGA
Total				



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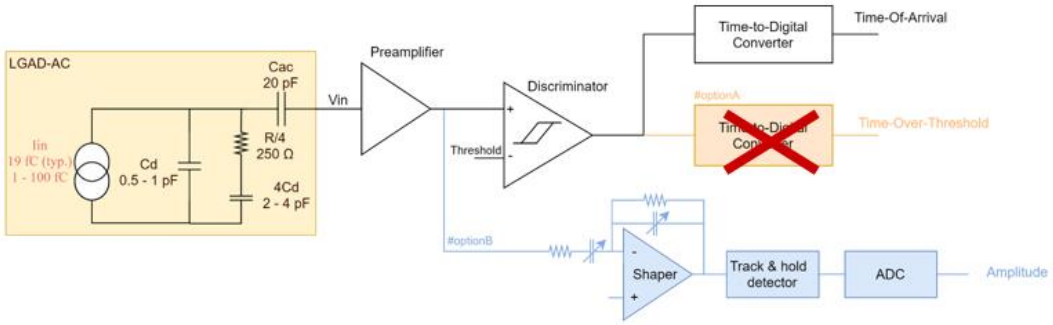
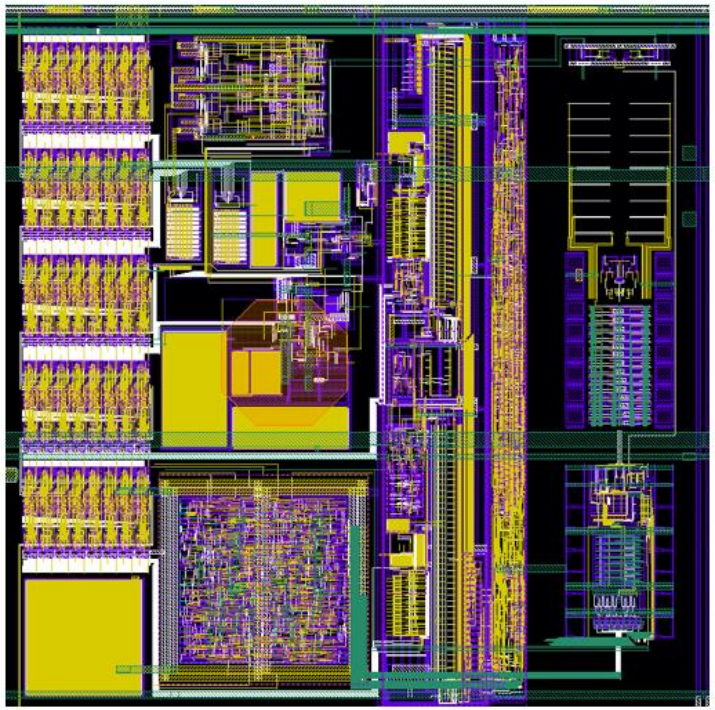
130 nm at OMEGA [Damien Thienpont]

EICROC0 : one pixel overview

- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes





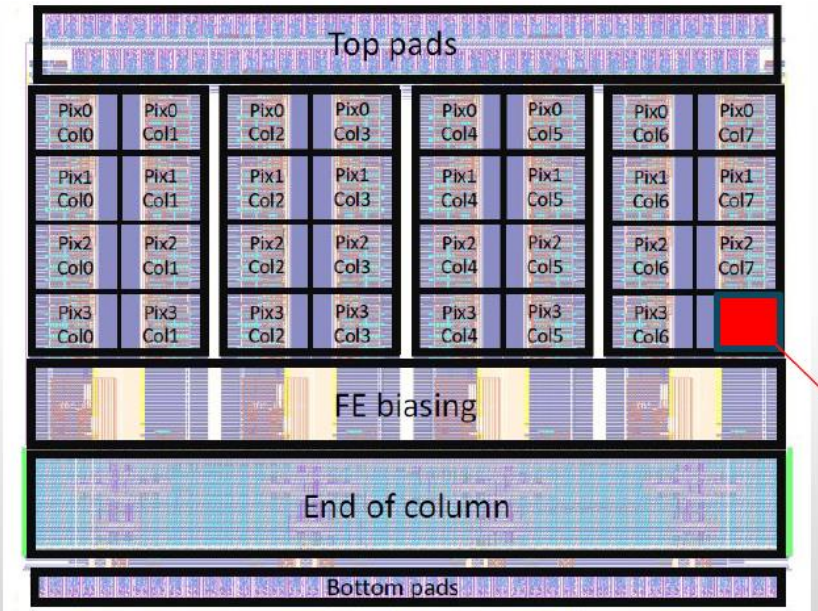
Slow control | PA +discri | TOA TDC | 8b 40M ADC

EICROC ePiC meeting 9 jan 2024

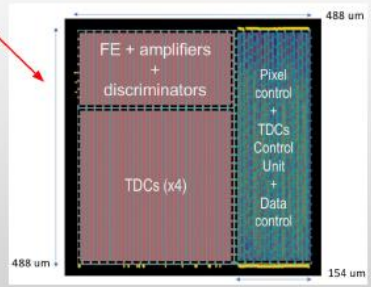
9

110 nm at INFN TO [Angelo Rivetti]

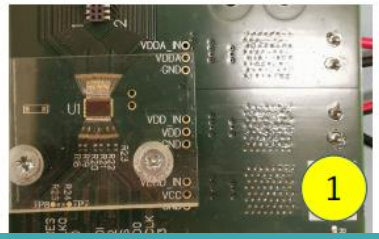
ALCOR ASIC



- 32 channels 4x8 pixels array
- pixel size 440 x 440 μm^2
- SiPM connection through wire bonding pads (top side)
- End of Column performs readou and SPI configuration
- 4 LVDS serializers (one every two columns) for data transmission
- Analogue I/O on the top side
- Digital I/O on the bottom side



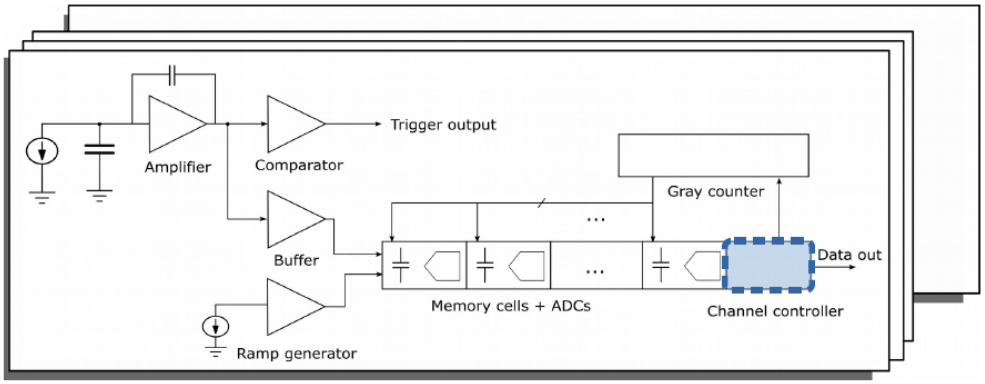
- **Extensively characterised**
- **Engineering run production, several samples**



Multi-purpose waveform sampling ASIC in 65 nm

INFN

- Sample and digitise in an capacitor array
- Each sampling cells contains a Wilkinson ADCs
- Simpler to increase the sampling frequency in future iterations
- 256 digitizing cells, organised in buffers of programmale length for derandomisation



130 nm at WEEROC [Julien fleury]

Applications for LIROC

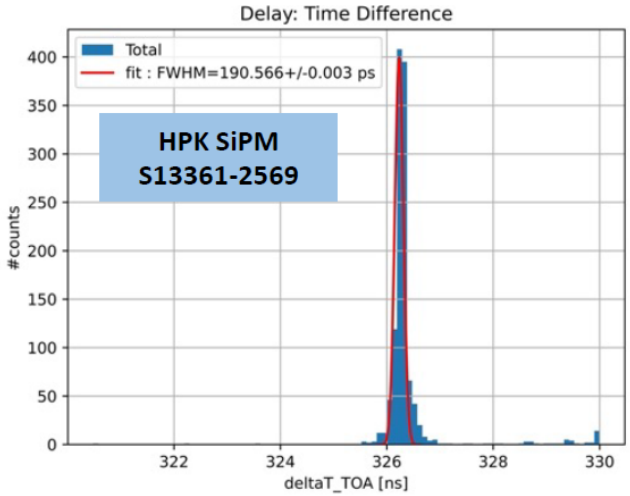
- QUANTUM : True Random Number Generation : Random Power spa
- LIDAR : atmospheric LIDAR : ADS / CNES
- LIDAR : Onera
- LIDAR : ISRO
- LIDAR : Leica Geosystem

130 nm at WEEROC [Julien fleury]

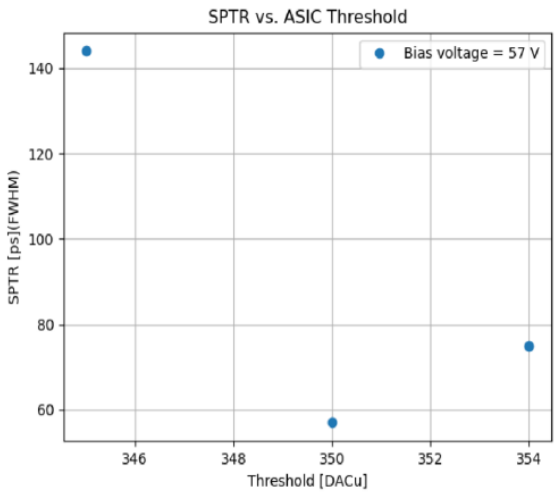
Liroc-picoTDC system: Improved time resolution (SPTR)

HPK SiPM S13361-2050NE-08

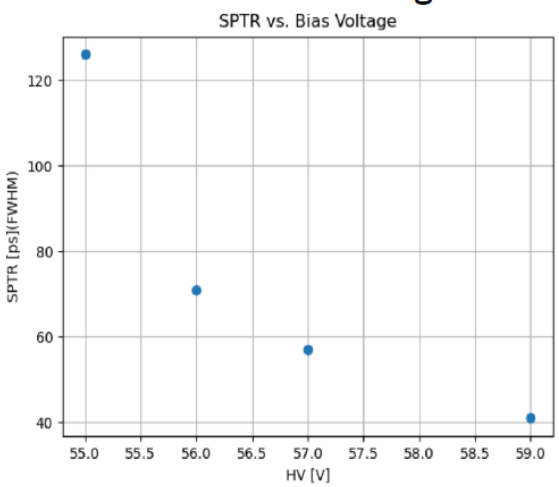
TOA Distribution



SPTR vs. Threshold



SPTR vs. Bias Voltage



→ TOA measurement: best SPTR HPK S13361-2569 is **191 ps** (FWHM) at 57 V .

→ Improved SPTR for a standard HPK S13361-2050NE-08: **58 ps** (picoTDC) compared to 167

JINST — Published by IOP Publishing for Sissa Medialab
Received: May 31, 2023
Revised: August 15, 2023
Accepted: September 21, 2023
Published: October 4, 2023

Study experimental time resolution limits of recent ASICs at Weeroc with different SiPMs and scintillators

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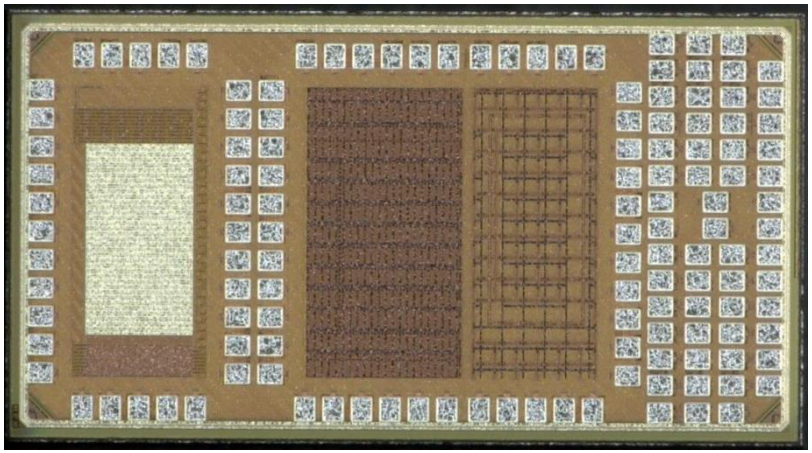
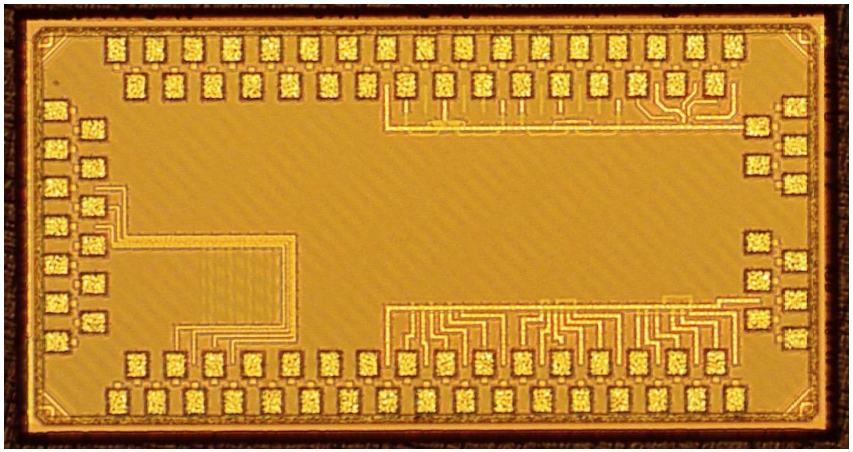
WP11.2 deliverable

- D11.1 : MPW in 28 nm

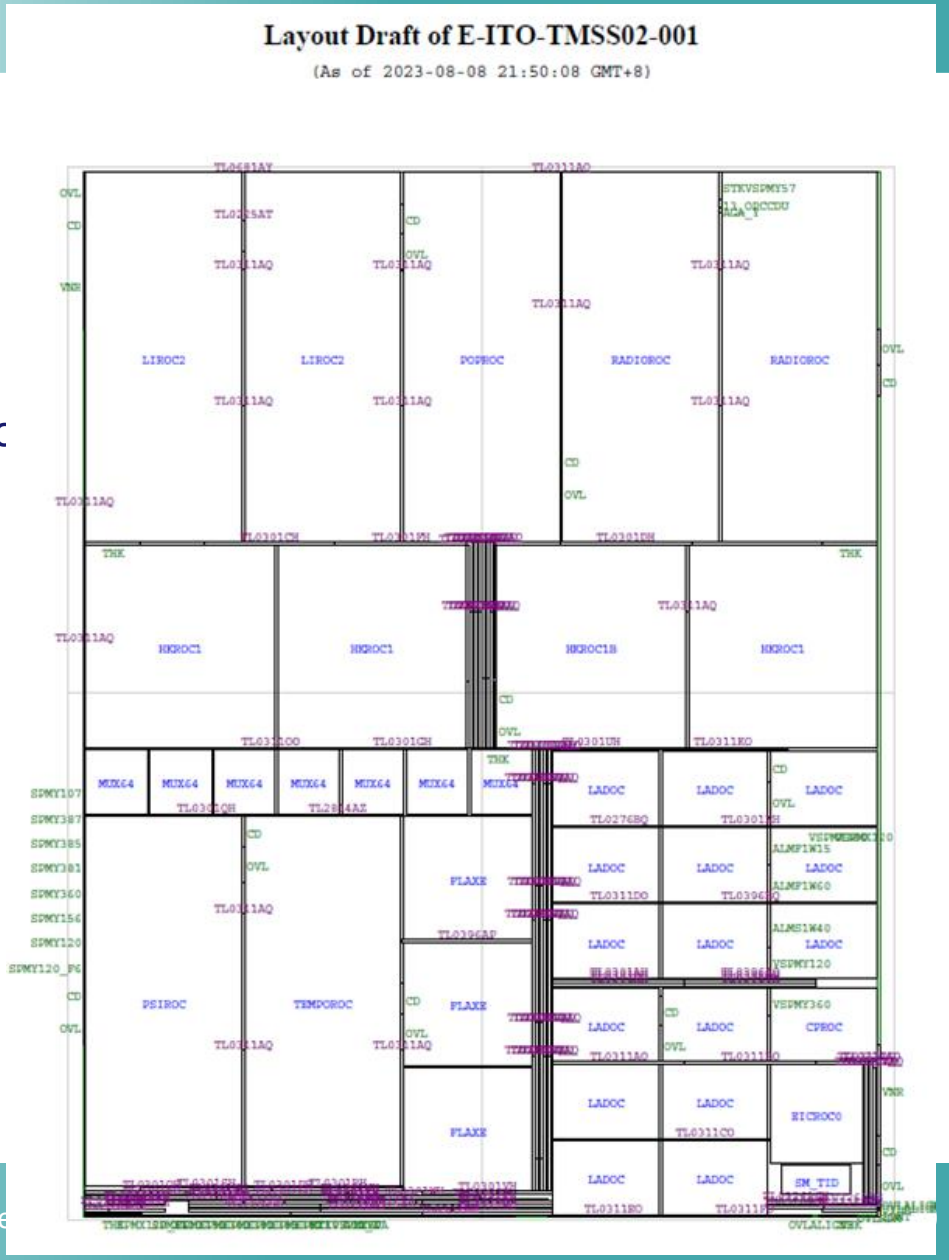




WP11.3 Deliverable

- D11.2 : MPW in 130 nm

- 5 chips from AIDA :
  - FLAXE (AGH) : Si/GaAs readout
  - EICROC (OMEGA/AGH/CEA) : LGAD readc
  - CPROC (OMEGA) : RISC5
  - LIROC (WEEROC) : SiPM timing
  - PSIROC (WEEROC) : Si readout



Summary

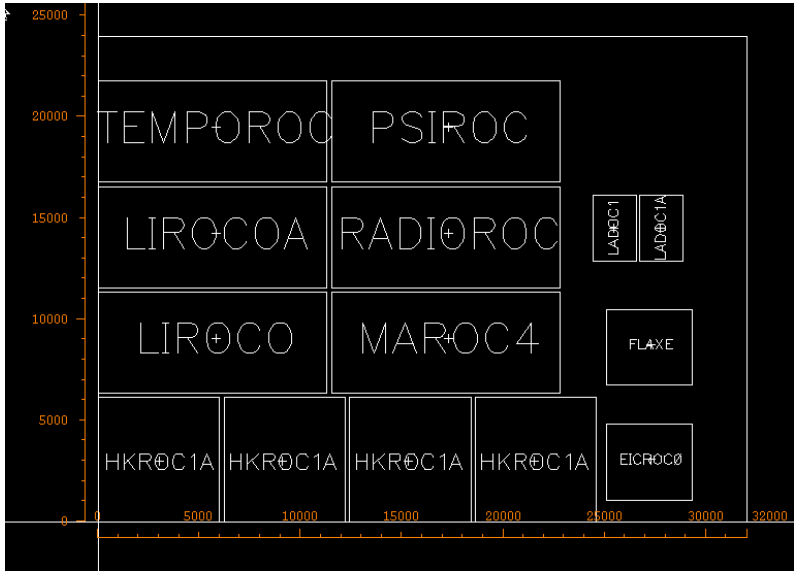
- 2 main pillars in AIDA INOVA
  - Explore 28 nm technology performance for HEP
  - Provide readout ASICs in 130nm for other WPs
- 2 fabrications done in 2023 to match these objectives
  - Milestones MS45/46 and deliverables 11.2/11.3
- First results shown at then meeting, more to come…
- More designs also continuing…
- At least 3 publications (AGH), probably more to be counted

backup

AIDA engineering run

- AIDA participation in a 130nm engineering run constitutes D1.1
  - ~25% of the reticle area = 25% of the total cost (250k€)

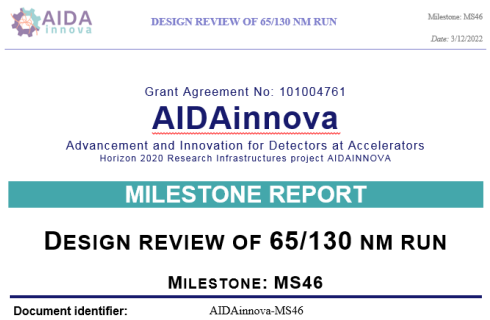
- 4 chips from AIDA-INNOVA partners on this run
  - FLUXE (AGH)
  - EICROC (OMEGA/AGH/CEA)
  - LIROC (WEEROC/OMEGA)
  - PSIROC (WEEROC)
  - Submission scheduled jan 2023
  - Several hundreds of chips will be available



- Chips reviewed in november 2022
  - Constitutes Milestone MS46

Deliverables/Milestones

- 2 Milestones and 2 deliverables
  - MS 11.1 and 11.2 (MS45 MS46) passed end 2022
  - D11.1 and 11.2 are the corresponding chips


AIDA innova DESIGN REVIEW OF 65/130 NM RUN Milestone: MS46 Date: 3/12/2022

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

DESIGN REVIEW OF 65/130 NM RUN

MILESTONE: MS46

Document identifier: AIDAinnova-MS46

MS11.1	**Design review of 28 nm MPW**	**11.2**	**18**	**report**
MS11.2	design review of 65/130 nm run	11.3	18	report

Deliverables related to WP11	
D11.1: MPW 28 nm *The deliverable is a multi-project wafer fabrication with the different test ASICs in CMOS 28 nm*	24
D11.2: MPW 65/130 nm *The deliverable is a multi-project wafer fabrication with ASICs in CMOS 65 and/or 130 nm that can be used to readout detectors from the other WPs and in particular WP8*	24
D11.3: Measurement reports *Each of the ASIC fabricated in the 2 previous deliverables will have its design and performance documented in a report*	42