Update on RD50 series HV-CMOS prototypes development

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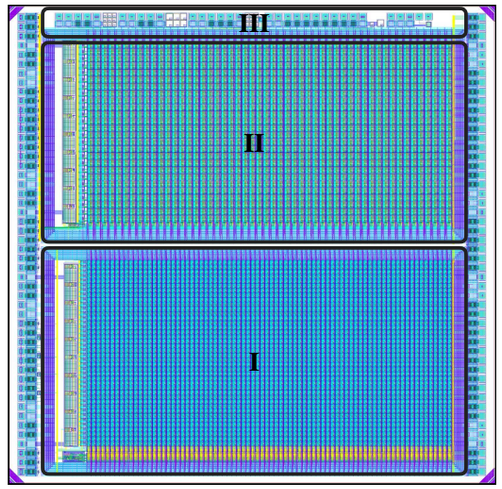
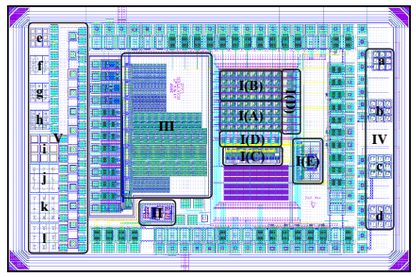
RD50 DMAPS prototype chips

- Four DMAPS prototypes have been designed by RD50 CMOS group.
- All fabricated in LFoundry 150 nm HV-CMOS process.

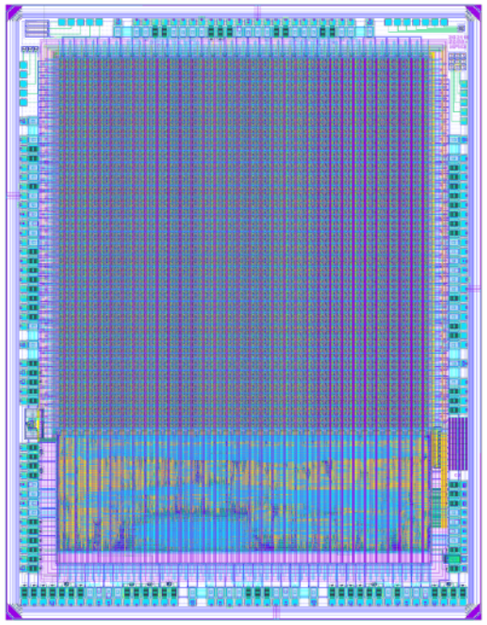
RD50-MPW1 (2017)



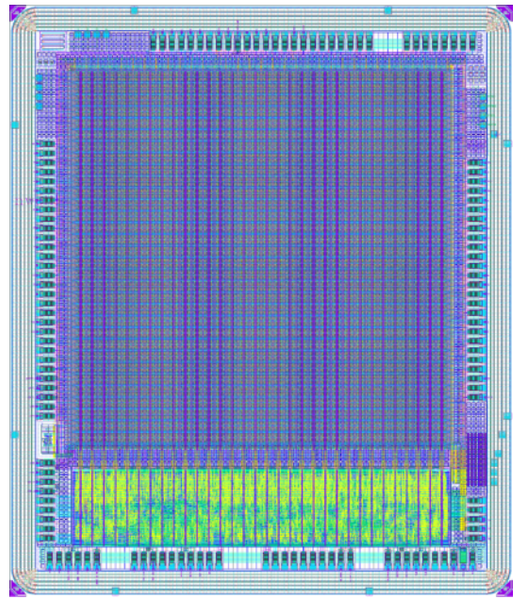
RD50-MPW2 (2019)



RD50-MPW3 (2021)



RD50-MPW4 (2023)

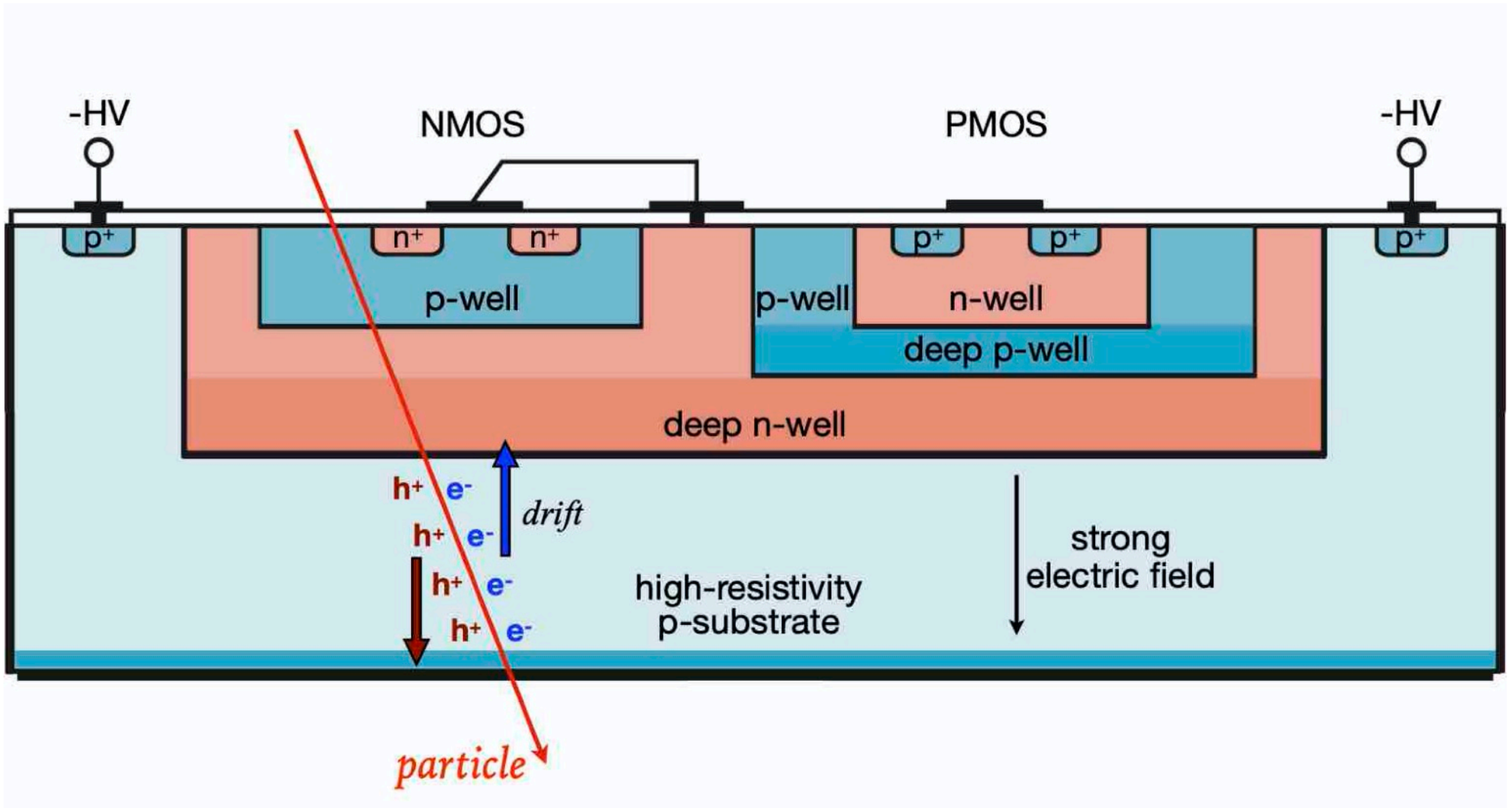


- **RD50-MPW1**: test the LF150 process, low V_{BD} (55 V) and high I_{Leak} (~ μA).
- **RD50-MPW2**: high V_{BD} (130 V), low I_{Leak} (~ nA) and fast analog pixel.
- **RD50-MPW3**: implement large pixel matrices and fast digital readout. DESY testbeam
- **RD50-MPW4**: eliminate high noise and new guard rings for higher V_{BD} (~600 V).

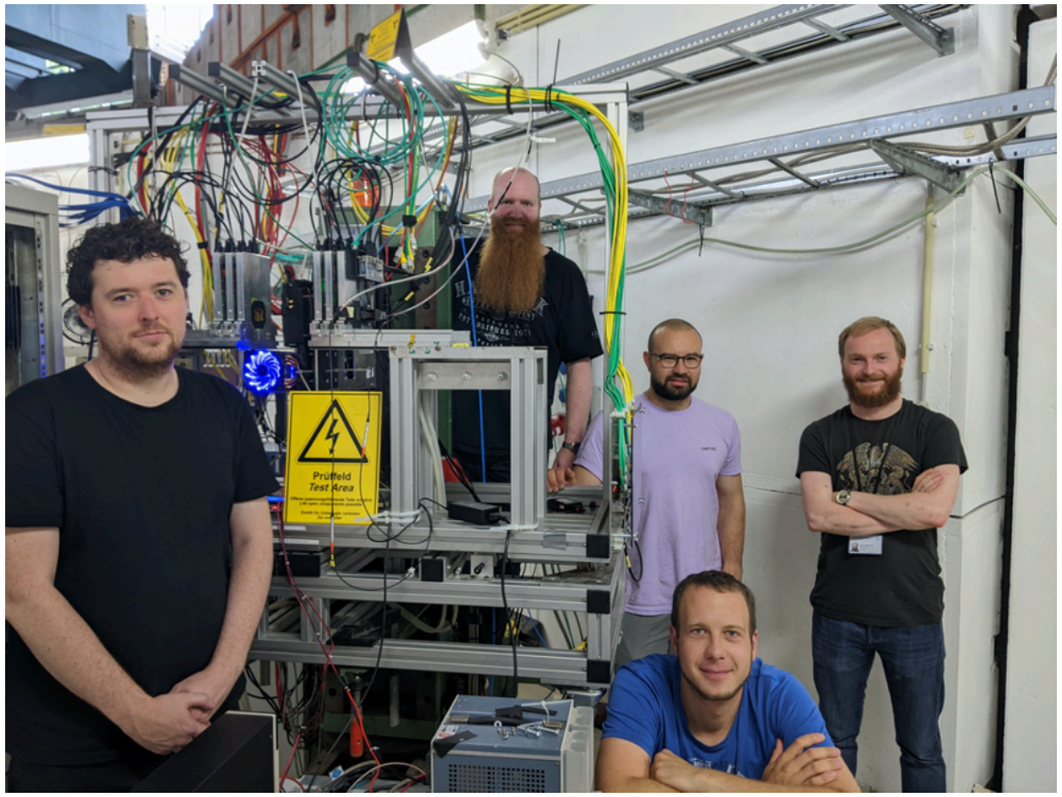
Lab measurement

Pixel sensor cross-section

- Large charge collection electrode is used.
- Both NMOS and PMOS transistors can be used.
- High bias voltages are applied from the top side or back side after backside processing.

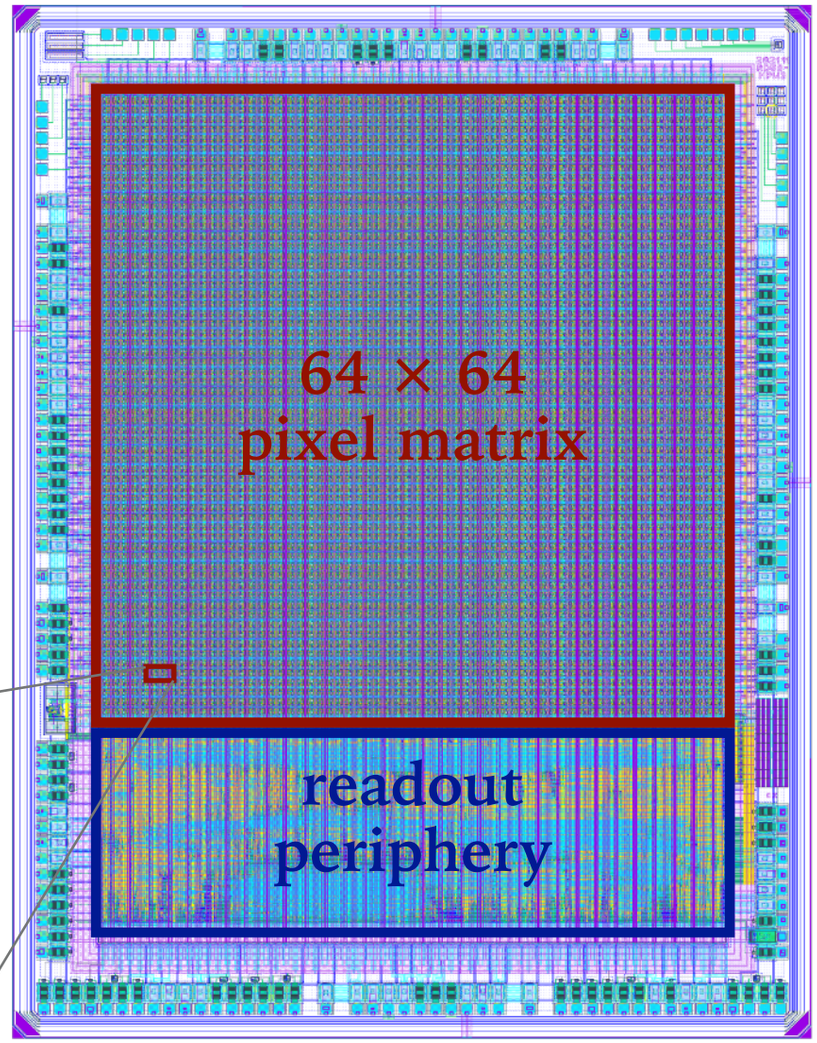


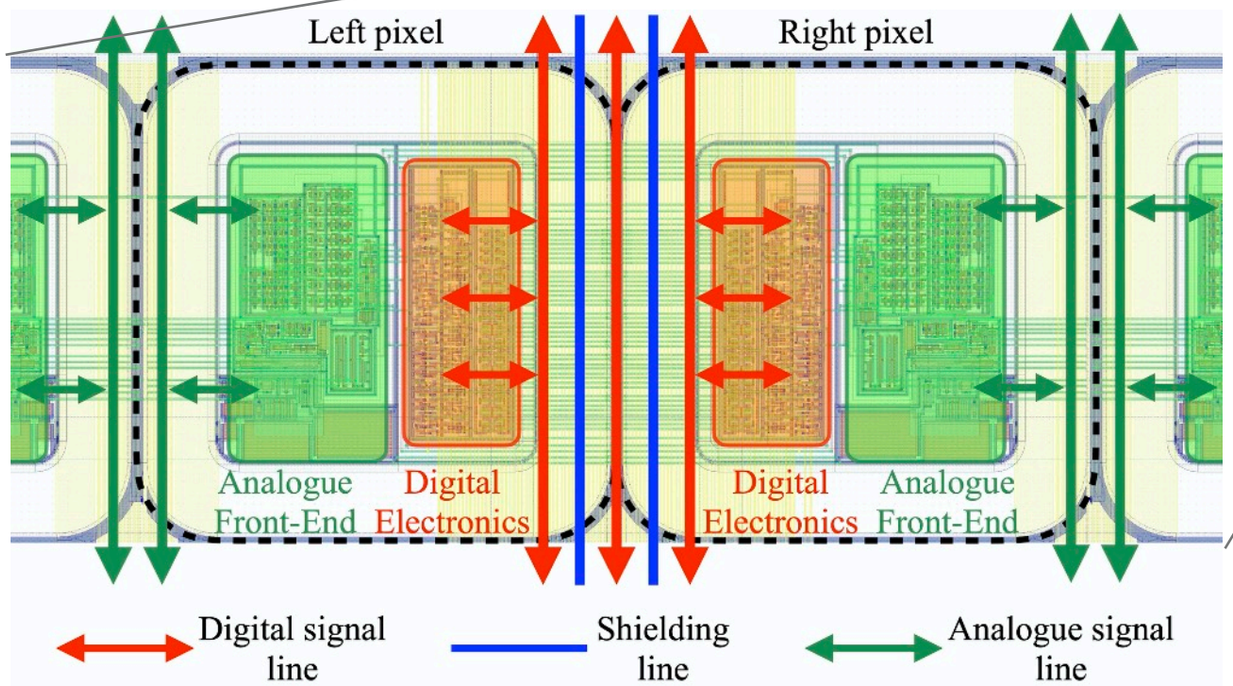
RD50-MPW3 DESY testbeam result



Recap of RD50-MPW3

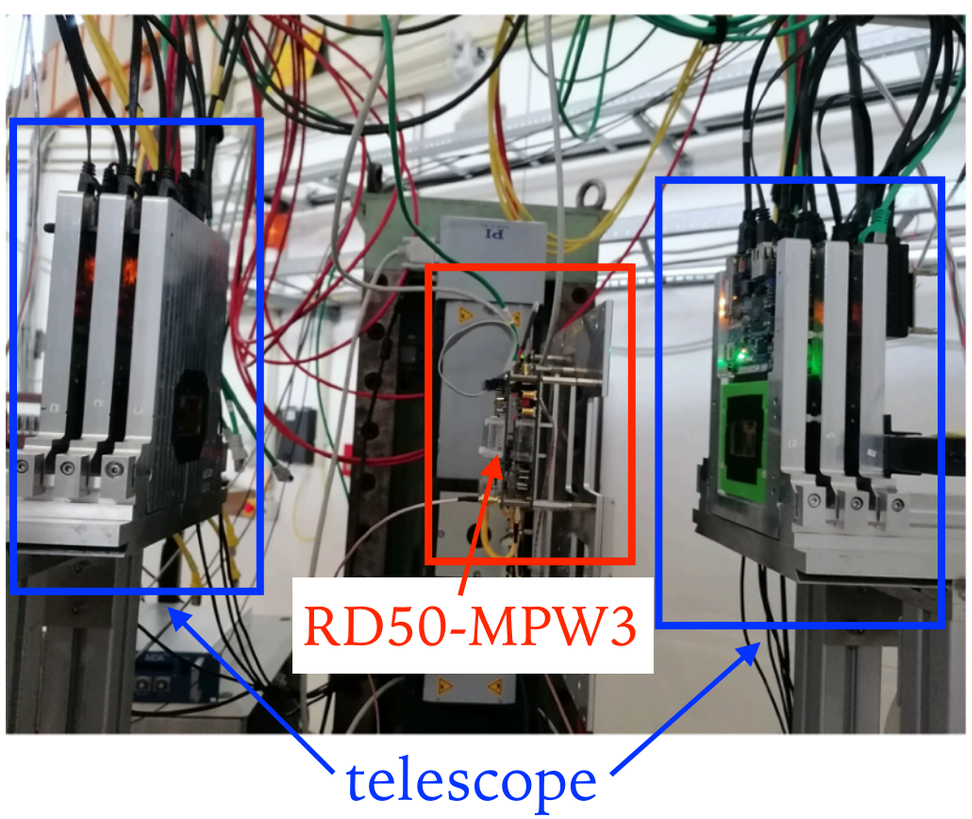
- **RD50-MPW3** is mainly composed of a 64 × 64 pixel matrix and a digital readout periphery.
  - ➤ pixel matrix is in double-column architecture with FE-I3 style readout;
  - ➤ optimised readout periphery for fast chip configuration and data transmission.
- Pixel size is 62 μm × 62 μm.
- Analogue and digital readout embedded inside pixel.

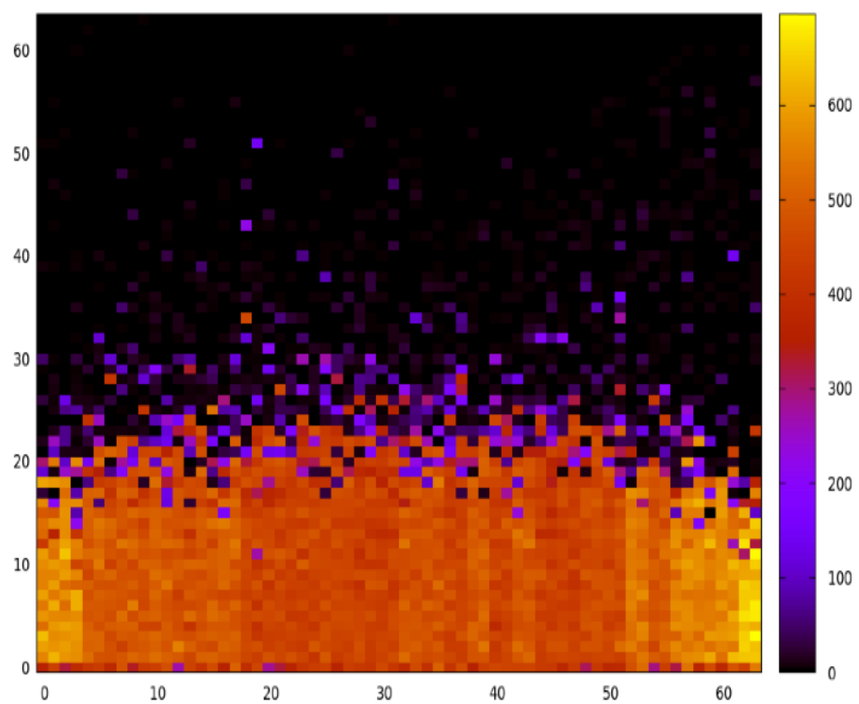




Testbeam of RD50-MPW3 – setup

- Testbeam at DESY in July 2023.
- DAQ is based on Caribou. The DUT is placed in the Adenium telescope made of 6 ALPIDE planes.
- Both un-irradiated and irradiated samples are tested with cooling setup.
- Samples were biased to 90V.
- Due to the large coupling noise from the digital periphery, a high threshold 200 mV (~ 5 ke$^-$) was used.

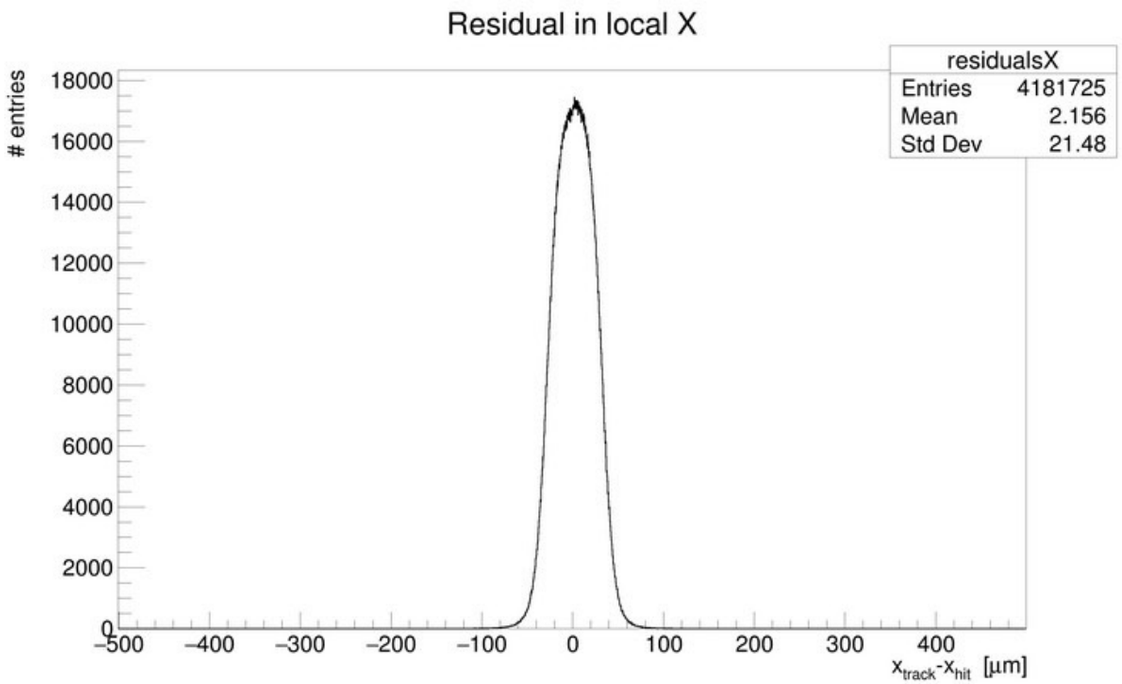


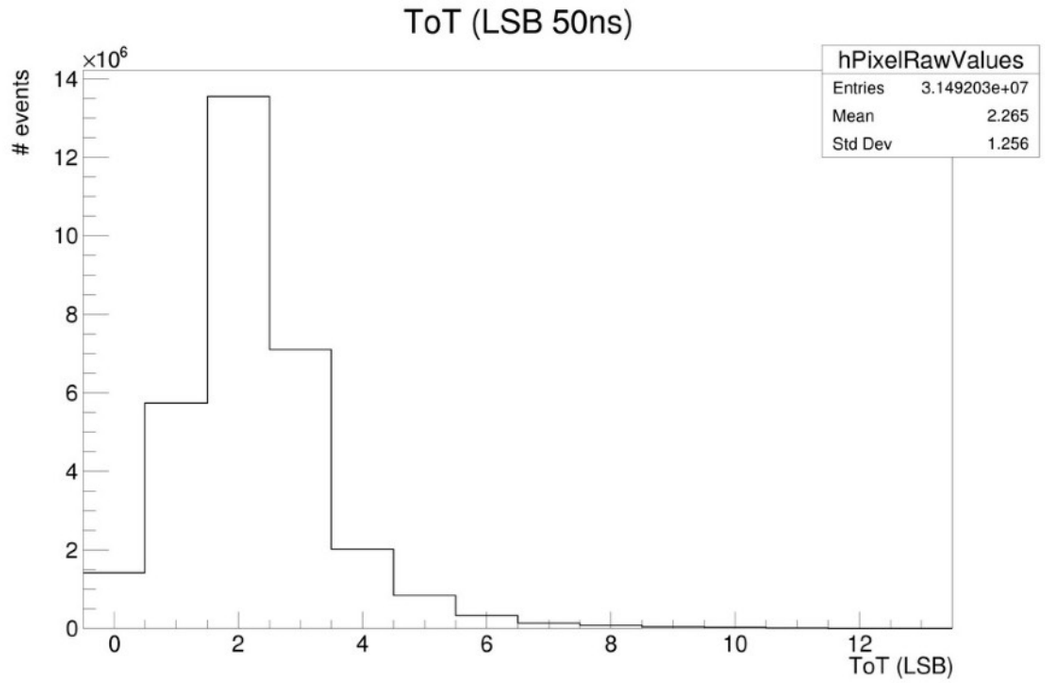


Noise hits in RD50-MPW3

Testbeam of RD50-MPW3 – latest results

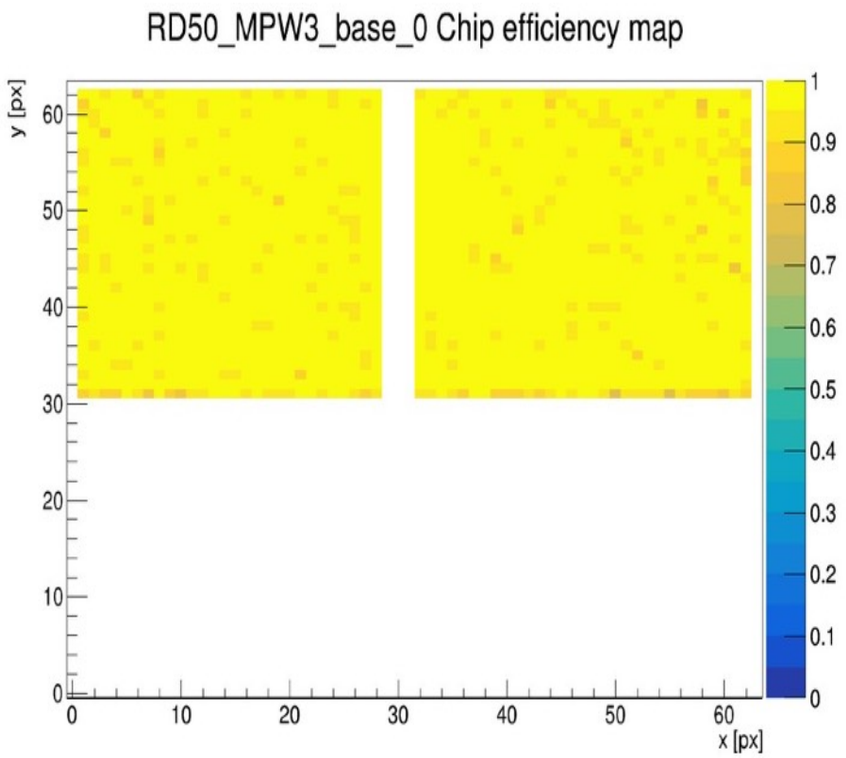
- Spatial resolution is ~21.5 µm in both x and y directions.
- Close to expected resolution: pixel pitch / $\sqrt{12}$ = 62 µm / $\sqrt{12}$ ≈ 18 µm.
- Mean ToT values of ~2.26 LSBs (on 50ns base).

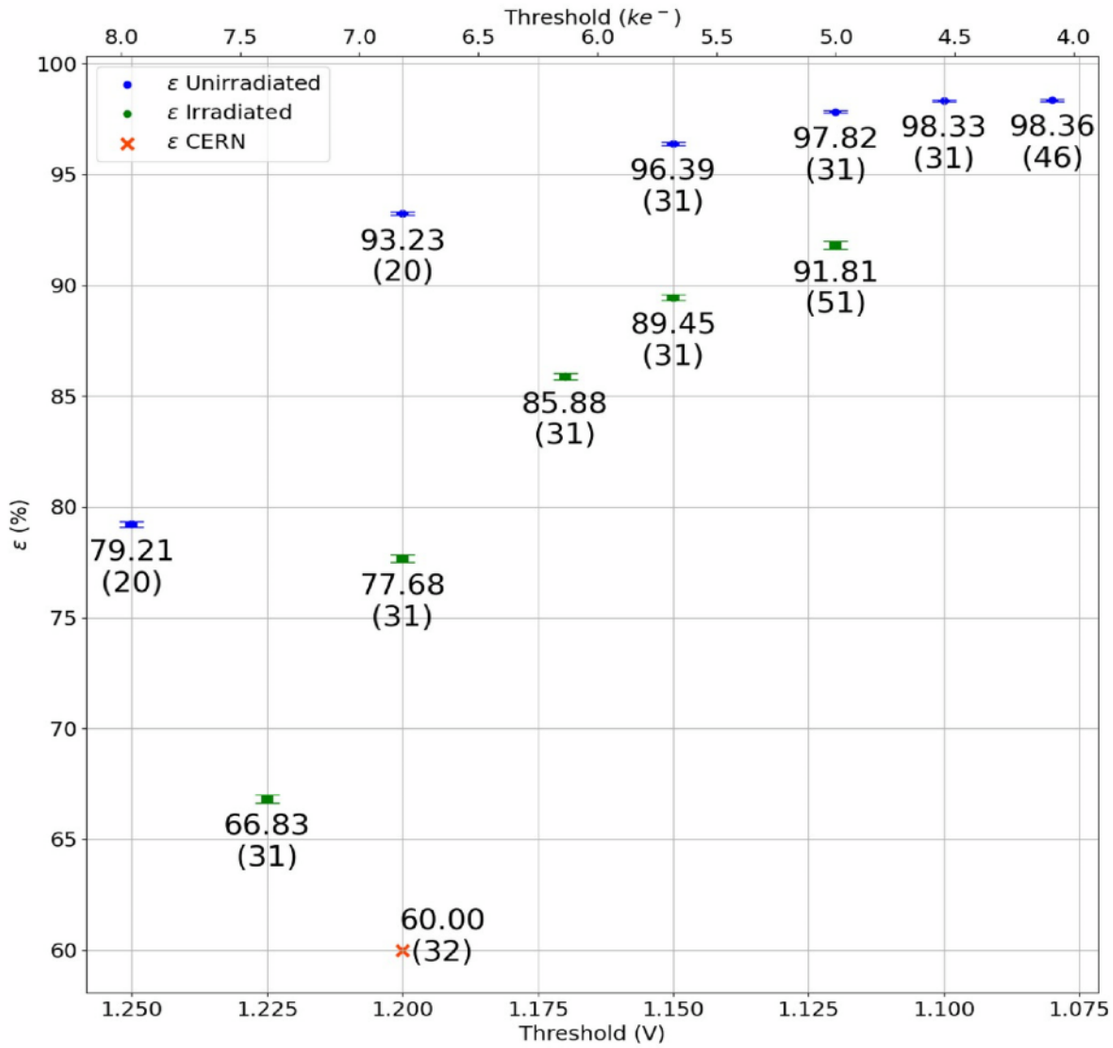




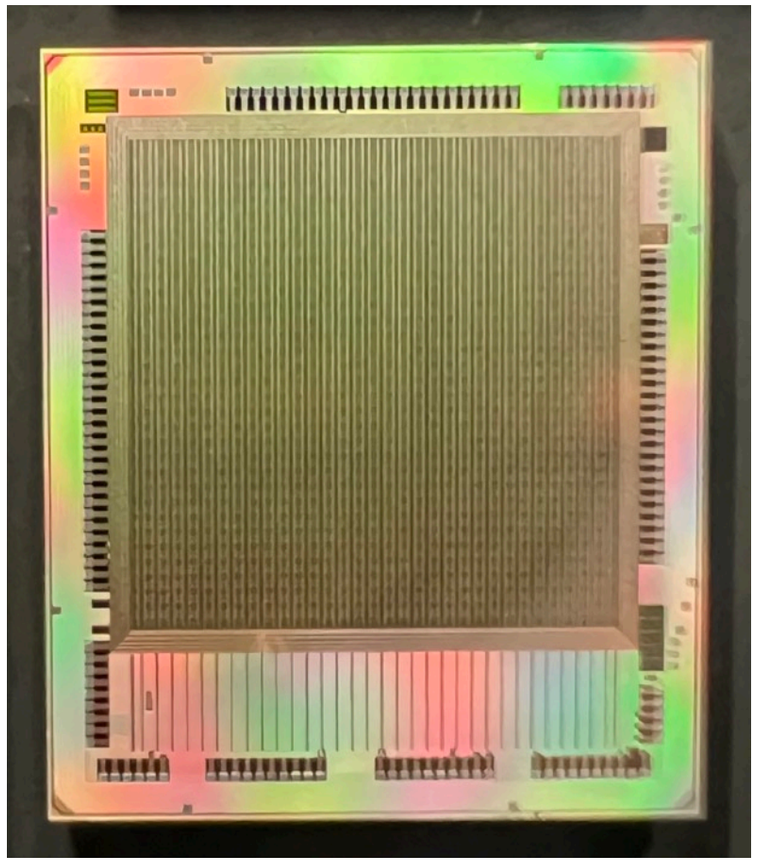
Testbeam of RD50-MPW3 – efficiency

- Due to noise issue ~bottom half of the matrix was masked (number of masked rows indicated by numbers in brackets).
- ~98.36% total efficiency for an un-irradiated sample.
- Efficiency drops on an irradiated sample (1E14 MeV n_{eq}).



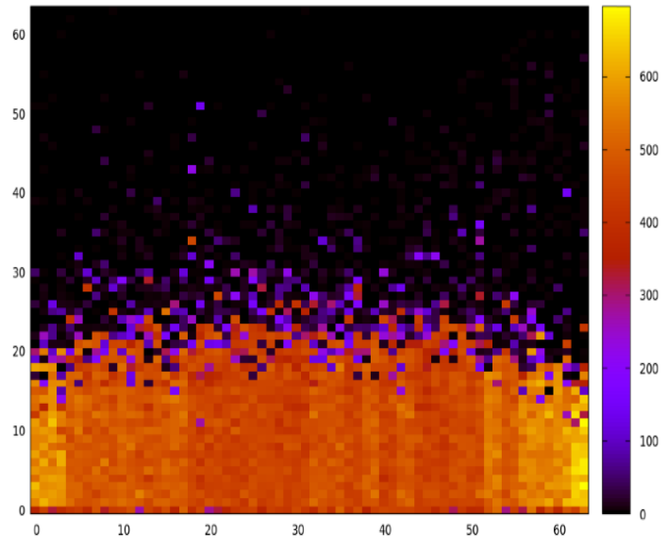


RD50-MPW4 design and initial results

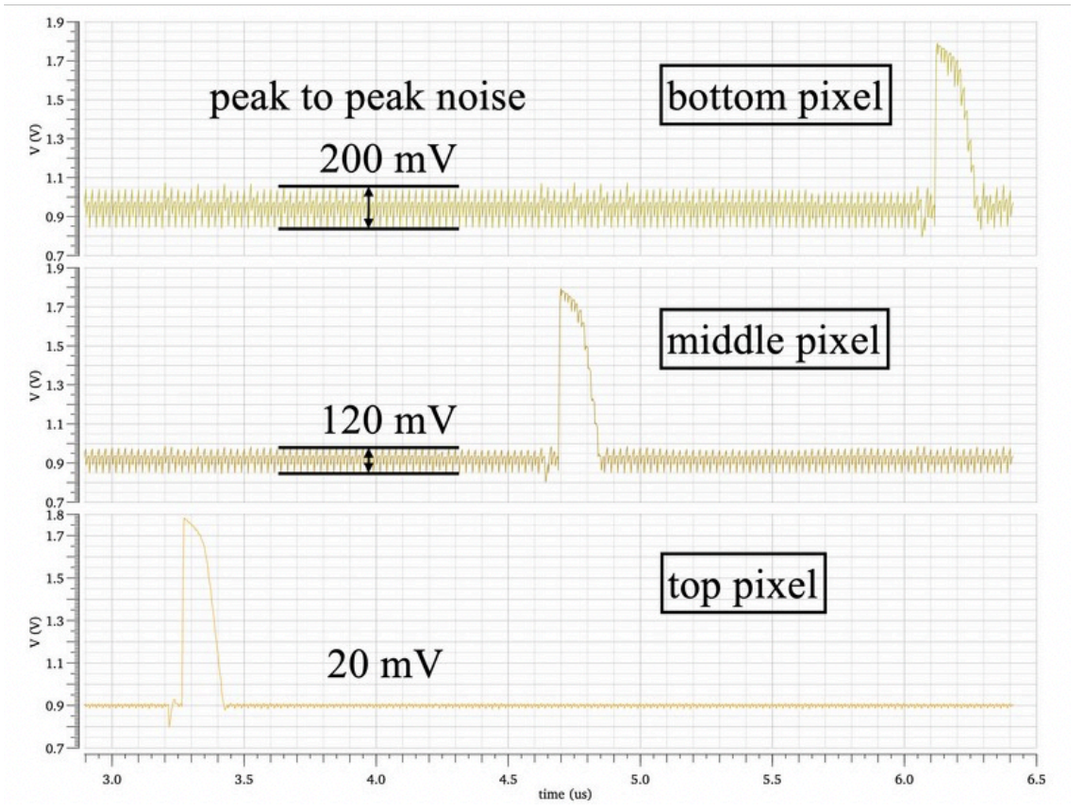


Design of RD50-MPW4

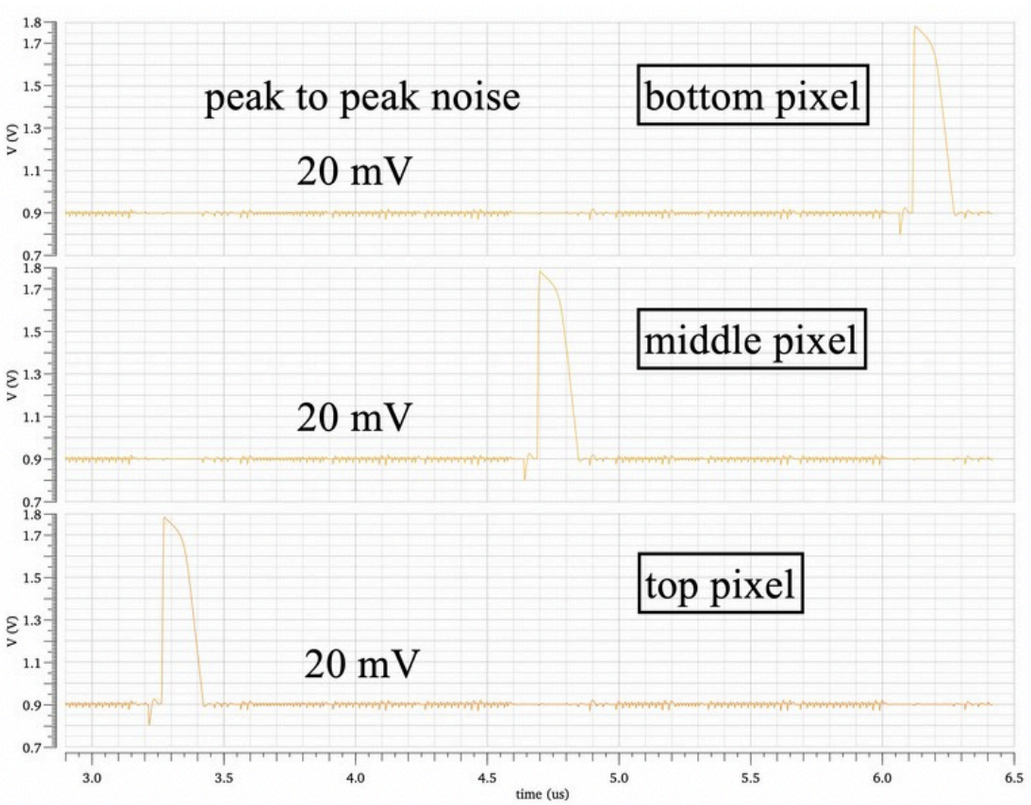
- Eliminate high noise in RD50-MPW3 pixel matrix.
  - ➤ Post-layout simulations show the high noise coupled from the digital readout periphery can be removed by separating the power and ground lines of the pixel matrix and readout periphery.



Noise hits in RD50-MPW3



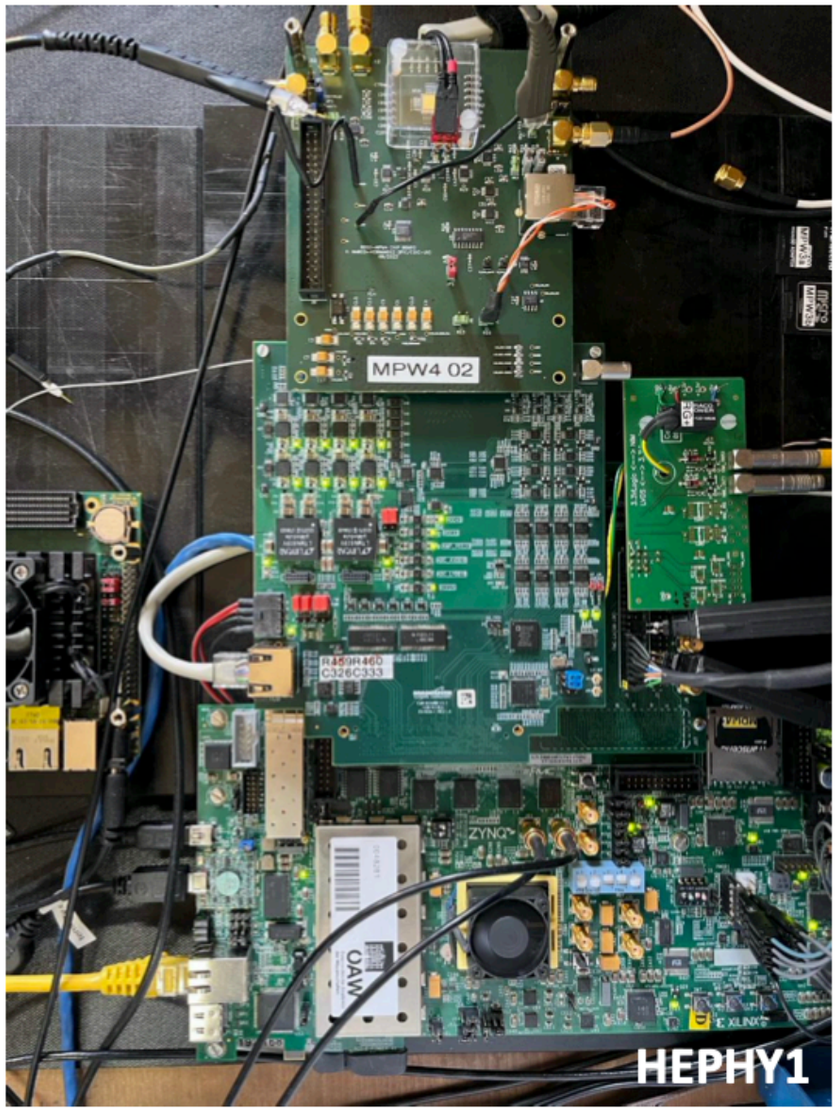
Shared power and ground
(RD50-MPW3)

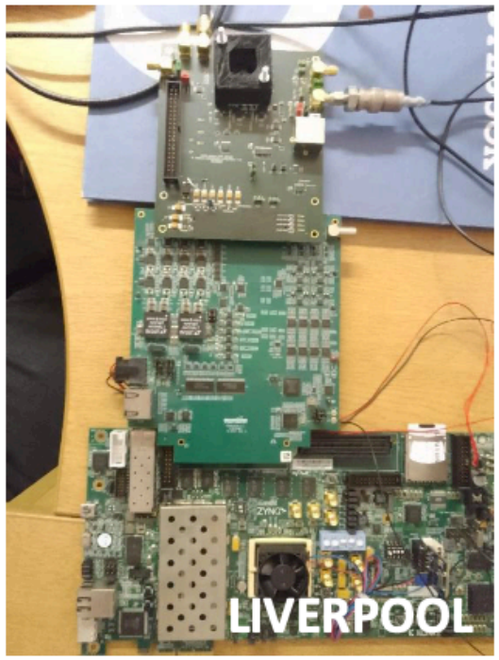


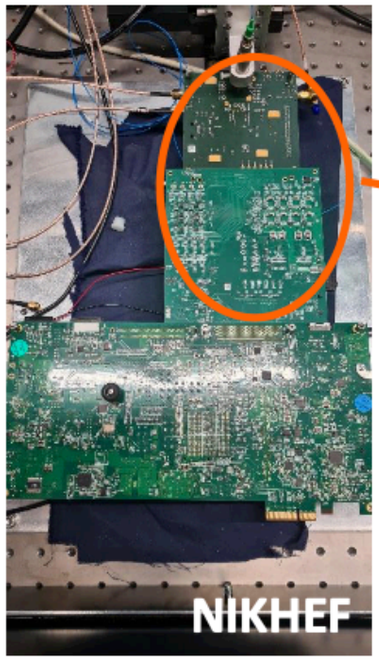
Separated power and ground
(RD50-MPW4)

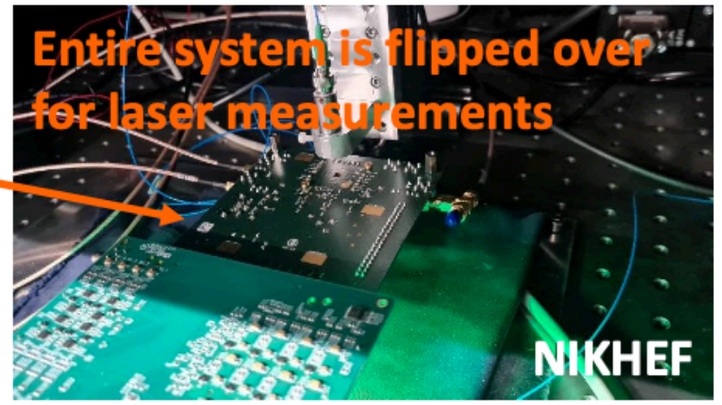
DAQ of RD50-MPW4

- DAQ is based on Caribou.
- Being measured at different institutes.









- **Xilinx Zynq-7000 SoC board**
  - ZC706 (ZC702 possible too)
- **Control and Readout (CaR) board**
  - Provides common services
- **Custom chip board**
  - Provides chip specific features

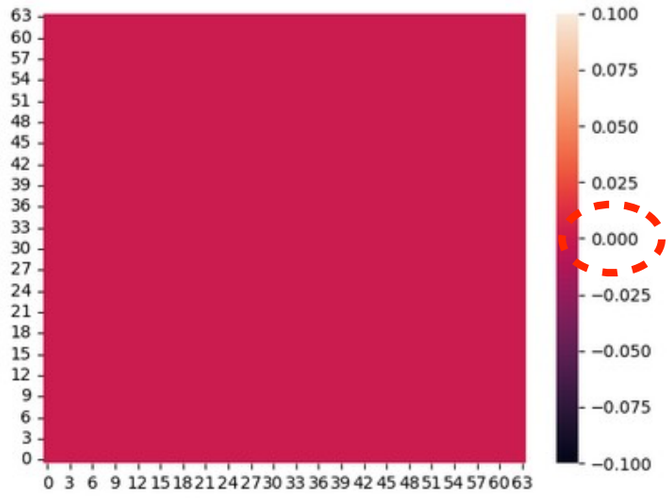
(and more sites
currently getting ready)

Initial results of RD50-MPW4 – noise elimination

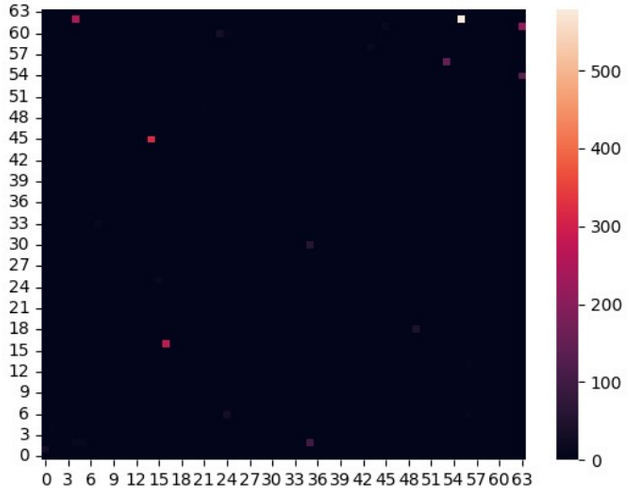
- No noise hit at a low threshold of 100 mV, only a few noisy pixels at a extreme low threshold of 30 mV.
- A few noisy pixels when 10 voltage pulses are injected to selected pixels.

Noisy hits in RD50-MPW4

Threshold = 100 mV

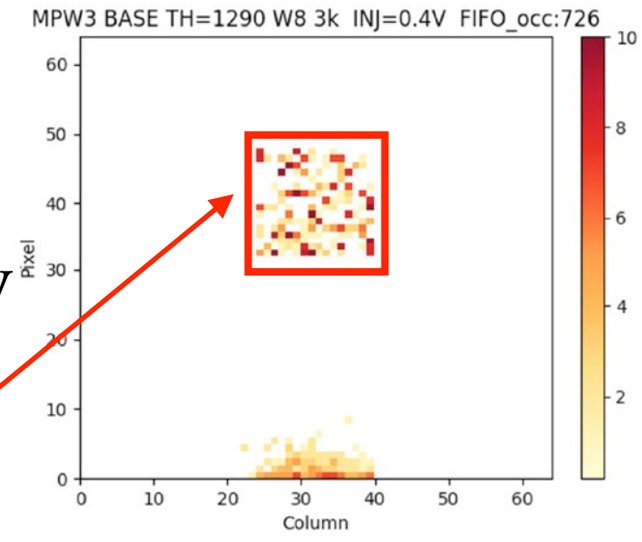


Threshold = 30 mV



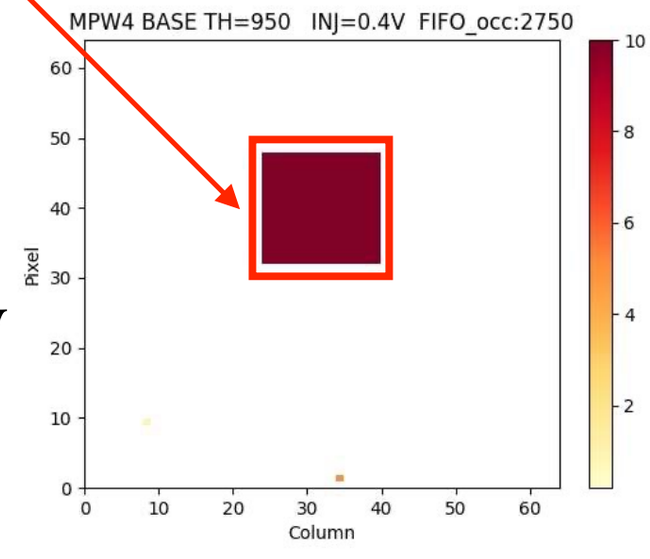
Injecting 10 voltage pulses

RD50-MPW3
Threshold = 390 mV



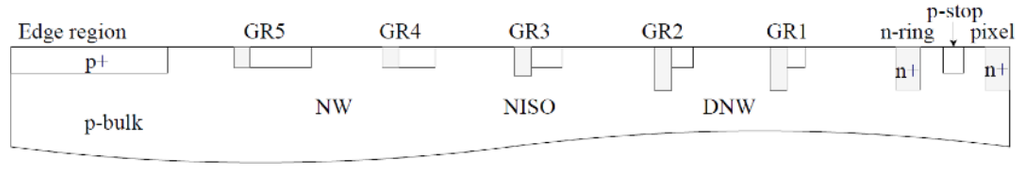
Inject 10 pulses into these pixels

RD50-MPW4
Threshold = 50 mV

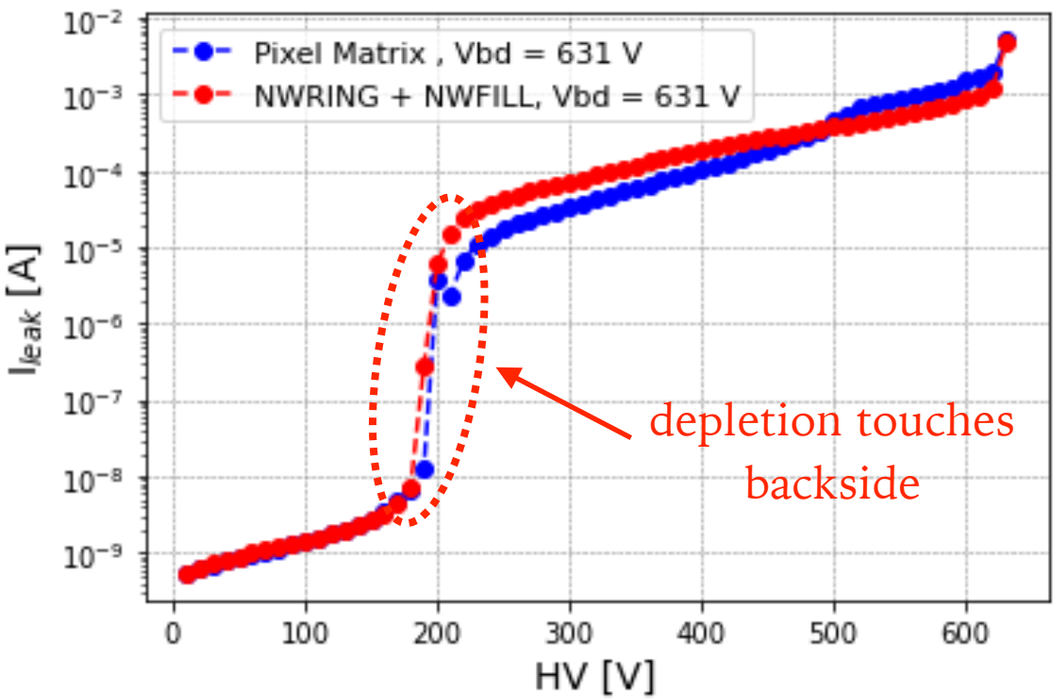


Initial results of RD50-MPW4 – improved breakdown

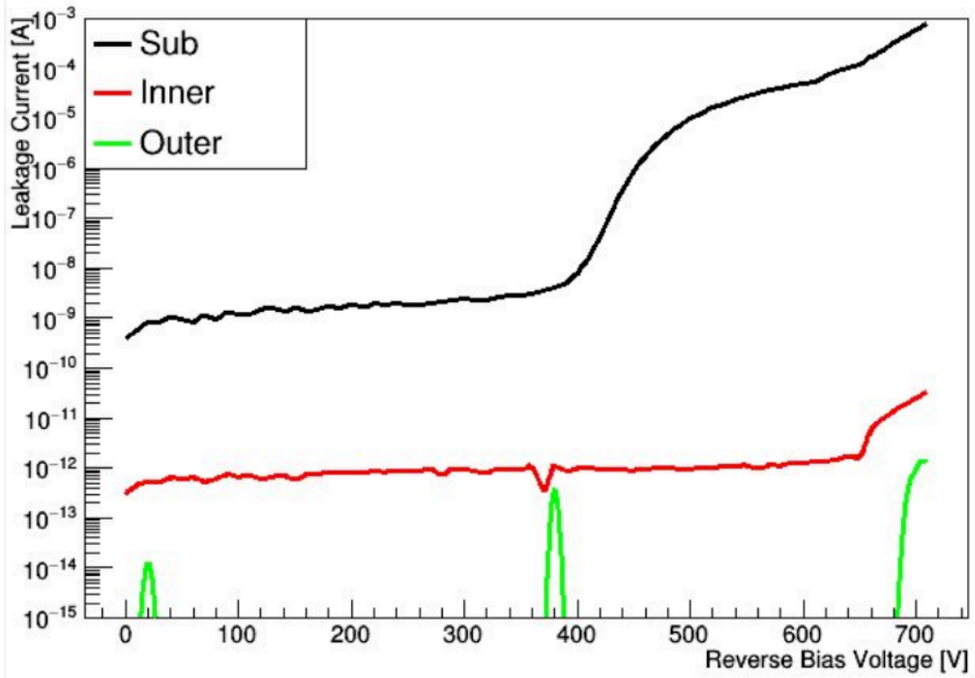
- Improve breakdown voltage with new chip rings.
- 3 kΩ·cm wafers. Samples thinned to 280 μm.
- High voltage applied from top side or back side:
  - ➤ Topside bias: leakage increases to mA at ~200 V (120 V for RD50-MPW3);
  - ➤ Backside bias: after backside processing, leakage increases at ~ 400 V.
- Breakdown at ~600 V.



Topside bias
(no backside processing)

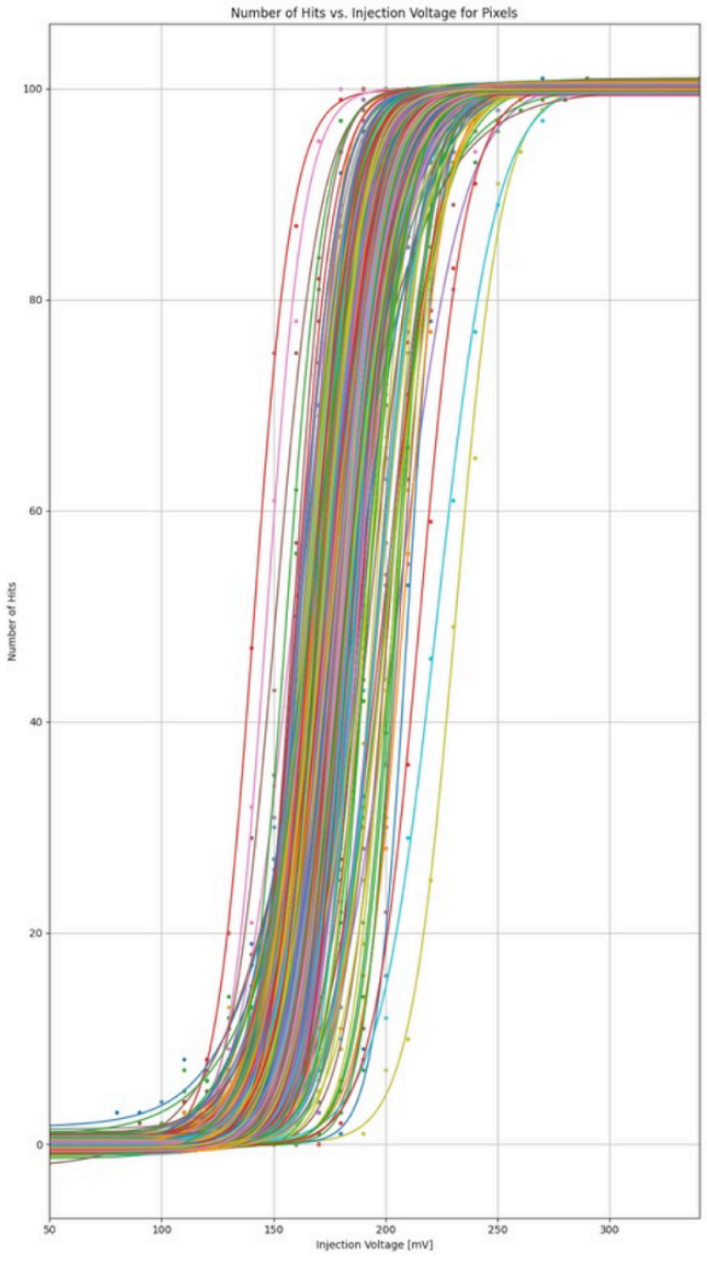


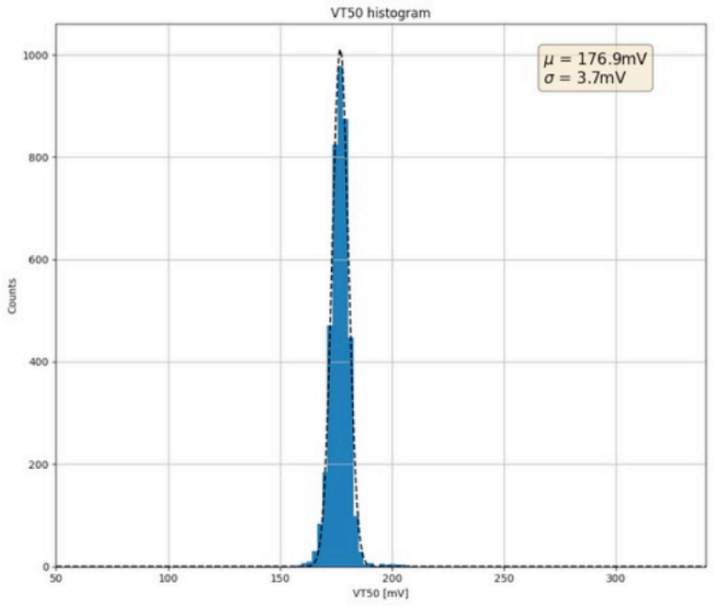
Backside bias
(backside processed)

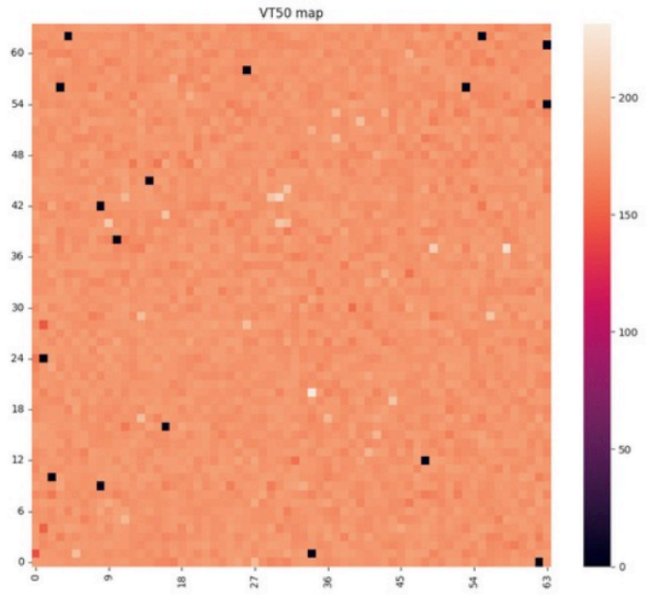


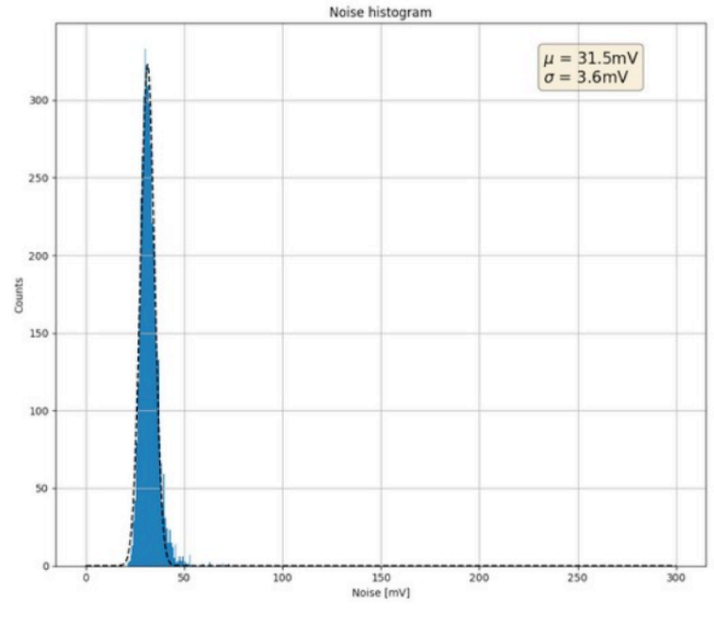
Initial results of RD50-MPW4 – pixel performance

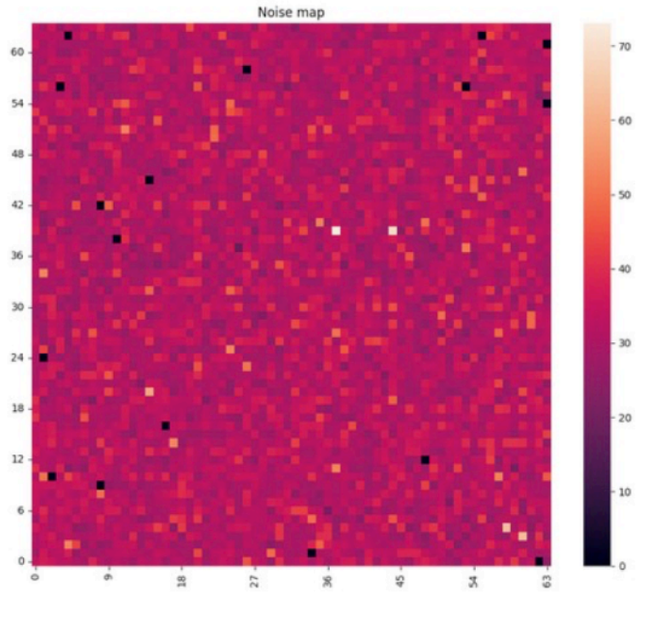
- S-curve scan on the pixel matrix:
  - ➤ small threshold dispersion;
  - ➤ noise ~200 e^- (ENC).











Summary

- Testbeam on RD50-MPW3 at DESY
  - ➤ high noise observed on pixels close to readout periphery.
- RD50-MPW4 is designed to fix the issues found in RD50-MPW3 and further increase breakdown voltage.
- RD50-MPW4 samples delivered in Jan. 2024, being measured in lab:
  - ➤ breakdown ~600 V;
  - ➤ high noise issue in RD50-MPW3 has been solved.
- Being irradiated this week: 1E14, 3E14, 1E15, 3E15, 1E16, 3E16 n_{eq}/cm^2.
- Testbeam measurement at DESY has been booked for RD50-MPW4 in April.
- This R&D work will continue under the umbrella of DRD3.

Acknowledgements:

- This work has been partly performed in the framework of the CERN- RD50 collaboration.

- It has received funding from the European Union's Horizon 2020 Research and Innovation programme under grant agreement 101004761 (AIDAinnova).

- The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)