# Light readout in DarkSide-20k: from Silicon Photo Multiplier dies to the Photo Detection Units integration in the NOA facility

XIII International Conference
on New Frontiers in Physics
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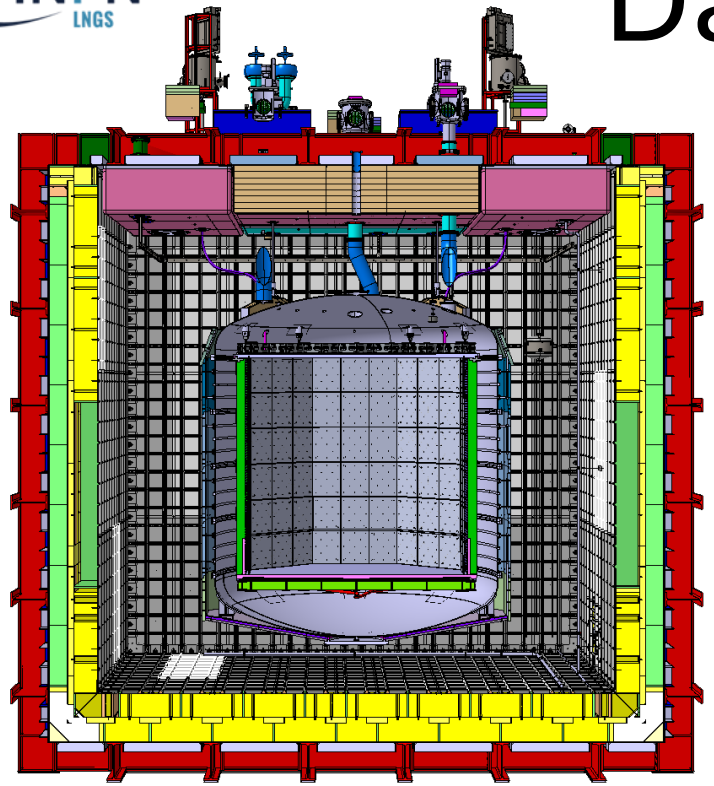
L. Consiglio, INFN LNGS

on behalf of DarkSide-20k collaboration

# Overview

- DarkSide-20k detector structure and installation
- Large area cryogenic Silicon Photo Multiplier technology
- Nuova Officina Assergi (NOA) facility for photosensor packaging and test
- Silicon wafer characterization campaign
- Production processes of DarkSide-20k Photo Detection Unit (PDU)
- Tile test QA/QC and PDU warm test
- Perspectives

# DarkSide-20k detector



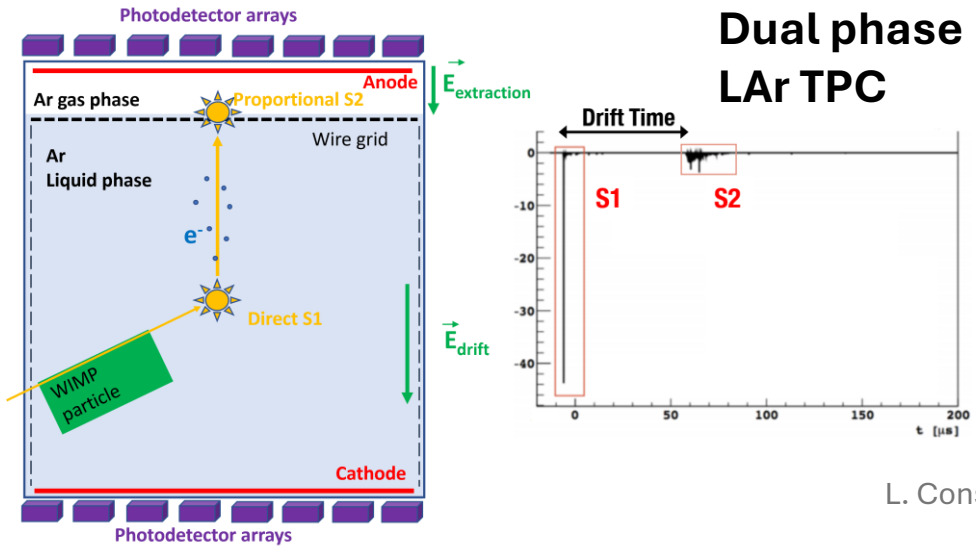
## Breakthrough technologies:

1) low radioactive Underground Argon (UAr) depleted of $^{39}Ar$
2) Large area cryogenic radiopure Si-Photo Multipliers 26 $m^2$
3) Material screening for radiopurity qualification (sub mBq/kg)

Background goal: < 0.1 neutron WIMP-like events in 200 t*yr

## Nested structure

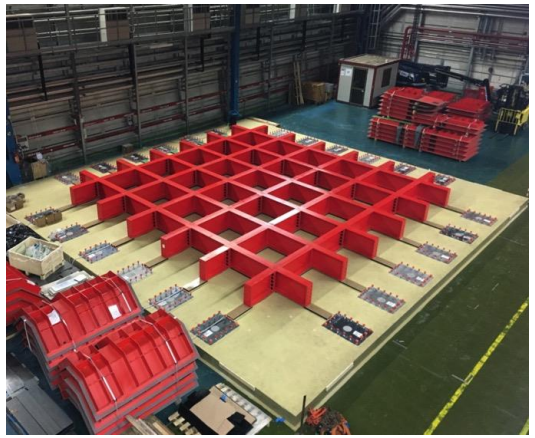
- Inner Detector: octagonal dual phase TPC filled with UAr (active mass ~50 t, fiducial 20 t), coupled with an Inner neutron veto (active UAr mass 32 ton) within SS vessel
- Inner Detector panels Gd-loaded (1%) PMMA for n moderation and capture
- Plastic shielding around vessel (moderation of n from cryostat insulation)
- Outer muon veto for cosmogenics with SiPM arrays
- DUNE-like membrane cryostat filled with 650 t liquid AAr
- **SiPM array technology for signal readout**




**Dual phase LAr TPC**

# DarkSide-20k installation

***Cryostat beam structure construction started in 2023 in LNGS, 1400 m underground (~ 3400 m.w.e).***

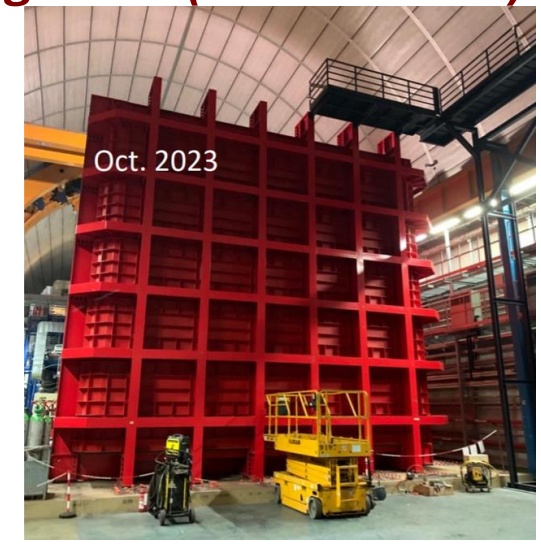


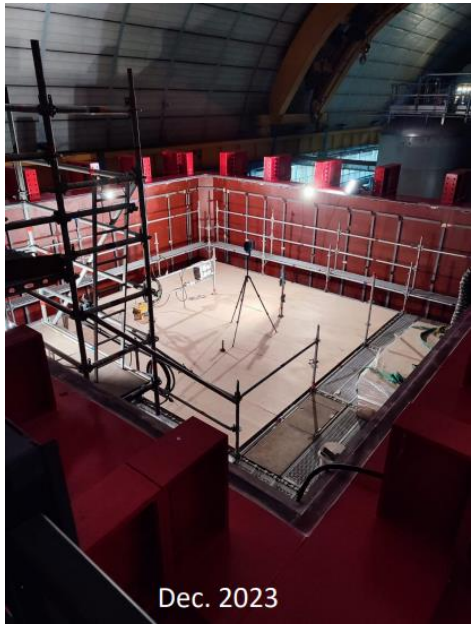
Positioning of the bottom beams on the insulation system

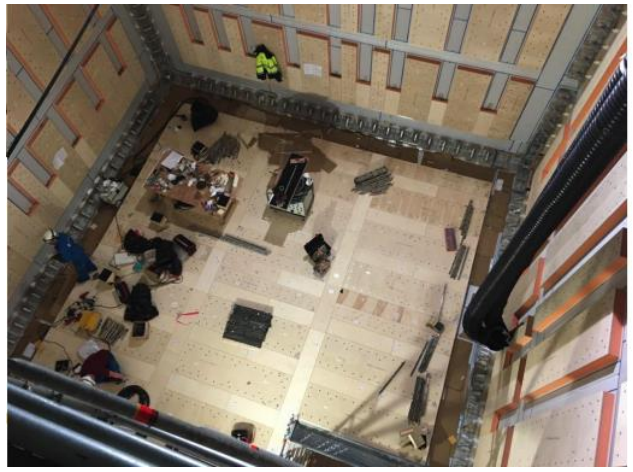
Beam structure assembly completed

Tertiary membrane panels installation

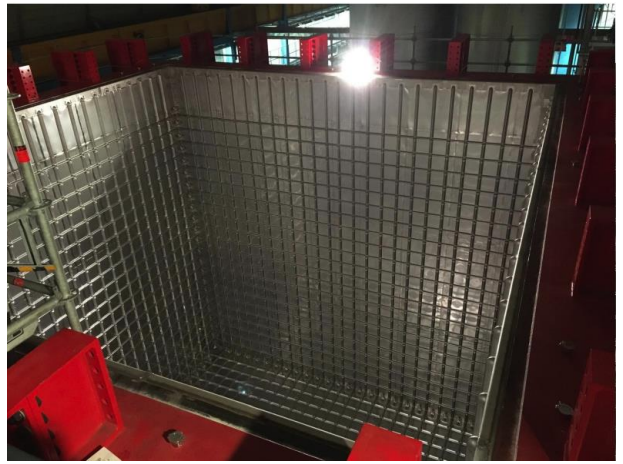

Tertiary membrane panels welding



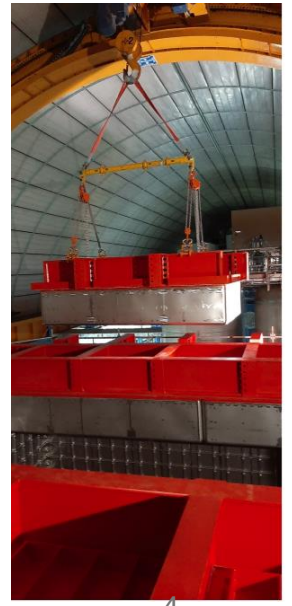



Cryostat cold structure
Insulation blocks installation



Primary membrane welding

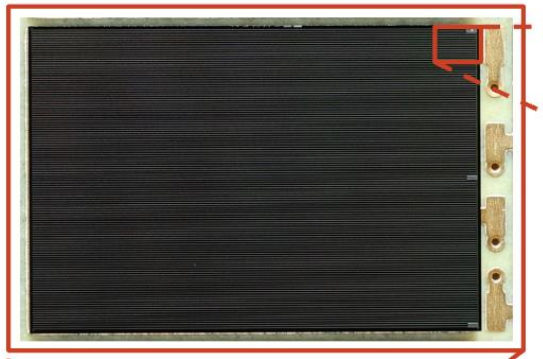


Top caps installation

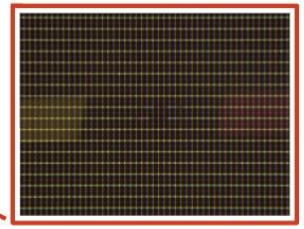
# Light detection: SiPM technology

- High performance cryogenic SiPMs (NUV-HD-CRYO by FBK) **ref. L. Consiglio talk ICNFP 2022**
- Low noise cryogenic electronics for large area readout (INFN LNGS)
- Technological transfer for photosensor mass production (LFOUNDRY)

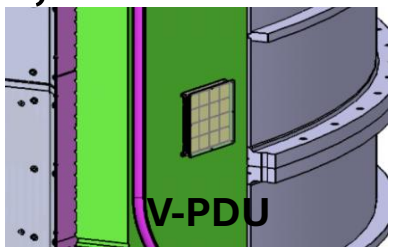
**SiPM 11.8 x 7.9 mm²**



**SPAD array**
**Pitch 30 µm**

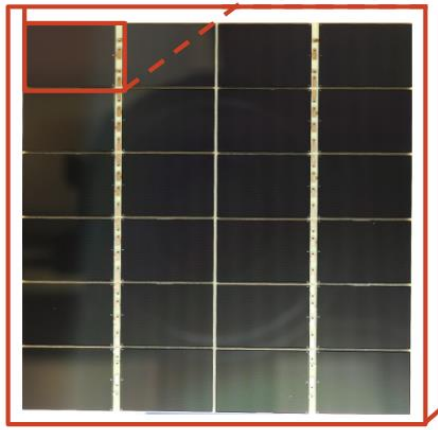


**TPC optical planes (top & bot): 528 PDUs;**
**8448 Tiles;**
**Inner Veto: 120 V-PDUs**
**Outer Veto: 32 V-PDUs**



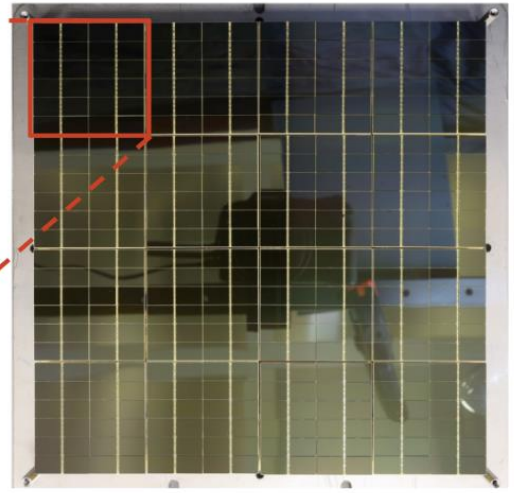

Total V-PDU surface 5 m²

**Tile: 24 SiPM**

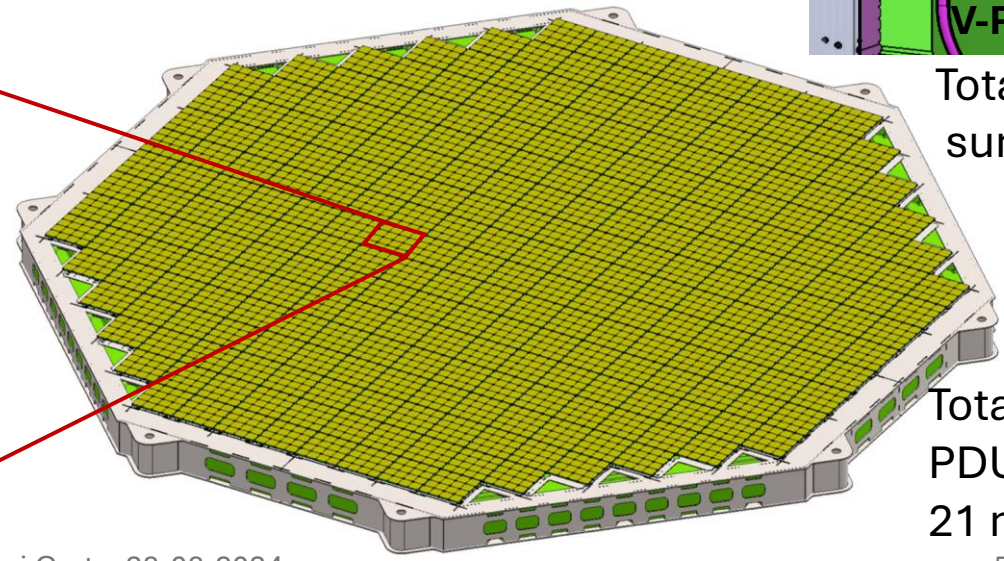


**4.95 x 4.95 cm²**

**PDU: 16 tiles**

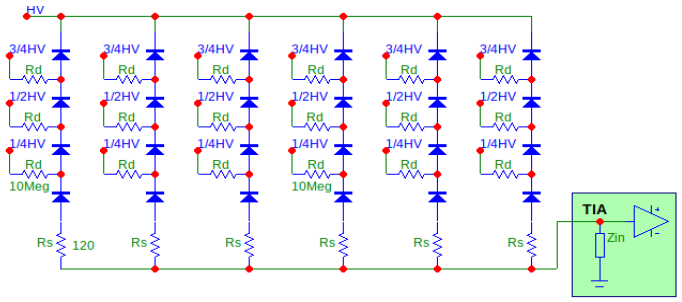


**20 x 20 cm²**



Total TPC PDU surface 21 m²

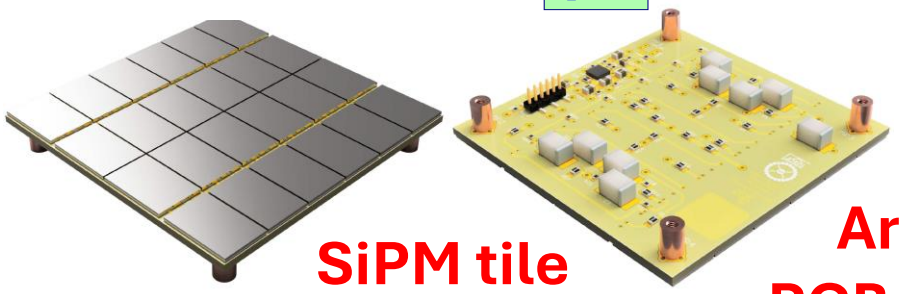
# Photo Detection Unit design




Fast low noise
Cryogenic Trans
Impedance Amplifier

**ref. L. Consiglio talk ICNFP 2022**

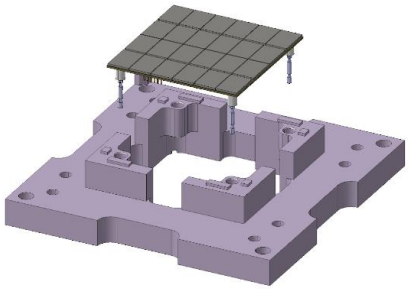
**Arlon MOTHERBOARD**



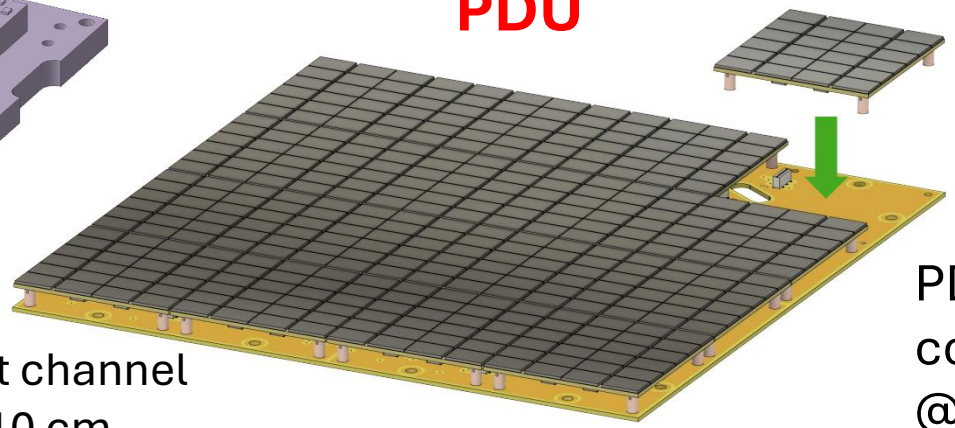
**SiPM tile**

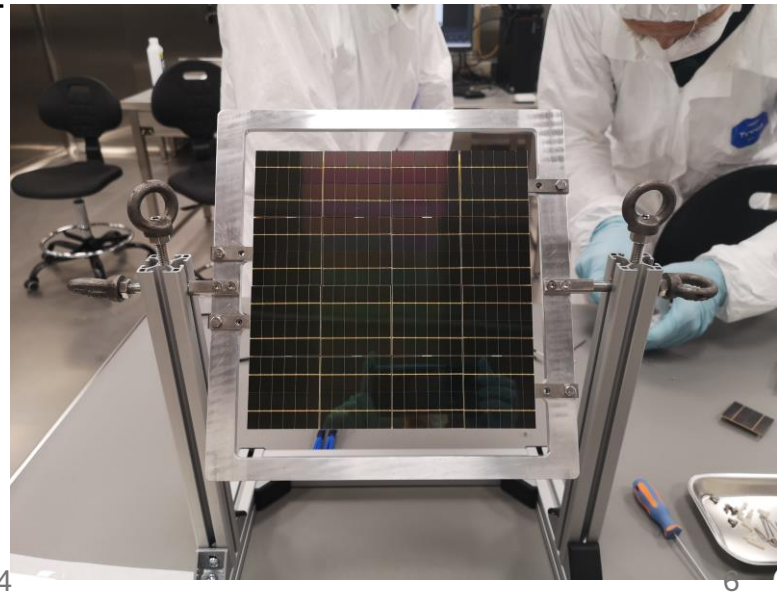
**Arlon PCB + FEB**

4 readout quadrants (Q1 Q2 Q3 Q4) each grouping 4 tiles
Steering Module (HV-LV remotely controlled)
Adder + SE to DIFF



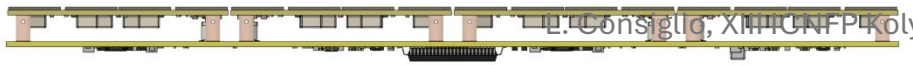
**PDU**



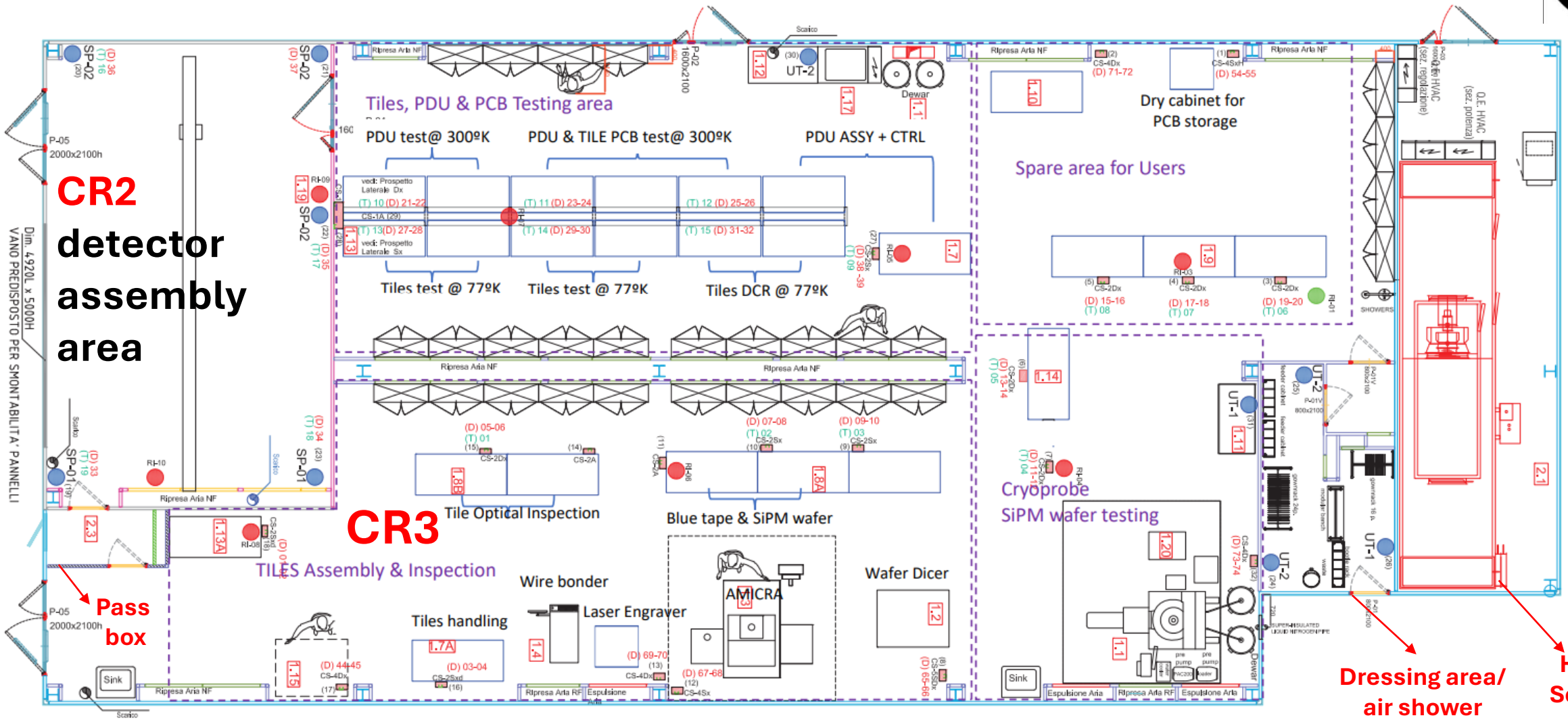


Single readout channel
size: 10 cm x 10 cm

PDU power
consumption
@77K: 2 W



# Nuova Officina Assergi for DS-20k SiPM packaging

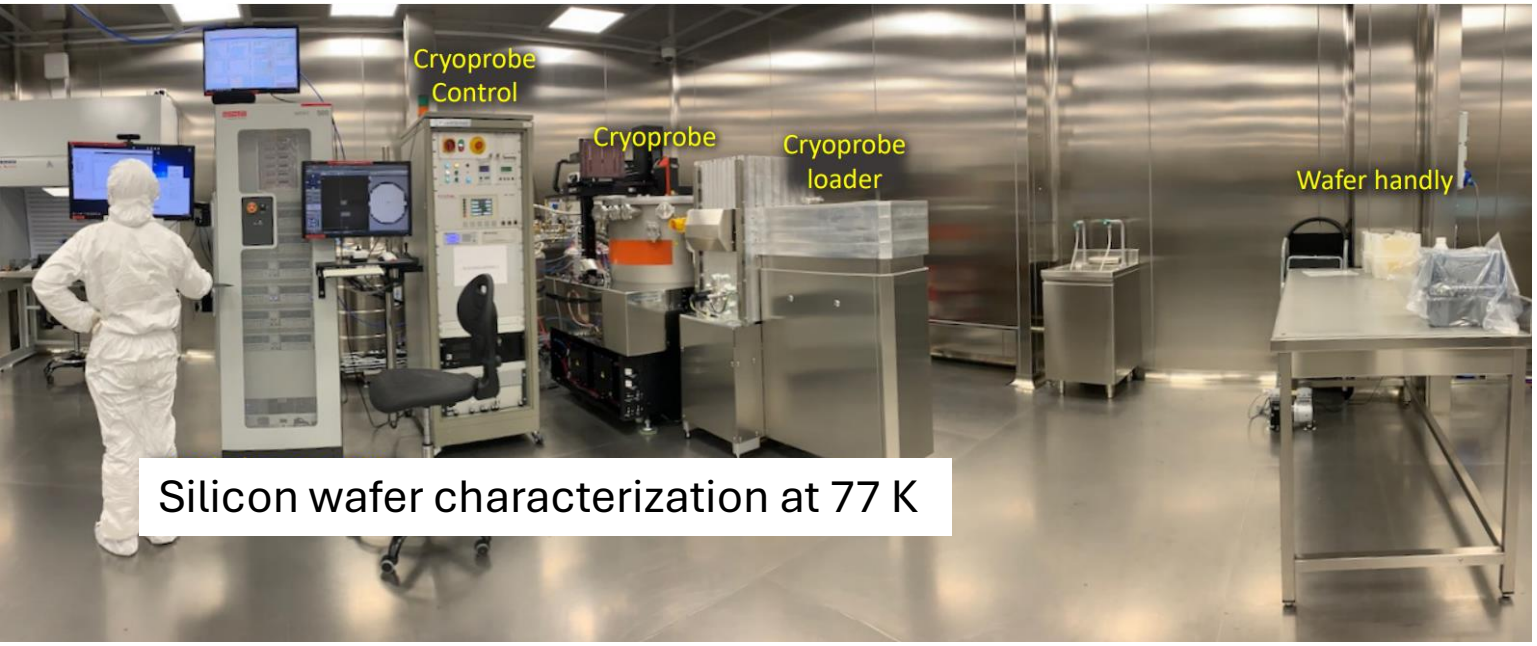



Class ISO-6 (ISO-5 from July measurements) with an overall area -> 421 $m^2$

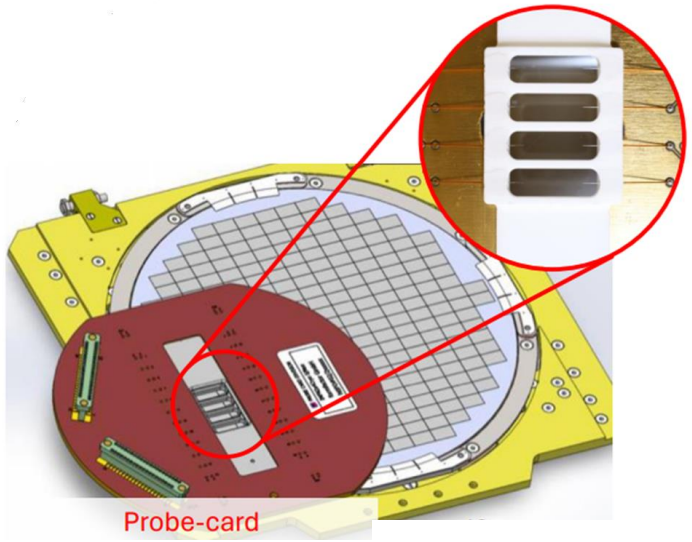
CR3 : 3.0 m high and an area of 353 $m^2$ : devoted to the SiPM test, packaging, and integration

CR2 : 5.8 m high and an area of 68 $m^2$ : devoted to large volume detector assembly

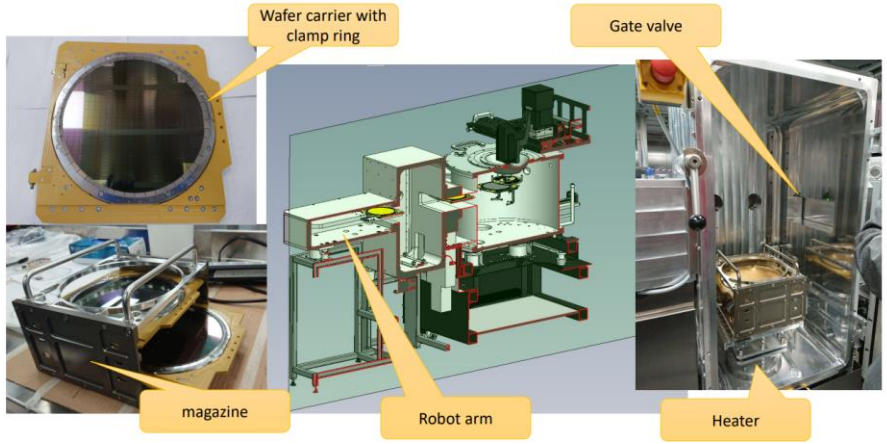
# Cryoprobe test area

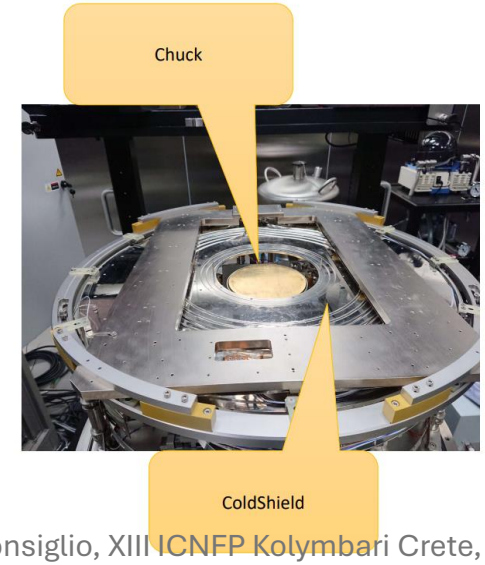


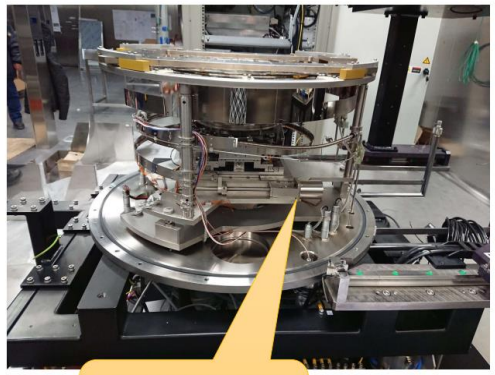

Silicon wafer characterization at 77 K

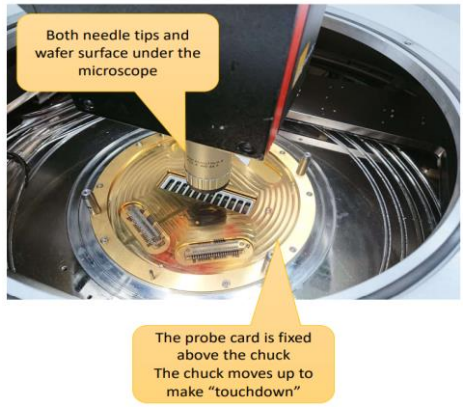



**2 x 4 array of needles for anode contacts**



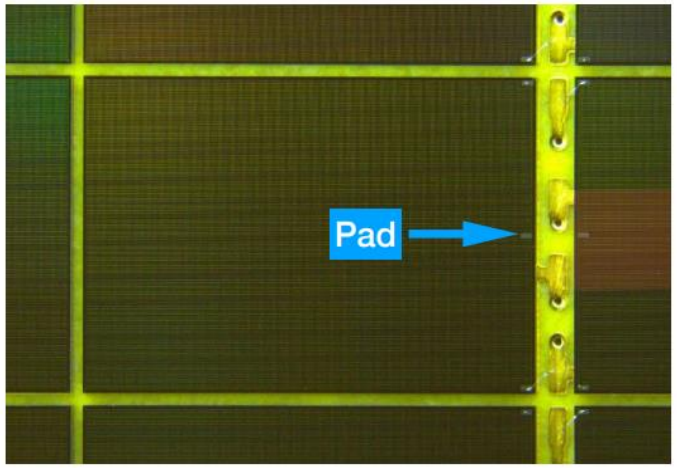



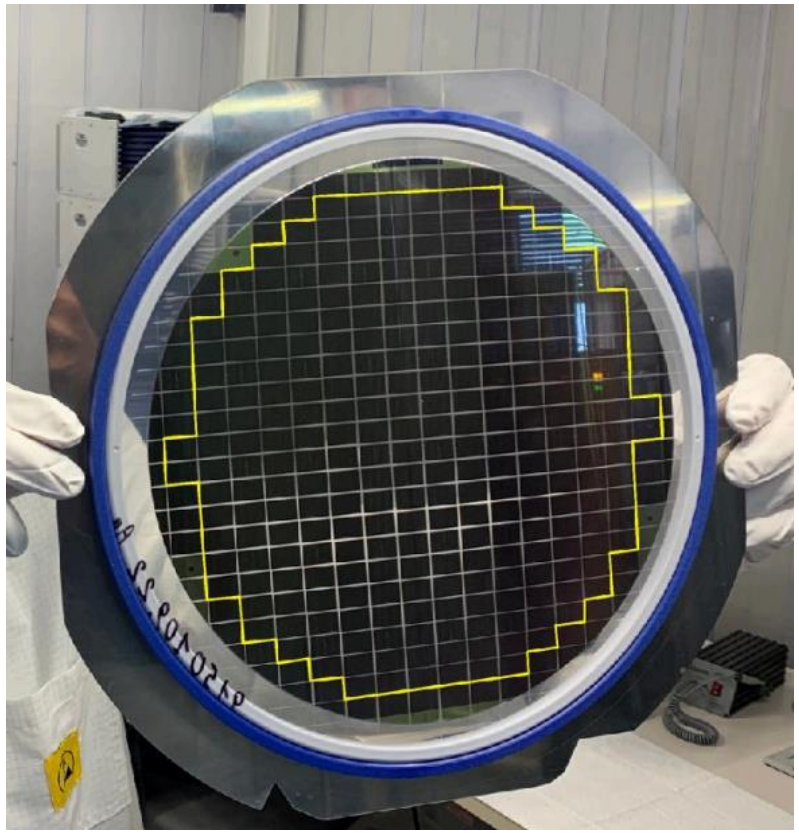
# Si wafers by LFOUNDRY

1400 wafers, 8 inches, 550 µm thick have been produced by LFoundry s.r.l. (Avezzano, AQ, Italy) and stored in NOA

268 dies/wafer (264 accessible for test).
Wafer produced in 57 lots (~25 wafers)

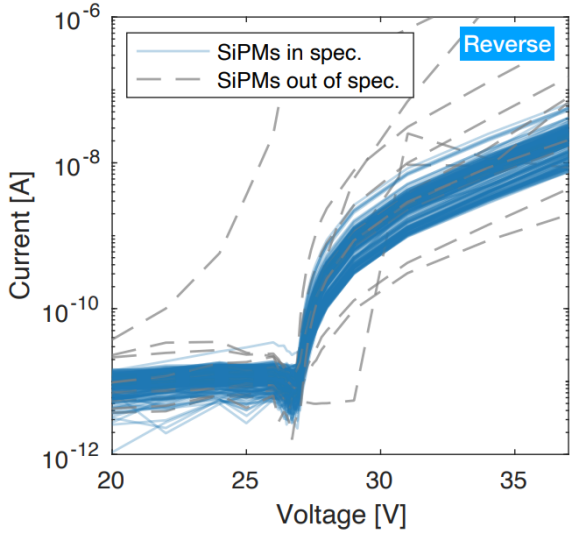

Each wafer in the Lot has a gold-coated backside that acts as the SiPM cathode.
The SiPM anode contact is composed by 3 short-circuited aluminum pads.
• One pad is used for cryoprobing, the other two for wire bonding.

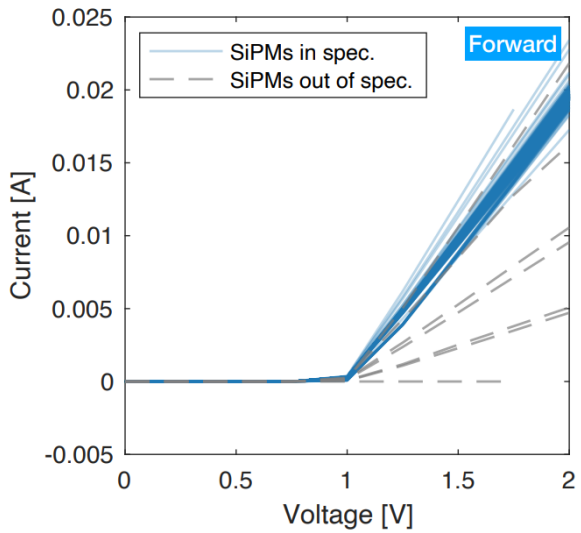


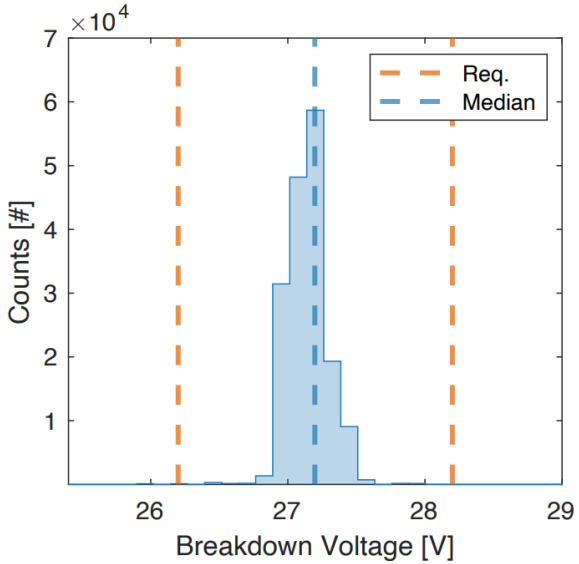
928 wafers tested for a total number of SiPMs= 244.992

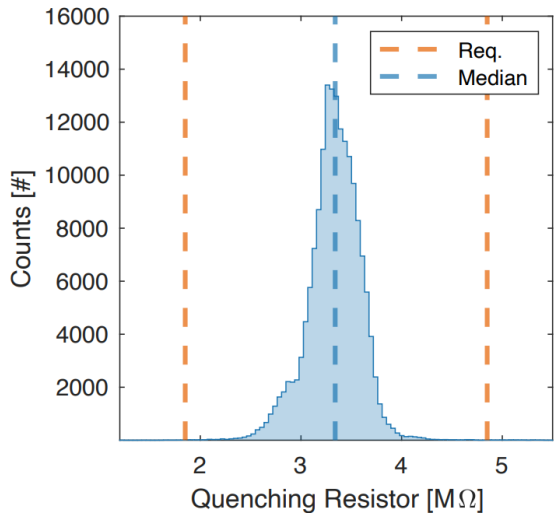
# Measured parameters

Reverse and Forward bias IV curves are measured on each wafer die at 77 K



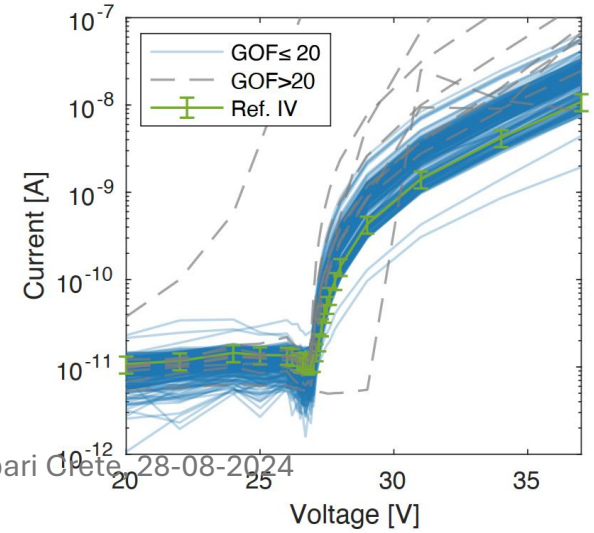

1. Breakdown voltage Vbd ∈ [27.2 ± 1.0] V

2. Quenching resistor Rq ∈ [3.35 ± 1.50] MΩ

3. Leakage current before breakdown (at 20 V)
   IL ≤ 40 pA

4. Goodness of FIT to ensure compliance
   of the wafer level IV curves (GoF ≤ 20)

5. Lot by lot variability monitoring

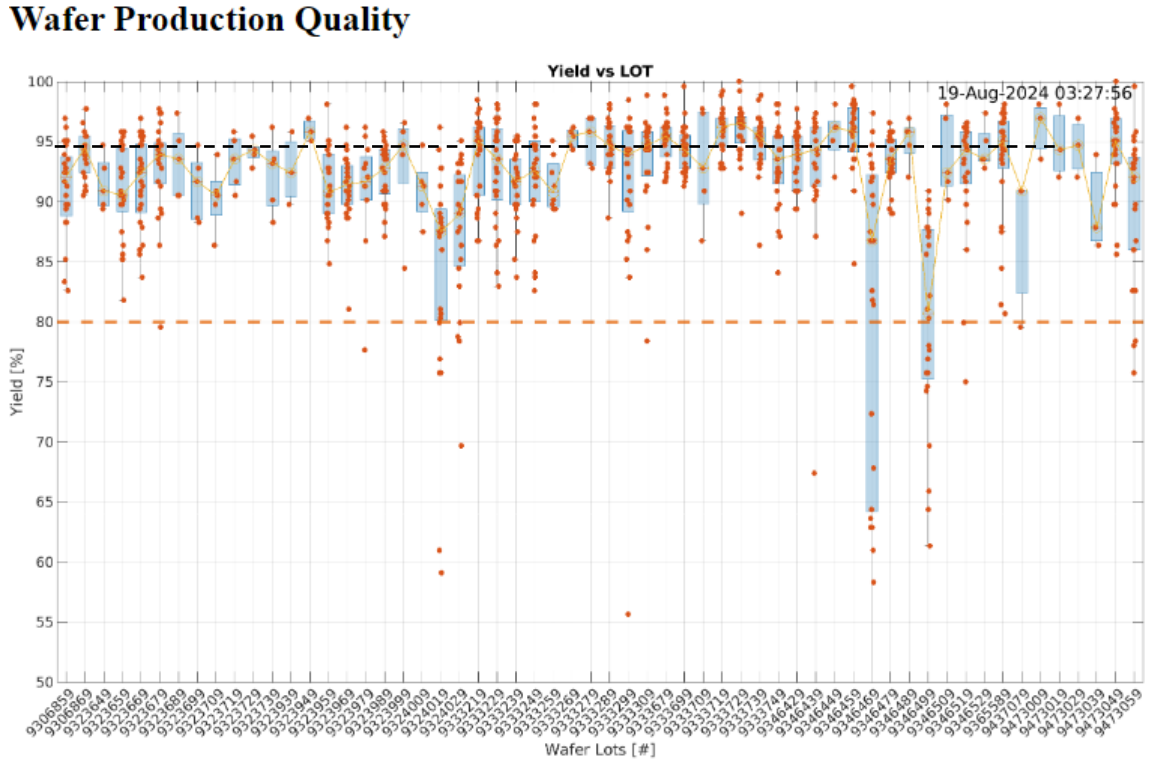


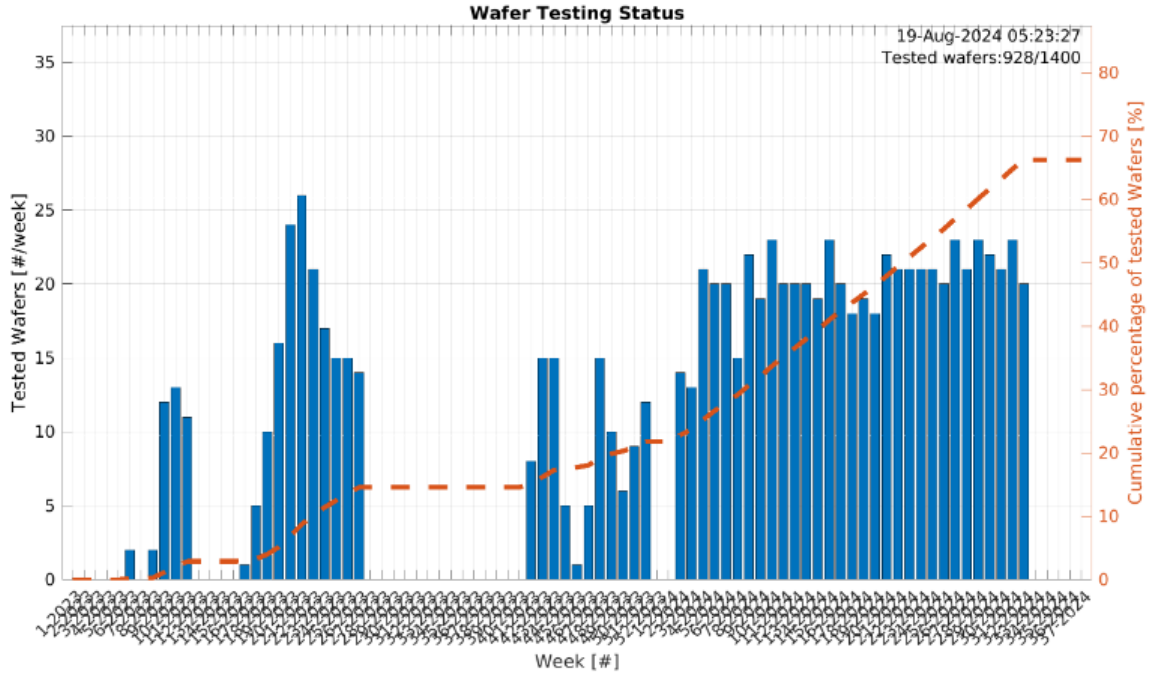

Measured IV

Reference IV

$$\mathrm{GOF} = \sum_i \frac{(I_i - k\bar{I}_i)^2}{\bar{\sigma}_i^2}$$

# Wafer test quality




Test rate: 22 wafers/week -> 66% out of the full production already tested -> completion expected by March 2025

Production Average Yield 94% (acceptance spec > 80%)

Shift operations on 12 hours from Mon-Fri

Measurement time: ~3 h/wafer (40 min cool down, 15 min alignment, 1 h 40 min test, 20 min warm up

# Packaging area

ADT 7122 DICER


AMICRA NOVA PLUS
FLIP CHIP BONDER


HESSE
WIRE BONDER

LASER ENGRAVER

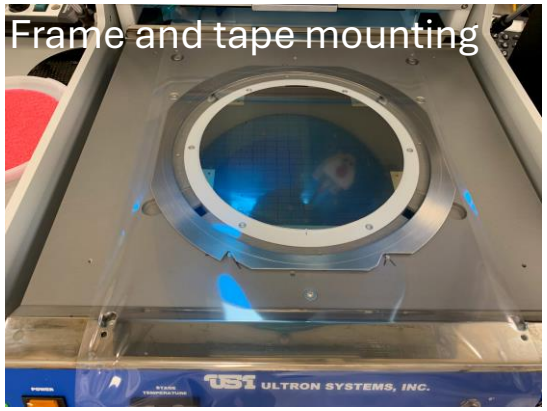
MICROSCOPE

PULL
TESTER

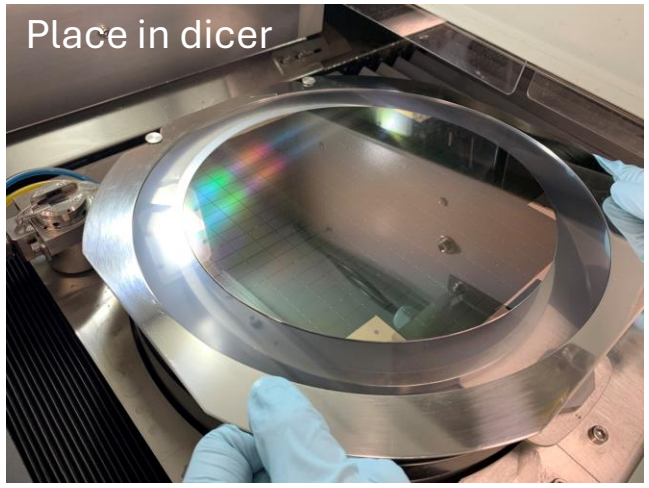
# Semi-conductor assembling system

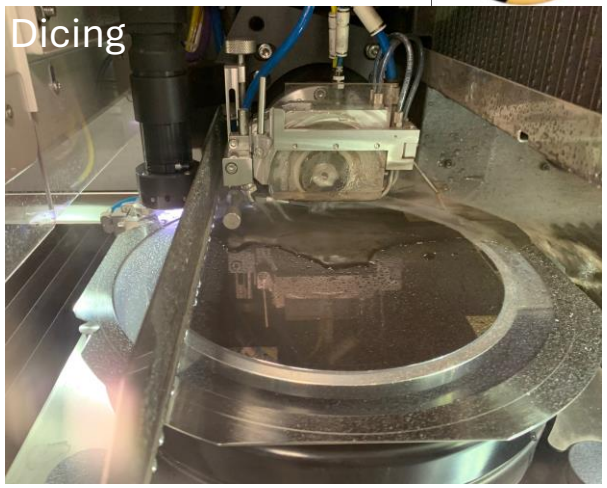

1. Frame mounter and tape release (6-8 inches) – blue tape is glued onto the wafer backside that is mounted on a metal frame to be handled into the dicer
2. UV-Curing (6-8 inches) – the wafer is cured by a UV light to reduce the adhesion strength of the tape and easily remove the diced SiPMs
3. Die-Matrix Expander (8 inches) – to space the SiPMs apart from each other on the blue tape

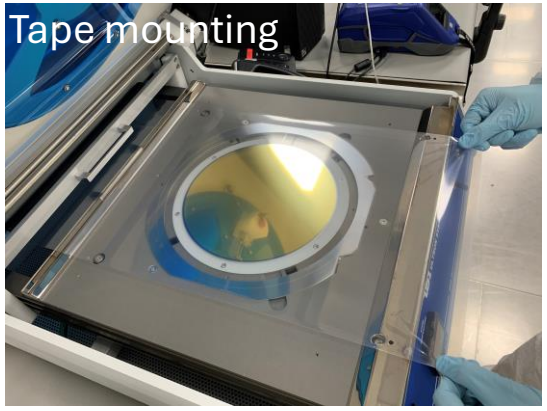
# Wafer handling and dicing

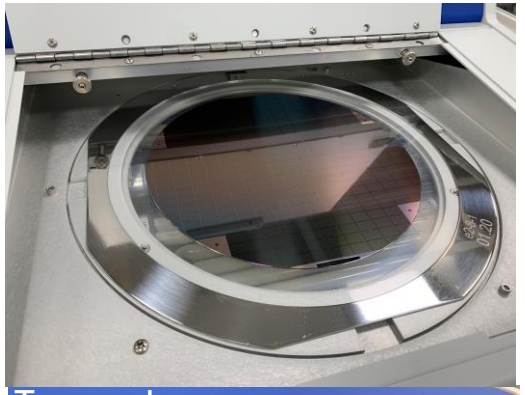


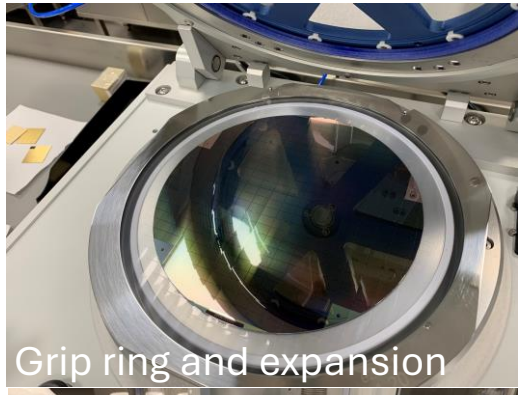


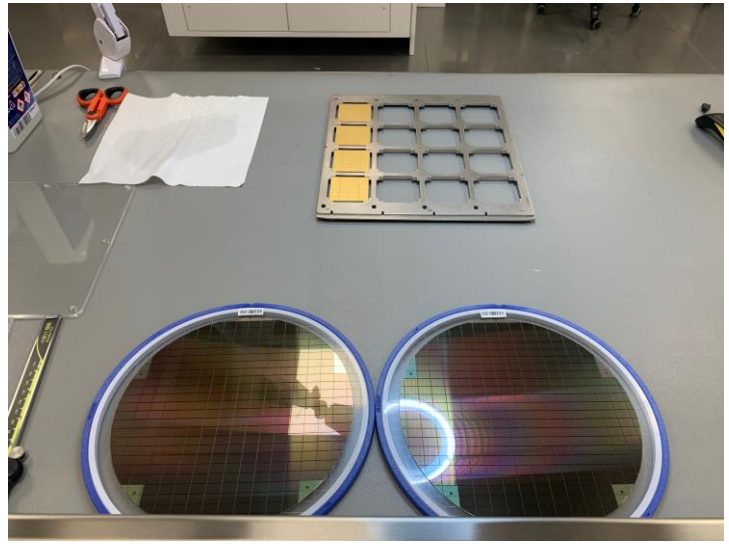






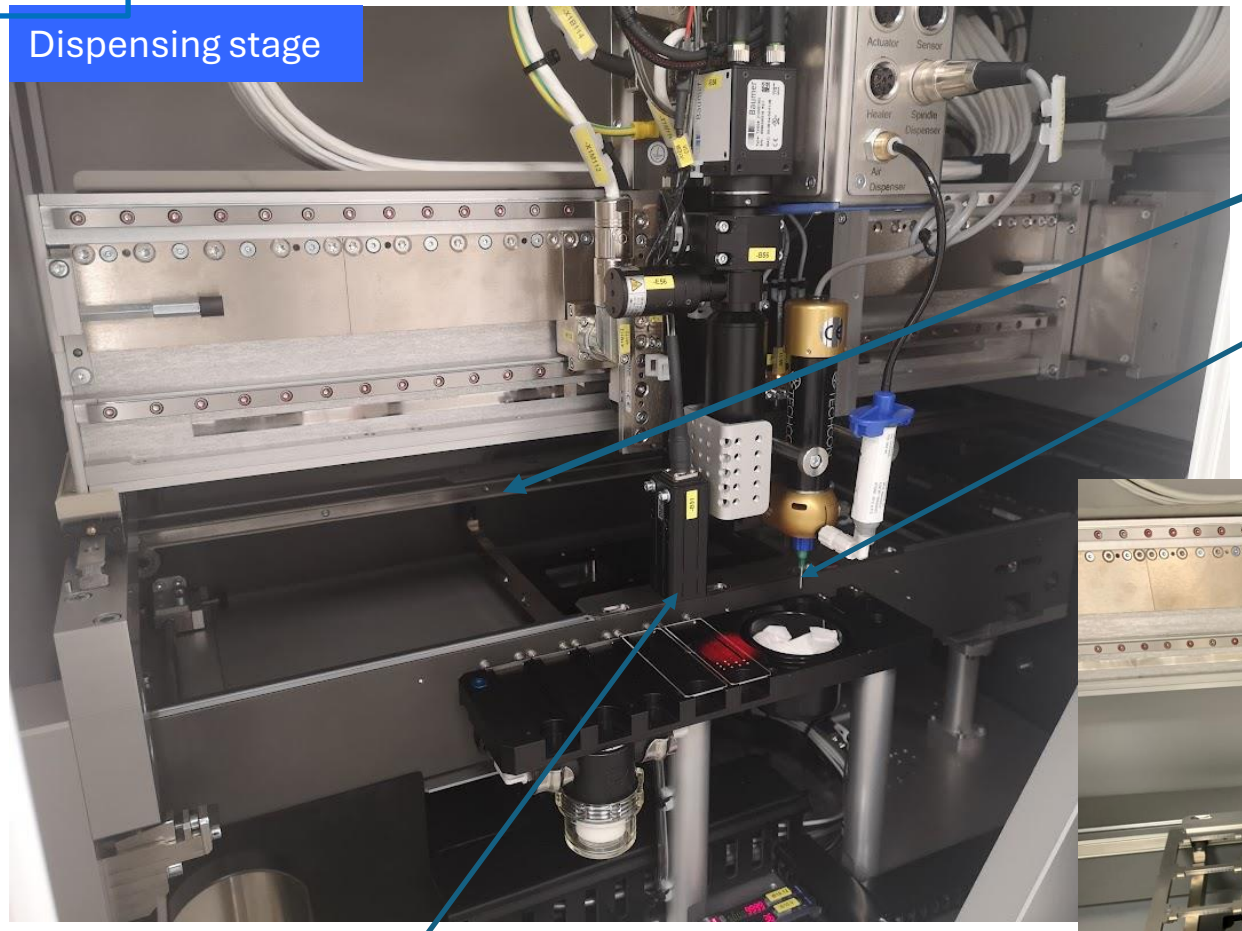

Ready to be processed

# Flip chip bonder: pre-processing stage

DarkSide-20k tile PCB

Frame holder for the PCBs each one to be assembled with 24 SiPMs

Dispensing stage



Conveyor

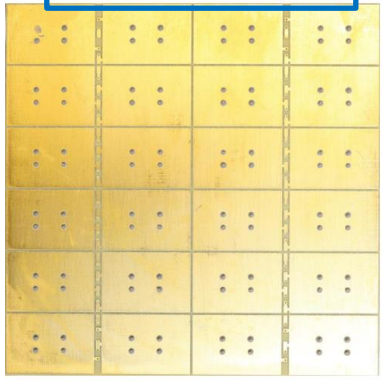
Dispenser

Solder paste dispensing

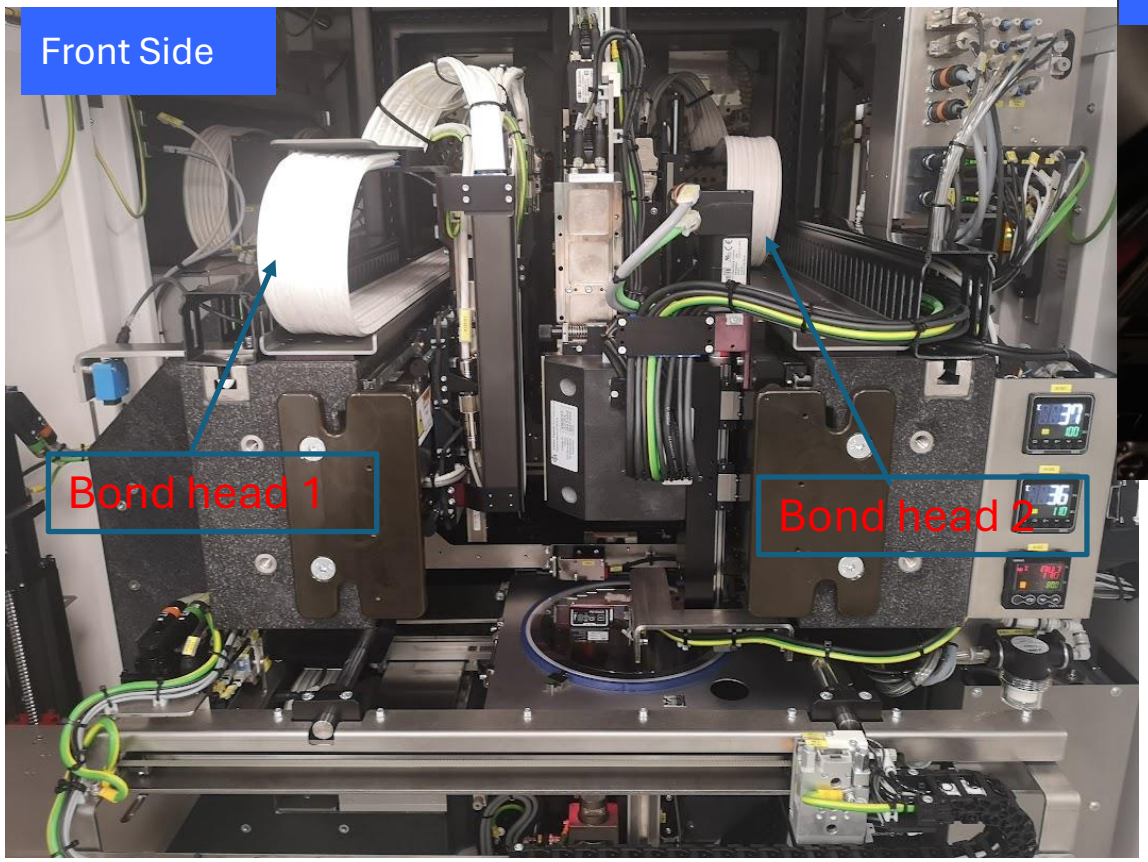
Camera

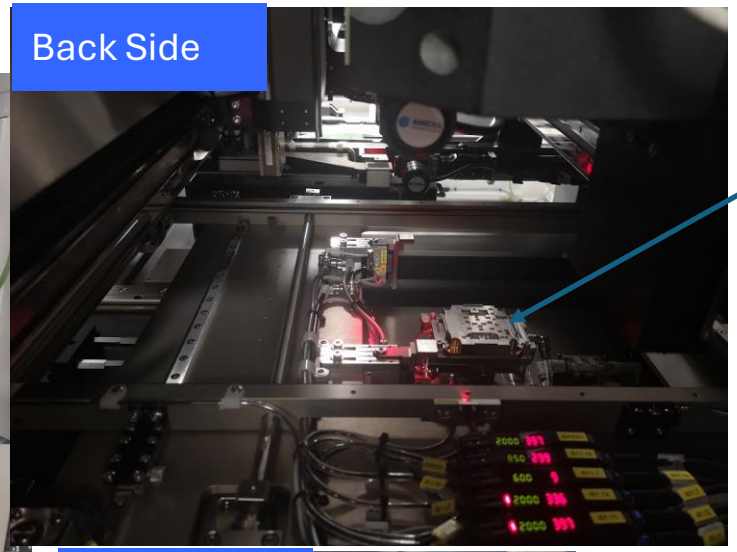
Dispensing time: <5 min/PCB
1 hour per tray

PCB post dispensing



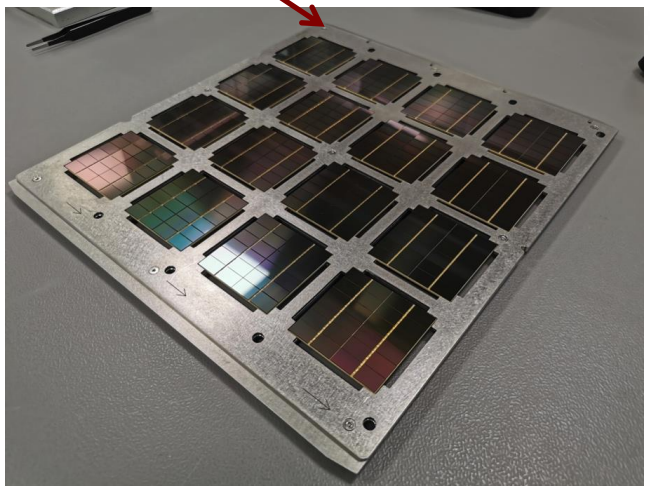
# Die bonding (no flip)




Heater plate
Max T 350°C


**Final Tiles**

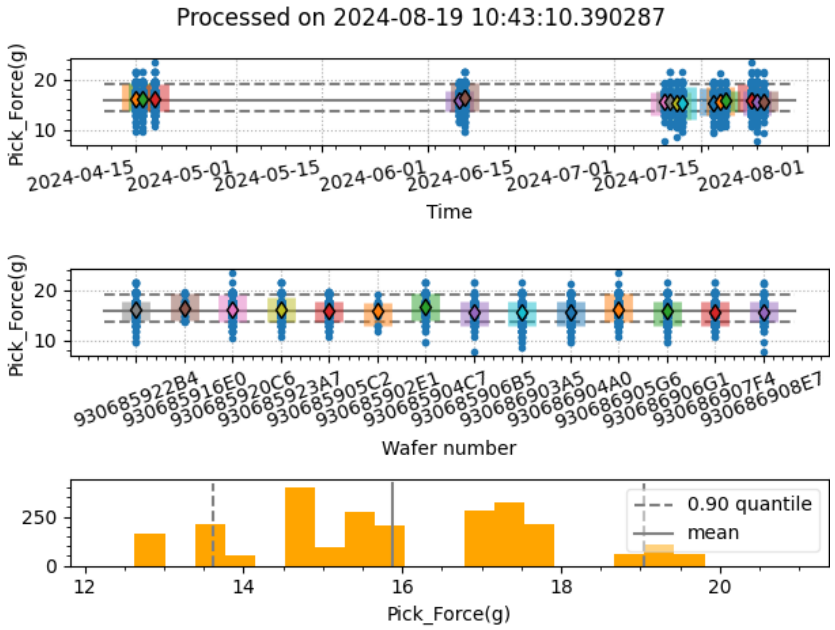


Pick & place time: 6 min/PCB + 1 min for chuck heating
Total time: 96 min + 16 min = 1 h 52 min

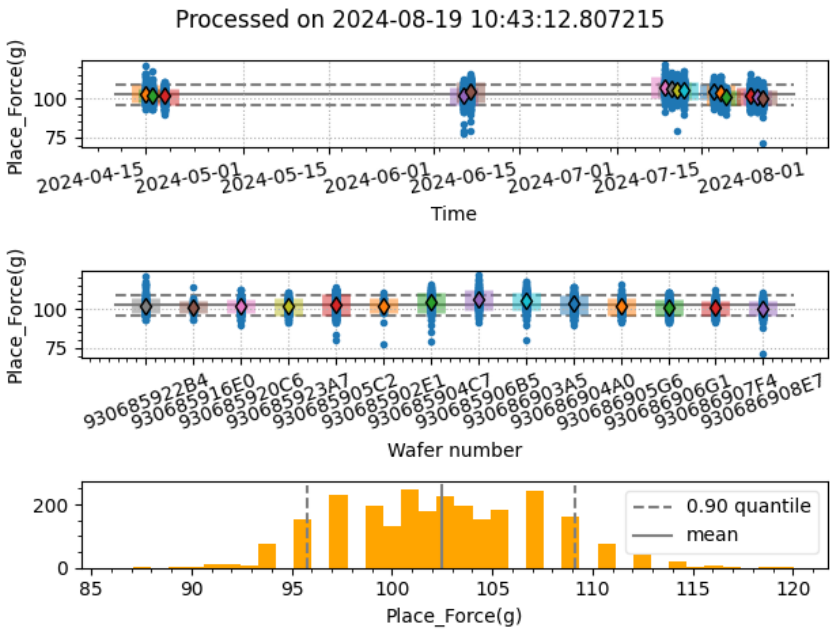
# Process stability

- The Themo Compression Bonding process starts with the PCB placed on the heater chuck.
- Heater temperature set at the temperature of 80 C.

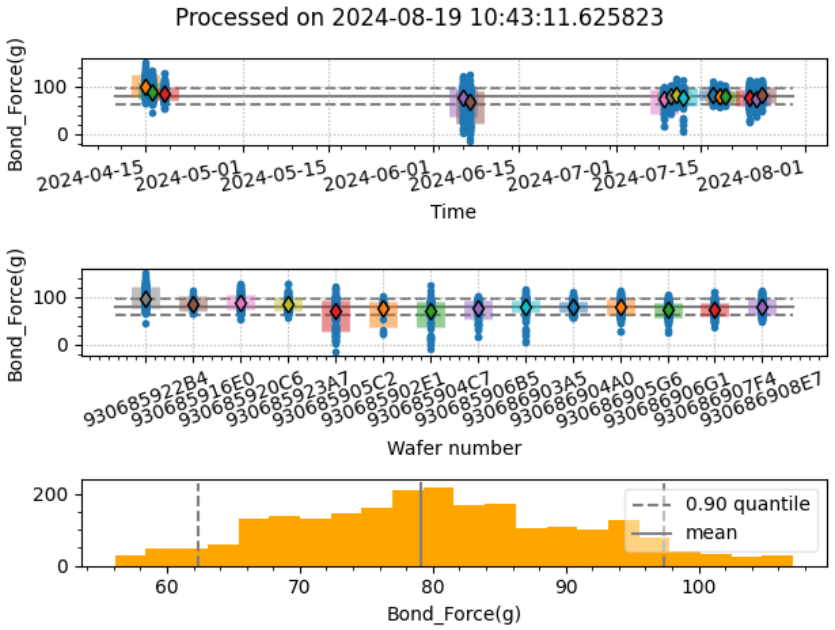
Each Bond Head performs the following operations:
-pick the die from the tape ( picking up Temperature 110 C, nominal pick up force 20 g)
-place the die in position on the PCB after aligning of the die with the substrate (placing Temp 120 C)
-bond the die applying the required force (100 g) for a defined period of time (5 s) (bond Temp 135 C) .




Pick up force

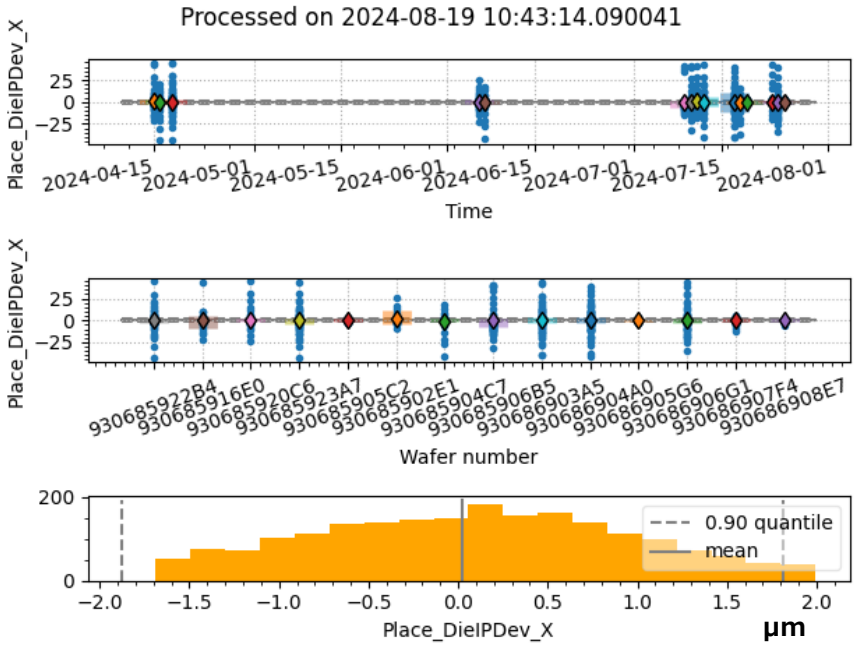



Place force



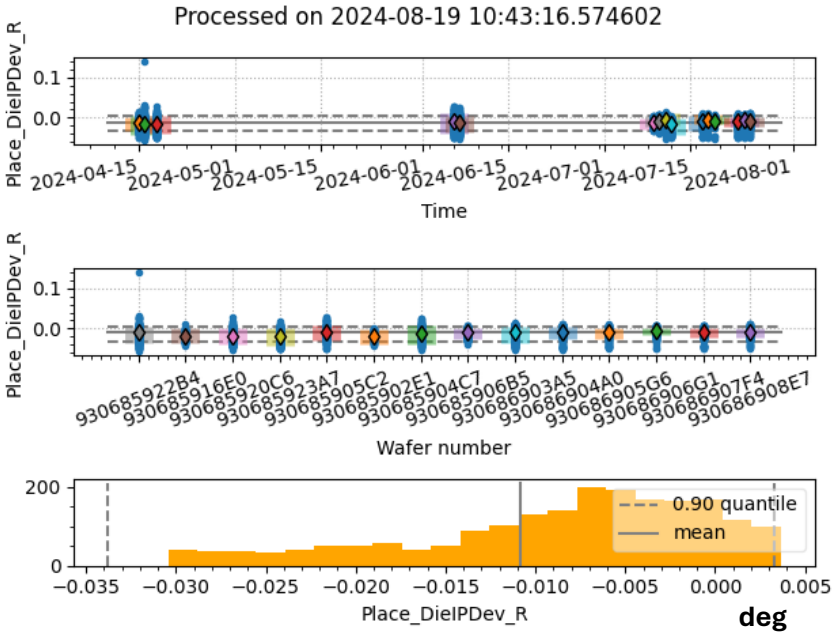

Bond force

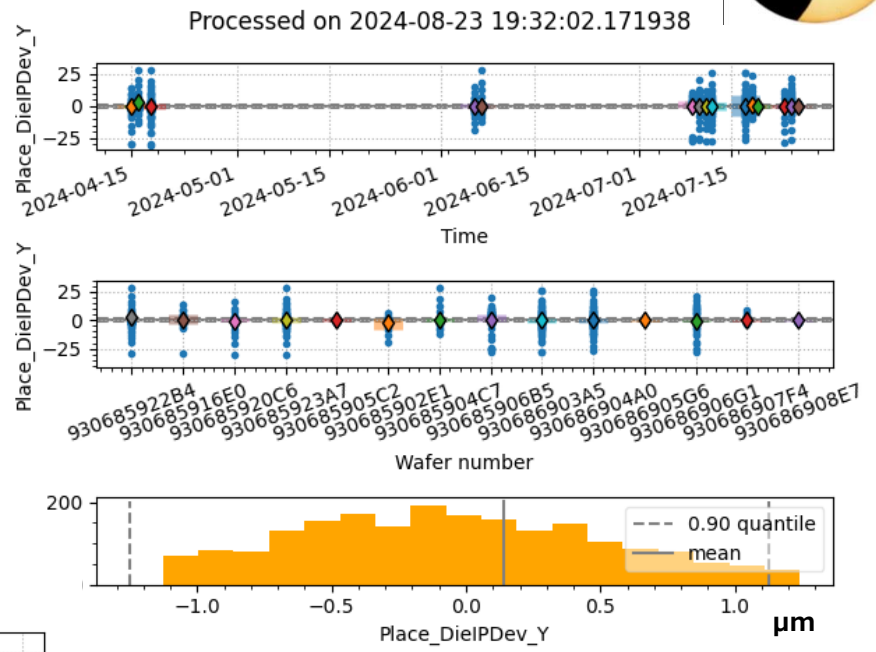
# Process accuracy




X displacement

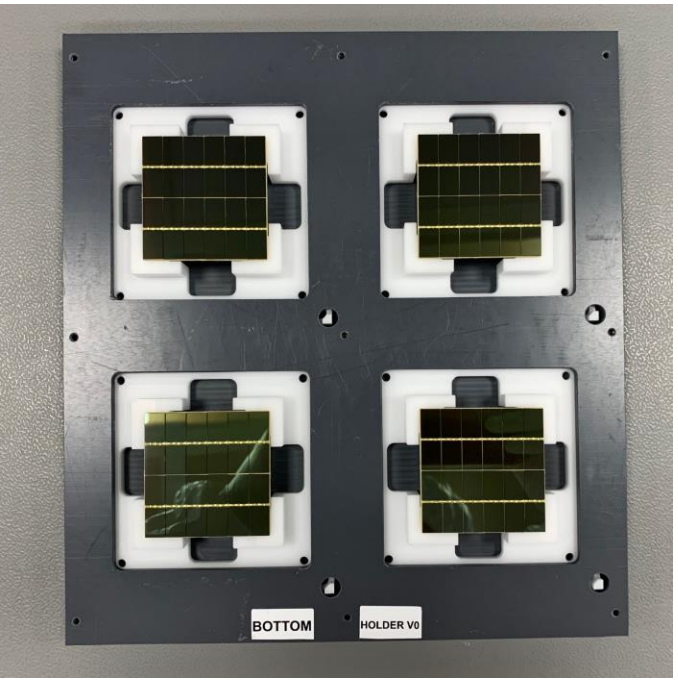
Rotation

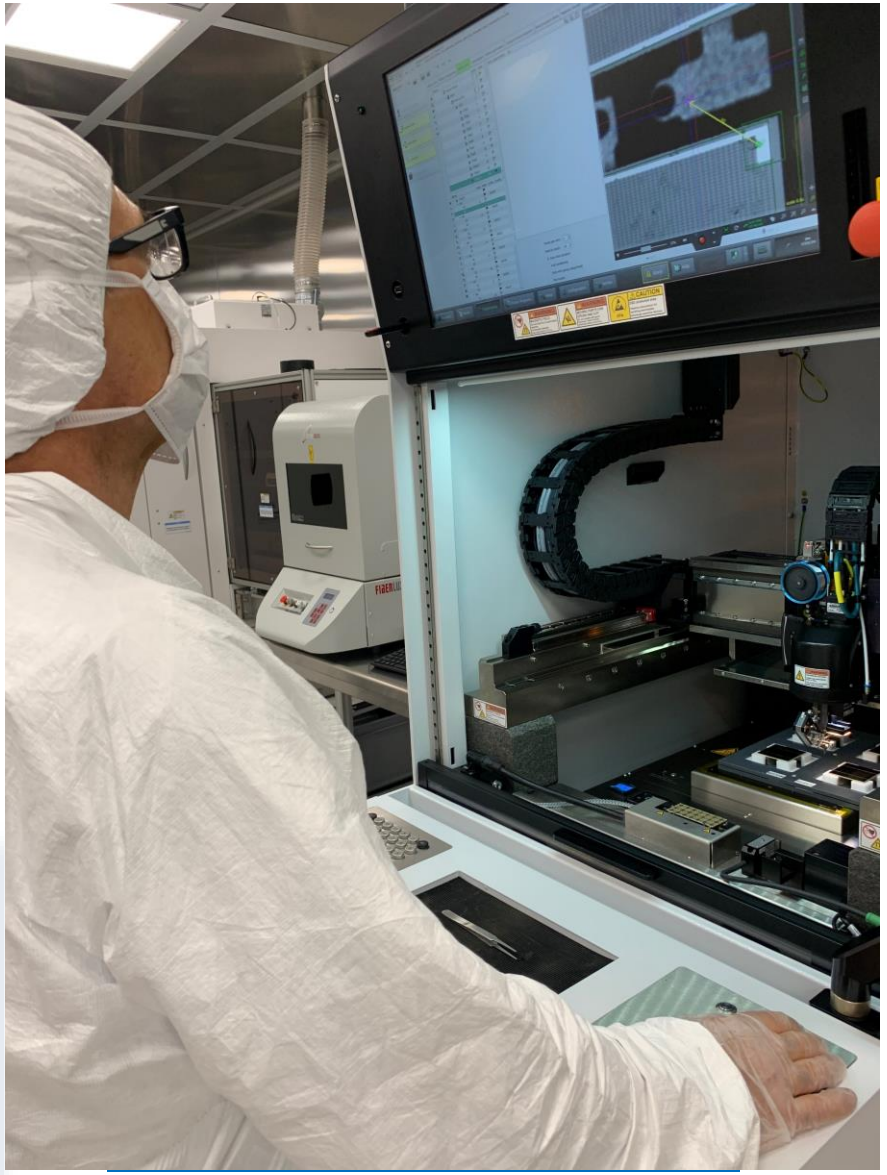


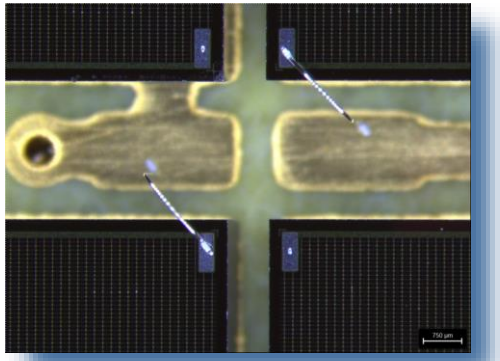




Y displacement

# Wire bonding



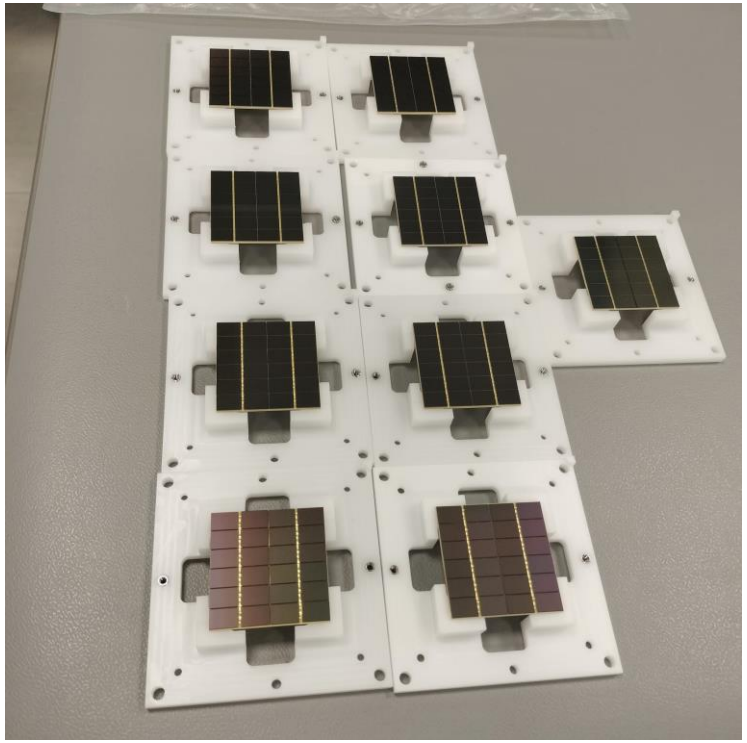


Bondhead BK06 designed for thin wire processes according to the wedge-wedge process (currently in use)

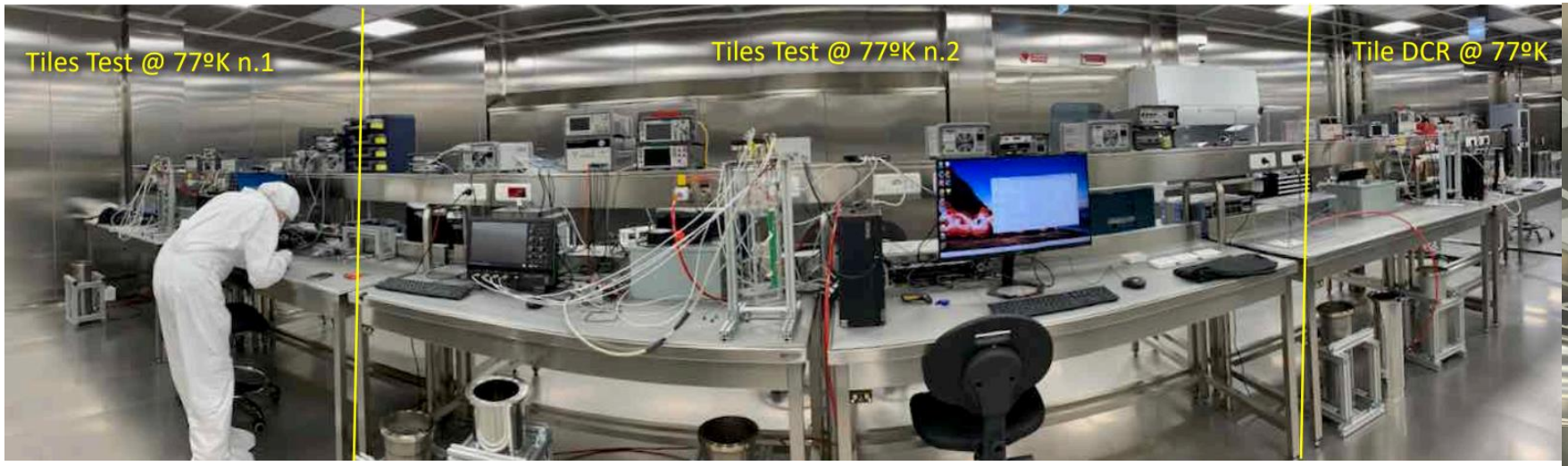
Bondhead DA06 deep access with a compact design available for bonding inside difficult to access devices

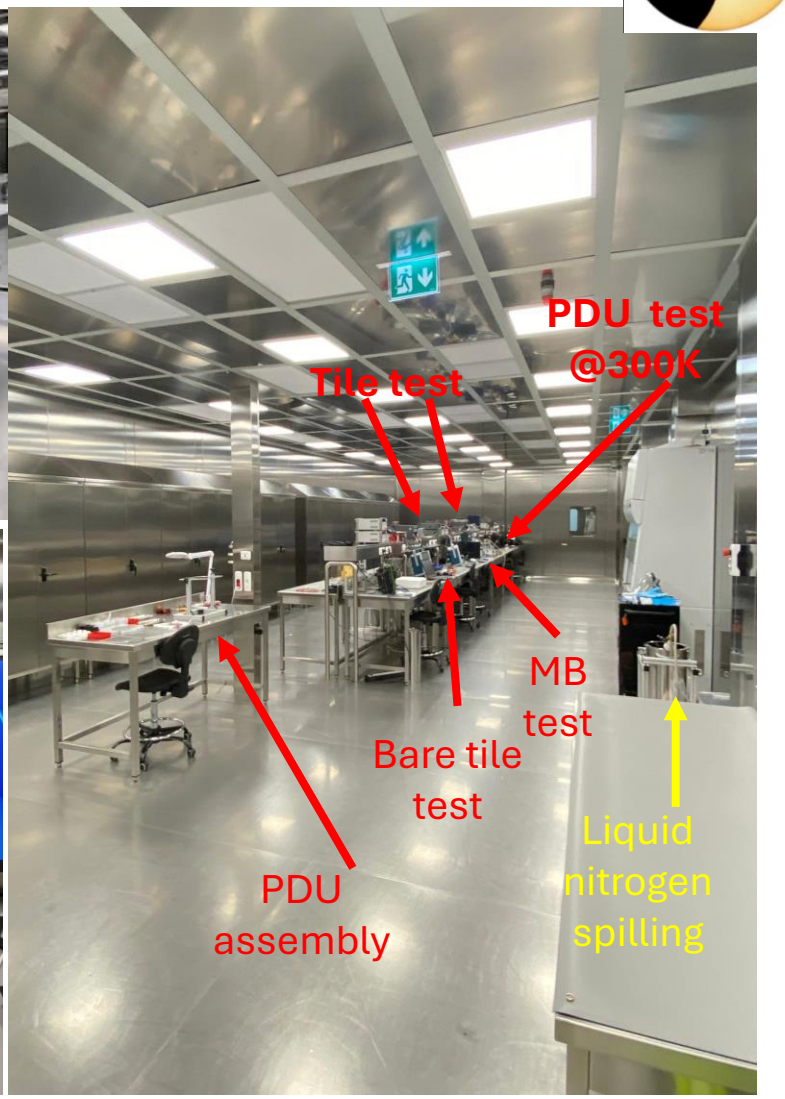
Bondhead BW01 for gold wire processes for the ball-wedge bonding method

Alignment & Bonding time: 15 min/4 tiles



# Test area

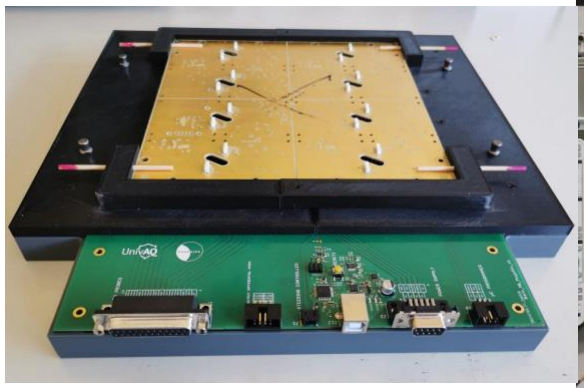


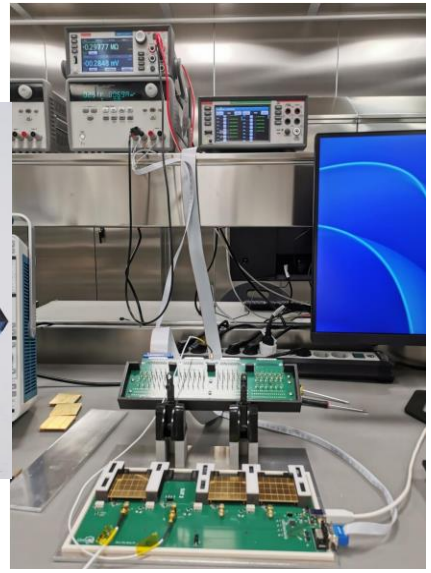




3 test set up: 4 tiles each
2 set up devoted to:

- warm test:
  electronics characterization
- cold test
  -electronics characterization
  -laser light response
- Thermalization with gaseous $N_2$ flux

Motherboard set up





Bare tile set up

1 set up for DCR measurement

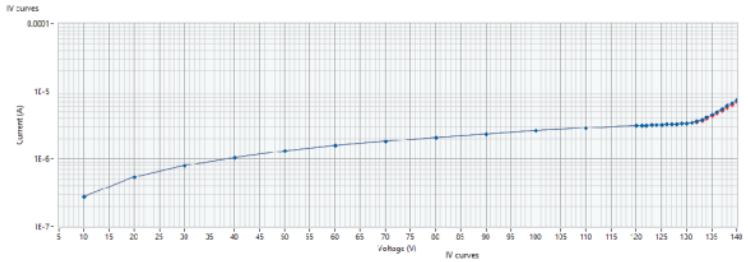
# QA/QC parameters

## IV acquisition

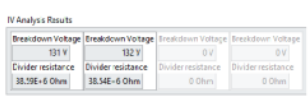
- IV and Noise measurement (warm and cold)
- Pulse counting (cold only) at [132, 136, 140, 144] V

QA-QC parameters

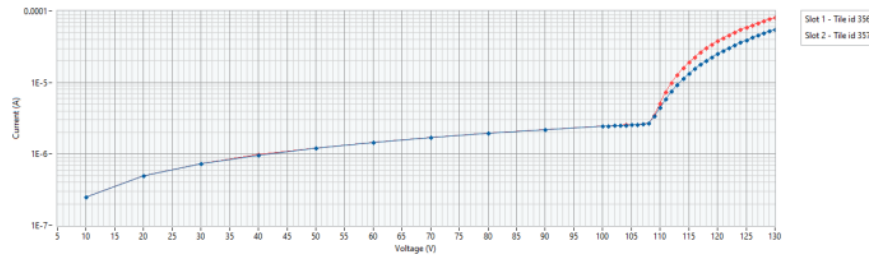
- for IV: breakdown voltage and divider resistance
- for Noise: RMS, spectrum maximum, spectrum integral, spectral shape
- for Pulses: Single PE mean (amplitude and charge) and resolution and SNR(amplitude), rise and fall times of average SPE waveform at [136, 144] V




**Warm**
Steps of 10 V up to 120 V
then steps of 1 V up to 140 V

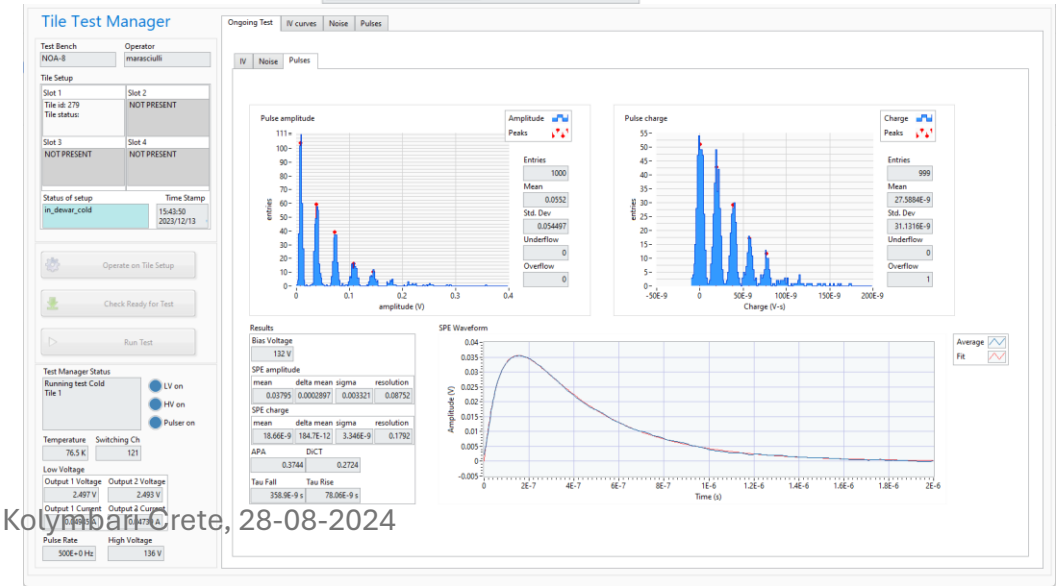



**Common**
Smaller steps and delay (1s) in ramping up.
Current measure repeated 5 times for each step, then take the median.





**Cold**
Steps of 10 V up to 100 V
then steps of 1 V up to 130 V
**The tiles are illuminated with laser**

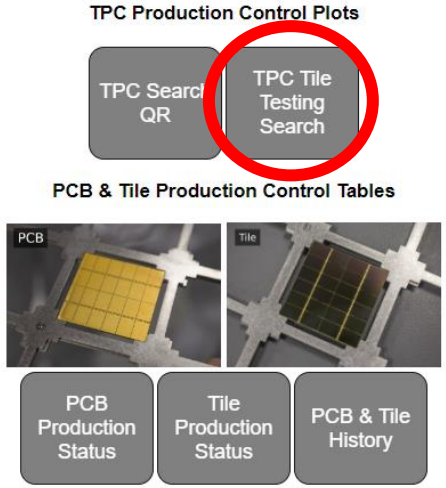


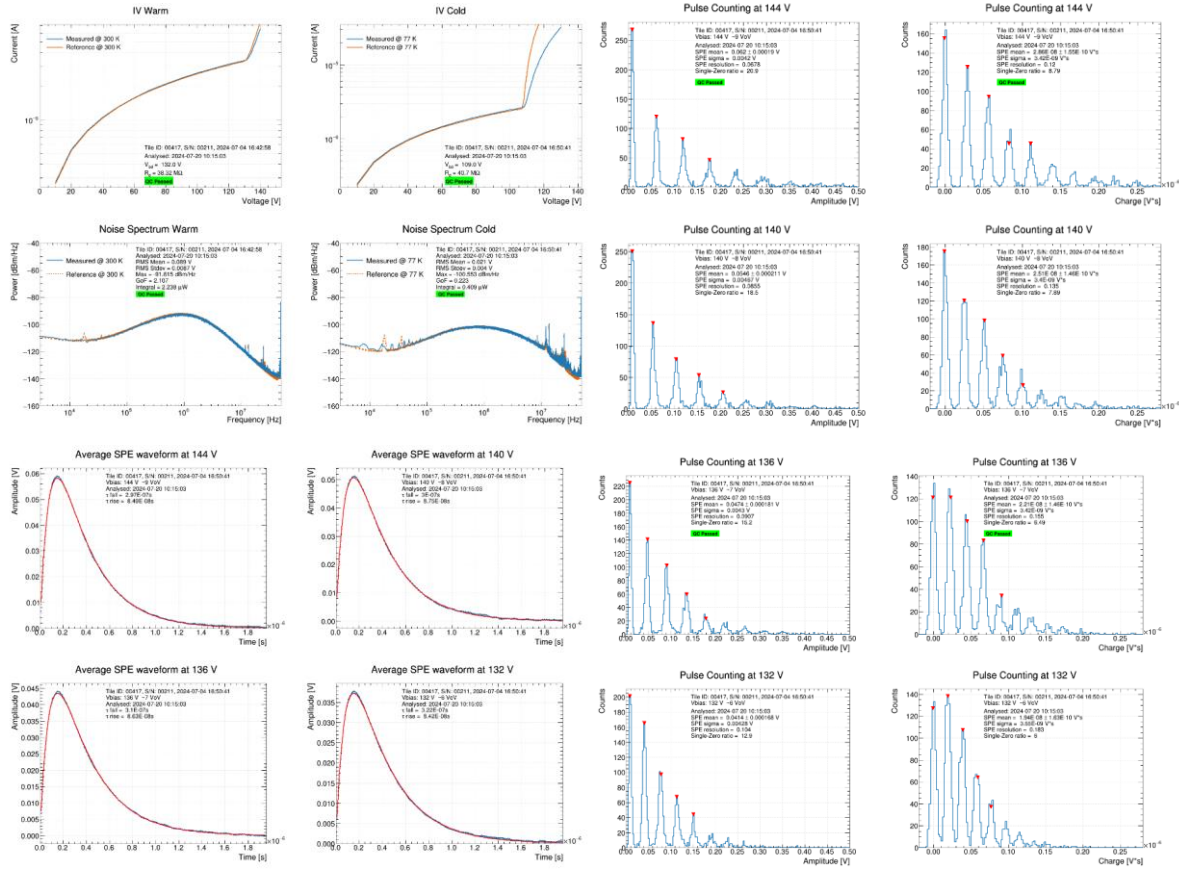
# Database

Test data are saved in the collaboration database

- tile tracking  by means of QR code
- summary tables with values of QA-QC parameters and tile classification
- webpage with the plots of a single tile test
- Work in progress to add cumulative histograms with QA-QC parameters starting from the production


**DarkSide-20K Database - TPC**



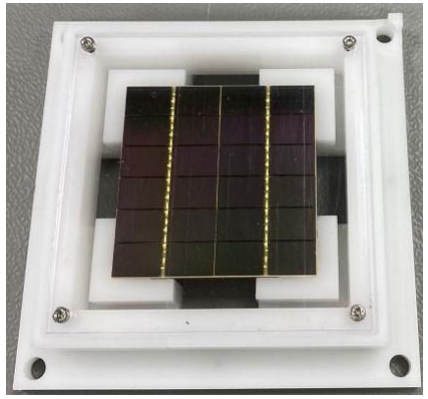



# Tile Dark Count Rate

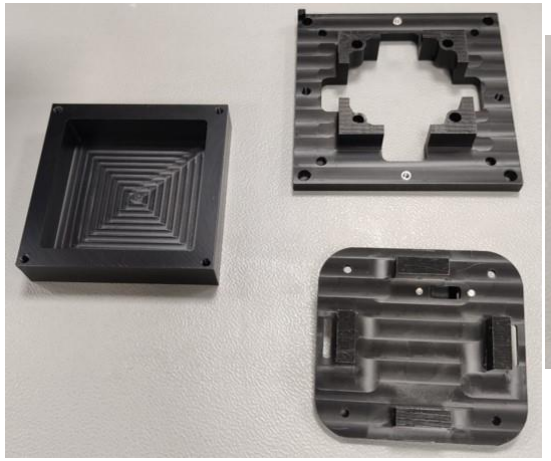
DCR measurements performed by mounting the tiles inside a custom black box in a bath of liquid nitrogen. Raw SiPM signals are acquired in a 10 μs window and analyzed to extract the DCR from the statistical distribution of delay times between consecutive signals.

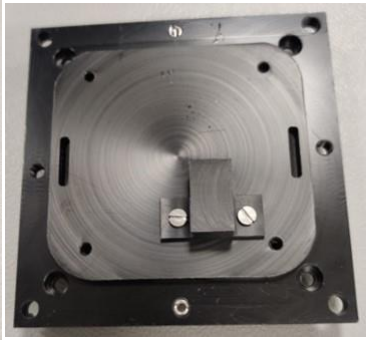
Preliminary measurements show DCR level of the order of $10^{-2}$ Hz/mm$^2$, while higher values are correlated to tiles misbehaviors or defects on the SiPM surface.

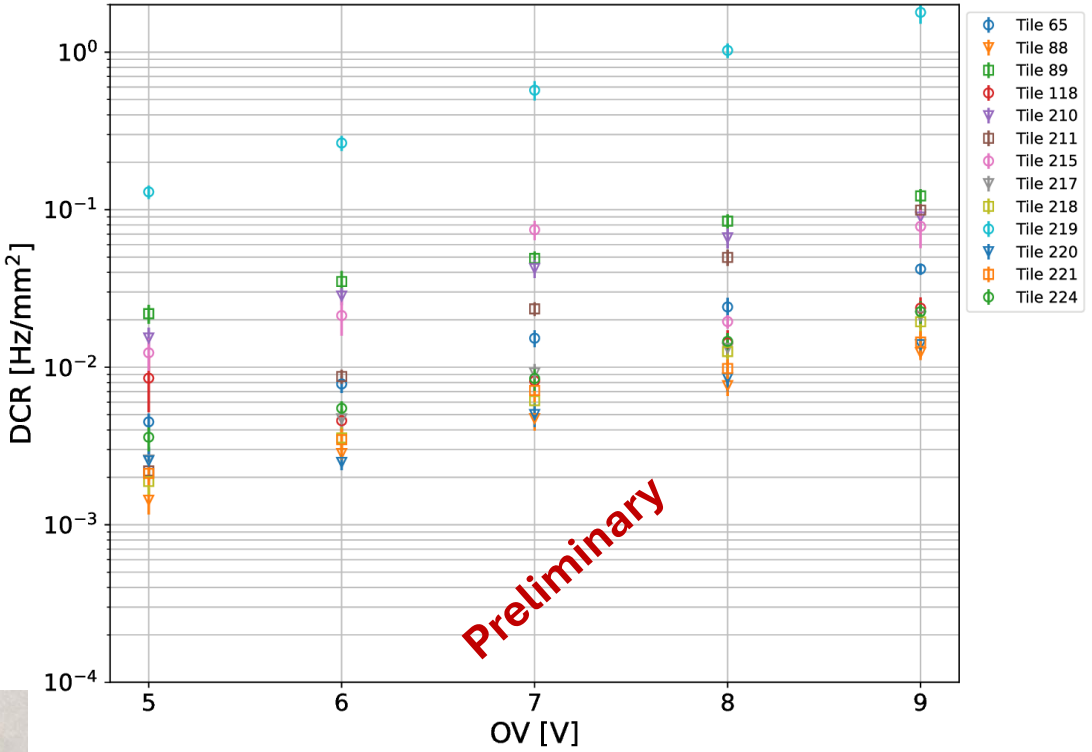
MuGS box

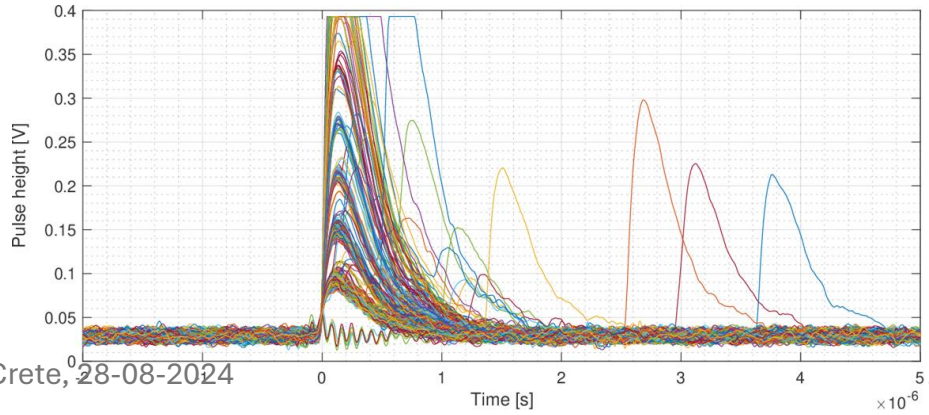


Dark MuGS box

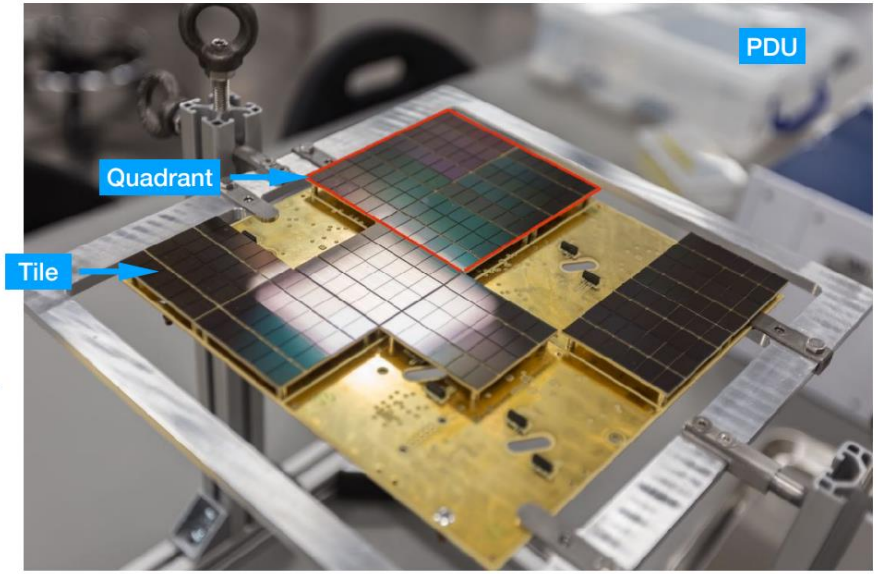


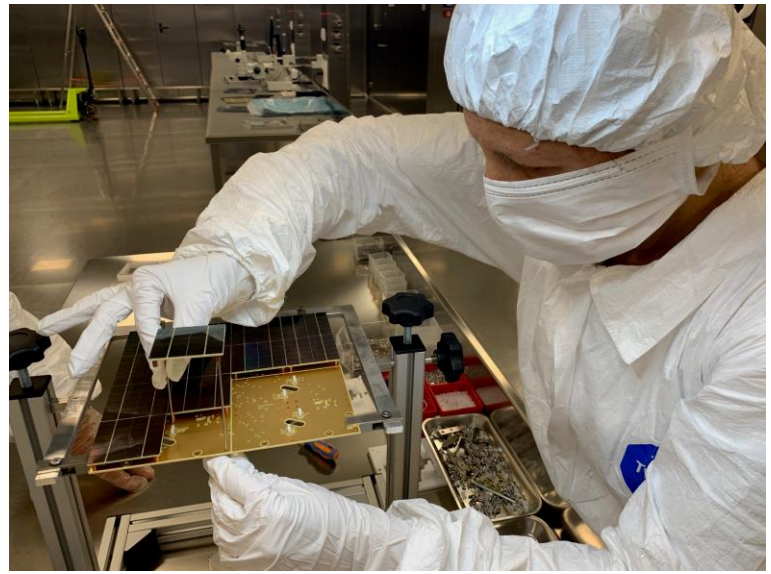




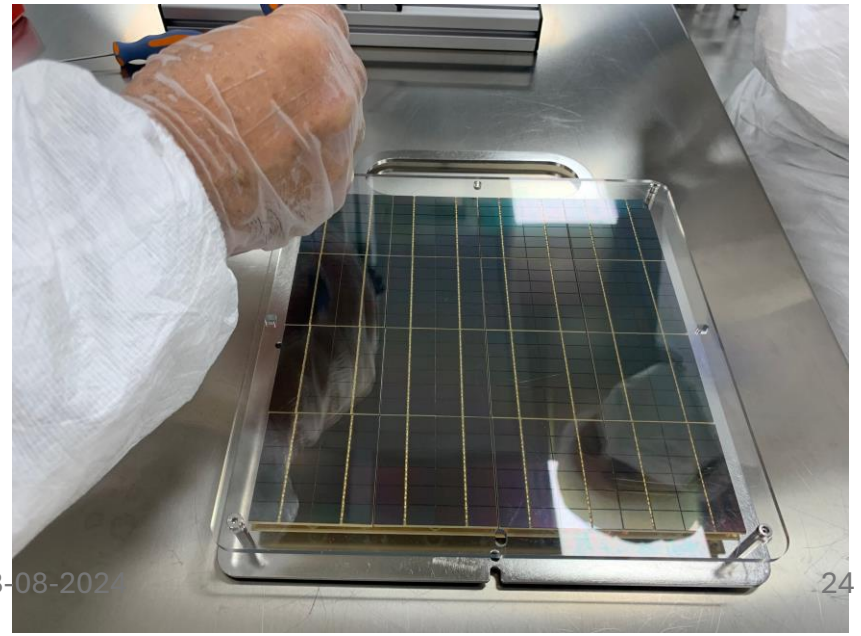



# PDU assembly



- Custom mechanical support
- threaded rods
- screwdriver with controllable torque
- custom stainless steel handhandler
- acrylic protection

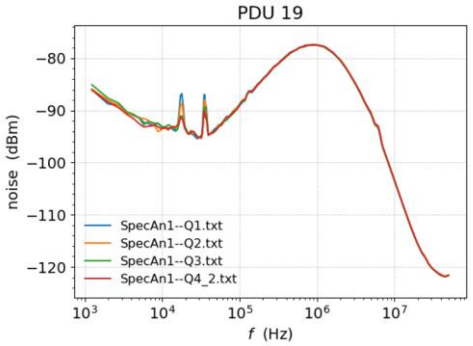


# PDU warm test

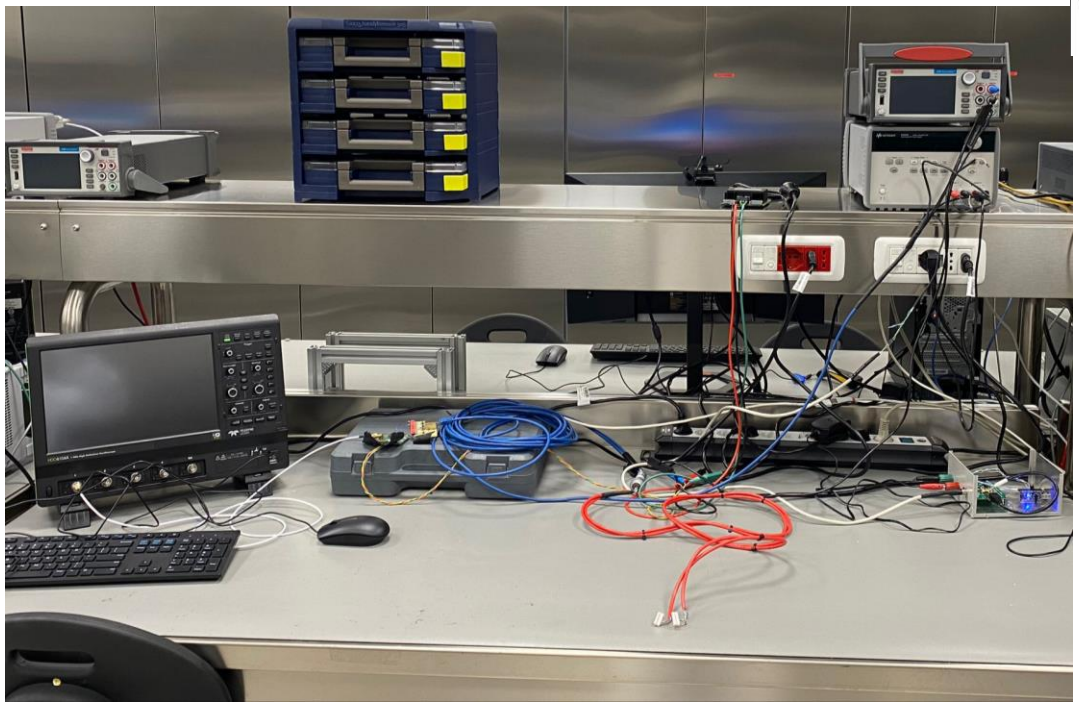
I-V curves and noise spectra of all single Tiles

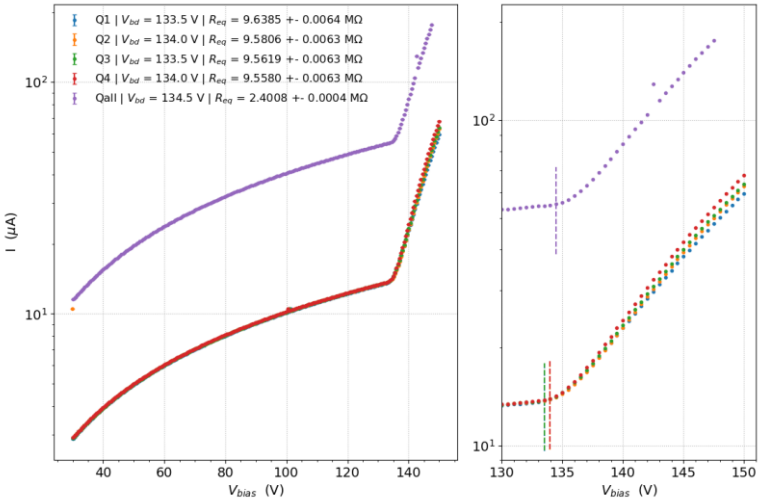
Automated with LabVIEW

Results uploaded on the collaboration database

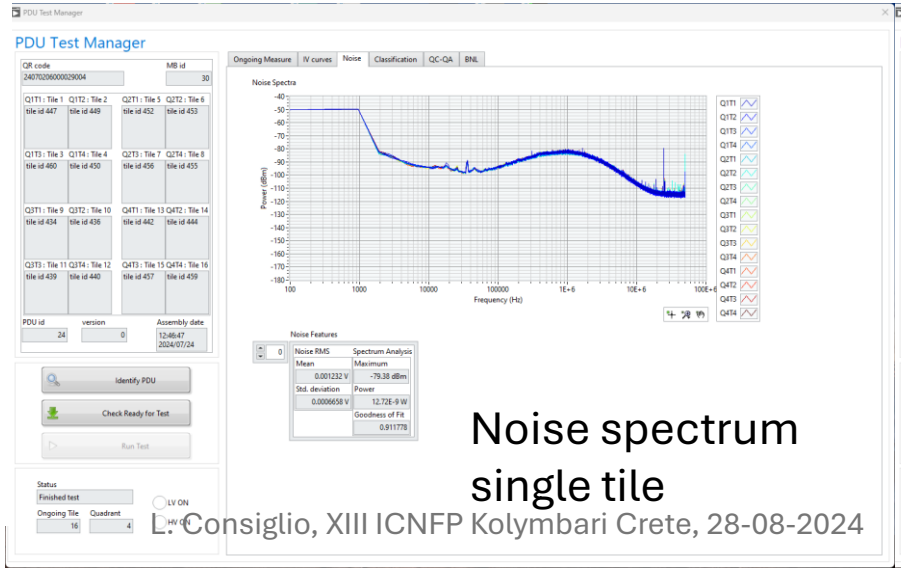



Noise spectrum - quadrant

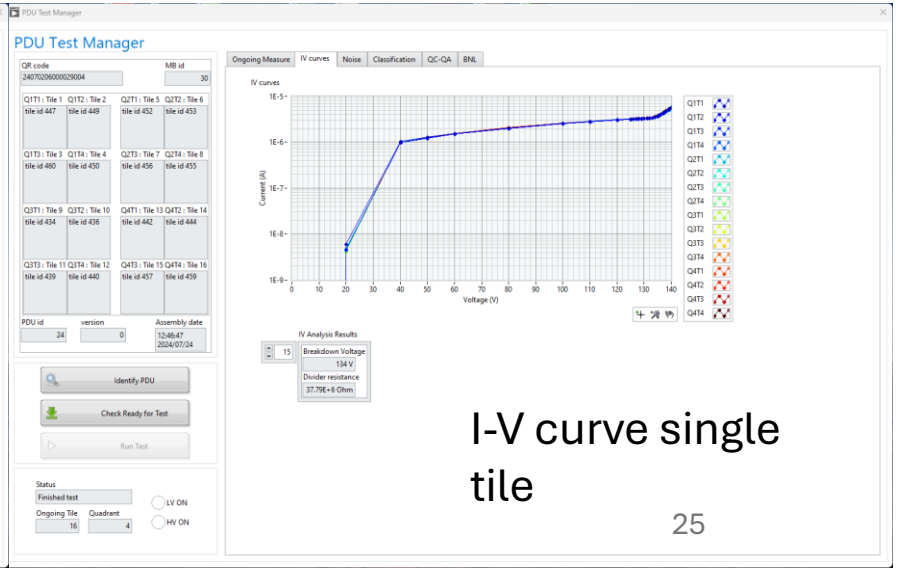





I-V curve - quadrant



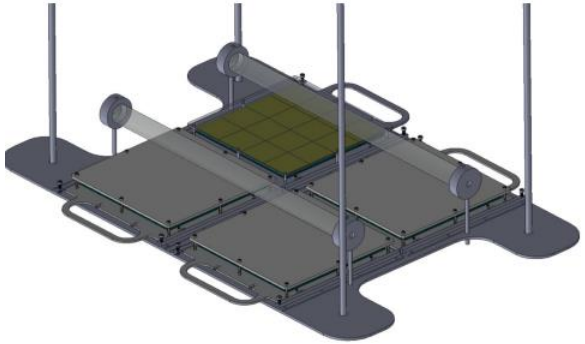

Noise spectrum single tile



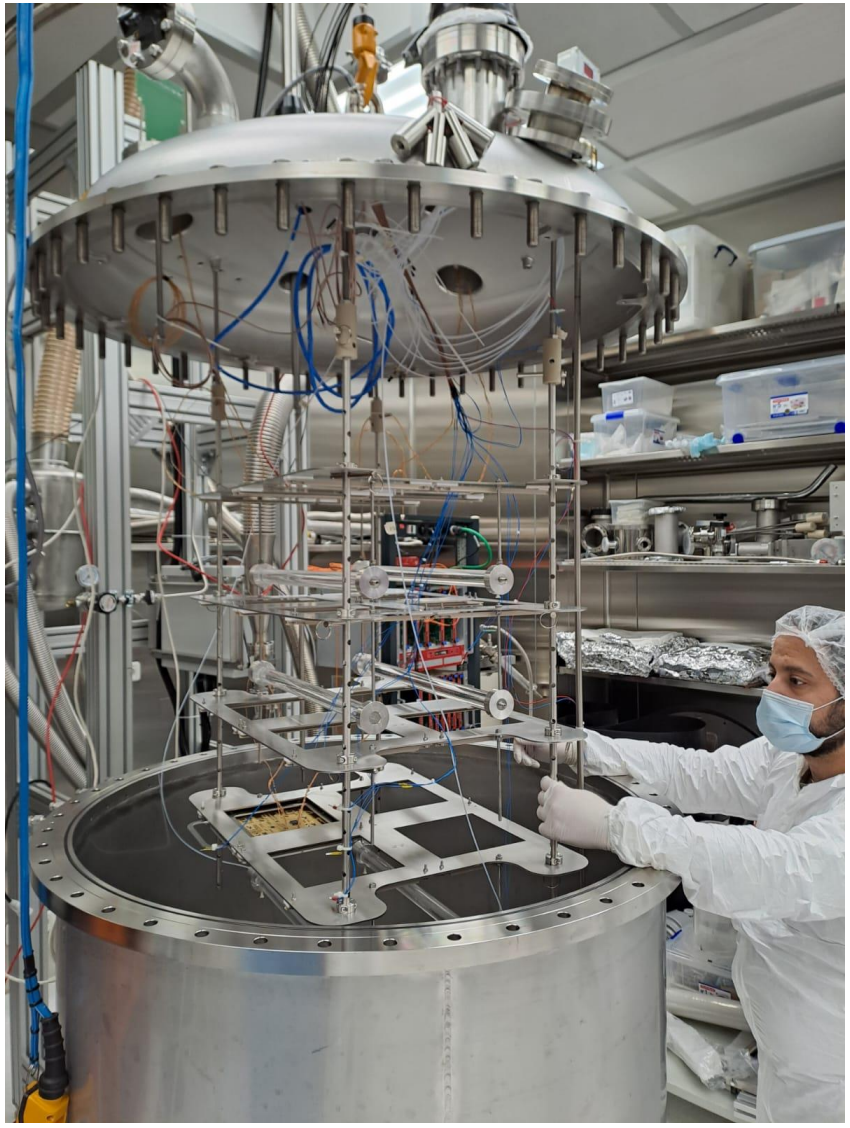

I-V curve single tile

# Napoli Test Facility

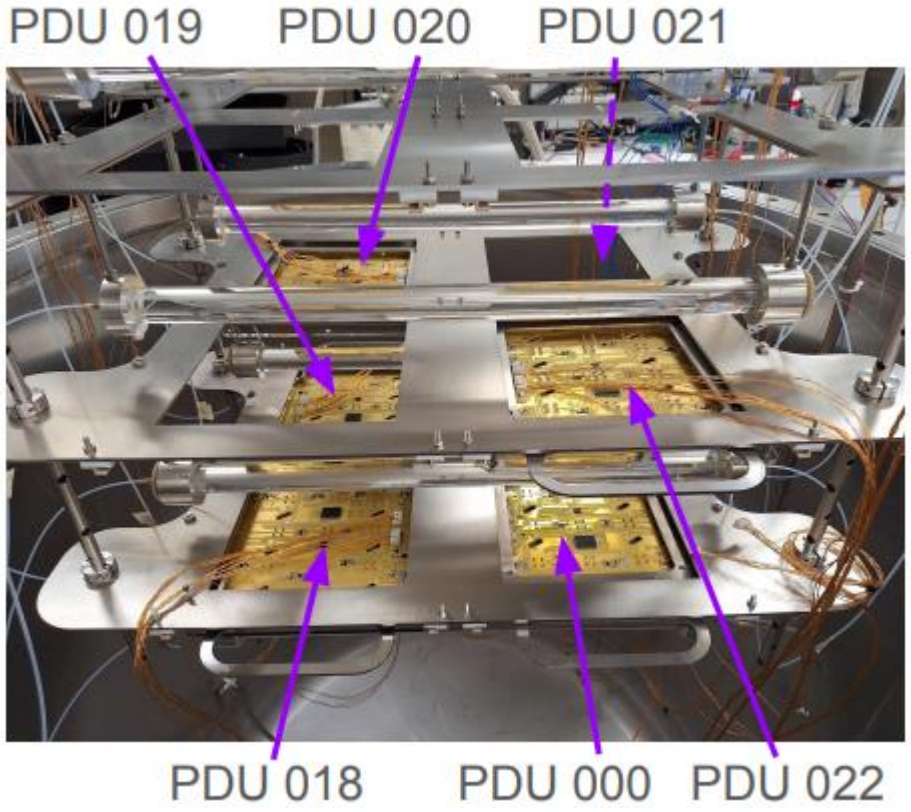
PDU characterization in liquid nitrogen in an ISO-6 clean room (50 $m^2$)



Mechanical structure composed 4 levels each hosting 4 PDUs. Full integration with light distribution system.



- First 6 pilot pre-production PDU tested at NTF
- 3 new pre-production PDUs shipped to be tested



# Outlooks

- DarkSide-20k cryostat construction in Hall C to be completed by 2024
- NOA  packaging and test machines with the tile characterization set up and PDU warm test  fully operational
- Process set up, qualification and training on the machines completed
- Silicon wafers characterization campaign in progress -> 66% tested -> completion by spring 2025
- Pre-production of 10 PDUs almost completed (by Aug 2024)
- PDU production will start in Sept 2024 with the first 10% TPC tiles production & test + PDU assembly in NOA and is expected to be completed by fall 2025.

# THANKS FOR ATTENTION