The Next Upgrade of the ALICE Inner Tracking System: ITS3

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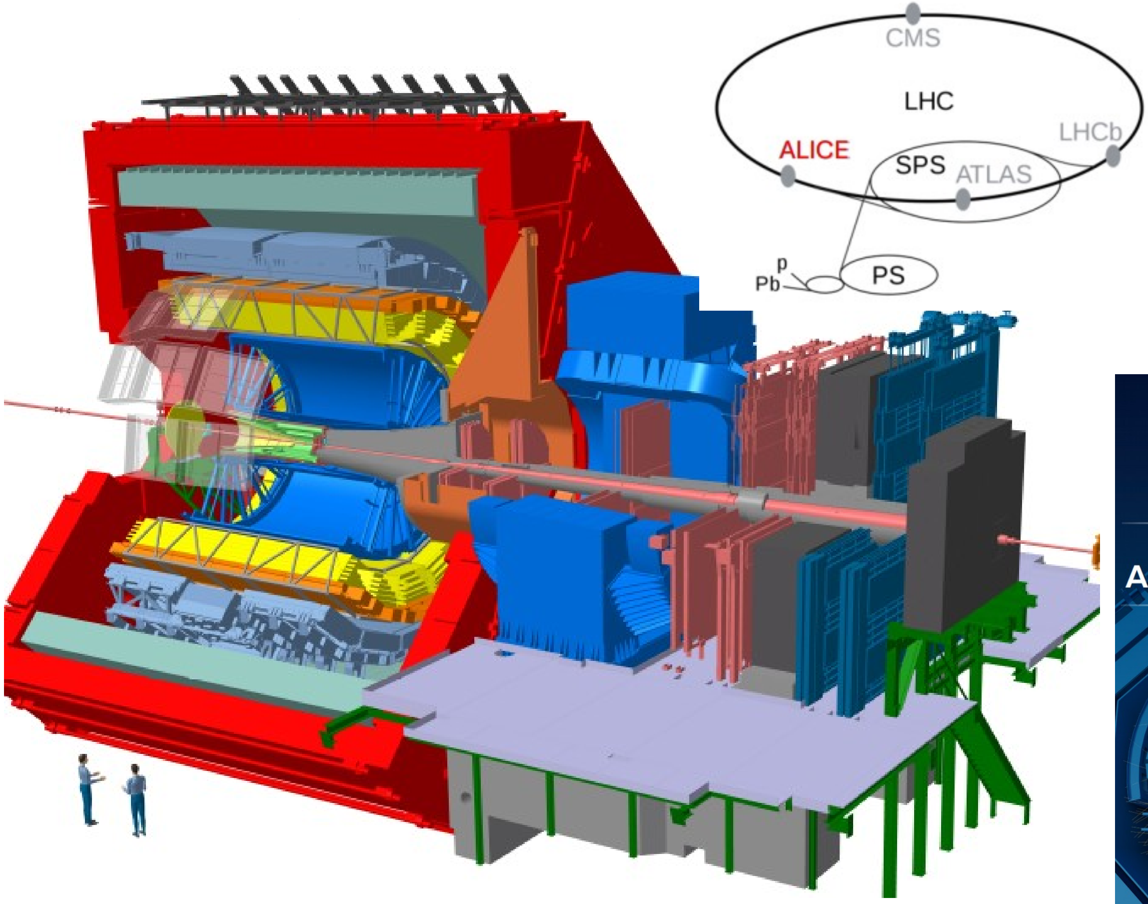
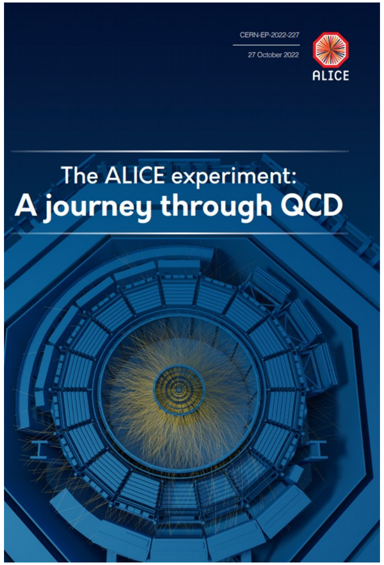
Università degli Studi di Bari & INFN Bari

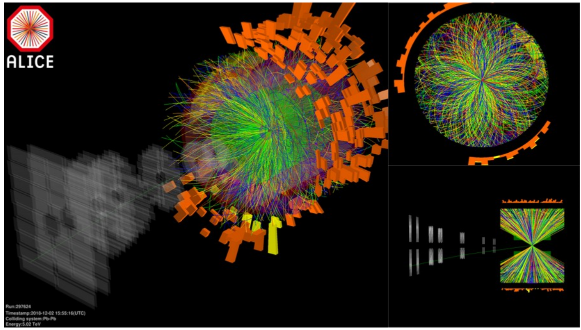
The ALICE experiment



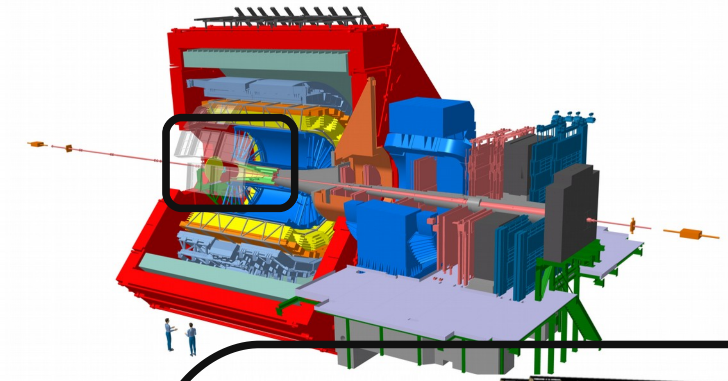
- **Main goal of the ALICE Physics program:** study the properties and the evolution of a heavy ion collision, with a particular attention to the **Quark-gluon plasma (QGP)** state: *deconfined state of strongly-interacting QCD matter*
- Review paper (ALICE highlights in Run 1 & 2)

  DOI: 10.1140/epjc/s10052-024-12935-y



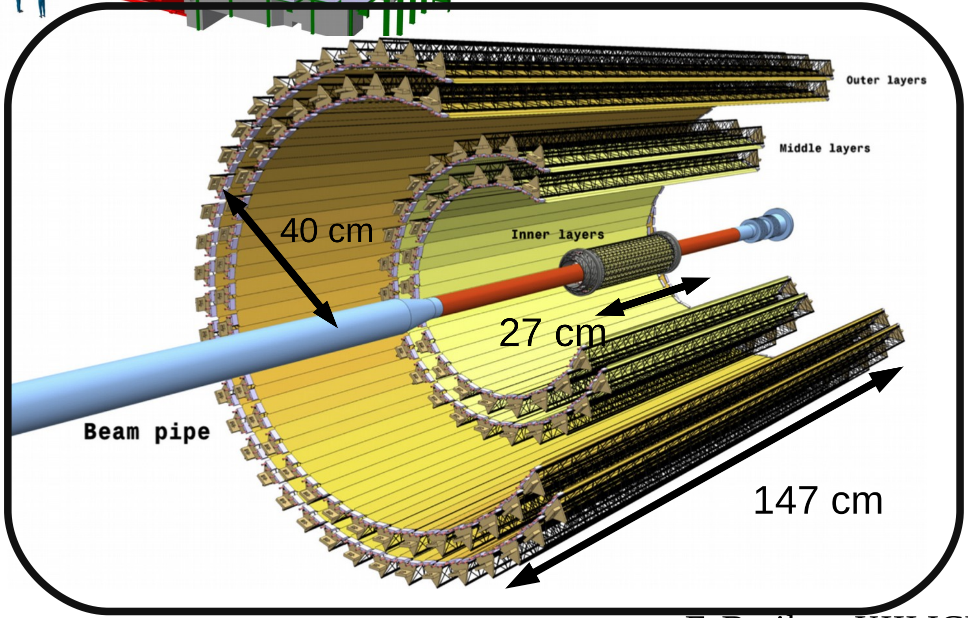


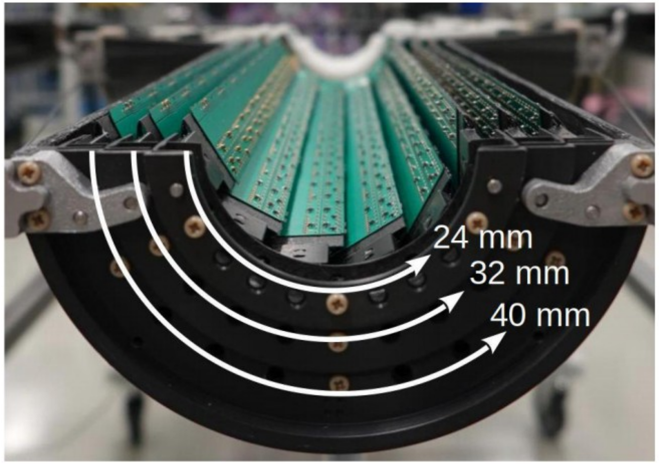
ALICE Inner Tracking System 2: ITS2



Current innermost tracker:

- Inner Tracking System (ITS) based on Monolithic Active Pixel Sensor ALPIDE
- Installed during Mar-May ‘21 (LHC LS2)
- 7 layers
  - 3 Inner Barrel (IB)
  - 4 Outer Barrel (OB)
- ~ 10 m² active silicon area (> 20k MAPS), 12.5 Gpixel
  - Layer 0 ~ 24 mm from interaction point
    - Inner barrel: X/X0 ~ 0.35%



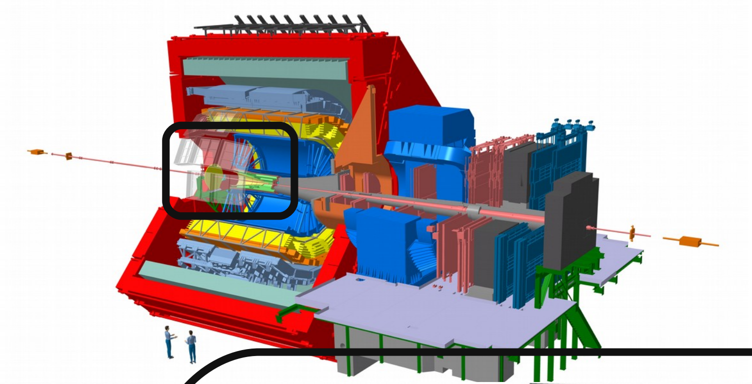


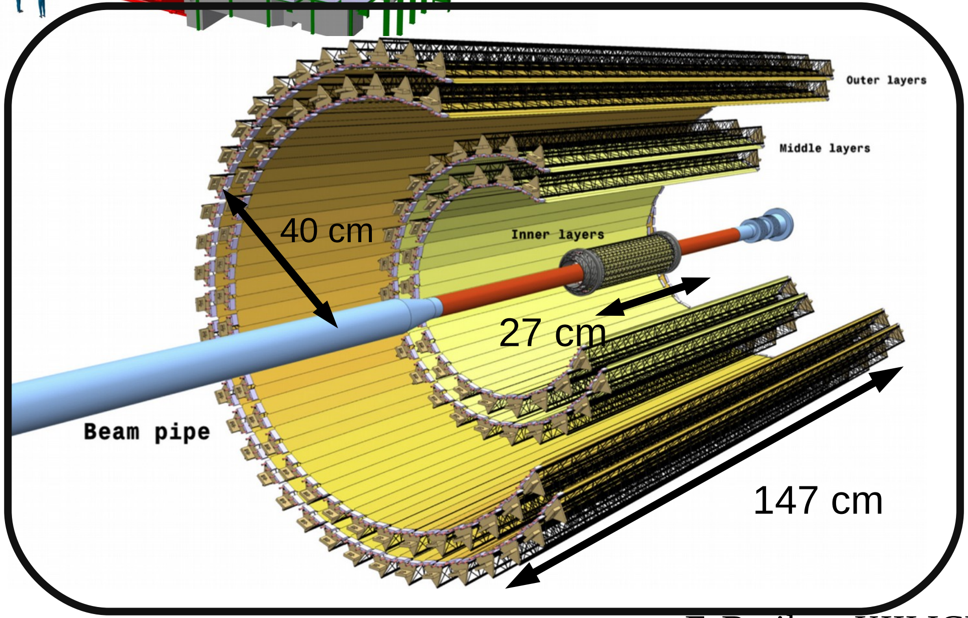
ITS2: assembled three inner-most half-layers

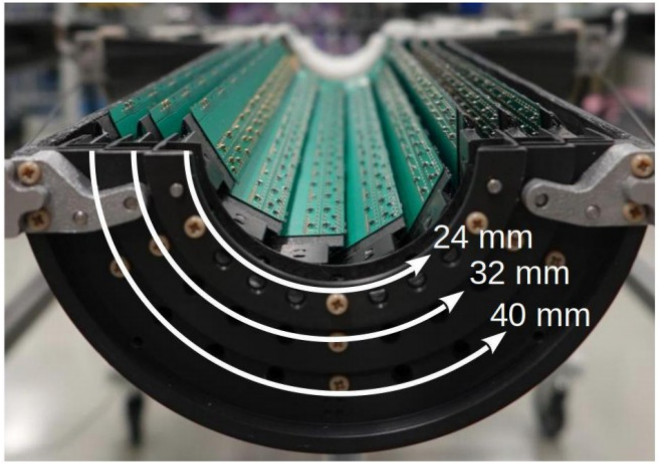
doi:10.1088/0954-3899/41/8/087002

ALICE Inner Tracking System 2: ITS2

Can we reduce the material budget further?





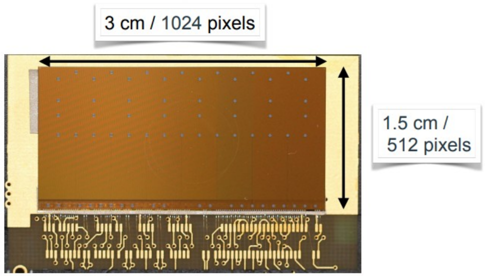


ITS2: assembled three inner-most half-layers

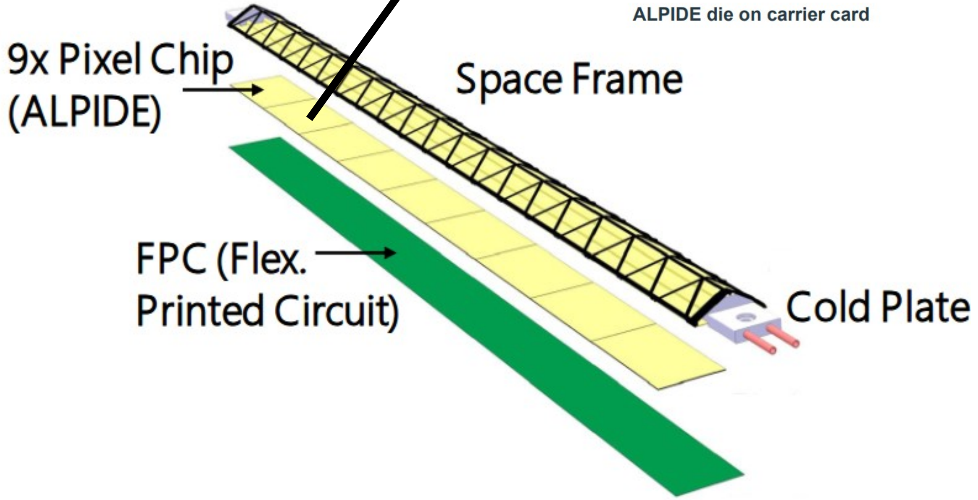
ITS2 inner barrel: material budget

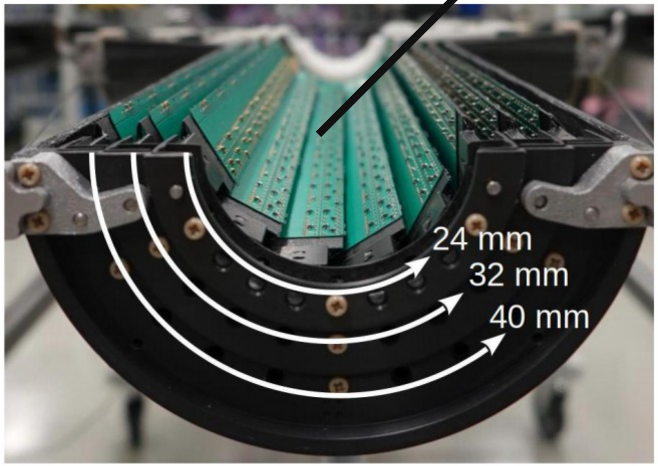
ITS2 Inner Barrel Stave

Nine pixel sensors on a **polyimide flexible printed circuit (FPC)** + carbon fibre support structure (**Space Frame**) + water cooling circuit (**Cold Plate**).



ALPIDE die on carrier card

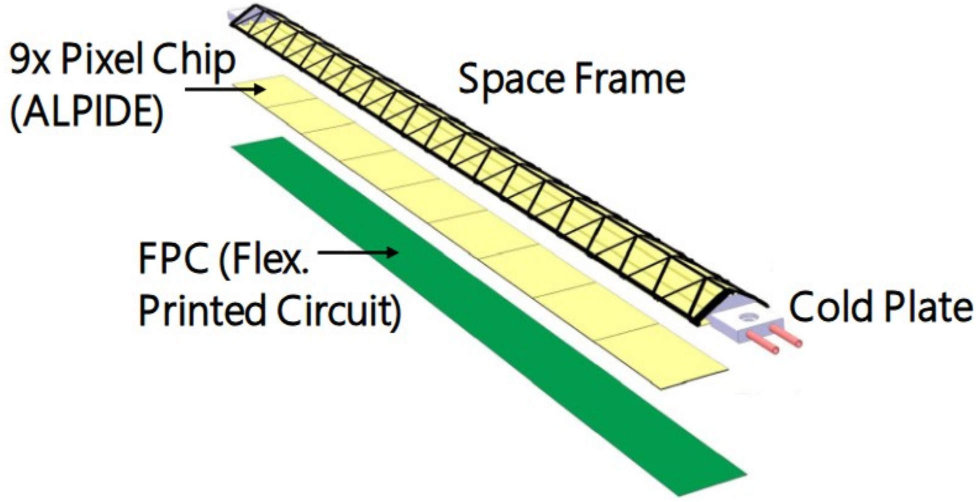




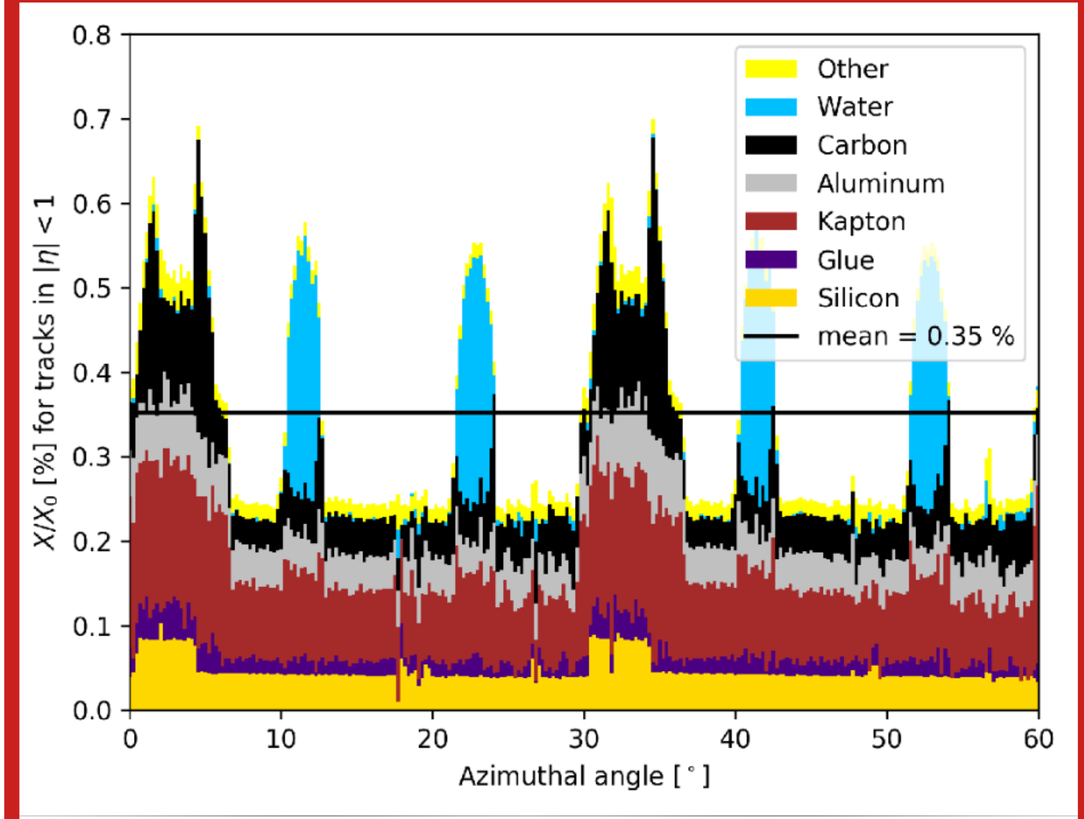
ITS2: assembled three inner-most half-layers

ITS2 inner barrel: material budget

- **Observations:**
  - Silicon: 1/7th of total material
  - Irregularities due to support/cooling and overlapping staves



CERN-LHCC-2019-018 / LHCC-I-034 01/12/2019

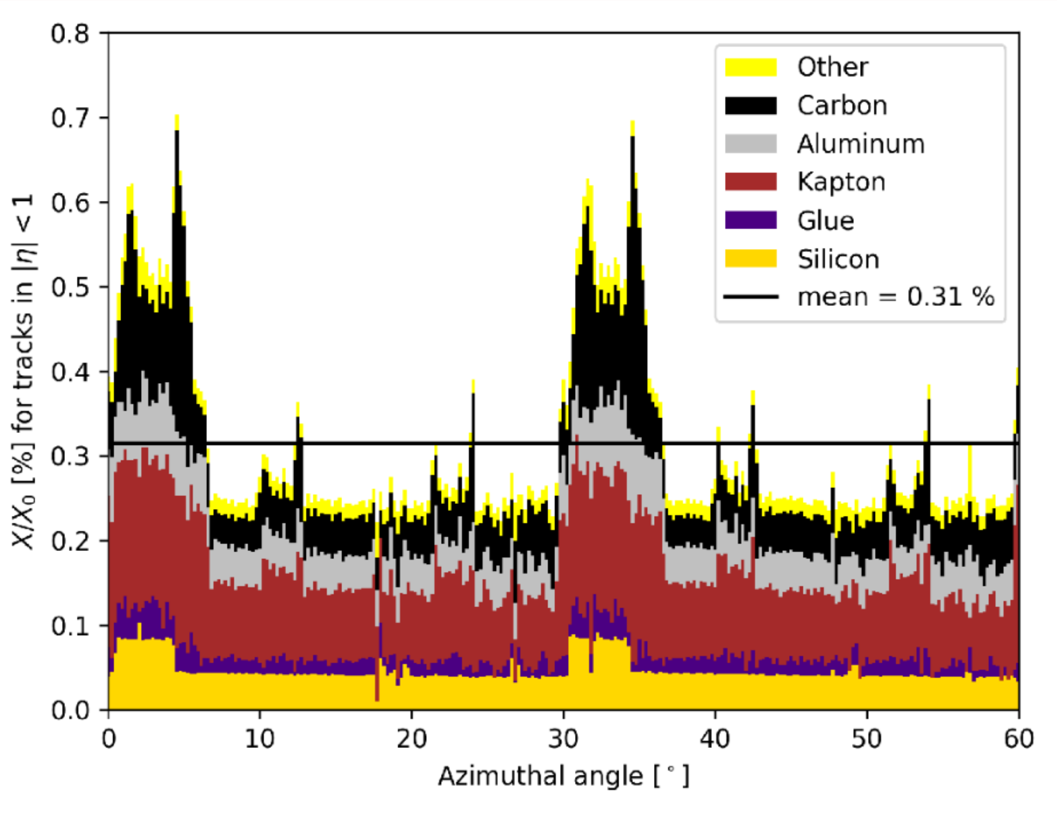


The azimuthal distribution of the material of ITS2 Layer 0 traversed by particles with |η| < 1. The angular interval in the figure corresponds to two staves;

ITS2 inner barrel: material budget

CERN-LHCC-2019-018 / LHCC-I-034 01/12/2019

- **Observations:**
  - Silicon: 1/7th of total material
  - Irregularities due to support/cooling and overlapping staves
- ***Removal of water cooling:***
  - possible if power consumption stays below 40 mW/cm^2



ITS2 inner barrel: material budget

CERN-LHCC-2019-018 / LHCC-I-034 01/12/2019

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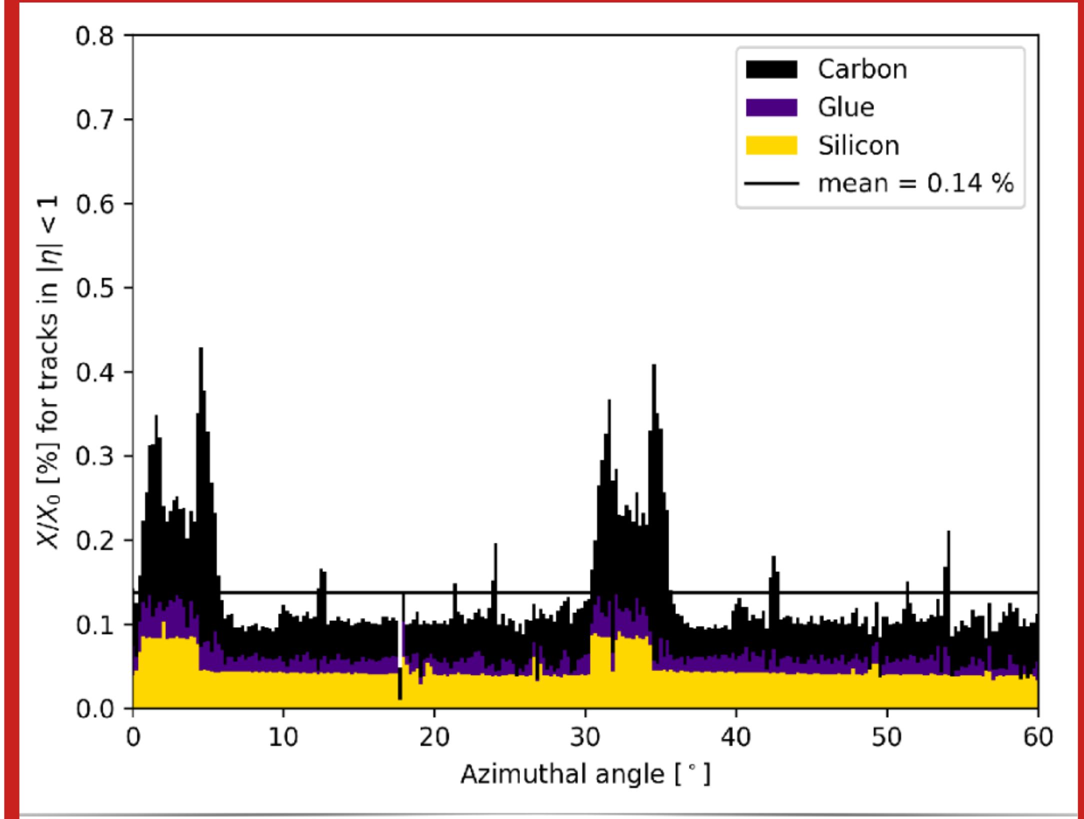

ITS2 inner barrel: material budget

CERN-LHCC-2019-018 / LHCC-I-034 01/12/2019

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- ***Removal of water cooling:***
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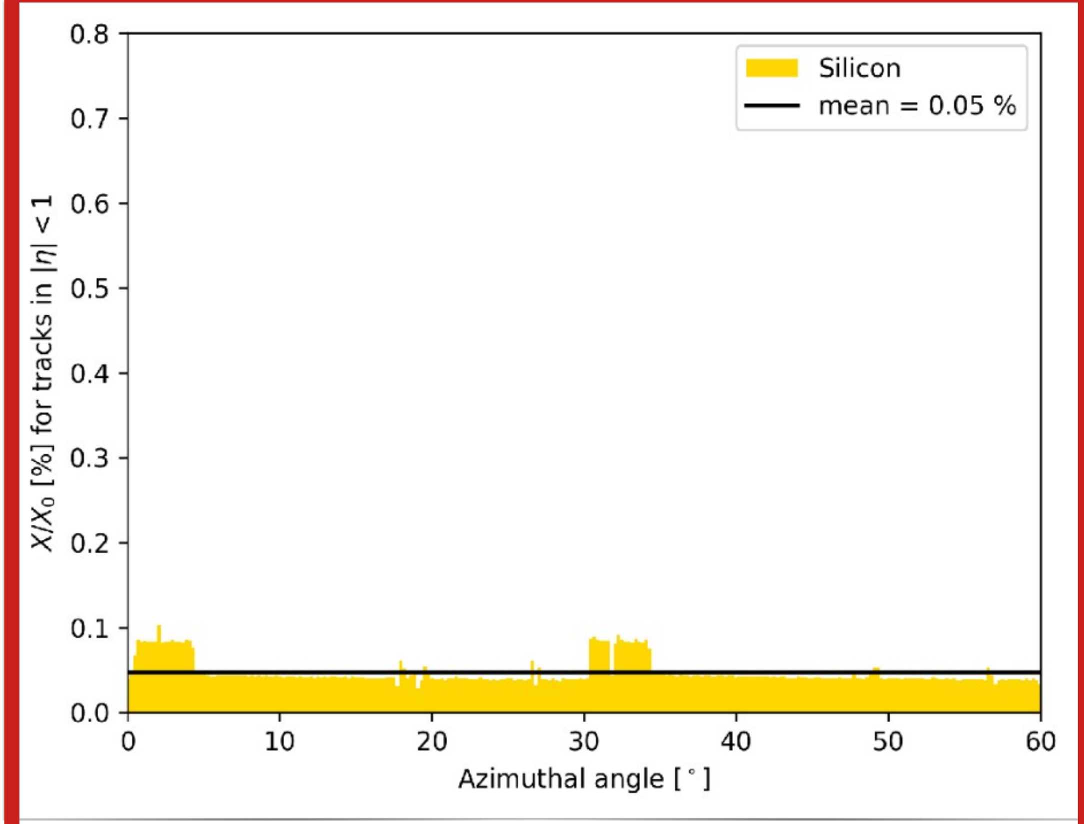
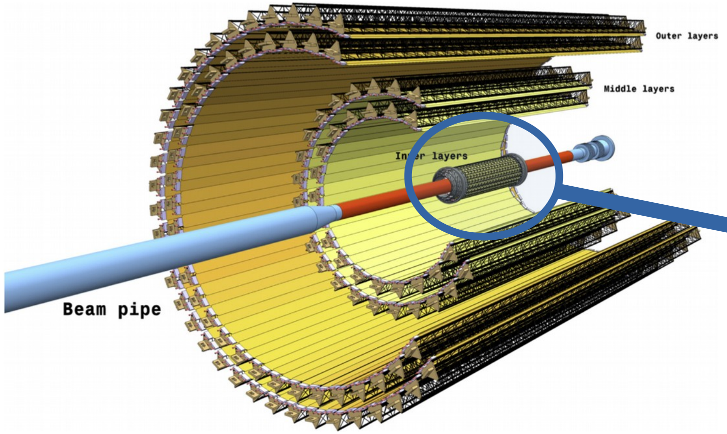
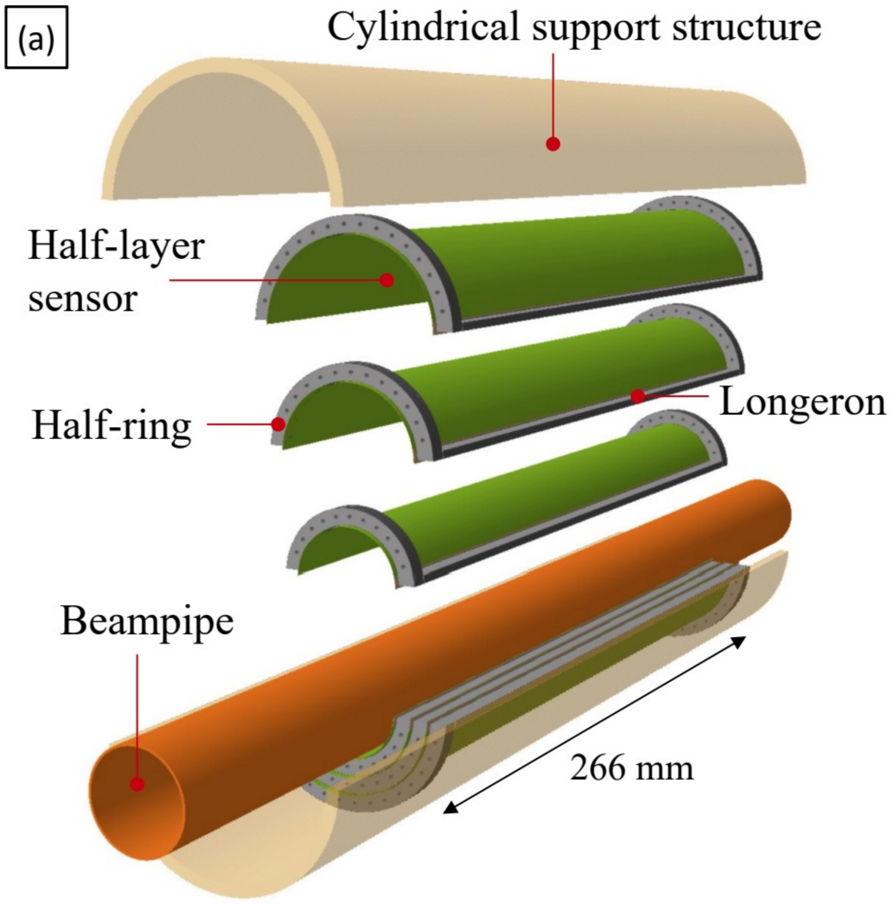
- ***Removal of the circuit board (power + data)***
  - possible if integrated on chip
- ***Removal of mechanical support***
  - benefit from increased <u>stiffness</u> by rolling Si wafers



ITS3 layout

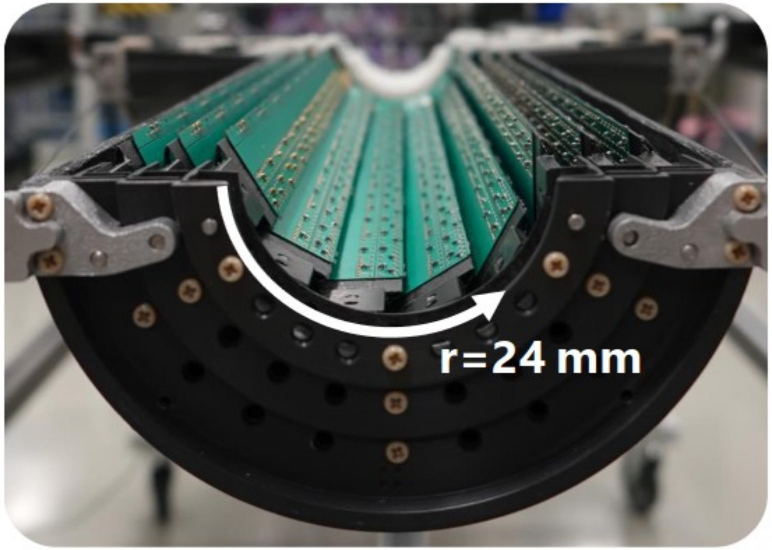


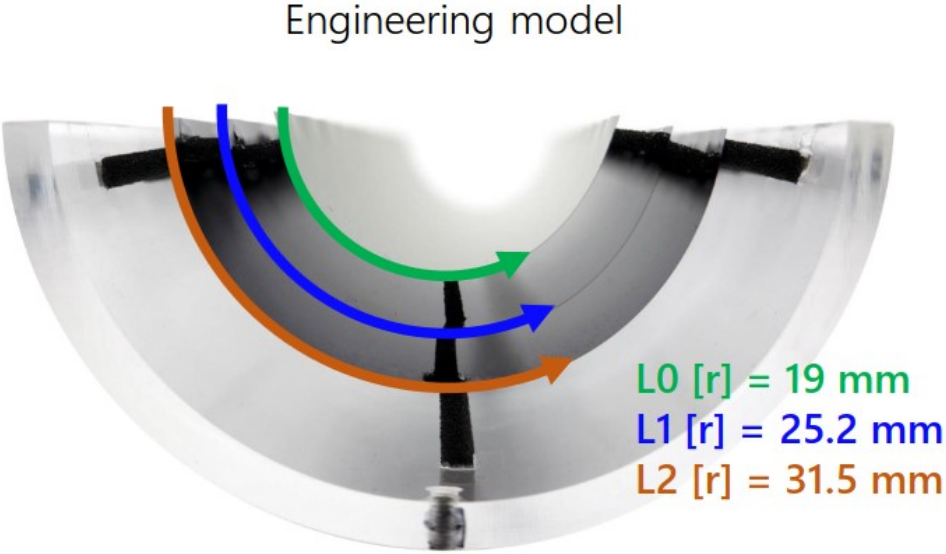


- Replacement of the ITS2 Inner Barrel with 3 layers of **bent** wafer-scale sensor ASIC
  - Three concentric cylindrical layers that are split into an upper and a lower half
  - Each such half-layer is made of one single piece of silicon

ITS3 – benefits

- Closer to interaction point:
  - innermost layer radius from 24 mm to 19 mm (thanks to the new beam pipe radius: 18 mm → 16.2 mm)
- Reduction of material budget per layer → from 0.35% X/X0 to 0.07% X/X0
- Homogeneous material distribution

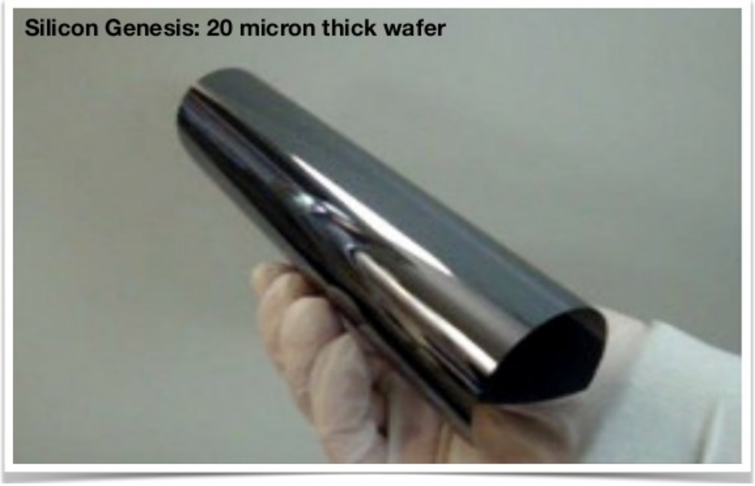


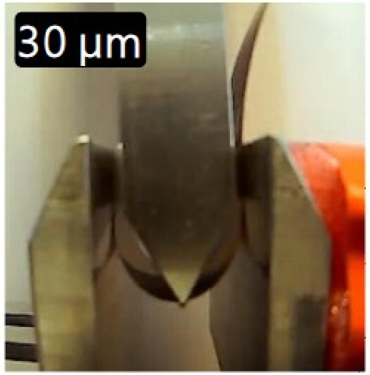


ITS3 requirements and R&D

- **MAPS in 65 nm technology** (TPSCo* CMOS)
- 300 mm wafer-scale chips, fabricated using **stitching****
- **Bending of silicon,** thinned to < 50 µm → flexible (bent to target radii)
- Air cooling and ultra-light mechanical supports (carbon foam)

CERN-LHCC-2024-003/ALICE-TDR-021
https://cds.cern.ch/record/2890181/files/ALICE-TDR-021.pdf





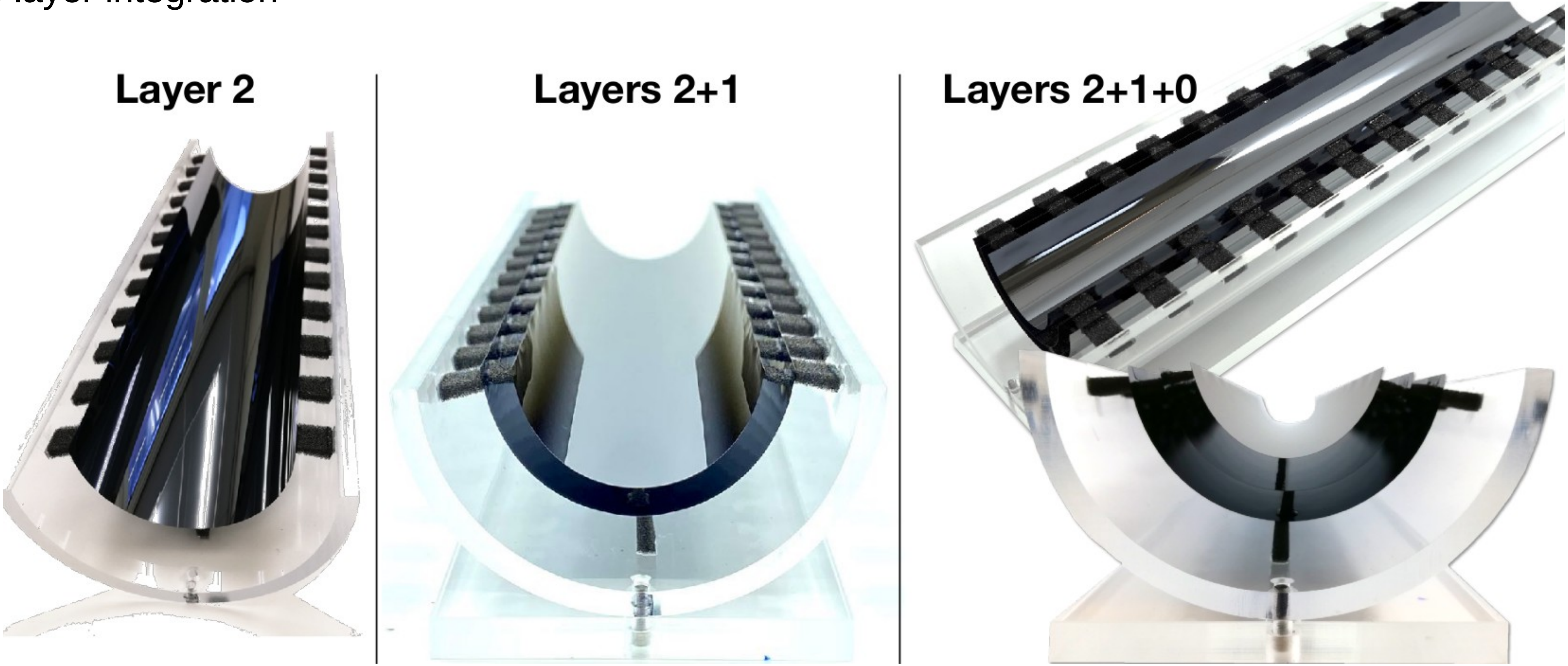
ALPIDEs (180 nm) bent to ITS3 target radii

* Tower Partners Semiconductor Company

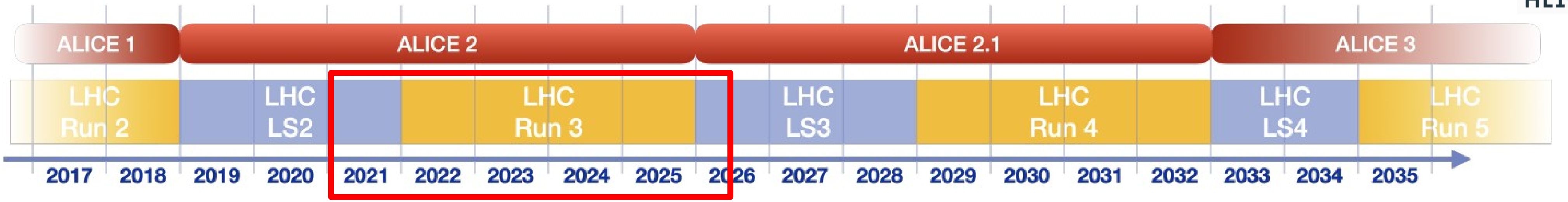
**** Stitching technique:** *Tower Semiconductor Ltd. Stitching design rules for forming interconnect layers, US Patent 6225013B1. 2001.* Stitching allows the connection of otherwise unconnected reticles on a wafer already at wafer production stage.

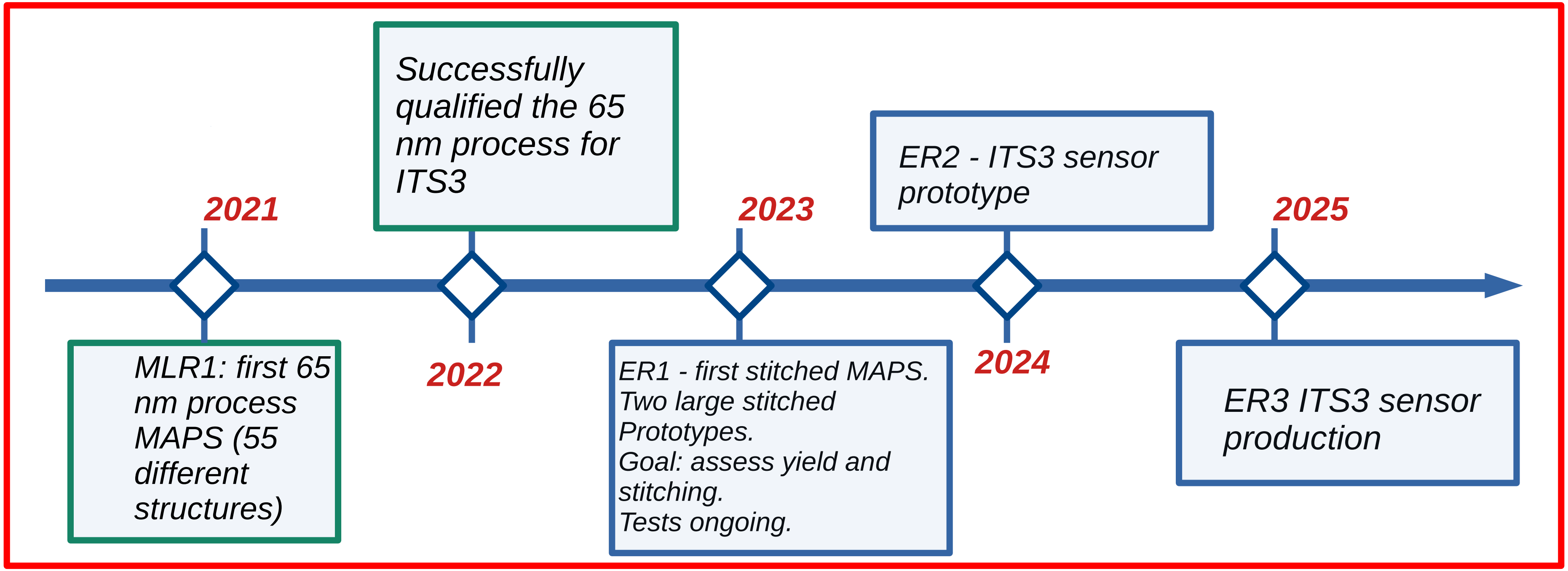
ITS3: layer assembly

3 layer integration



The ITS3 roadmap

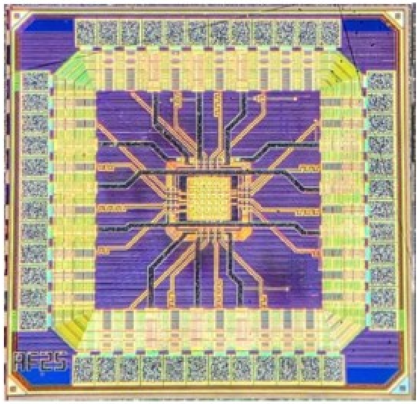


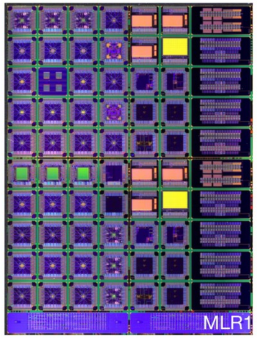


MLR1: 65 nm technology qualification

Goals: Learn technology features / Characterize charge collection / Validate radiation hardness

1.5 mm

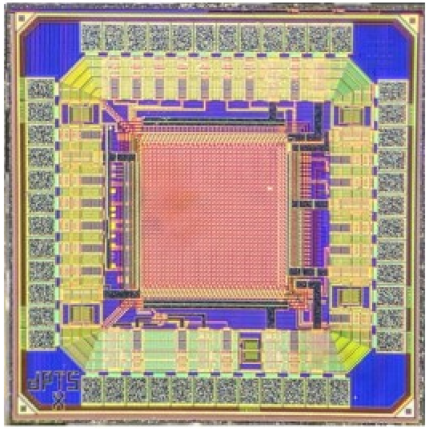




Analogue Pixel Test Structure (APTS)

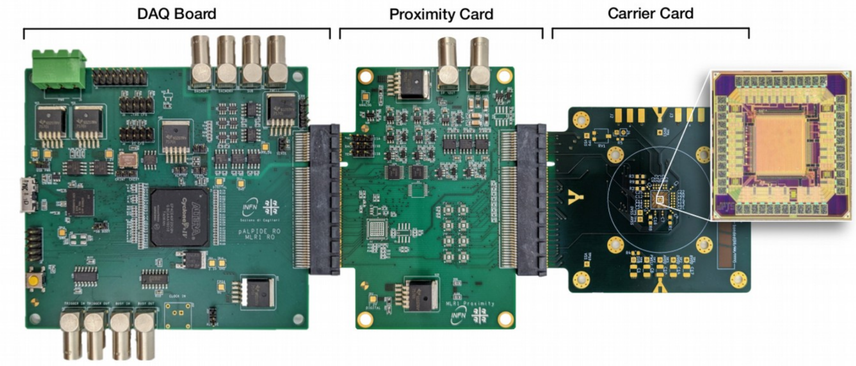
- Matrix: 6x6 pixels
- Direct analog readout of central 4x4
- OpAmp buffer for enhanced time resolution
- SF buffer for stable readout
- Pixel pitch: 10, 15, 20, 25 µm

1.5 mm



Digital Pixel Test Structure

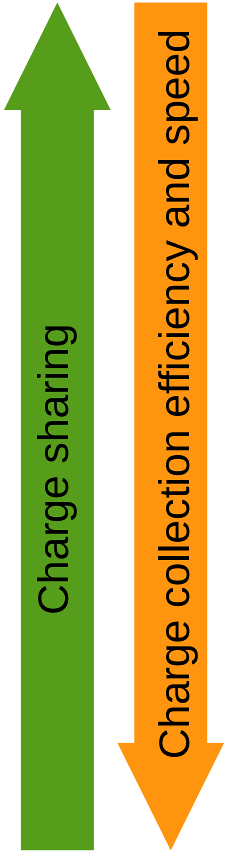
- Matrix 32x32 pixels
- Digital readout
- Pixel pitch: 15 µm

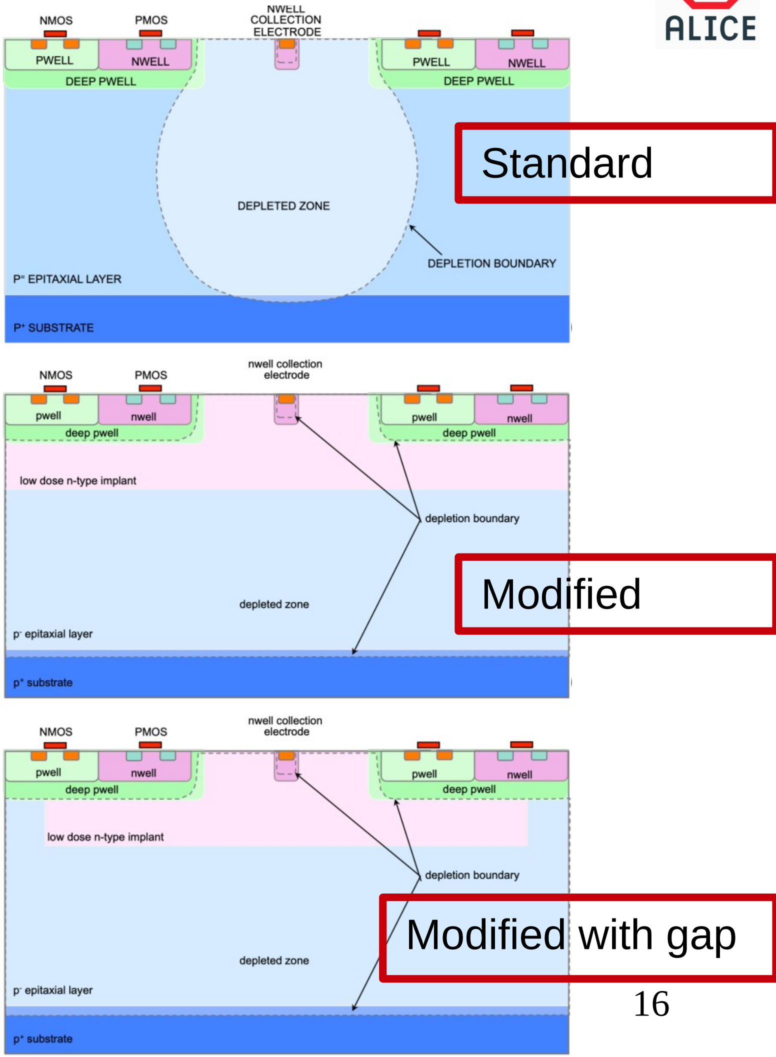


Intensive qualification strategy: validation in terms of charge collection efficiency, detection efficiency and radiation hardness

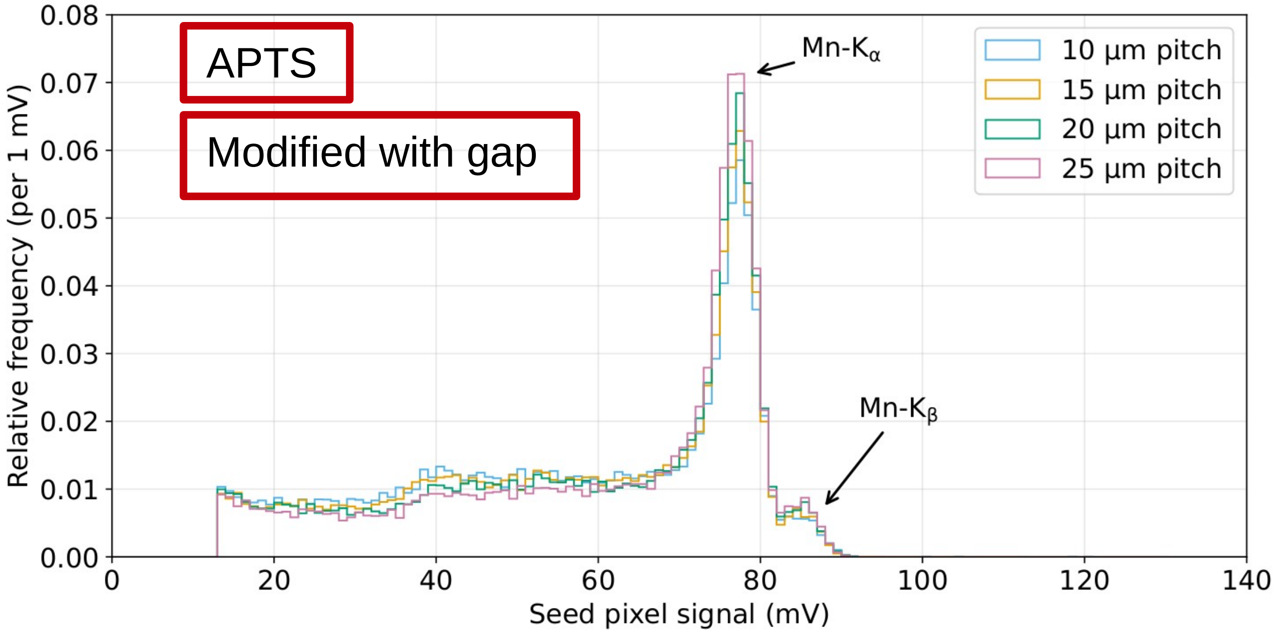
Developments: process modification

- Based on MAPS and TPSCo 65 nm CMOS technology, 50 µm thick
- Three different chip designs for characterization and qualification purposes:
  - **Standard type** (similar in ALPIDE)
  - **Modified type**
  - **Modified type with gap**





65nm technology – ^{55}Fe source response



Seed pixel (pixel with the highest signal in an event)

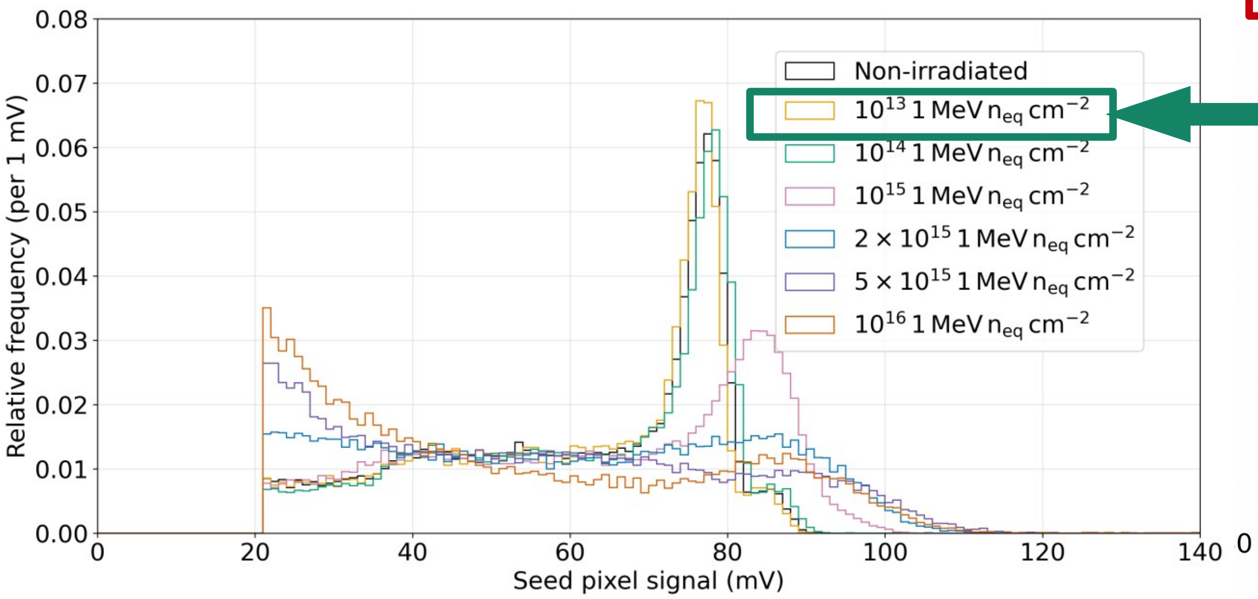
Seed pixel signal spectra measured with APTS sensors at V_{sub} = − 1.2 V ^{55}Fe emitted X-rays (5.9 and 6.5 keV photons)

Comparison of pitches for APTS with process modification:

- Pixels of different pitches show similar results → indication of very efficient charge collection
- Allows to choose optimal pitch for the final sensor

Radiation hardness

APTS

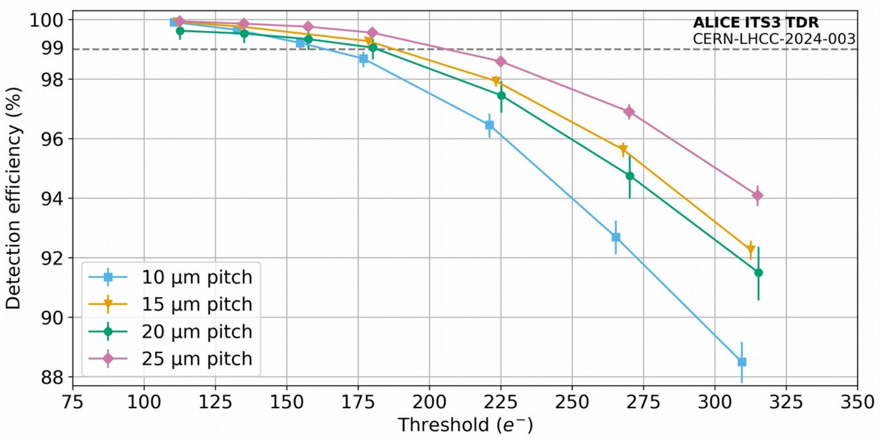


Seed pixel signal spectrum (^{55}Fe), 15 µm pixel pitch, modified with gap type, APTS sensor irradiated to different non-ionising radiation fluences.

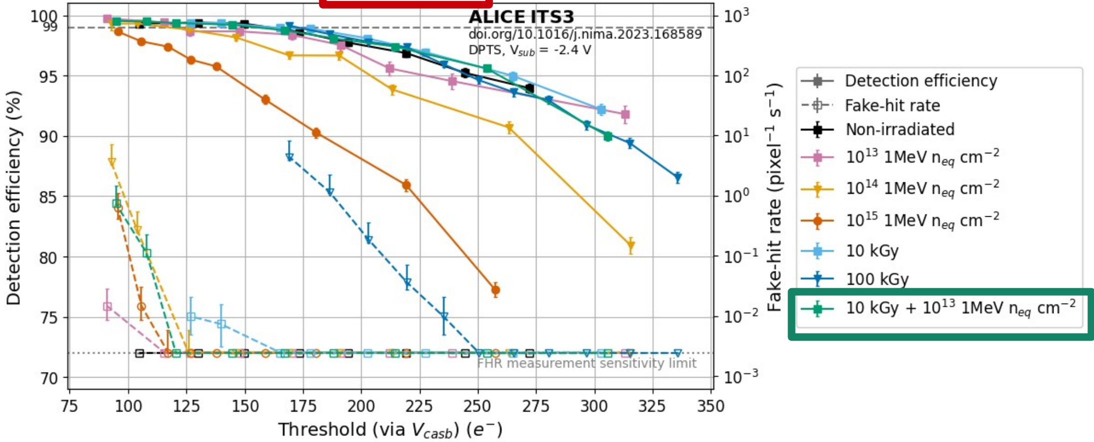
Up to the ITS3 radiation hardness requirement (10^{13} 1 MeV n_{eq} cm^{-2}), **the effect of the irradiation is negligible**.

Detection efficiency & Fake hit rate

APTS



DPTS



APTS **detection efficiency** vs. threshold for different pixel pitches, measured at V_{sub} = 0 V

- it increases with increasing pixel pitch
- possible operation without reverse substrate bias

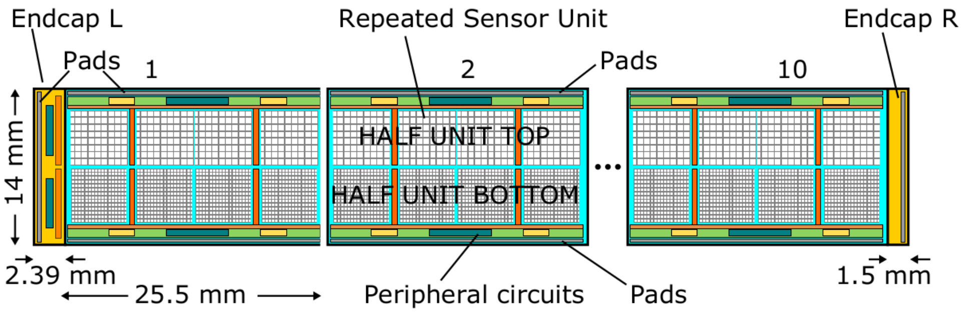
DPTS (15 µm pixel pitch) **detection efficiency** and **fake-hit rate** as a function of average threshold (V_{sub} = -2.4 V).

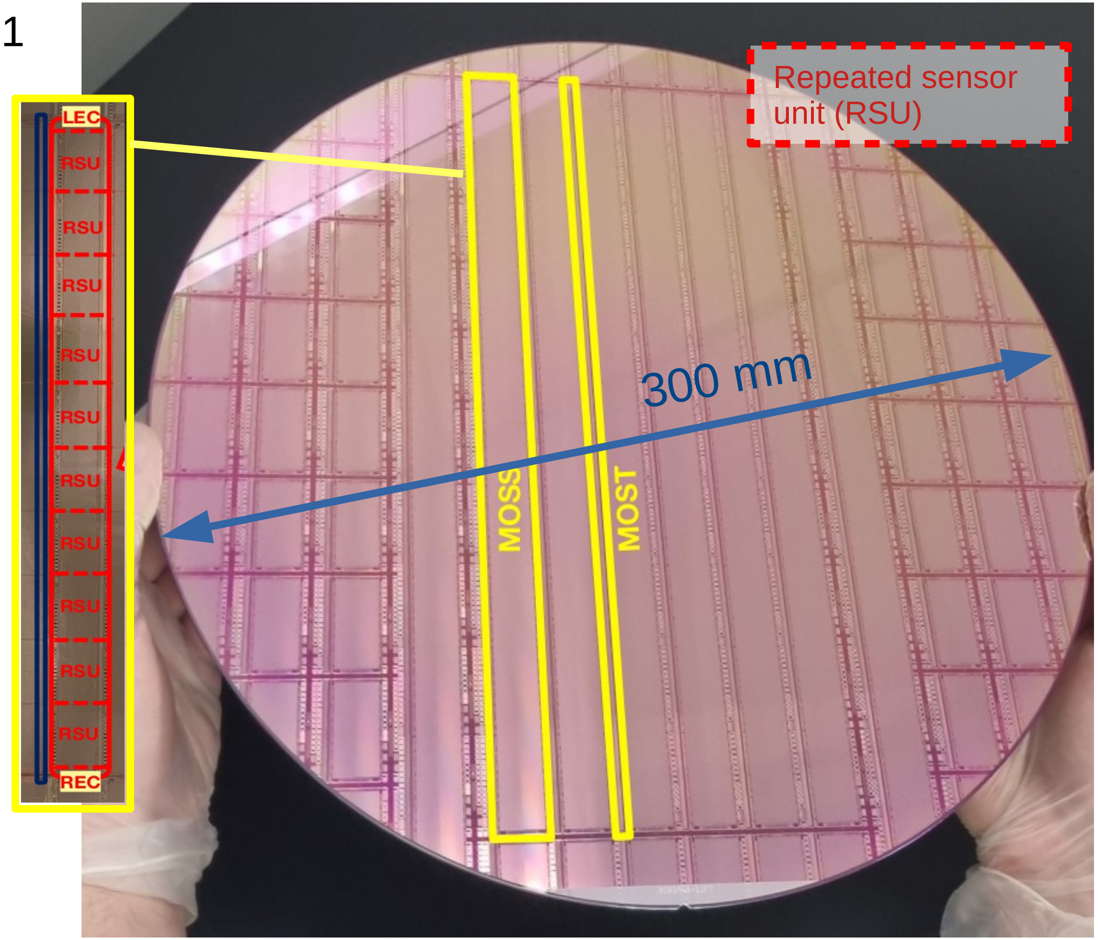
Irradiation dose received by the chips is indicated by colour (green for dose relevant for ITS3).

Efficiency > 99% and FHR < 2×10^{-3} pix^{-1}s^{-1} after irradiation at ITS3 requirements

Stitched MAPS in Engineering Run 1 (ER1, 65 nm)

- Stitched prototypes, produced in engineering run 1 (ER1) in summer 2023, 24 wafer, ***six of each sensor*** per wafer
  - **MOSS (MOnolithic Stitched Sensor)**
    - 14 x 259 mm^2
    - 6.72 Mpixel, different pitches (18 and 22.5 μm)
- First subset thinned down to 50 μm
- ***Goal:*** *Show feasibility of stitching process (laboratory + test beam)*

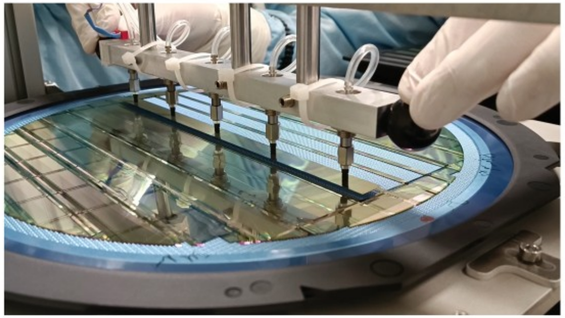


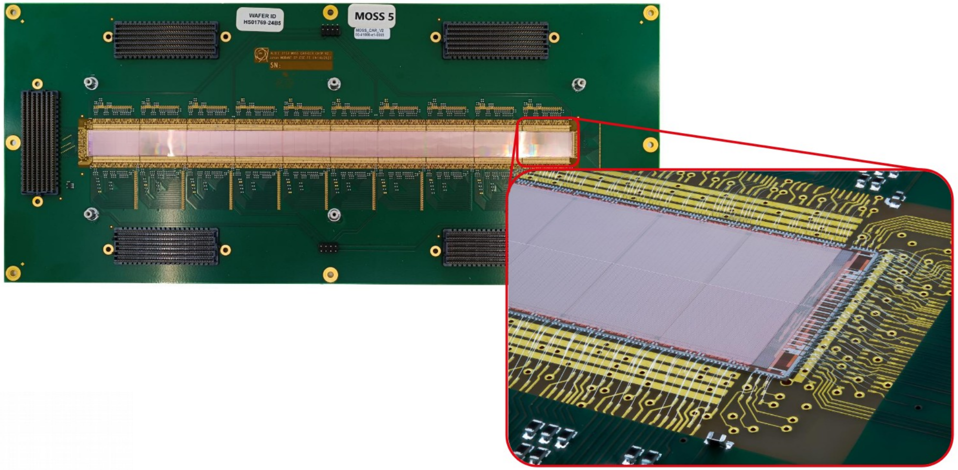


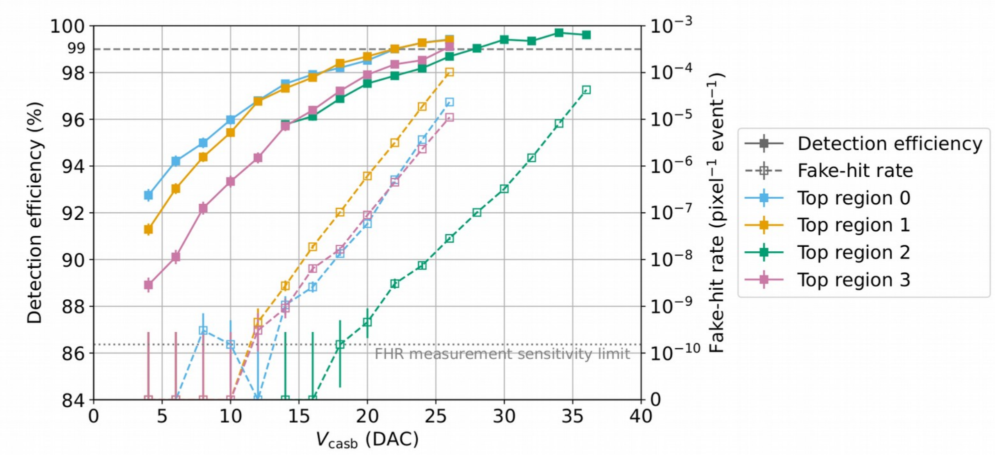
Stitched MAPS in Engineering Run 1 (ER1, 65 nm)

Handling of such a large, thin chip is not trivial → development of tools and procedures!

Picking, mounting, bonding



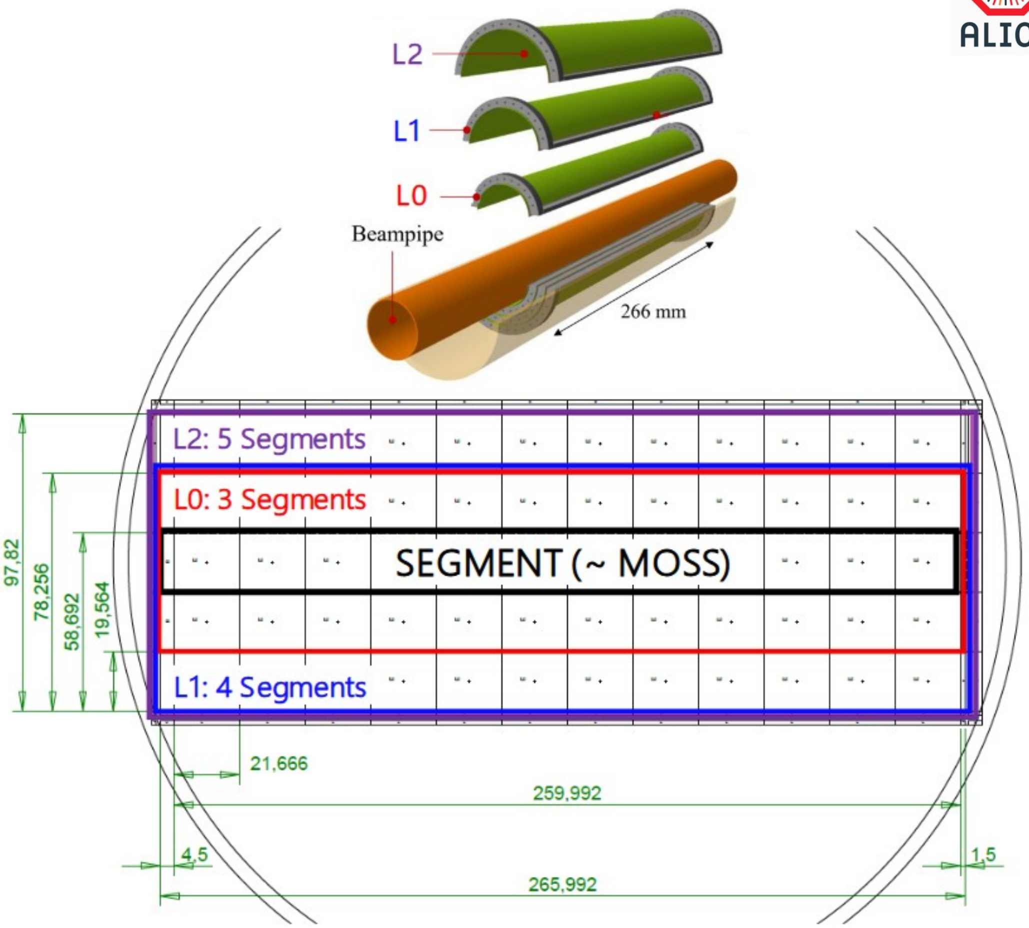




- Test on the pixel matrix: chip is operational
- Beam test campaigns at the CERN PS: efficiency expected from MLR1 chips is confirmed
- Yield: currently under study with extensive characterization campaign with wafer prober

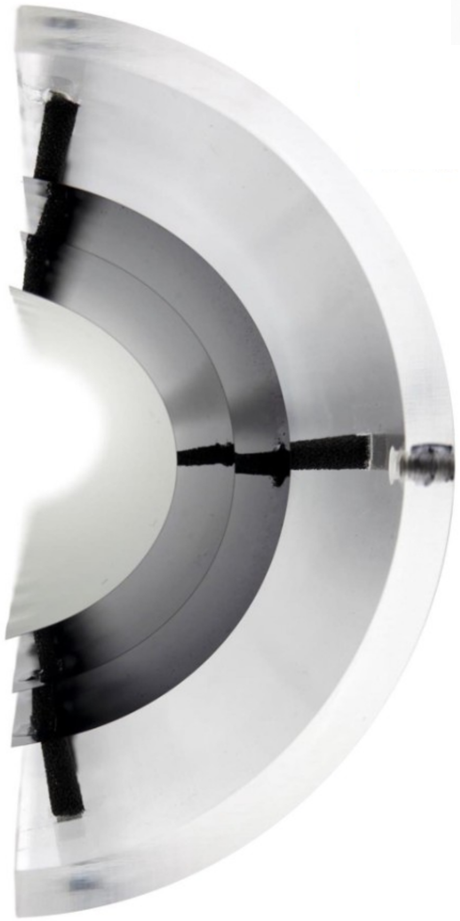
Future ITS3 milestones

- **ER2 - full size prototype sensor with ITS3 specifications**
    - Modular design: each sensor is divided into 3, 4, or 5 segments with 12 RSUs
    - Powering and readout only from end-caps
    - Submission to the foundry in fall 2024
- **ER3 – final sensor production**
- **Final assembly and commissioning**



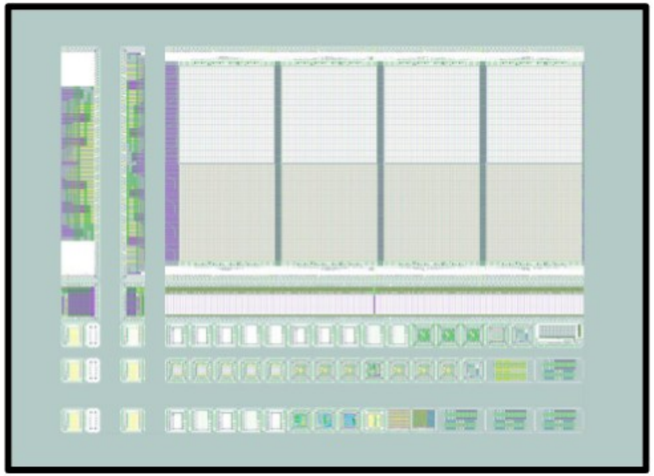
Summary

- ITS3 will be installed during **LS3** to be ready for **LHC Run 4 (2029-2032)**
- Key R&D milestones achieved, in particular,
  - 65nm technology has been validated for the use in ITS3:
    - modified-with-gap design is more efficient compared to the modified and standard design
    - all the tested chips show detection excellent efficiency over large threshold range term for the ITS3 radiation hardness requirements (10 kGy + 10^{13} 1 MeV n_{eq} cm^{-2})
- Stitching qualification is ongoing:
  - MOSS design is functional
  - First studies on first large-scale stitched sensors performance (ER1) shows promising result → to be extended on more chip and wafers

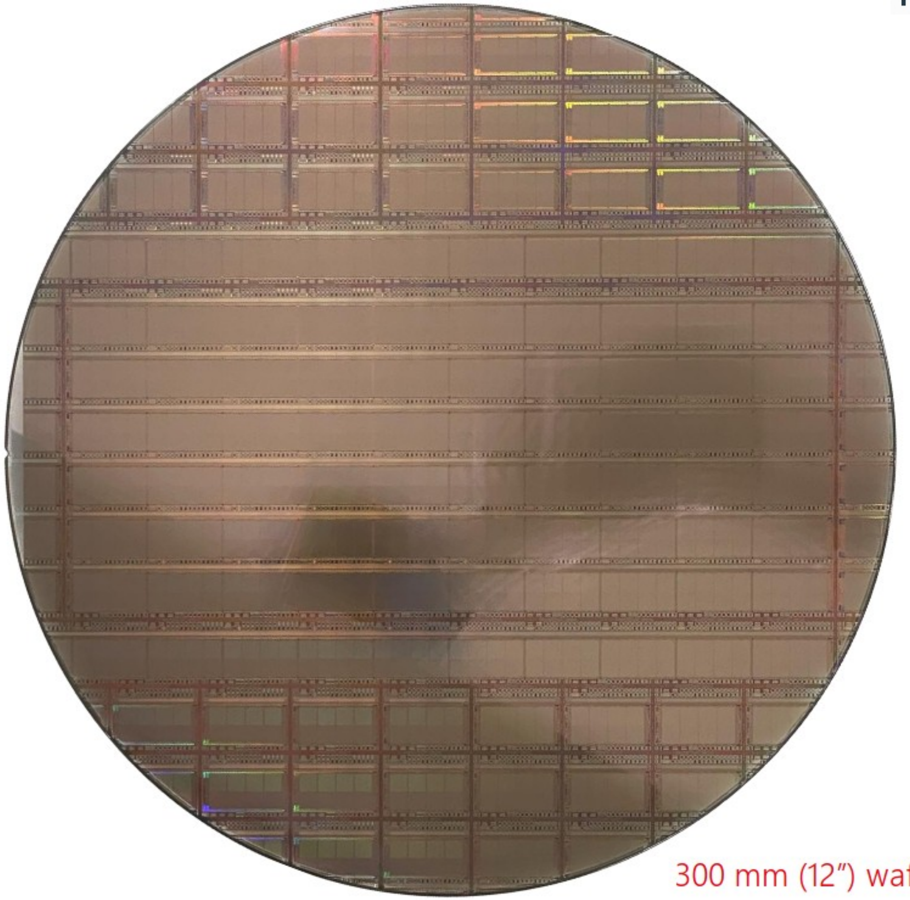


Backup

ER1 wafer



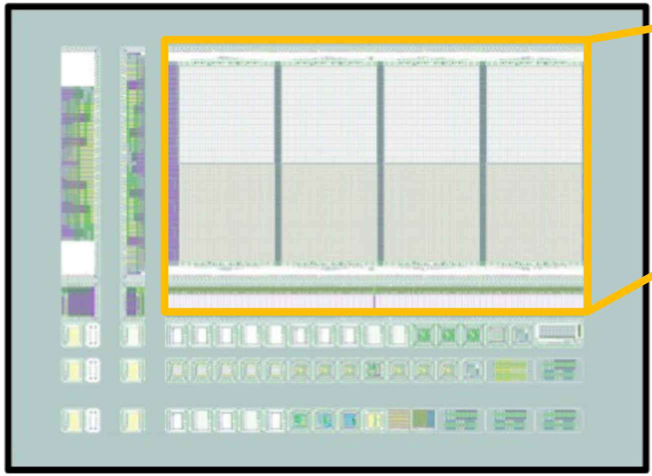
Design reticle



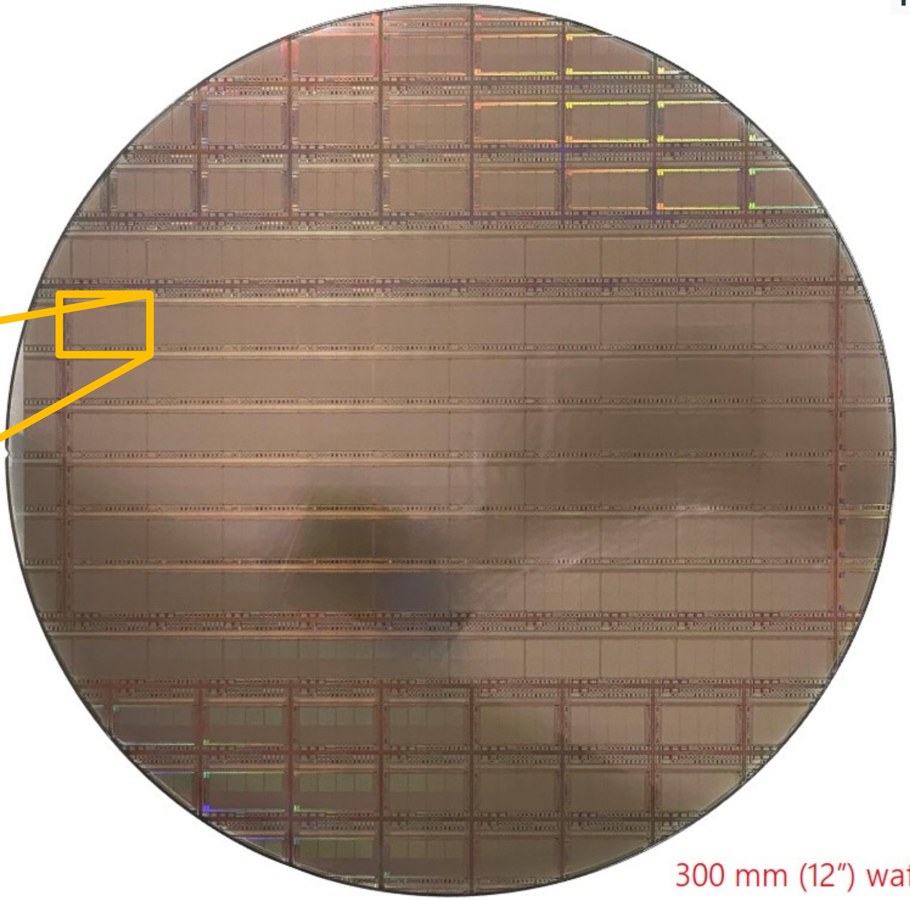
300 mm (12”) wafer

ER1 wafer

Repeated sensor unit (RSU)

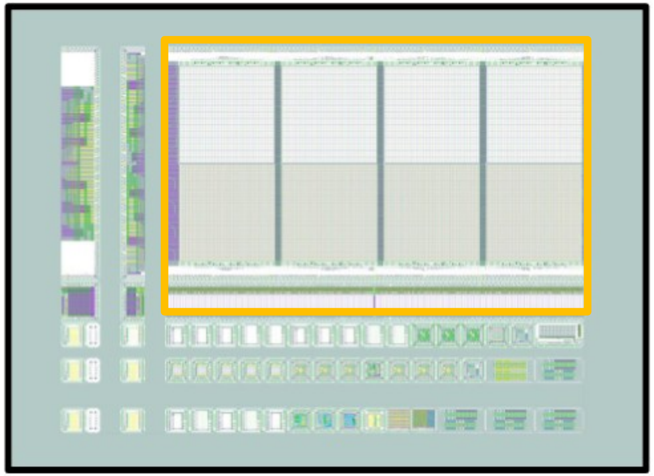


Design reticle

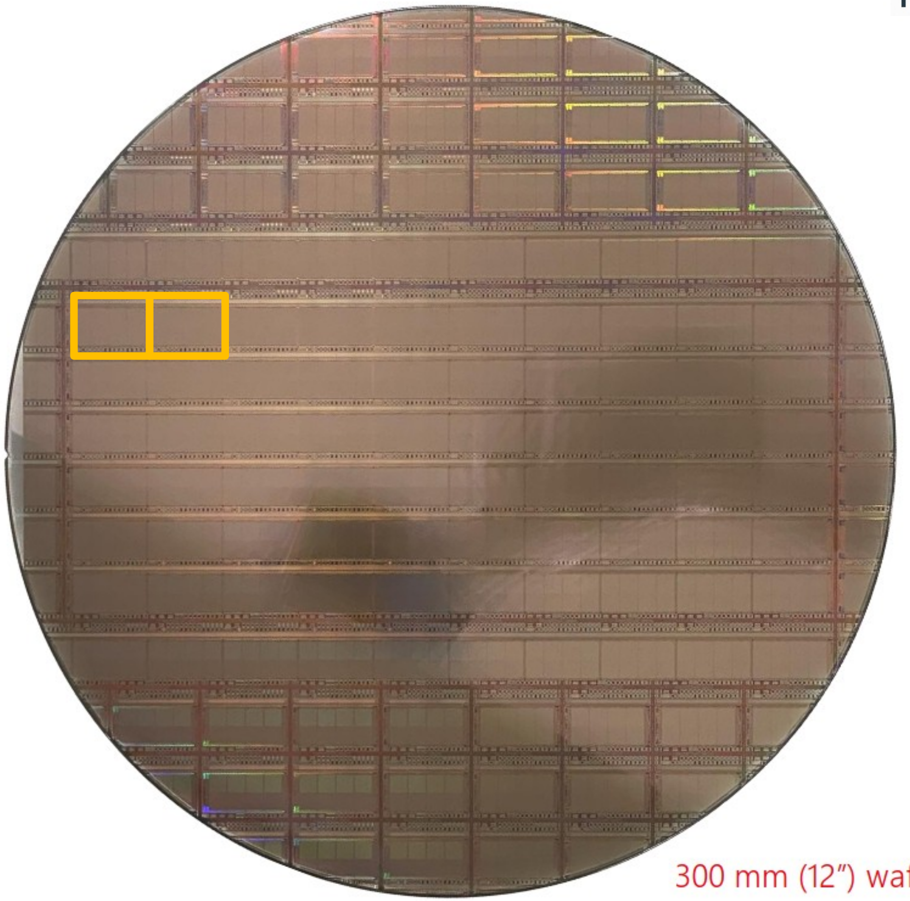


300 mm (12”) wafer

ER1 wafer



Design reticle



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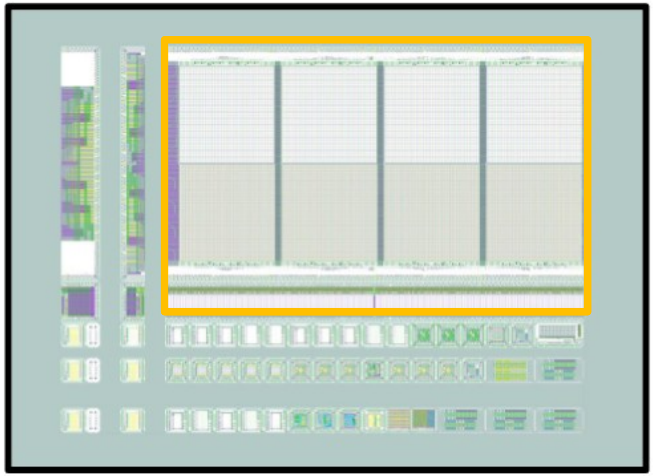
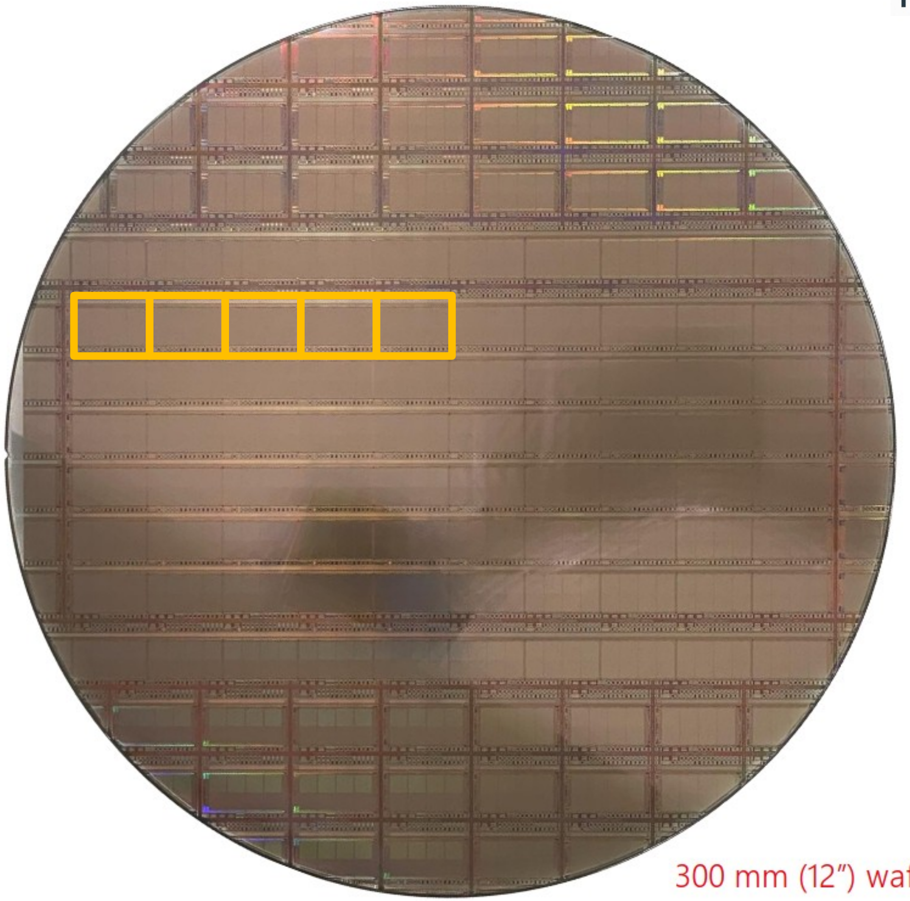


Design reticle



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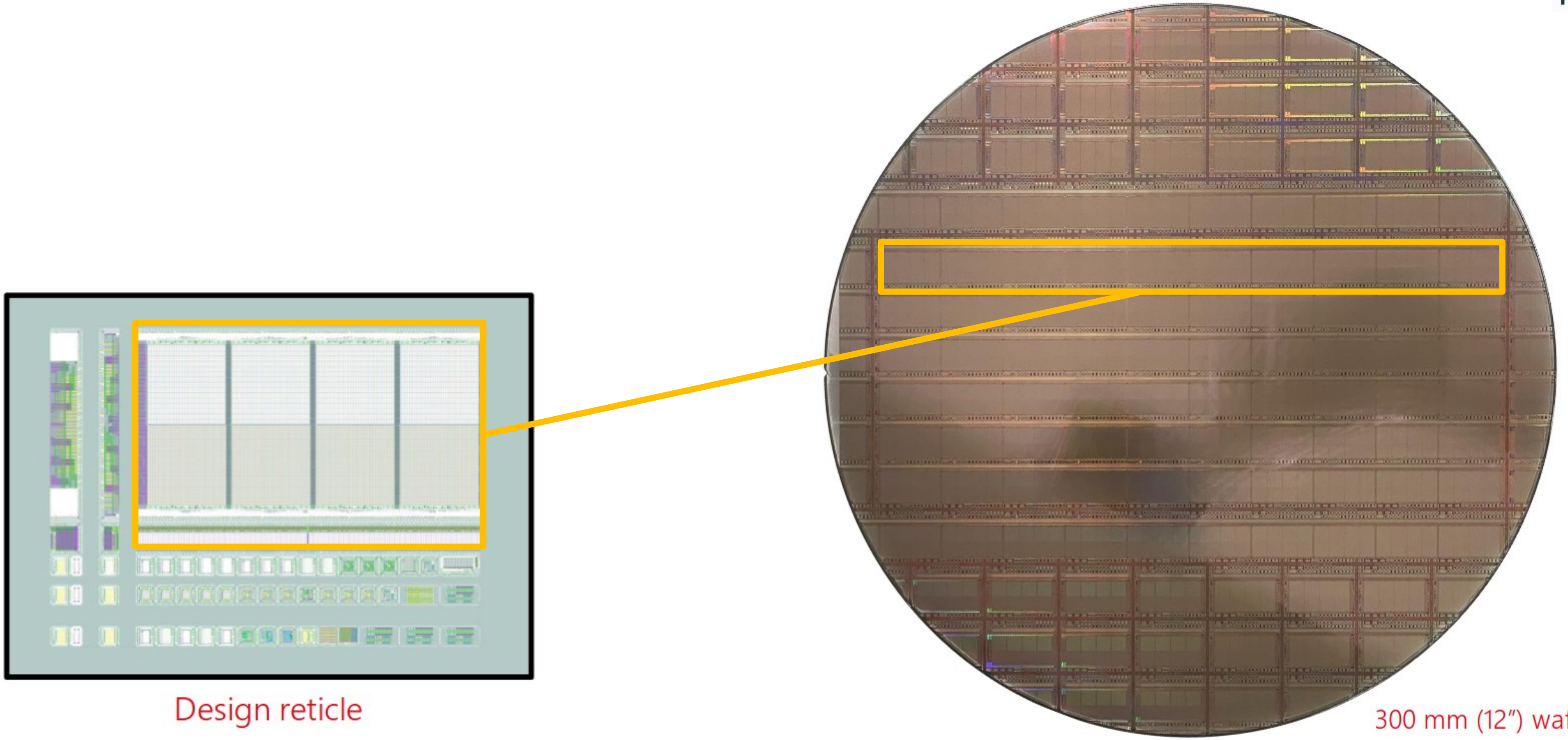
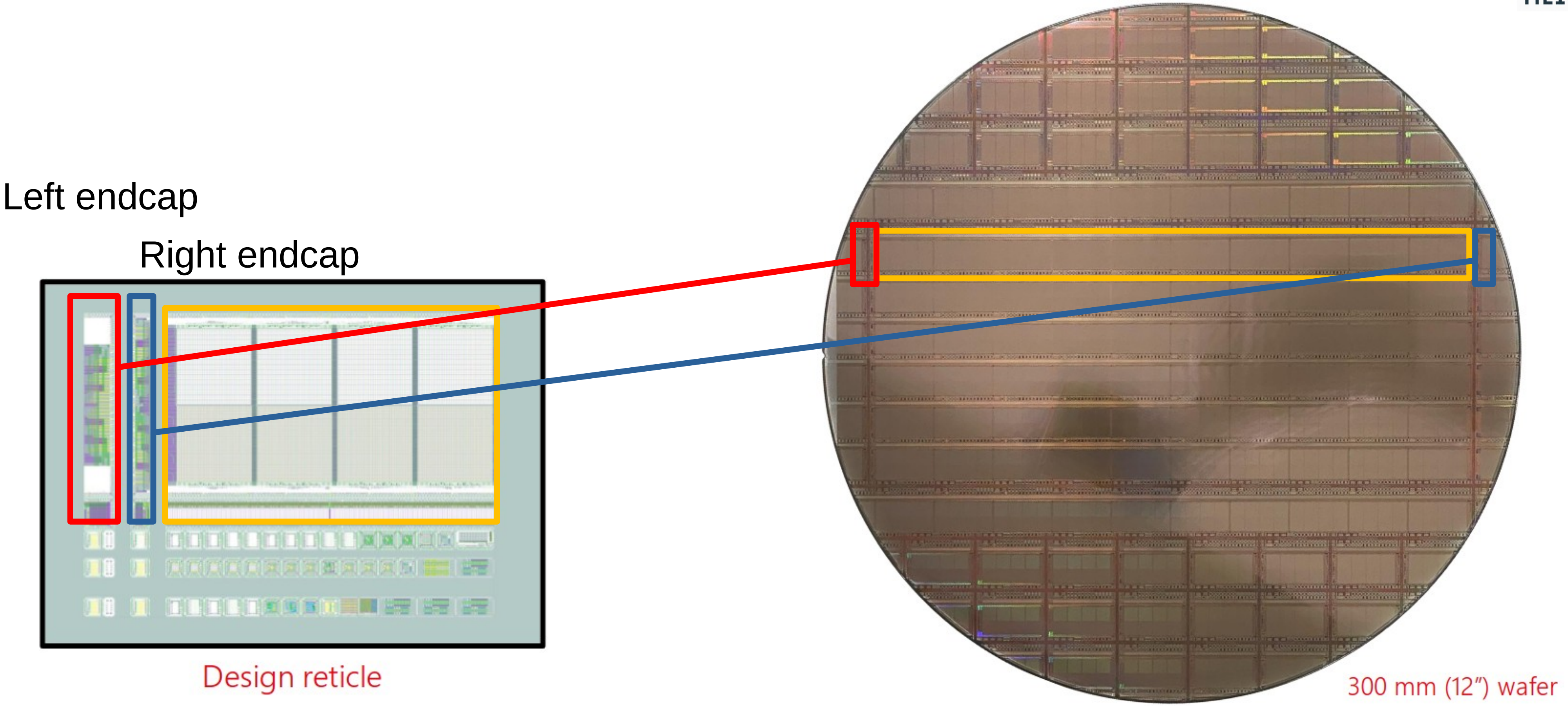


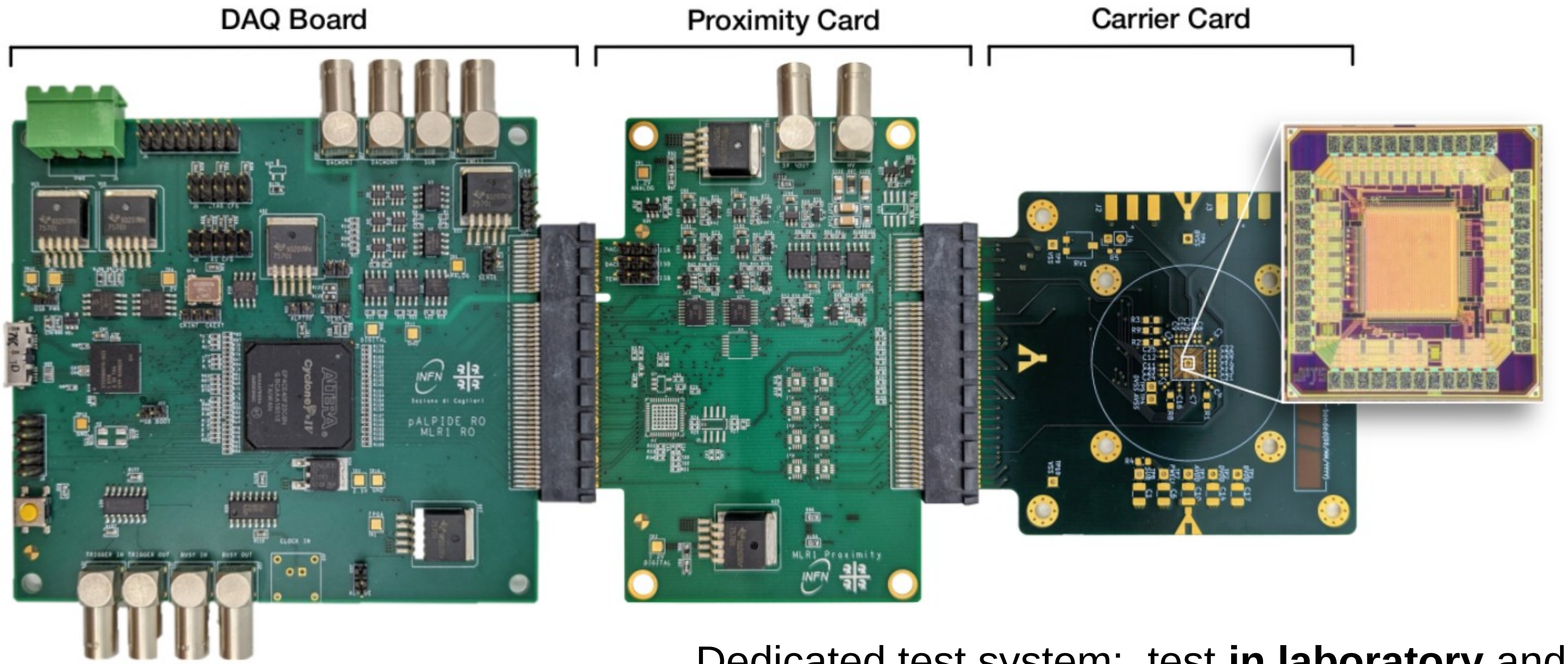
Design reticle

300 mm (12”) wafer

ER1 wafer



Qualification strategy

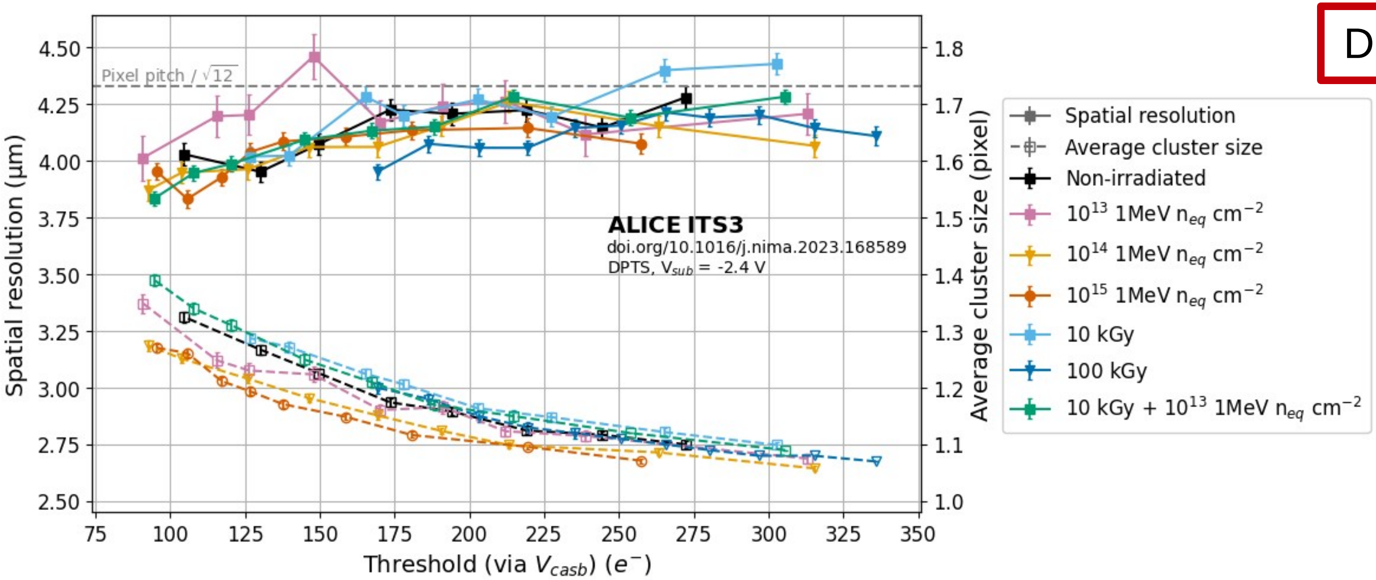


Dedicated test system: test **in laboratory** and **test beam facilities**

- The chips are glued and wire-bonded to carrier card PCBs
- Test system provides power, biasing, control and readout

Spatial resolution

DPTS



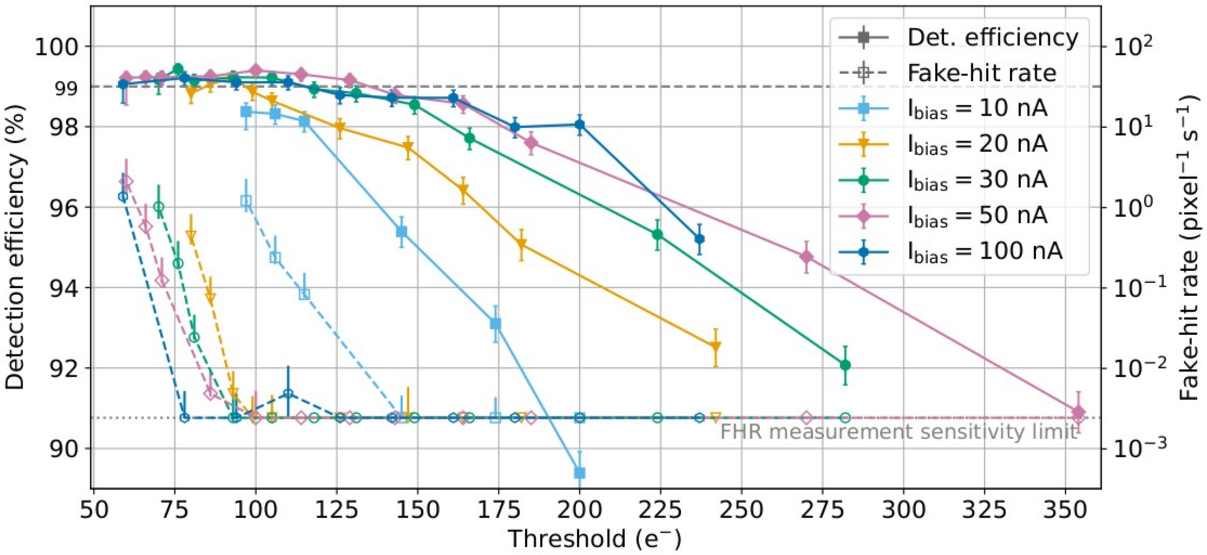
DPTS (15 μm pixel pitch) **spatial resolution** (solid lines) and **average cluster size** (dashed lines) Vs threshold

- The spatial resolution measured slightly better than pixel pitch / √12 (no degradation with received dose)
- Slight systematic decrease of average cluster size with the increasing non-ionising radiation dose

Nuclear Inst. and Methods in Physics Research, A 1056 (2023) 168589
https://www.sciencedirect.com/science/article/pii/S016890022300579X?via%3Dihub

Power consumption

DPTS



DPTS front end designed to investigate **power consumption**, critical aspect for the ITS3 (ITS3 target < 40 mW/cm^2):

- at least a main current I_{bias} of 30 nA is needed
- 16 mW/cm^2 as measured on 15 μm pixel
- 7.6 mW/cm^2 if projected to the final ITS3 sensor pixel pitch

Circuit

The topology of the circuit follows an evolutionary path with roots in the ALPIDE sensor chip used in the ITS2.

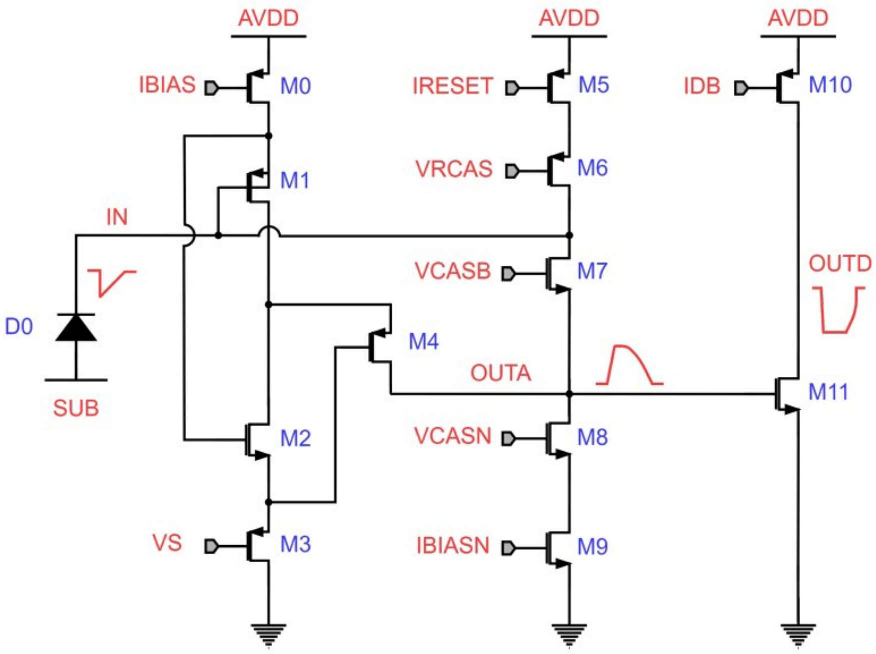


Figure 3.40: Simplified schematic of the pixel front-end amplifier and discrimination sections.

General requirements for the sensor ASIC design

Table 2.1: ITS3 general parameters.

Beampipe inner/outer radius (mm)		16.0/16.5	
IB Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	19.0	25.2	31.5
Length (sensitive area) (mm)	260	260	260
Pseudo-rapidity coverage[a]	±2.5	±2.3	±2.0
Active area (cm^2)	305	407	507
Pixel sensors dimensions (mm^2)	266×58.7	266×78.3	266×97.8
Number of pixel sensors / layer		2	
Material budget ($\%X_0$ / layer)		0.07	
Silicon thickness (µm / layer)		≤50	
Pixel size (μm^2)		$O(20 \times 22.5)$	
Power density (mW/cm^2)		40	
NIEL ($1\,MeV\ n_{eq}\ cm^{-2}$)		10^{13}	
TID (kGray)		10	

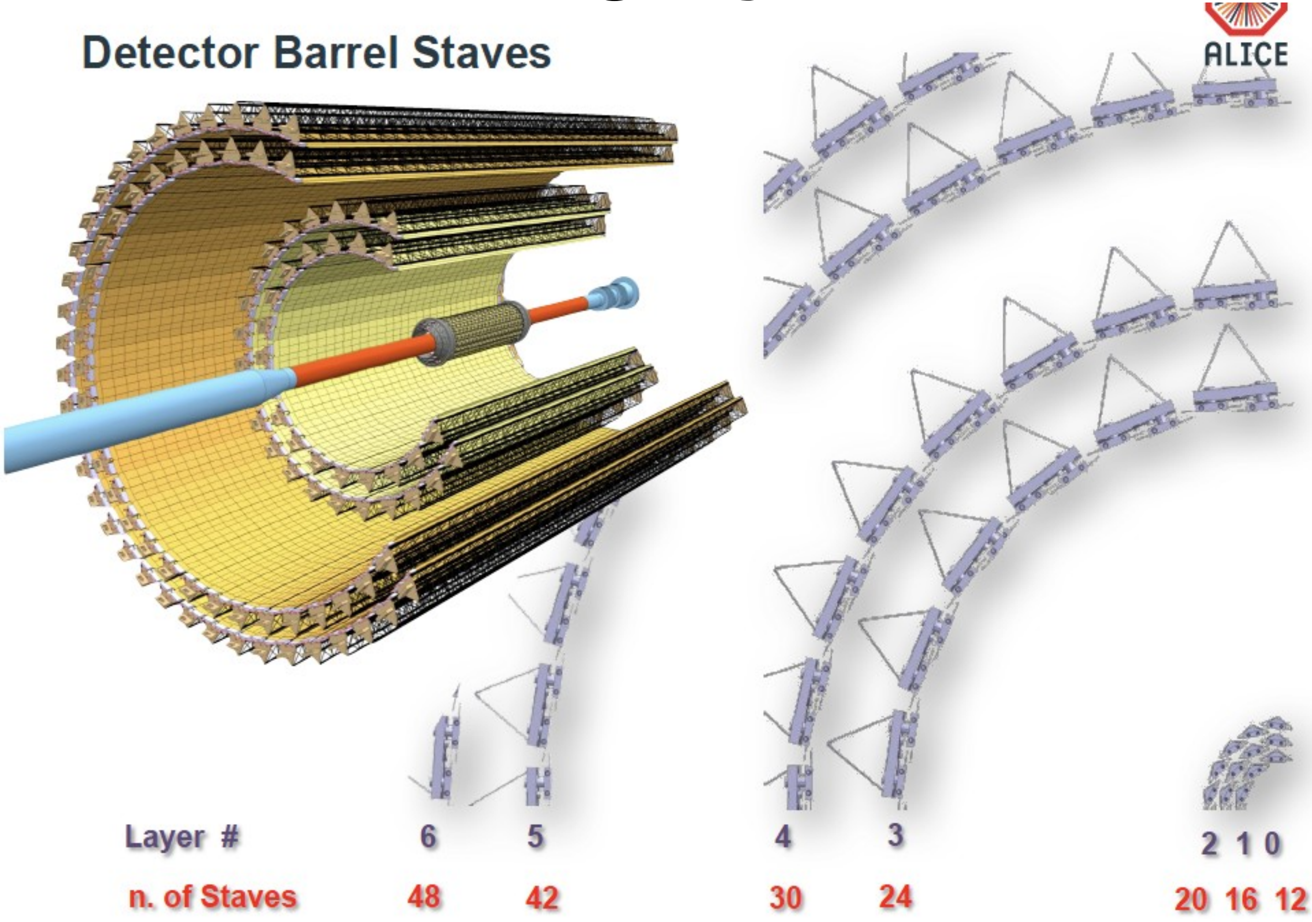
[a] The pseudorapidity coverage of the detector layers refers to tracks originating from a collision at the nominal interaction point ($z = 0$).

General requirements for the sensor ASIC design

Table 3.2: General requirements for the sensor ASIC design.

Particle Rate	
Pb-Pb Interaction Rate (average)	50 kHz
Pb-Pb Interaction Rate (expected peak rate including safety factor of 2)	164 kHz
Total particle flux (@164 kHz, Layer 0, z=0 cm)	$5.75\,\mathrm{MHz\,cm^{-2}}$
Hadronic flux (all centralities, @164 kHz, Layer 0, z=0 cm)	$2.55\,\mathrm{MHz\,cm^{-2}}$
QED electrons flux (@164 kHz, Layer 0, z=0 cm)	$3.20\,\mathrm{MHz\,cm^{-2}}$
Detection Performance	
Single point resolution	$\lesssim 5\,\mu\mathrm{m}$
Pixel pitch	$< 25\,\mu\mathrm{m}$
Fill factor (fractional sensitive area)	$> 92\%$
Detection efficiency	$> 99\%$
Fake-hit rate	$< 0.1\,\mathrm{pixel^{-1}\,s^{-1}}$
Fake-hit occupancy (10 µs Frame Duration)	$< 10^{-6}\,\mathrm{pixel^{-1}\,frame^{-1}}$
Frame duration programmable	$2 - 10\,\mu\mathrm{s}$
Readout Efficiency	
Fraction of Pb-Pb interactions fully recorded, Layer 0	$> 99.9\%$
Fraction of incomplete Pb-Pb interactions, Layer 0	$< 1 \times 10^{-3}$
Power Budget	
Power Dissipation Density, Active Region	$< 40\,\mathrm{mW\,cm^{-2}}$
Power Dissipation Density, Peripheral Region	$< 1000\,\mathrm{mW\,cm^{-2}}$
Radiation Load	
NIEL	$10^{13}\,1\,\mathrm{MeV}\ n_{eq}\ \mathrm{cm^{-2}}$
TID	10 kGy
Environmental Conditions	
Target Operating Temperature	15 °C to 30 °C

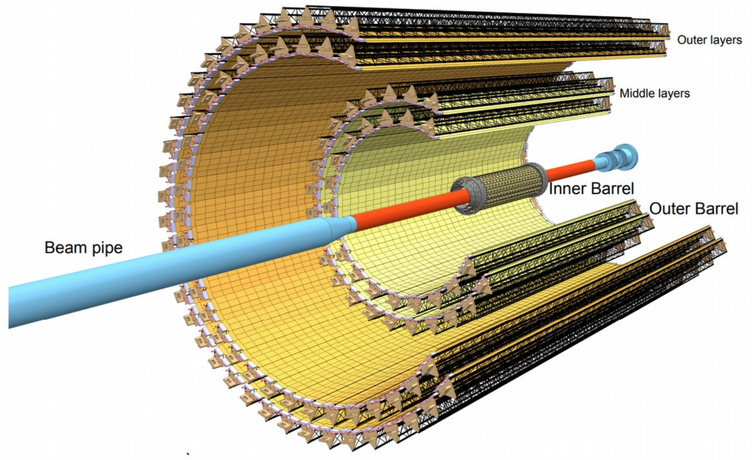
ALICE Inner Tracking System 2: ITS2



ITS2

Table 4. Main layout parameters of the new ITS2.

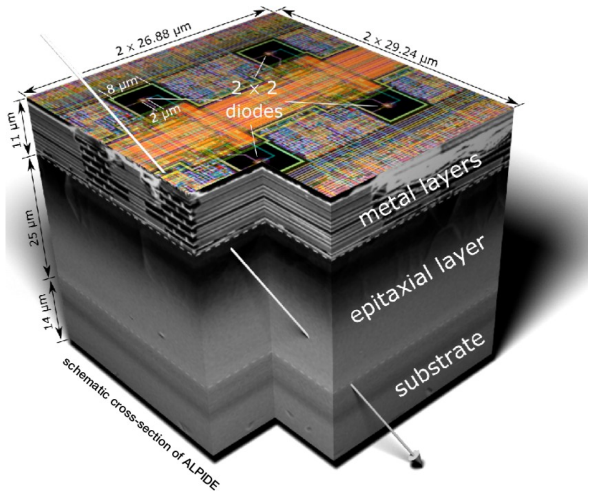
Layer no.	Average radius (mm)	Stave length (mm)	No. of staves	No. of HICs/ stave	Total no. of chips
0	23	271	12	1	108
1	31	271	16	1	144
2	39	271	20	1	180
3	196	844	24	8	2688
4	245	844	30	8	3360
5	344	1478	42	14	8232
6	393	1478	48	14	9408

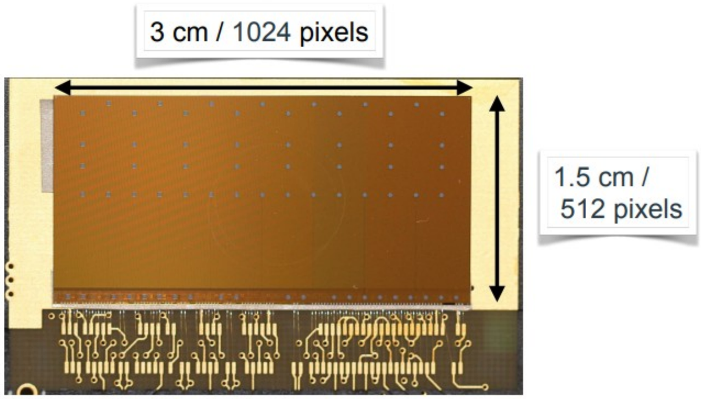


https://iopscience.iop.org/article/10.1088/1748-0221/19/05/P05062/pdf

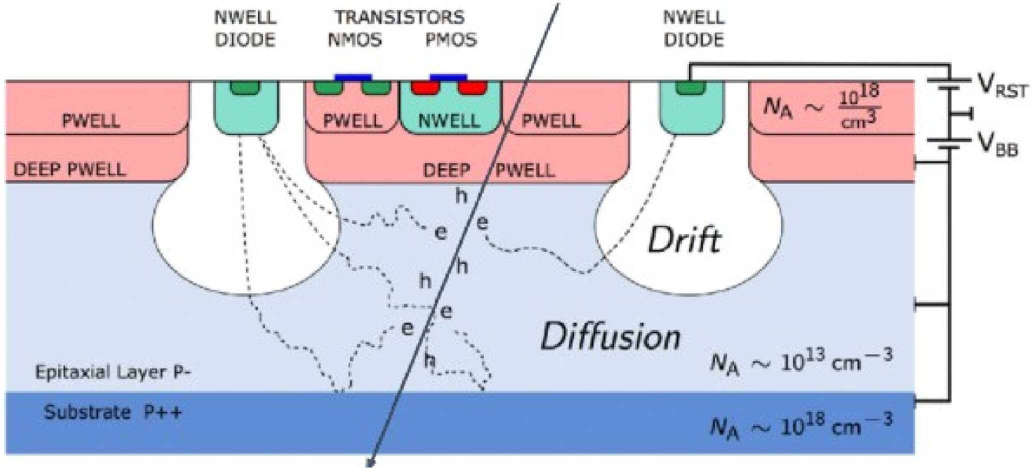
ALICE Inner Tracking System 2: ITS2

Built using **ALPIDE**, a Silicon pixel chip based on 180 nm Monolithic Active Pixel Sensor (MAPS)





ALPIDE die on carrier card

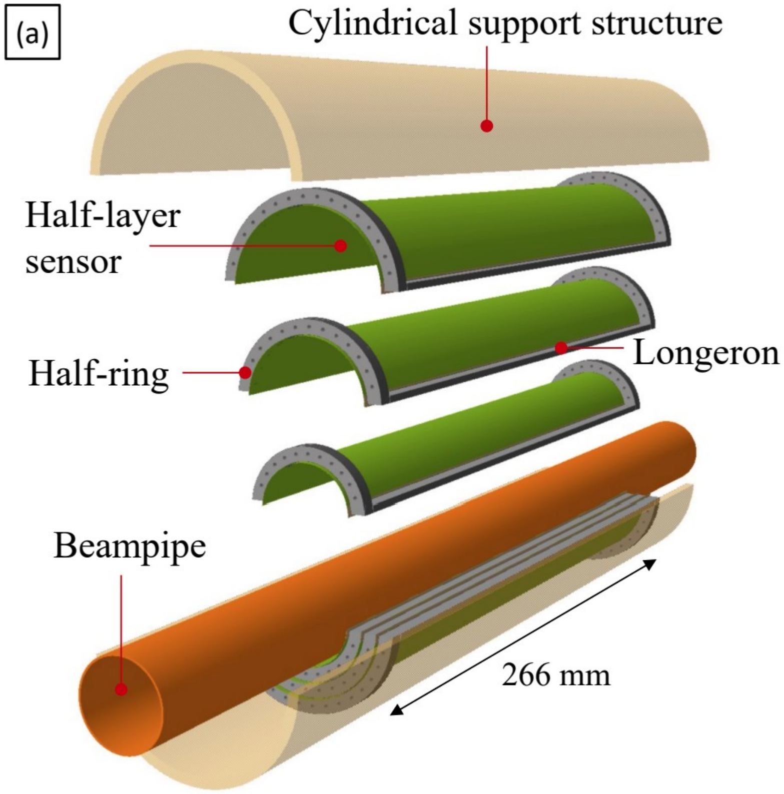


ITS2

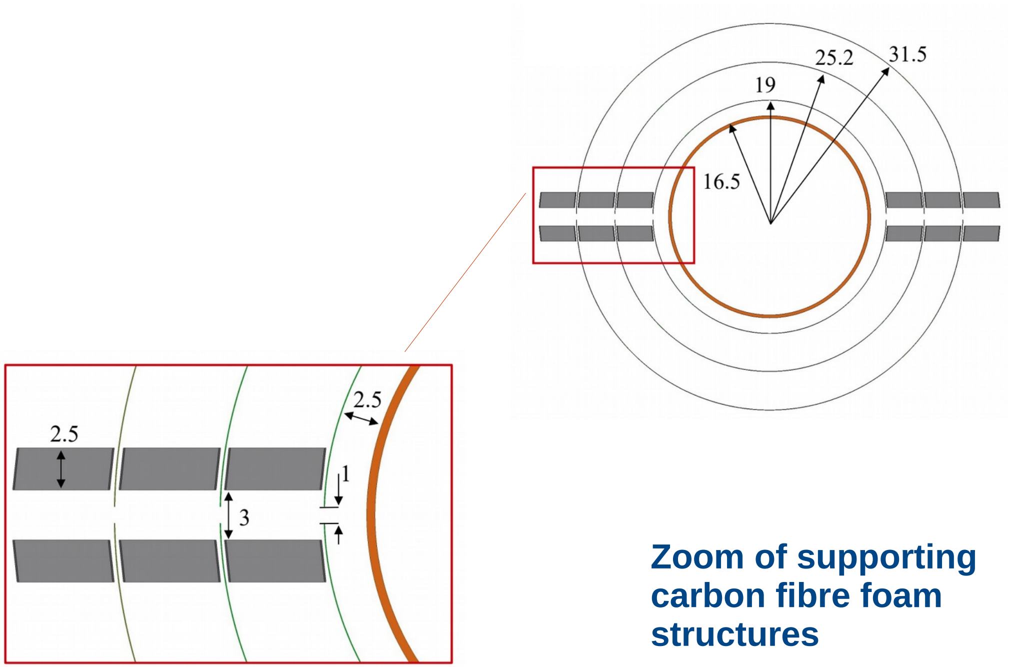
Parameter	Inner Barrel	Outer Barrel
Chip dimensions [mm × mm]	15×30	
Silicon thickness [µm]	50	100
Spatial resolution [µm]	5	10 *(5)*
Detection efficiency	> 99%	
Fake-hit probability [$\text{evt}^{-1}\text{pixel}^{-1}$]	$< 10^{-6}$ ($\ll 10^{-6}$)	
Integration time [µs]	< 30 (*10*)	
Power density [mW/cm^2]	< 300 (~ *35*)	< 100 (~ *20*)
TID radiation hardness* [krad]	270	10
NIEL radiation hardness* [$1\ \text{MeV}\ n_{eq}/\text{cm}^2$]	1.7×10^{12}	1×10^{11}
Readout rate, Pb-Pb interactions [kHz]	100	

https://iopscience.iop.org/article/10.1088/1748-0221/19/05/P05062/pdf

LS3 replacement of IB (2026-2028)

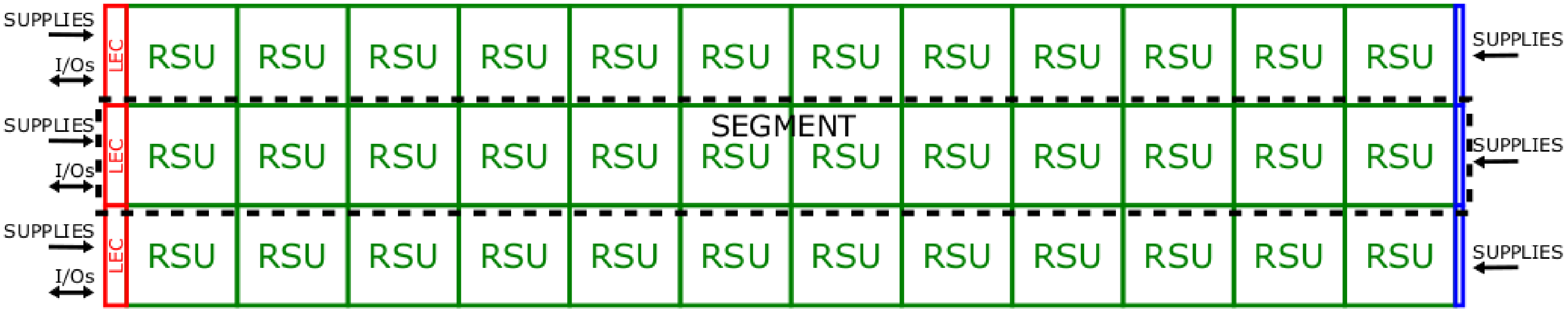


Radial distance (mm) of beam pipe and layers 0, 1, 2.



Zoom of supporting carbon fibre foam structures

Stitched MAPS in Engineering Run 1 (ER1, 65nm)



Stitched MAPS in Engineering Run 1 (ER1, 65nm)