Upgrade of the LAr ATLAS calorimeters – an overview

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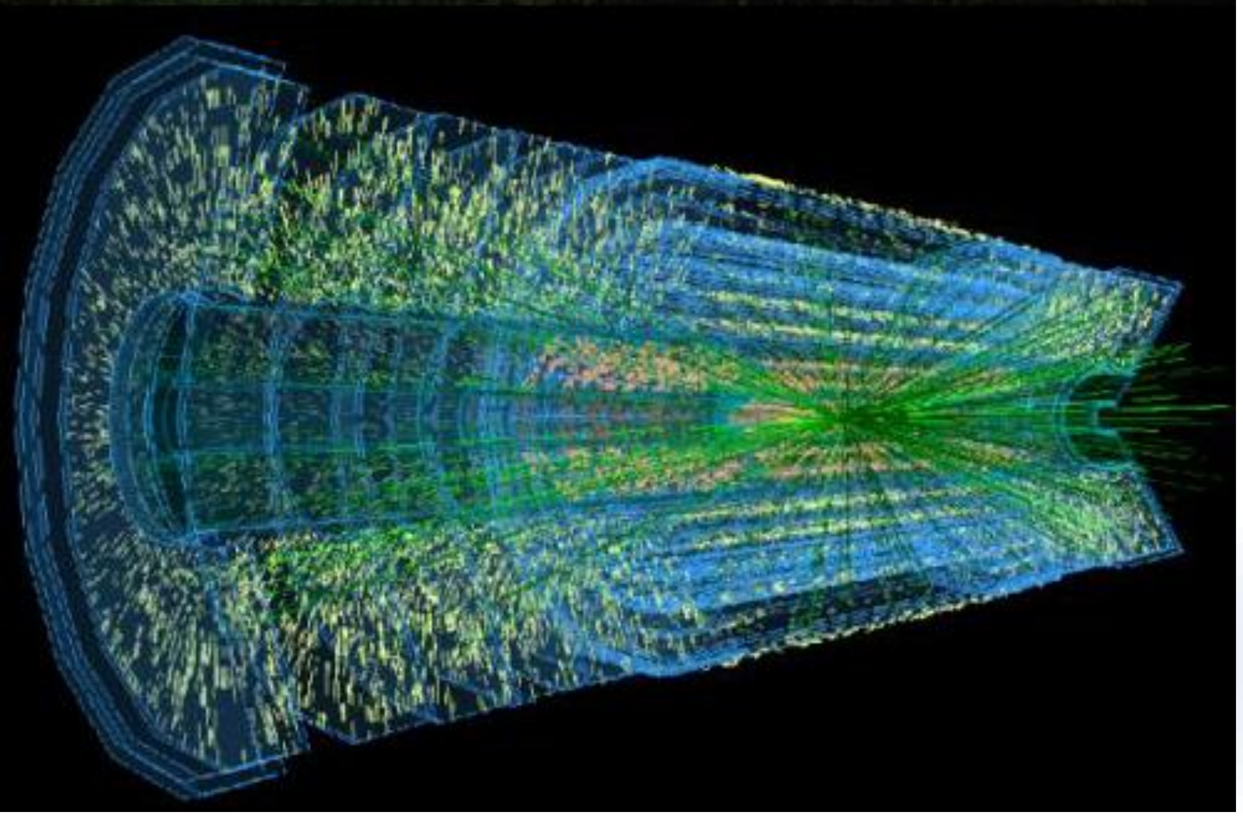
On behalf of the ATLAS Liquid Argon Calorimeter Group

XIII International Conference on New Frontiers in Physics

The ATLAS Experiment



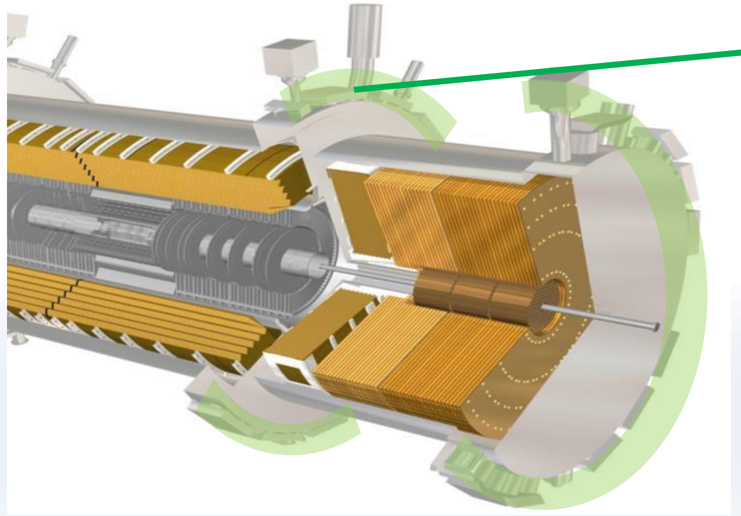
- ATLAS is one of the four main detectors at the Large Hadron Collider

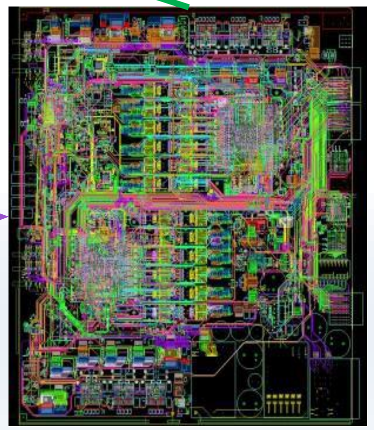
- A collider upgrade in 2026-2028 will increase the luminosity up to 7x the design value →High-Luminosity LHC (HL-LHC)
- 140-200 simultaneous proton-proton collisions are expected every 25 ns

- The liquid-argon (LAr) calorimeters will measure the energy of electrons, photons and hadronic particles in each of the 182.468 calorimeter cells

- New calorimeter electronics is needed to cope with improved ATLAS trigger system: trigger rate 100 kHz (today) → 1 MHz (HL-LHC)
  trigger latency 2.5 μs (today) → 10 μs (HL-LHC)
- New on-detector electronics due to radiation extreme condition

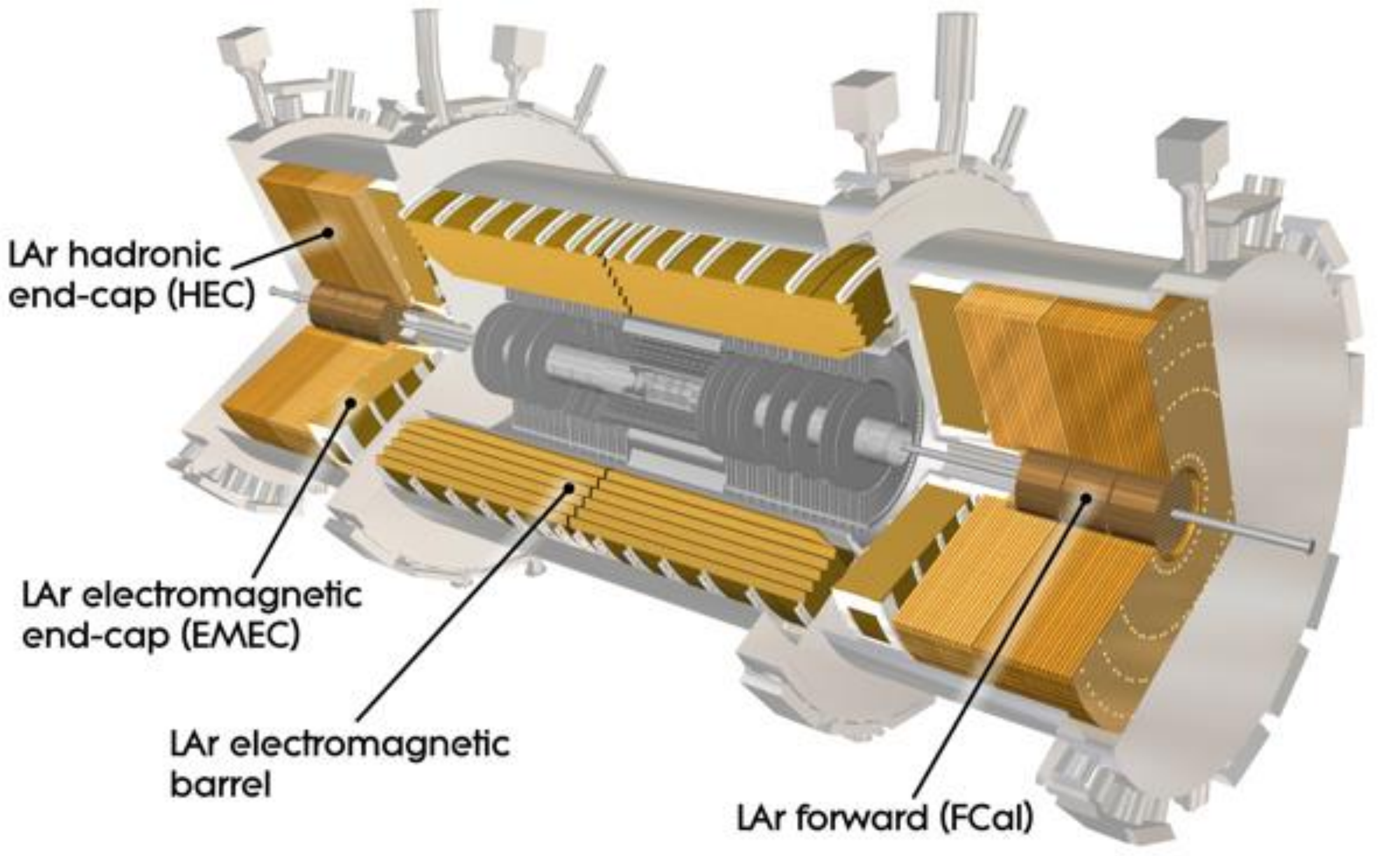
new LAr calorimeter electronics





The ATLAS Liquid Argon (LAr) Calorimeter

- Sampling calorimeter based on **liquid argon** as **active medium**.
- Measures energy, position and timing of **electromagnetic showers** (electrons and photons) + jets.



EM calorimeter (barrel + endcap)

- Lead + LAr
- 173,312 read-out channels
- Coverage: |η| < 3.2

Hadronic Endcap (HEC)

- Copper + LAr
- 5632 read-out channels
- Coverage: 1.5 < |η| < 3.2

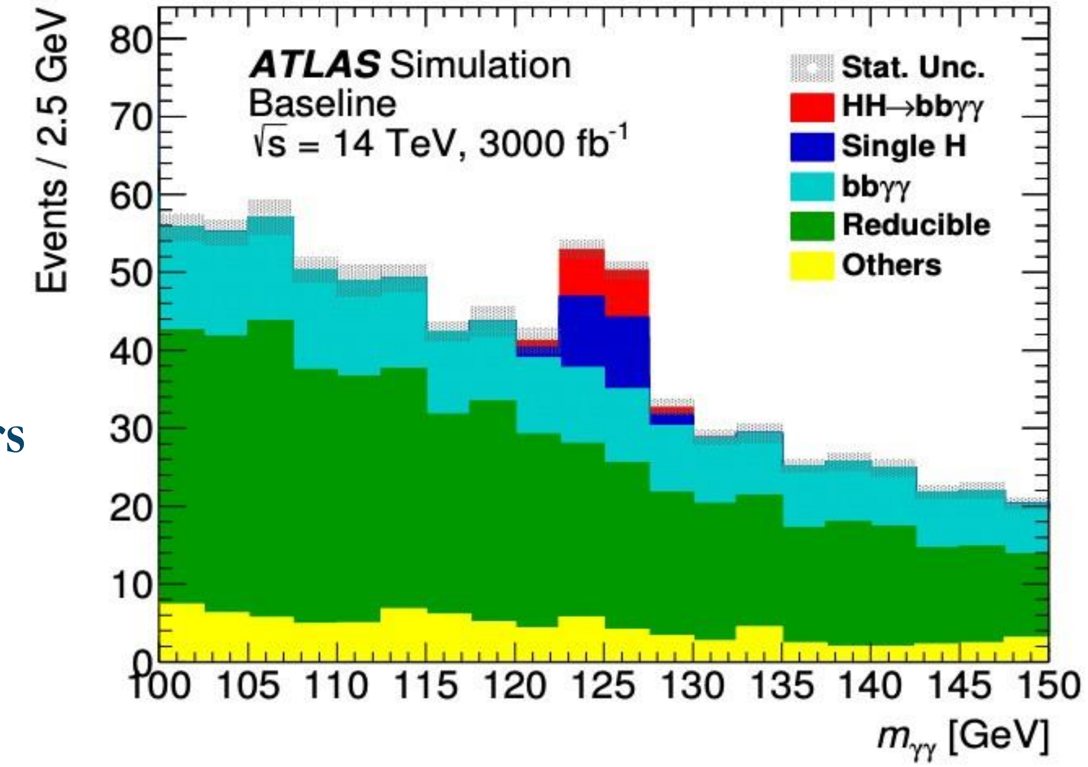
Forward Calorimeter (FCal)

- Copper/Tungsten + LAr
- 3524 read-out channels
- Coverage: 3.1 < |η| < 4.9

The High Luminosity LHC (HL-LHC) Phase

- During Run 4, ATLAS is expected to collect **3000 fb^{-1}** of data (**× 20 w.r.t. Run 2 data**) during more than **10 years of operation**.
- Achieved thanks to instantaneous luminosity up to $7 \times 10^{34}\ cm^{-2}s^{-1}$= 7 × design luminosity.
- **Challenging operation** environment!
  - ATLAS trigger & data acquisition (**TDAQ**) system needs to handle **simultaneous *pp* interactions** (= **pileup** ⟨μ⟩) up to ~**200**.
  - Stronger **radiation tolerance** for on-detector electronics is needed.

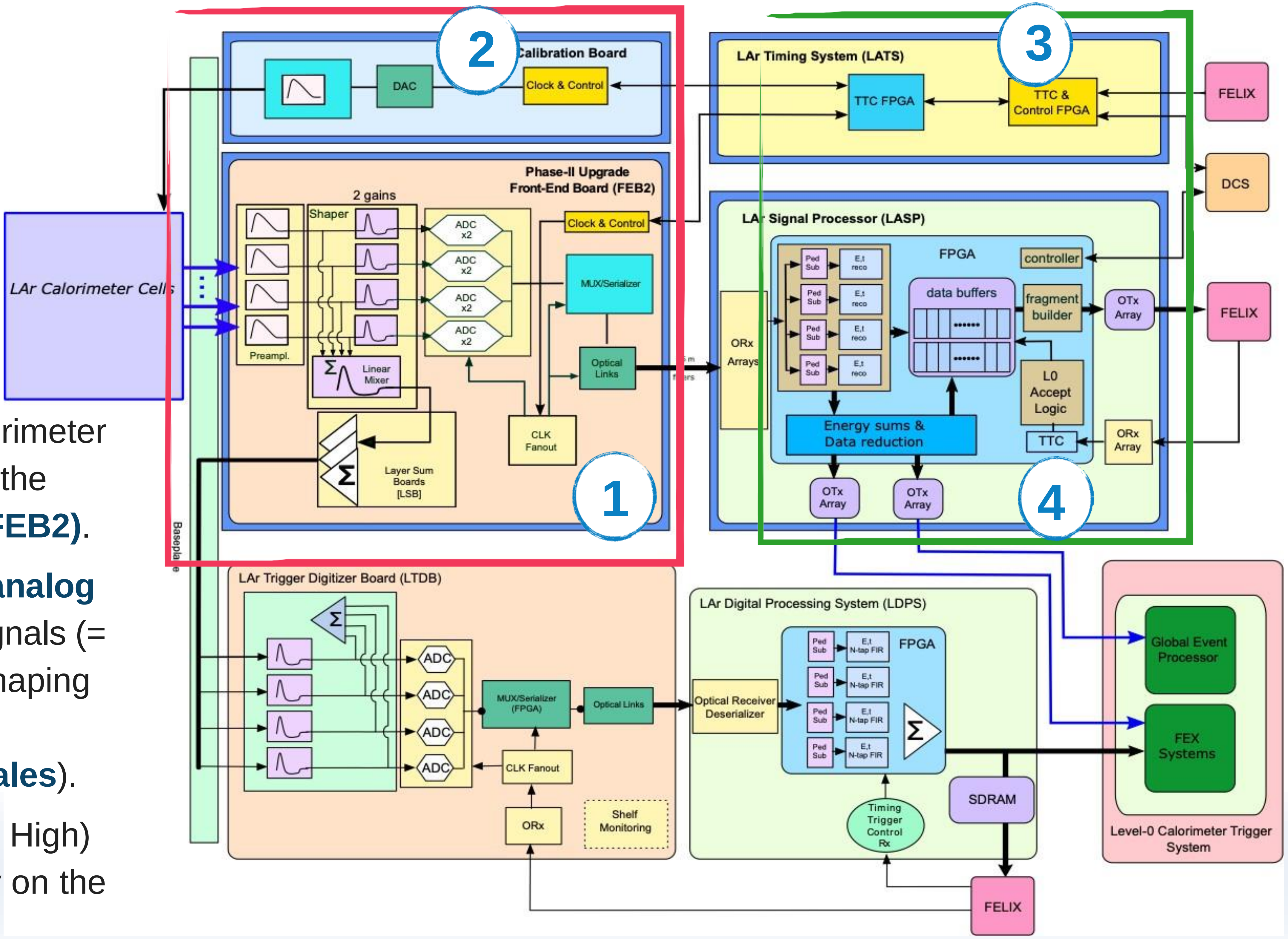
- To **survive** the **extreme conditions** of the **HL-LHC data-taking**, the ATLAS detectors will undergo major upgrades (= **Phase 2 upgrade**!).
  - Includes redesigning and replacing the **readout electronics** for the **LAr calorimeters**
  - Will have to cope with the **increased data-volume** at HL-LHC and tolerate stronger radiation doses, while retaining **excellent performance** for the **measurements** of **incoming electrons, photons, and jets**.



The High Luminosity LHC (HL-LHC) Phase

On detector

Off detector



Signals from the calorimeter cells are read out by the **Front End Boards (FEB2)**.

The FEB2s perform **analog processing** of the signals (= preamplification + shaping and splitting in **two** overlapping **gain scales**).

Both gains (Low and High) are **digitized** directly on the FEB2s.

Digitized signals are sent via optical links from the FEB2s to the LAr Signal Processing boards (**LASPs)**.

LASPs perform **digital filtering** and **accurate** and **fast energy & timing calculations**.

LASPs also send **inputs** to the **trigger system** (= will **receive full granularity calorimeter data @40 MHz**)!

Second complementary **TDAQ chain** relies on the **Phase 1 trigger**.

On-detector electronics

The Front-End Board (FEB2)

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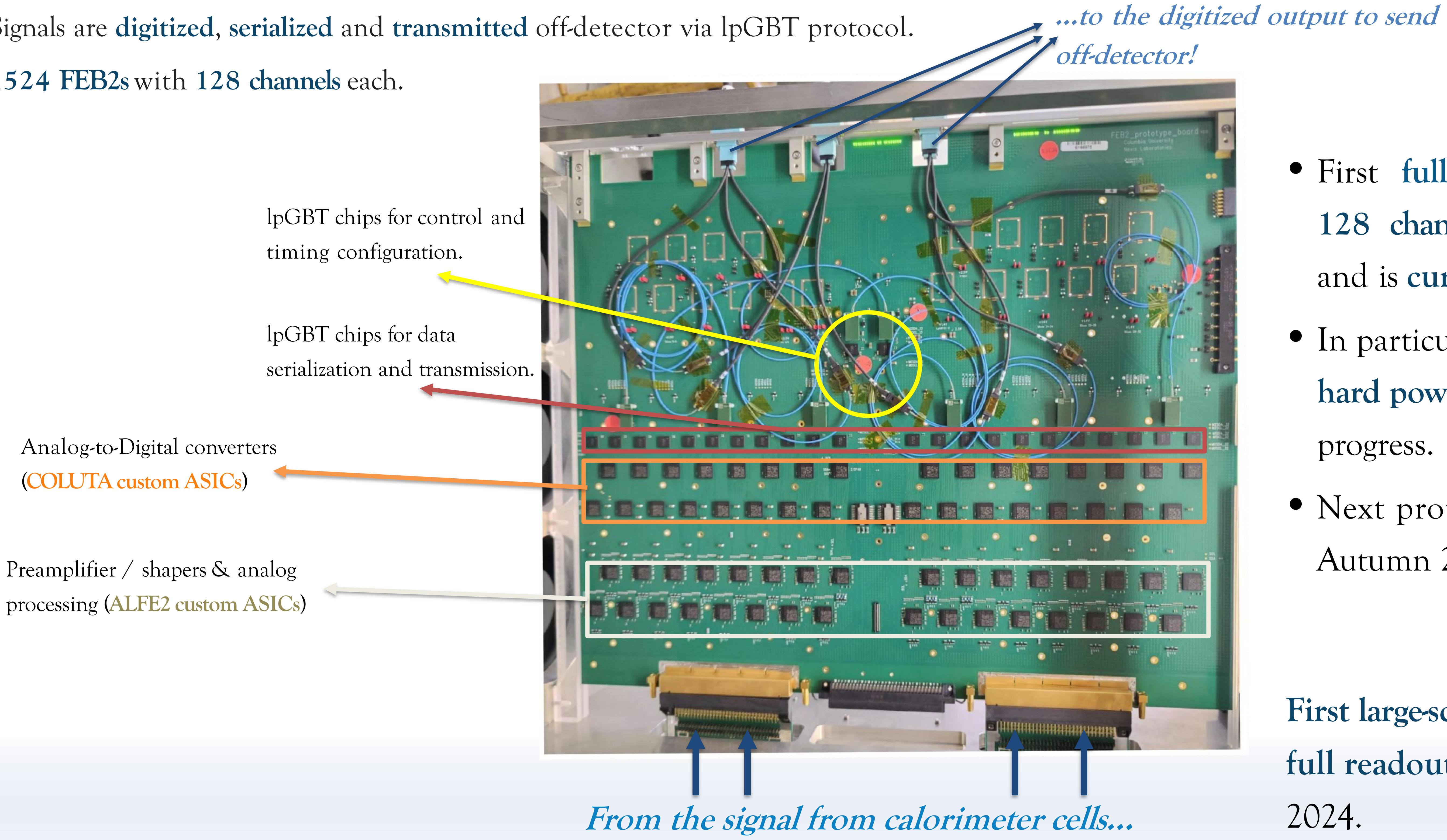
- The Front End Boards (FEB2s) receives signals from calorimeter cells and perform **analog processing**.
- Signals are **digitized**, **serialized** and **transmitted** off-detector via lpGBT protocol.
- **1524 FEB2s** with **128 channels** each.

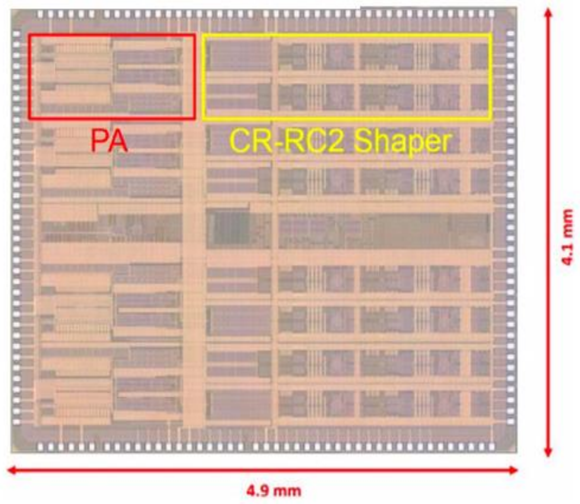


- First **full-size prototype** (with **all 128 channels** populated) is **ready**, and is **currently being tested**.
- In particular, tests for **radiation-hard powering solutions** are in progress.
- Next prototype expected in Autumn 2024.

First large-scale integration test of the **full readout chain** is expected for fall 2024.

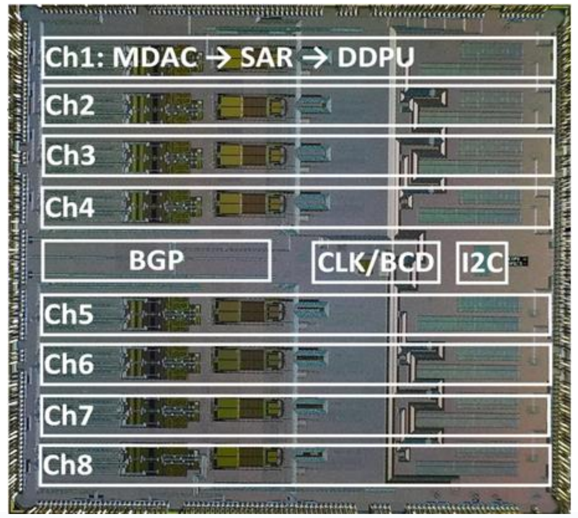
ALFE2 and COLUTA custom ASICs

ALFE2 custom ASIC: Pre-Amplifier/Shaper (PA/S)



- Based on 130 nm CMOS technology, provides **amplification** and **bipolar CR-(RC)^2 shaping** over **two overlapping gain scales** (High and Low).
- Each ASIC will handle signals from 4 calorimeter cells, and provide 9 differential inputs to the ADCs (= 4 analog signals x2 gains + 1 sum signal for hardware trigger).
  - Non-linearity < 0.1% and noise 150 nA (greatly exceeding the 350 nA requirement!) for 10 mA channels.
  - Radiation tolerance: performant after 12 kGy doses (8 times over the expected dose!).

COLUTAv4 custom ASIC: Analog to Digital Converter (ADC)



- Based on 65 nm CMOS technology, **digitizes** PA/S outputs at **40 MHz** on a **14-bit dynamic range** with two gains (required to cover the full required 16-bit dynamic range) and > 11-bit resolution.
- It covers **8 channels** = 4 analog LAr signals × 2 gains.
  - Excellent uniformity performance with injection of 2MHz sine wave
  - Low pedestal noise: RMS of 12 ADC counts.

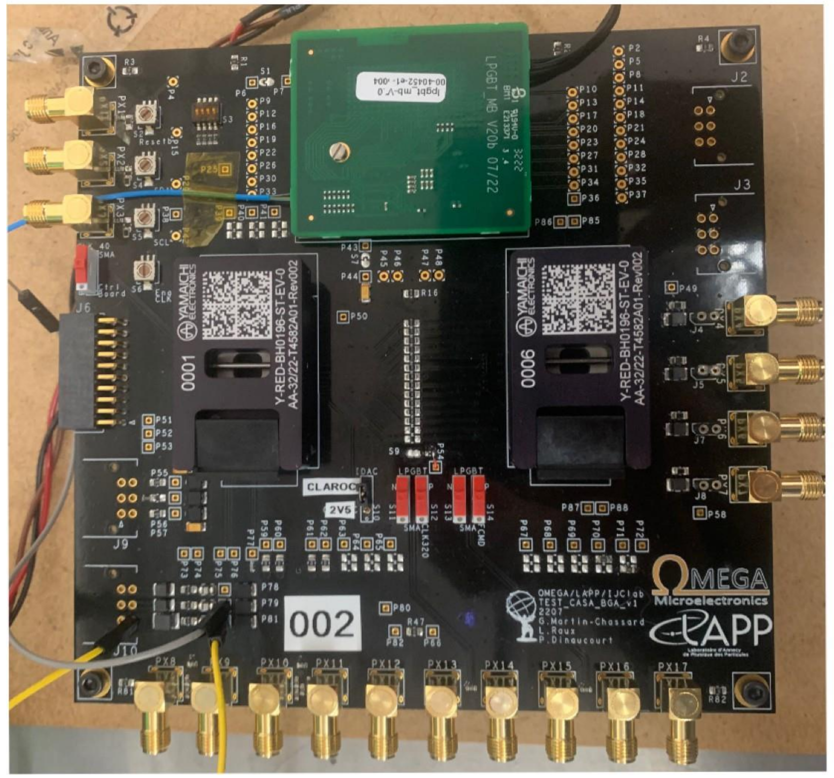
Both ASICs are **concluding** the **pre-production stage**, and **entering mass production**.

Preparation of setup for **automatic testing of the full production** in advanced stage!

Calibration Board

- The calibration boards inject **known** calorimeter **signals** at the LAr copper electrodes with **16-bit dynamic range** to **calibrate** read-out electronics.
- **128 boards** (with **128 channels** each) are needed to calibrate 182,468 cells!

LADOC / CLAROC test board



CLAROC custom ASIC

- **Creates pulse** by opening high frequency (HF) switch.
- Based on 180 nm HV-CMOS (XFAB) technology.   Needed to **cover full dynamic range**.

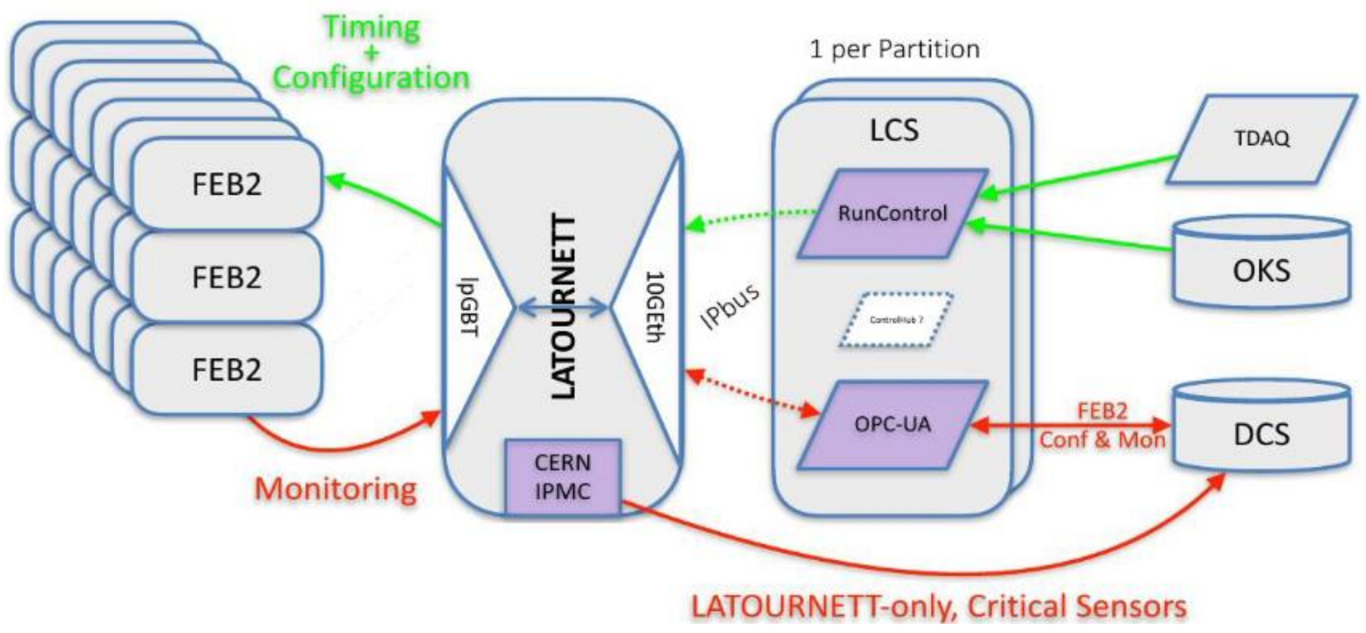
LADOC custom ASIC

- 16-bit **Digital to Analog Converter**, commands HF switch (based on 130 nm TSMC technology).

- Both ASICs in their current version (CLAROCv4 and LADOCv2) exceed **linearity requirements of a factor between 2 and 10!**
- Further radiation testing of ASICs is ongoing.
- Construction of second version of **full-scale board** (CABANEv2) **in progress**.
- Both ASICs **entering mass production**: LADOCv2b is the **final version**, now in mass production, while CLAROCv4b is submitted.

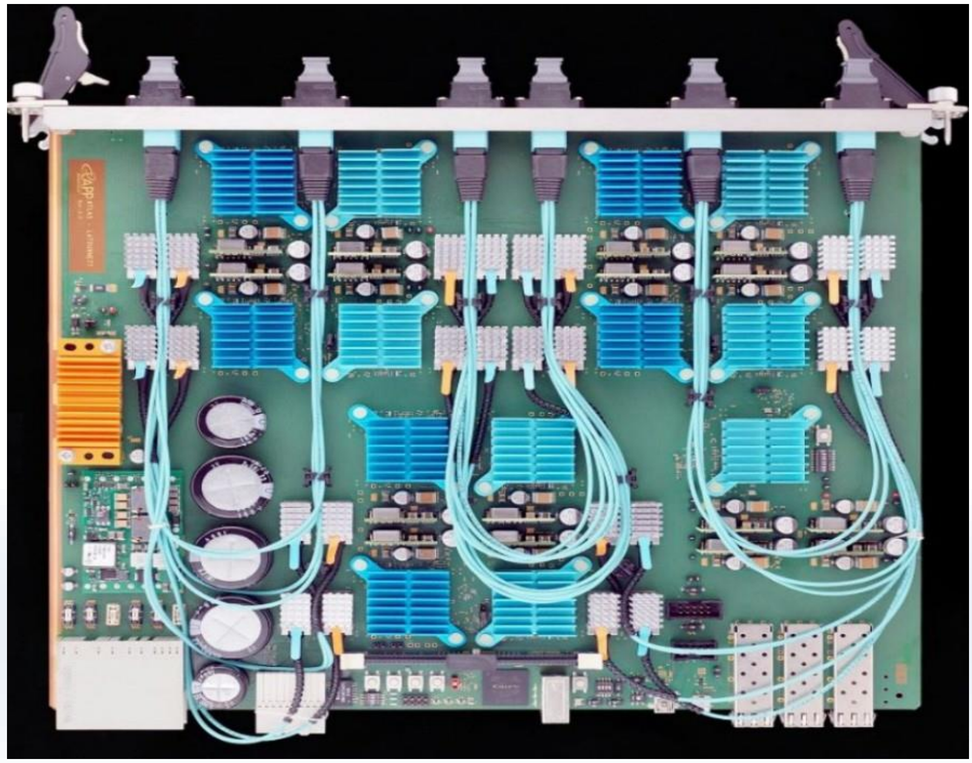
Off-detector electronics

LAr Timing System (LATS)



- The **LAr timing system (LATS)** handles Trigger, Timing and Control (**TTC) distribution, configuration, and monitoring** of the **FEB2** and **Calibration** boards, relying on **lpGBT protocol**.
- **30 LATOURNETT ATCA blades.**
  - Each equipped with **1 central + 12 array** Cyclone 10 GX **FPGAs**.
  - **Each controls 72 on-detector boards** with two dual links for redundancy

LATOURNETT v1



- First design of the board done and **two prototype** board produced. Several testbenches installed
- Proposed architecture for **integration** with **ATLAS TTC and TDAQ systems**.
- Several integration tests with FEB2 (+LASP) and Calibration board done.
- Fabrication of second prototype (LATOURNETT v2) **to start in early 2025.**
- **New integration tests** foreseen after the hardware becomes available.
- **Software and firmware development ongoing** with LATOURNETT v1 and FPGA devkits.

Lar Signal processor (LASP)

The LAr signal processor (LASP) applies **digital filtering** to waveform from the FEB2, calculates **energy** and **time**, and **transmits to TDAQ** systems.

- Considering **ML architectures** to implement in FPGA for **energy reconstruction**.

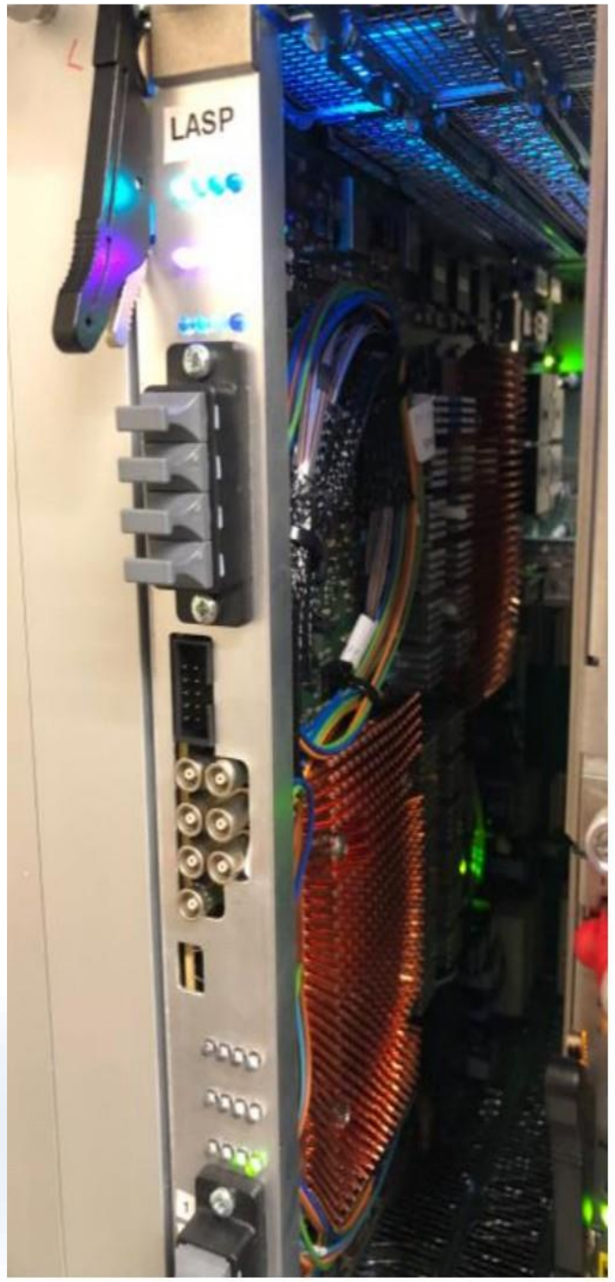
LASP ATCA board (main blade)

- Receives data from up to 6 FEB2s (= **768 channels**) using lpGBT protocol at 10.24 Gbps.
- Computes energy and time in real time (= for each LHC bunch crossing @40 MHz).
- **Sends output** to the trigger system **at 25 Gbps**.
- Data is buffered for 10 μs until a trigger decision is reached.
- Upon a trigger accept, data is sent to the DAQ system.
- Implemented using two **Intel Agilex** FPGAs per blade.

Smart Rear Transition Module (sRTM)

- Complements LASP main blade.
- Used for data transmission and TTC integration.

LASP test board



- A first set of test boards are produced, and are continuously running in test bench.
- **Regular monitoring** of **temperature**, **voltage** and **current** in place.
- Validated power, I^2C sensors, and FPGA configuration.
- Work ongoing on the firmware, aiming to **optimize** FPGA **resource usage** and **power** consumption.
- Prototype for LASP blades and sRTM being finalized (foreseen for end of 2024).
- **Long series of tests** in stand-alone and within the full system are foreseen for this year, to **verify TDR specs**!

Conclusion

- On-detector and off-detector electronics for the LAr Calorimeters are being re-designed, to cope with the challenges of data taking conditions at HL-LHC.
- All electronics will be replaced by 2029, and are designed to run throughout the full HL-LHC operation (~ 2041).
- Major progress on LAr Phase 2 upgrade:

FEB2

- Promising test results on FEB2 pre- prototype, and new full-size FEB2 prototype ready and now being tested.
- First large-scale integration test of the full readout chain is expected for Fall 2024.

Custom ASICs

- Custom ASICs meet / exceed specifications!
- ALFE2, COLUTA, CLAROC and LADOC ASICs now entering mass production.

Calibration board

Fabrication of second version of full-scale board in progress.

LATS

Fabrication of new LATS prototype to start in early 2025, then additional stand-alone and system integration tests are foreseen.

LASP

- Prototype for LASP blades and sRTM being finalized (foreseen for June 2024), and work on firmware ongoing.
- Long series of tests in stand- alone and within the full system to verify TDR specs.

On schedule for installation into ATLAS cavern after the end of Run 3!

Thanks for the attention