Technical challenges and performance of the new ATLAS LAr Calorimeter Trigger

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Agenda

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  - Signal
- Phase-I upgrade
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  - On-detector firmware
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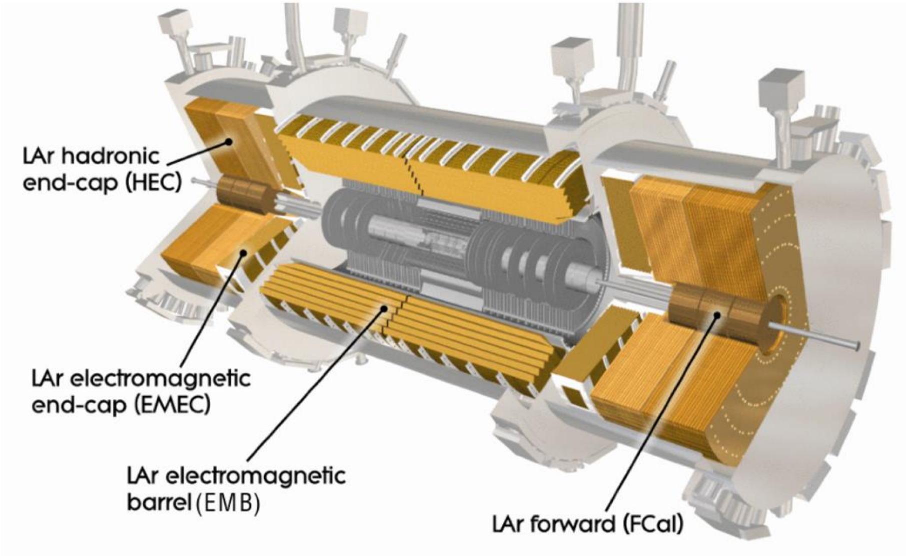
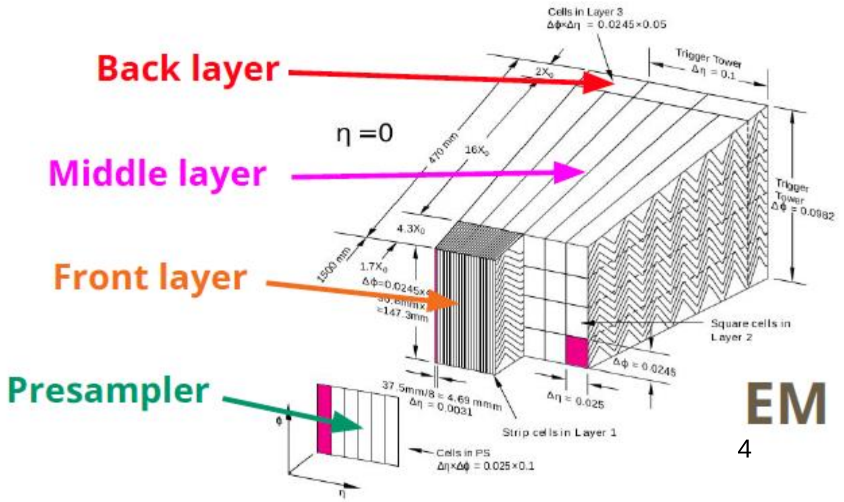
  - Digital trigger efficiency
- Summary

ATLAS Liquid Argon Calorimeter

ATLAS Liquid Argon Calorimeter

- **R&D** started in 1990 [1]
- **Sampling calorimeter** segmented in HEC, EMEC, EMB, and FCal
- **Active material** → Liquid Argon (LAr)
- **Passive material** → Lead (EM), Copper (HEC), Copper + Tungsten (FCal)
- Each segment consists of 4 layers (FCal → 3):
  - **Presampler (EM):** measure energy loss before calorimeter
  - **Front layer**: distinguish π^0 and γ
  - **Middle layer**: deepest, absorbs most of the EM shower
  - **Back layer** → catch the tail of EM shower
- 180k calorimeter cells, coverage **|η| <4.9**

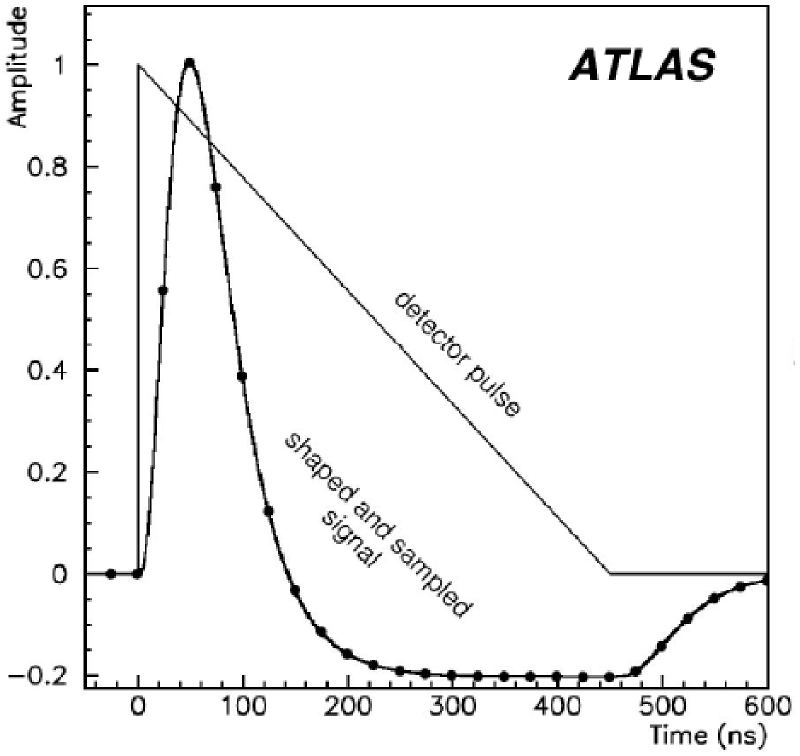




[1] ATLAS Experiment. 1996. "ATLAS Liquid-Argon Calorimeter : Technical Design Report." CERN-LHCC-96-041. *CERN Document Server*. CERN. https://cds.cern.ch/record/331061.

LAr Calorimeter Signal

- Signal formation based on the ionization of the **liquid Argon** triggered by passing particle
- Ionization current is produced by applying **high voltage** in the LAr gap (250-2500V)
- Particle shower produces **triangular pulse** signal that is amplified, shaped, and digitized in the front-end
- Energy is estimated from pulse **amplitude**, **calibration constants** and **optimal filter coefficients**



$$E_{\text{cell}} = F_{\text{DAC}\to\mu\text{A}} \cdot F_{\mu\text{A}\to\text{MEV}} \cdot \frac{1}{\frac{\text{M}_{\text{phys}}}{\text{M}_{\text{cali}}}} \cdot G_1 \cdot \sum_{i=1}^{N^{\text{samples}}} a_i\,(s_i - p)$$

- $F_{\text{DAC}\to\mu\text{A}}$: calibration board DAC to ionization current factor
- $F_{\mu\text{A}\to\text{MEV}}$: ionization current to energy conversion factor
- $\frac{\text{M}_{\text{phys}}}{\text{M}_{\text{cali}}}$: ionization to calibration pulse response
- G_1: gain
- $\sum_{i=1}^{N^{\text{samples}}} a_i\,(s_i - p)$: amplitude; a= optimal filtering coefficients, S= digitized sample, p= pedestal

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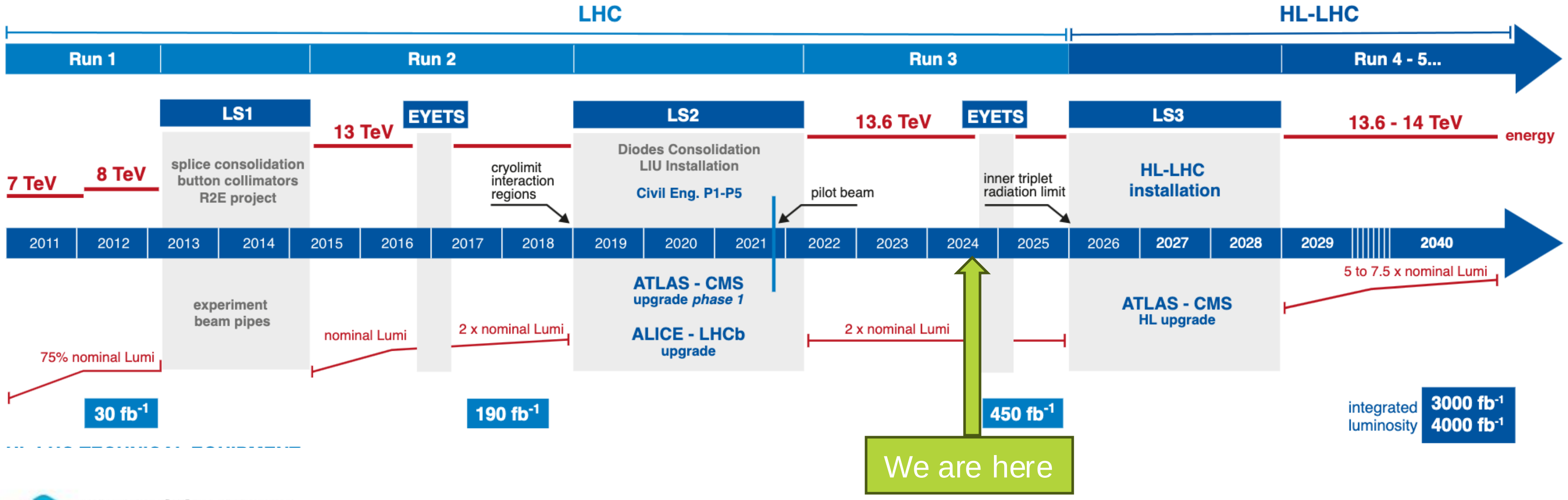
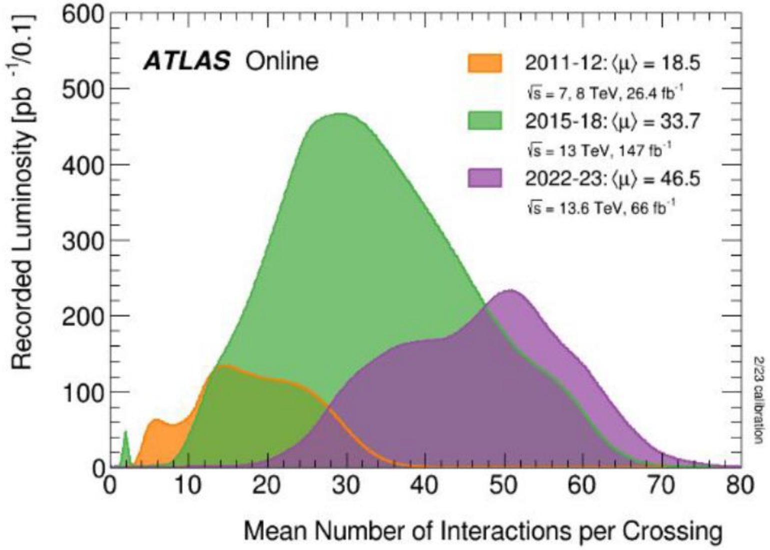
Phase-I upgrade

Outstanding results and upgrade motivation

- **First collisions** in 2010**, Higgs discovery** published in 2012 [1]
- **HL-LHC: increase luminosity** → higher chance to see rare events and improve measurements
- **Higher instantaneous luminosity** → More interactions per crossing (in-time pile-up)→ Trigger more selective to sustain maximum ATLAS L1 trigger acceptance rate of 100 kHz
- **New digital trigger system** implemented to address higher selectivity





[1] The ATLAS Collaboration. 2012. "Observation of a New Particle in the Search for the Standard Model Higgs Boson with the ATLAS Detector at the LHC." *Physics Letters B* 716 (1): 1–29. https://doi.org/10.1016/j.physletb.2012.08.020.

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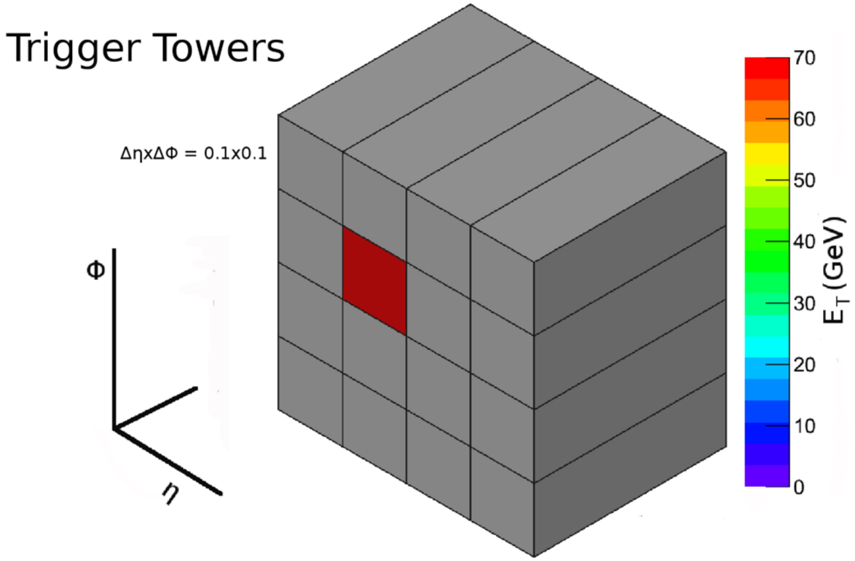
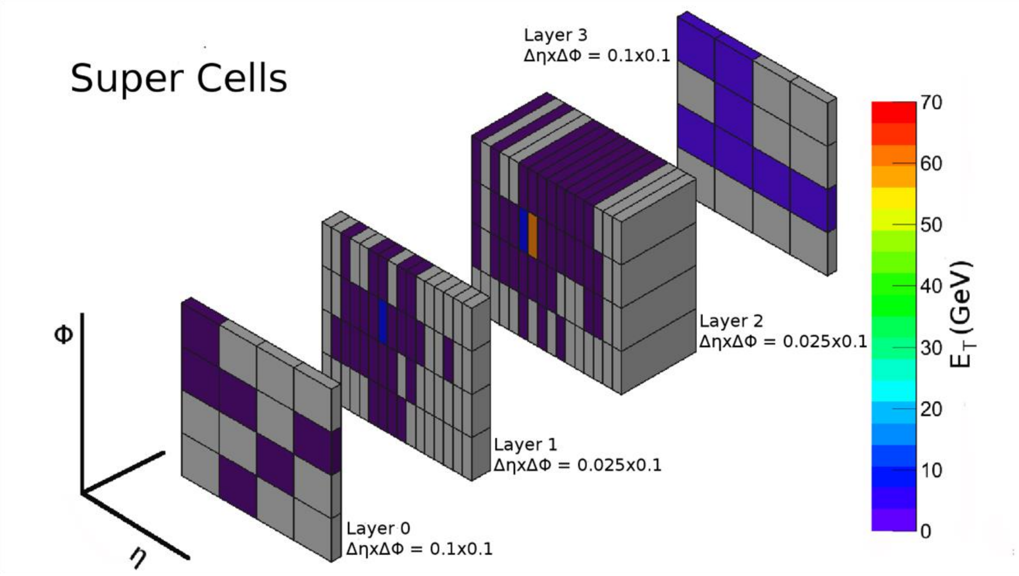
Granularity increase

- **Higher selectivity** achieved with **10-fold higher granularity** and **better segmentation** in the low-level trigger system [1]
  - **Legacy:**
    - 180k cells grouped into **5.4k Trigger Towers** ($\Delta\eta x \Delta\phi$ = 0.1x0.1) by summing analog signals
    - All 4 calorimeter layers summed together → **shower shape information lost** on low-level trigger system
    - **Analog signals** transmitted off-detector **using bulky parallel electrical cables** and **digitized on the computing room**
  - **Upgraded:**
    - 180k cells grouped into **34k Supper Cells** (Layers 1-2: $\Delta\eta x \Delta\phi$ = 0.025x0.1) by summing analog signals
    - Low-level trigger accesses shower shapes and higher granularity information
    - Analog sum **digitized on-detector** and transmitted off-detector using **optical fibers**
    - Preprocessing in the **digital domain** enables advanced signal processing techniques
  - Both systems are required to operate simultaneously during commissioning of digital trigger





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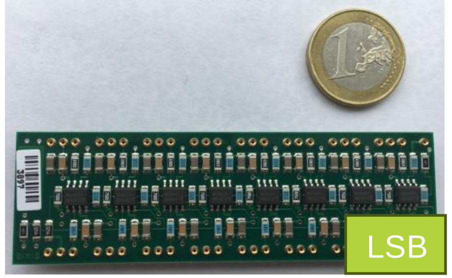
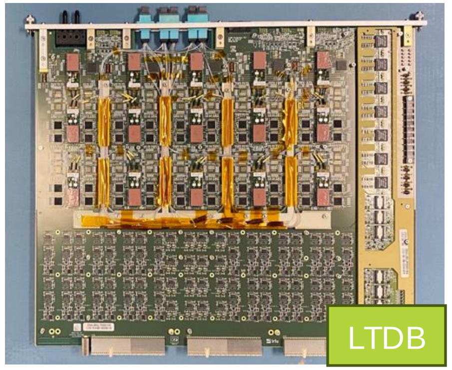
[1] Aad, G et al. 2022. “The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters.” *arXiv:2202.07384 [Hep-Ex, Physics:Physics]*, February. http://arxiv.org/abs/2202.07384.

On-detector electronics upgrade

- 114 new **Baseplane** cards:
  - Additional routing to allow concurrency for **digital** and **analog** trigger
- 2968 new **Layer Sum Board (LSB)** modules:
  - Provide **higher granularity analog sums** to digitizing system
  - **Plug-in** card for Front End Board, 6 different variants
- 124 new **LAr Trigger Digitizer Board (LTDB)** [1] modules:
  - Performs **shaping**, **sampling** and **digitization** of summed signals for up to **320 SCs**
  - **Custom-designed** 12-bit ADC at 40 MHz – 130nm TSMC process
  - Least significant bit → **150 (300) MeV** in Front (Middle) layer
  - Also generates legacy **Trigger Towers sums**
  - Serializes and transmits data from 8 SCs per fiber at **5.12 Gb/s**
  - Custom **LOCx2** high-speed transceiver and custom **LOCld** laser driver using 250 nm SOI process
  - Required to be operational for **HL-LHC** after exchange of power mezzanines





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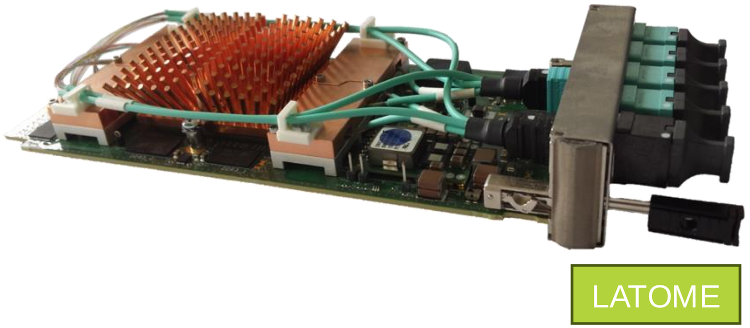
[1] Besin, Dominique, Heling Zhu, Massimo Lazzaroni, Stefan Simion, Hongbin Liu, Kai Chen, Herve Deschamps, et al. 2018. "Design and Evaluation of LAr Trigger Digitizer Board in the ATLAS Phase-I Upgrade." https://doi.org/10.1109/TNS.2019.2924795.

Off-detector electronics upgrade

- 30 new **LAr Carrier (LArC)** and **Rear Transition Module (RTM)**:
  - **Receive**, **deserialize**, **distribute**, and **propagate** timing, control and readout information
  - Based on AMD **Virtex 7 FPGA**, 22-layer Megatron-6 PCB, Texas CDCM6208 jitter cleaner
  - Hosts **IPMC** and **LATOME** mezzanine cards
- 30 new **Intelligent Platform Management Controller (IPMC)** for control and monitoring
- 116 new **LATOME** mezzanine cards:
  - **Receive**, **deserialize**, **decode**, and **align** SC information from LTDBs
  - Reconstruct **transverse energy** and identify respective **bunch crossing**
  - **Compress**, **encode**, and **serialize** energy values to L1Calo FEX systems
  - **Buffers** and send **configurable readout** information including **full-precision SC** data and **energy** value at Level-1 Accept rate (up to 100 kHz)
  - Based on the **largest Intel Arria 10 FPGA**, 16-layer Nelco 4800-20 SI PCB, and Broadcom 12-channel MicroPOD optical transceivers



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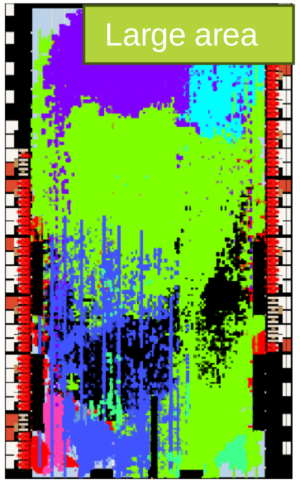
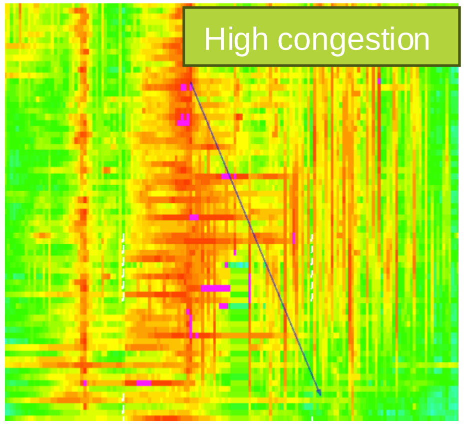
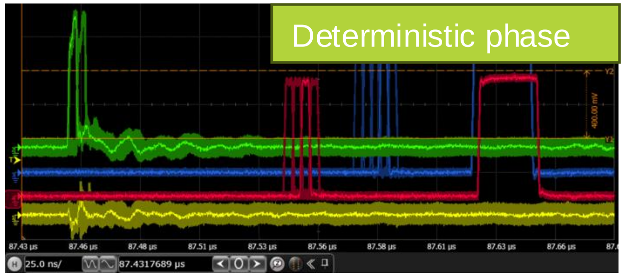
Off-detector electronics firmware

- Highly complex firmware requirements
  - Aggregate data processing rate of up to 250 Tb/s per LATOME card → **large area, high congestion**
  - Inputs running at 5.12 Gb/s and outputs running at 9.6 Gb/s and 11.2 Gb/s → **clock domain transfers**
  - Data needs to be aligned and combined to a single clock domain before processing → **deterministic phase**
  - Maximum latency allocation of 400 ns due on-detector memory buffer → **low-latency**
- First firmware version delivered in 2021 for the ATLAS Run 3 pilot run
  - Several **improvements over the time** such as pulse rate monitoring, baseline correction, robustness for clock switches, and more
- Firmware consolidated in 2024 and digital trigger used as default for Physics
- We are researching different architectures and tools to reduce logic area, latency, and easing timing closure
  - Leveraging **space** versus **time**-division multiplexing in different stages of the data processing
  - Adopting **High-Level Synthesis** for increased productivity and wider design space exploration
  - First HLS-based firmware upgraded being currently tested in ATLAS with collision beams







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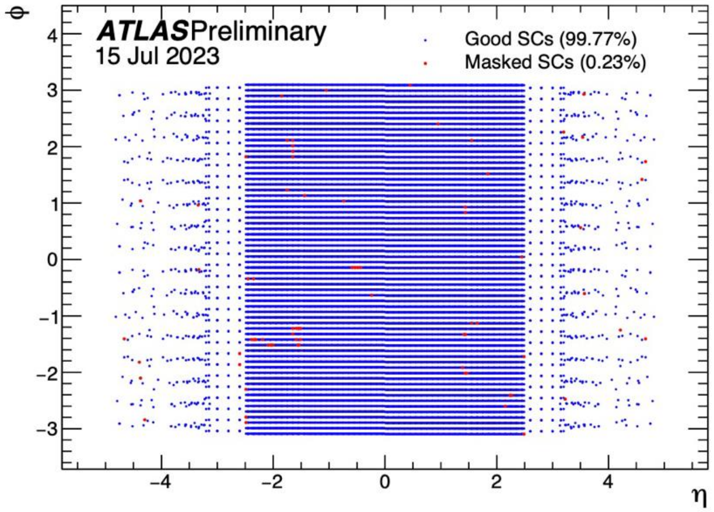
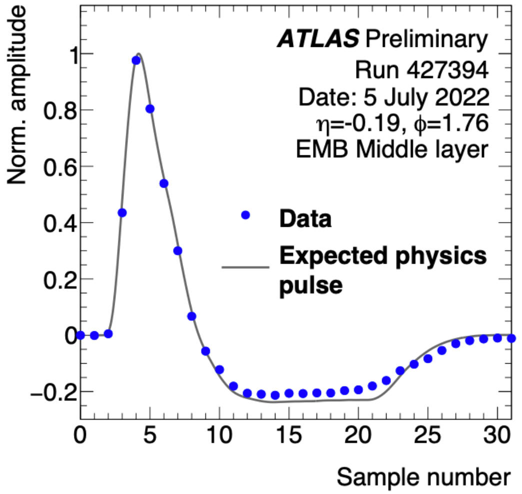
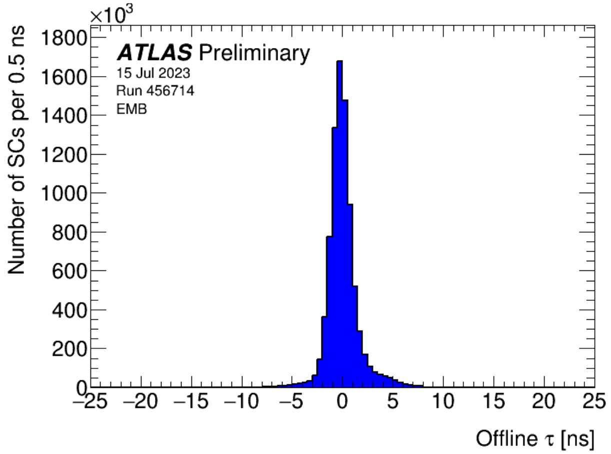
Performance

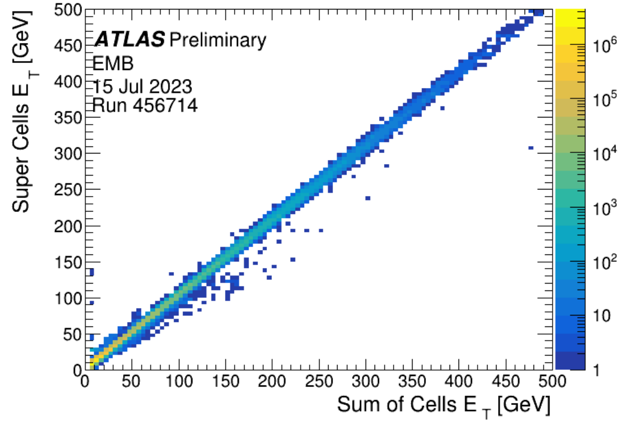
Super Cell Coverage and Pulse Shape

- More than 99% of SC coverage, only 0.23% masked → **more information used for trigger**
- Good agreement between SC pulse shape from readout data and the expected pulse shape from calibration → **distortions are compensated**
- Narrow peak timing distribution centered at zero → **avoiding early or late triggers**
- Super Cell energy agrees to energy from readout data (cell-by-cell) → **trigger uses accurate energy information**



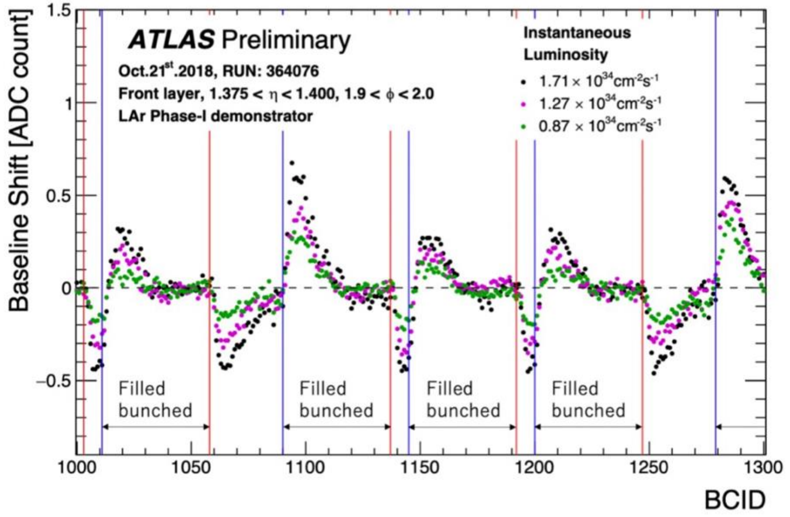


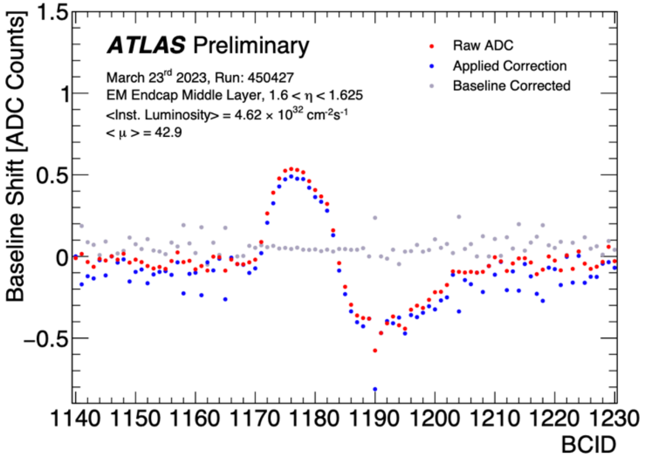




High-pileup environment challenges

- LAr pulses are longer than the bunch crossing period → **pulses overlap to each other (out-of-time pile-up)**
  - **Bipolar shape partially compensates it**
- Bunch structure contain gaps → **compensation is never perfect in particular at the start of the train**
- Baseline **per bunch crossing** over several LHC orbits computed to compensate for this shift
- Largest corrections are in the forward region and are up to 20 ADC counts





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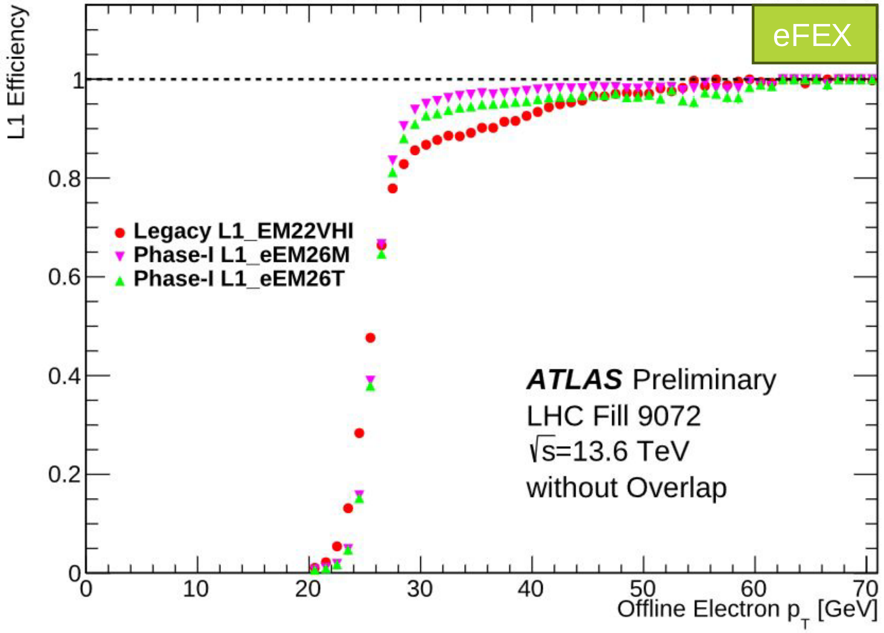
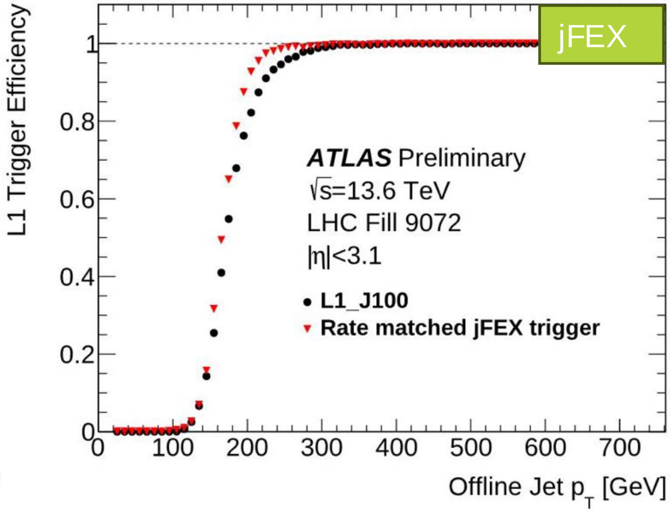
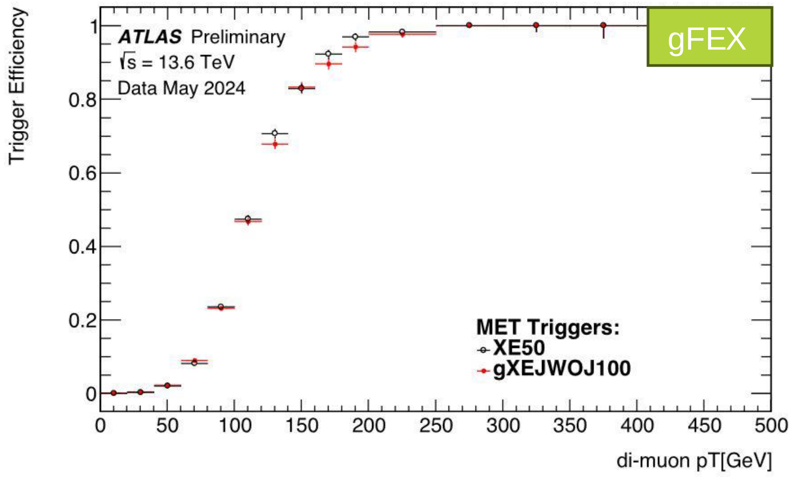
Digital Trigger Efficiency

- ATLAS low-level trigger now benefits from the increased resolution of the new digital trigger
- Decisions are made by Feature Extractors (FEX) of three types:
  - **eFEX (electromagnetic)** → e, γ and τ
  - **jFEX (jets)** → jets, τ and E_T^{miss}
  - **gFEX (global)** → large jets, ΣE_T and E_t^{miss}







- With the new current trigger:
  - **10% decrease** in the L1Calo rate for eFEX
  - **Comparable** rate for jFEX
  - Sharper turn-on curves → higher efficiency at the threshold

Summary

- The LAr collaboration designed, implemented, installed, and commissioned a major upgrade in the on-detector and off-detector electronics to cope with the increased pile-up conditions
- The new digital trigger system delivers energy information with 10-fold higher granularity and shower shapes are now available in the low-level trigger due to the layer segmentation
- Fully operational trigger and default for Physics since starting of 2024 and will remain in place for HL-LHC
- Thanks to remarkable work and commitment of the ATLAS LAr collaboration

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Thanks ;)