Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

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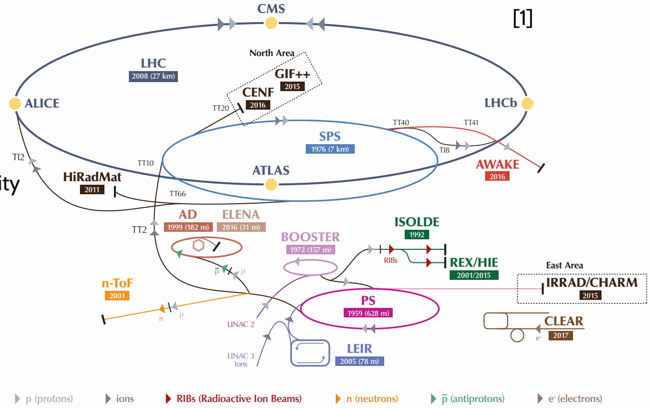
CERN Large Hadron Collider

- 27 km circumference collider
- Installed 100 m underground
- Proton-proton collisions:
  - 13.6 TeV of center of mass energy
  - Up to $2 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ instantaneous luminosity
- 4 large experiments:
  - ALICE
  - LHCb
  - CMS
  - ATLAS

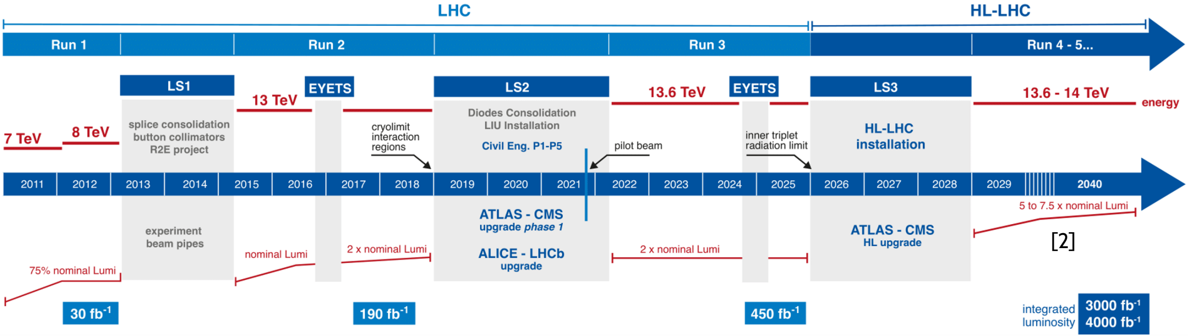
The CERN accelerator complex
Complexe des accélérateurs du CERN



LHC - Large Hadron Collider // SPS - Super Proton Synchrotron // PS - Proton Synchrotron // AD - Antiproton Decelerator // CLEAR - CERN Linear Electron Accelerator for Research // AWAKE - Advanced WAKefield Experiment // ISOLDE - Isotope Separator OnLine // REX/HIE - Radioactive EXperiment/High Intensity and Energy ISOLDE // LEIR - Low Energy Ion Ring // LINAC - LINear ACcelerator // n-ToF - Neutrons Time Of Flight // HiRadMat - High-Radiation to Materials // CHARM - Cern High energy AcceleRator Mixed field facility // IRRAD - proton IRRADiation facility // GIF++ - Gamma Irradiation Facility // CENF - CErn Neutrino platForm

CERN LHC Plan

- Currently, LHC is at the Run 3 stage
- The LHC program will be **extended** with a phase of **High Luminosity** (HL-LHC)
- Operating at an instantaneous **luminosity** around 7 times **larger** than nominal LHC
- This represents a significant challenge to the detectors $\rightarrow$ extensive set of upgrades
  - Need to cope with high **radiation** levels (inducing degradation of detector components) and high data-taking rates



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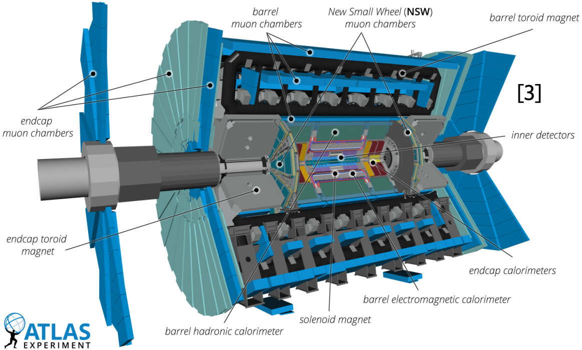
ATLAS Experiment

- Cylindric detector, 46 m long, 25 m diameter
- ATLAS studies the fundamental constituents of matter and the elementary forces
- Detect and measure the products of very high energy particle collisions
- To date, the main achievement was the discovery of the Higgs boson in 2012
- Different subsystems with various technologies allow measuring and identifying collision products:
  - Inner detector – track charged particle trajectories
  - Calorimeters – measure the energy of outgoing particles
  - Muon Spectrometer – detect muon track and energy
  - Magnet system – bend the trajectory of charged particles



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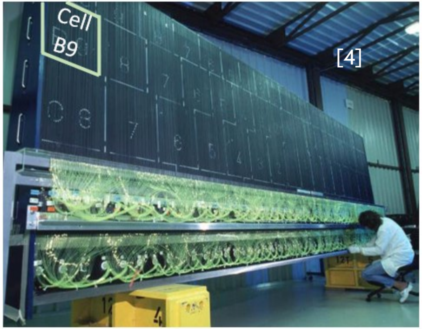
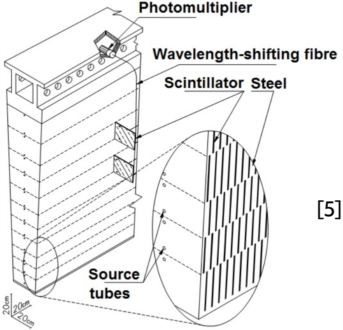
ATLAS TileCal Detector

- Central hadronic calorimeter covering $|z| < 612$ cm ($|\eta| < 1.7$)
  - Divided into 4 partitions (LBA, LBC, EBA and EBC)
  - Each partition is divided in azimuthal angle by 64 modules
- Measures the energy and direction of:
  - Hadrons and isolated muons
  - τ from hadronic decays
- Contributes to:
  - Missing transverse energy evaluation (to infer the presence of ν)
  - The detector trigger at Level 1 calorimeter stage
- Sampling calorimeter (interleaved in the proportion of 4.7:1):
  - Steel plates - absorber
  - **Plastic scintillator tiles** – active medium
- The **light** produced in **scintillators** is **collected** in two edges by **wavelength-shifting** (WLS) fibers
- The light is guided towards 9852 **photomultipliers** (PMT) by the WLS fibers
  - Each PMT reads a bundle of fibers connected to tiles - **cell**





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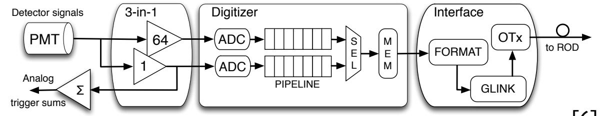
ATLAS TileCal Detector - Current Electronics

- TileCal electronics can be divided into On-detector (in harsh radiation environment) and Off-detector (outside of the detector cavern, out of radiation environment)
- **On-detector** electronics start where the fibers connect to the PMT block and are inside of the drawers
  - Two consecutive drawers make a Superdrawer, comprising:
    - The PMT block → light mixer, PMT, passive HV divider, 3-in-1 card:
      - Each 3-in-1 card shapes and amplifies the PMT analogue signal
    - Motherboard → Digitizer and Interface board
      - The Digitizer is responsible of digitization of analog signals from up to six 3-in-1 cards
      - The interface board distributes Trigger-Timing and Control (TTC) signals and transmits formatted data to back-end electronics → one per Superdrawer
- **Off-detector** electronics correspond to the readout drivers (RODs) that collect digitized information from the Interface card, format the data and send it to the readout buffers for processing by the Level-2 trigger



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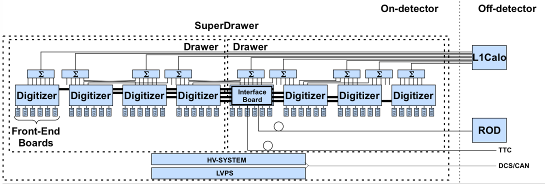
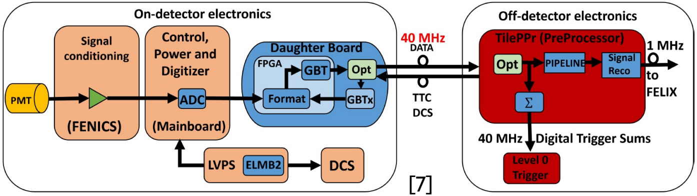


Upgrade Phase II - Overview

- As pointed out before, the condition during the HL-LHC will challenge the detector components with a high radiation environment and higher pile up from 60 to 200 collisions per bunch crossing
- The current readout architecture is not compatible with the new TDAQ system of ATLAS and with the timing requirements for trigger and data flow
- TileCal team is getting ready for the HL-LHC:
  - New **mechanical frames** (MiniDrawers) housing the new on-detector electronics
  - **Replacement** of ∼10% of the **PMTs**
  - Full **replacement** of both On/Off-detector **electronics**
  - Make the **digital trigger** readout at 40 MHz for all channels
  - Improve High and Low Voltage **power systems**
  - **Upgrade** Cs and Laser **calibration systems**



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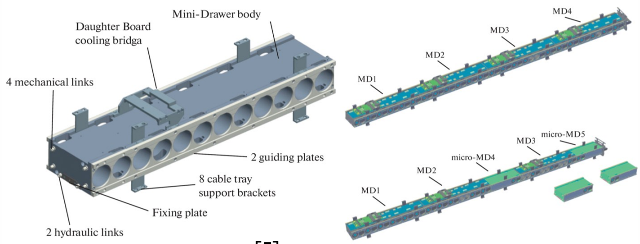
Upgrade Phase II - Mechanics

- Current TileCal drawers are difficult to extract for maintenance
- For the upgrade, smaller drawers will be equipped → MiniDrawers (MD) already produced
  - 4 MD for Long Barrel modules → 45 PMTs
  - 3 MD for Extended Barrel modules → 32 PMTs
- There are 7 different types to accommodate the different geometries in the extended barrel
- There will also be a tool for inserting/extracting the drawers easily



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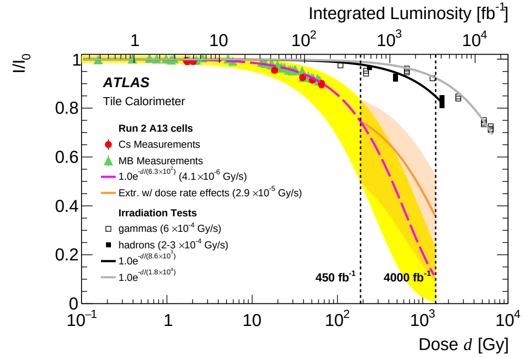
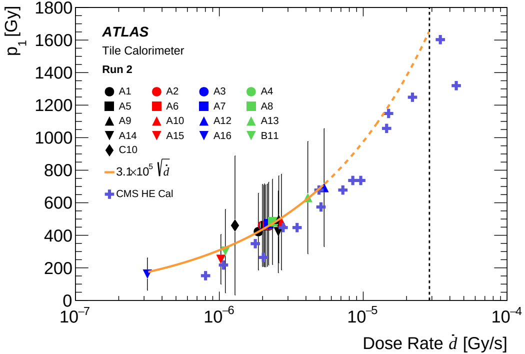
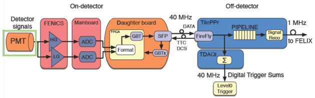
Radiation Hardness of Scintillator and WLS fibers for HL-LHC

- Studies on TileCal optical materials have been performed
- During the HL-LHC, the dose rate will increase around 7 times more than during Run 2
- The **higher** the **dose rate**, the **lower** the **degradation** for the same dose
- The response of **scintillators and fibers decreases** with the **radiation** exposure
    - One of the **most exposed cells** is estimated to have a relative light output of 40% at the end of the HL-phase

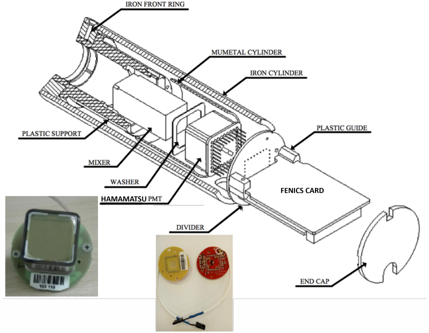




Upgrade Phase II - Photomultipliers



- Even if at the end of the HL-LHC we face some light output loss, the new PMTs (Hamamatsu R11187A), with better quantum efficiency, can mitigate the lower response from the optical components
- Dedicated test benches are being used at Bratislava, Pisa and CERN laboratories to test all the new PMTs (all produced)
- All PMTs will be connected to HV active dividers to provide better response stability at high anode currents
- For the upgrade, it is expected to replace about 1000 (10%) PMTs for the cells that present the most significant degradation



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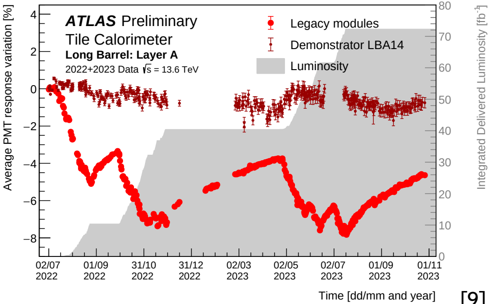

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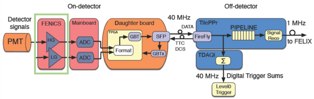
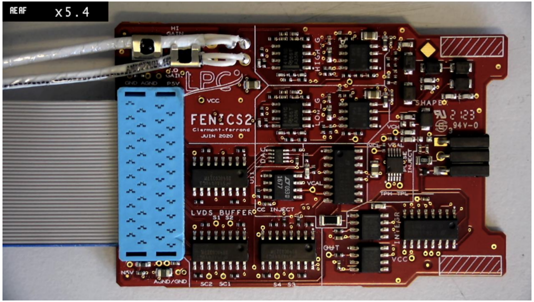
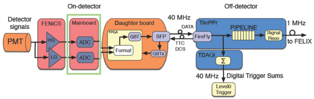
Upgrade Phase II - FENICS Card



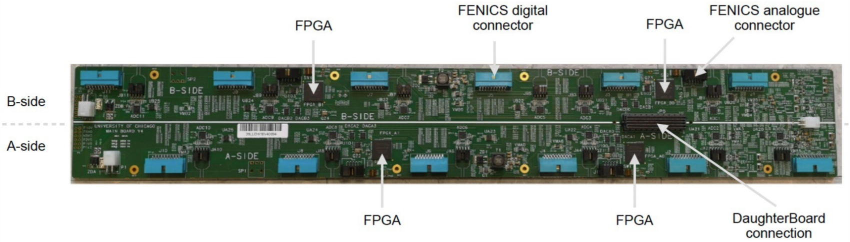
- FENICS stands for **F**ront **E**nd board for the **N**ew **I**nfrastructure with **C**alibration and signal **S**haping
- 9852 FENICS cards will replace the 3-in-1 cards to amplify and shape the analogue signal of the PMT pulse
  - Provide PMT pulse shaping with 2 gains amplifications - Low Gain $\times$ 0.4 and High Gain $\times$ 1.6 from 0.2 pC to 1000 pC dynamic range
  - With a current integration with 5 gains for ^{137}Cs calibration and for luminosity measurements
  - Built-in Charge Injection system for ADC calibration



Upgrade Phase II - Mainboard



- One Mainboard will be installed in each MiniDrawer
- The Mainboard receives and digitises the analogue signals from 12 FENICS cards:
  - 12 bit dual ADCs at 40 Msample/s for 2 gain signals
  - 16 bit ADC at 50 ksample/s for integrated signals readout
- Provides digital control and configuration of FENICS through the FPGAs and transmits data to the Daughterboard at high speed
- Responsible for independently, on each side, distributing the low power to the Daughterboard and FENICS
- All Mainboards are already produced



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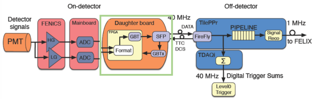
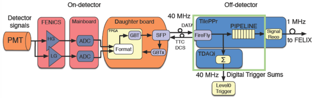
Upgrade Phase II - Daughterboard

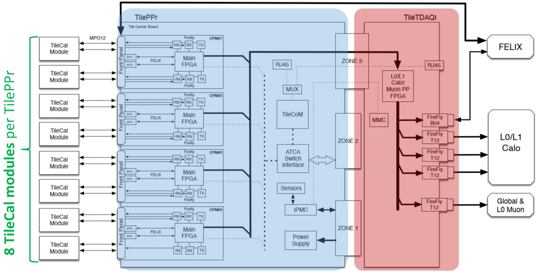


- The Daughterboard is the readout link and control board interconnecting the On and Off-detector electronics
- It uses optical links for data transmission
- It collects the digitised data from the Mainboards and sends it to the TilePPr
- Each side provides control and readout services for 6 PMTs (for redundancy)
- Receives and distributes LHC synchronised clocks, configurations and slow-control commands
- The Daughterboard has been submitted to NIEL, TID and SEE radiation tests

Upgrade Phase II - Off-detector



- The Off-detector electronics will be provided by the Tile PreProcessor (TilePPR) and the TDAQi system
- Responsible for processing, handling and reconstructing real time data
- Storage of up to 10 μs of consecutive data samples in pipeline memories
- Provide configuration and clock distribution to TileCal modules
- Will serve as the ATLAS trigger
- Will be used for data readout through ATLAS common system →FELIX interface



- One TilePPr is formed by 1 ATCA carrier, 4 Compact Processing Modules (CPM), 1 Tile Computer-on-Module (TileCoM) and one GigabitEthernet (GbE) switch → 32 TilePPr in total
- One CPM receives data from 2 TileCal modules (8 Mini drawers) in total, there will be 128 CPM
- 32 TDAQi will be required for the interface with L0Calo, L0Muon, Global and FELIX system

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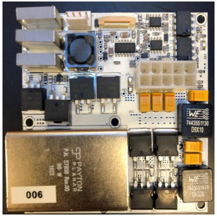
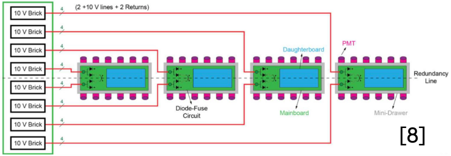
Upgrade Phase II - Low and High Voltage



Low Voltage

- The 200V DC modules input will be converted to 10V DC (LVPS bricks) and the usage of point-of-load regulators will control it to the operational voltages of the On-detector electronics
- These devices meet strong constraints in terms of radiation tolerance, noise, power efficiency and reliability
- Two bricks connected to each MainBoard



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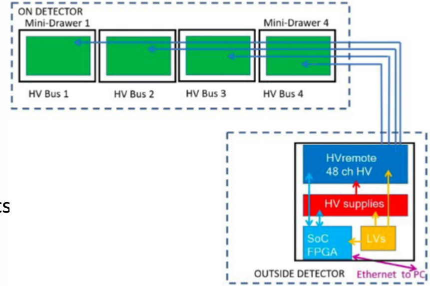
High Voltage

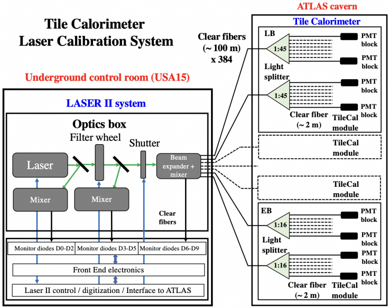
- New HV power supplies and regulators will be installed outside the cavern
- New 100 m long HV cables for each PMT will be installed
- HVremote board will set the high voltage to individual PMTs
- This will allow easier maintenance and no radiation constraints for electronics



Upgrade Phase II - Calibration Systems

Laser system:

- New TDAQ interface and control electronics board →ILANA
- New optical line with new integrating sphere for mixing LASER light and light from new LED matrix to simulate pile-up



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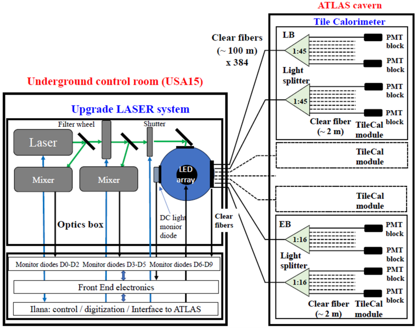
Cesium source calibration system

- The On/Off-detector electronics will be replaced
- New hydraulic system under study



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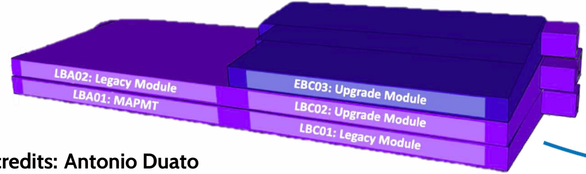
Upgrade Phase II - Test beam at the SPS

- Several test beam campaigns have been performed at CERN since 2015
- Two upgraded modules with new On and Off detector electronics are currently installed in the test beam area
- In the test beam, it is possible to use
  - different beams → hadrons, electrons and muons
  - different energies
  - different angles of incidence
- Main goal: performance studies and validation of the hardware data
- The 3 Cherenkov counters are used to identify the particles in the beam



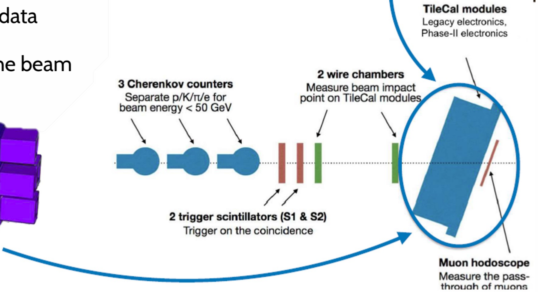
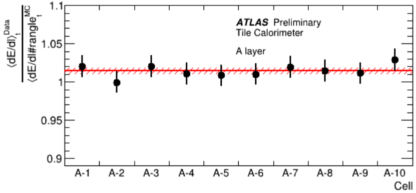


Image credits: Antonio Duato

Upgrade Phase II - Test Beam Results

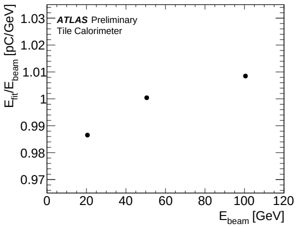
Muons

- 165 GeV Muons were used to study the layer uniformity since their deposited energy is a function of the path length in each cell
- Results show a layer uniformity within 1% with a maximum deviation of 1.4% and very good agreement between data and simulation for all the layers



Electrons

- For electron beam with different energy were used to determine the calorimeter response at the EM scale → calculating the pC/GeV
- The linearity of the calorimeter response was checked for electron beam with 20, 50 and 100 GeV



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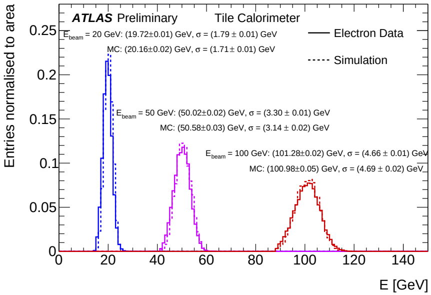
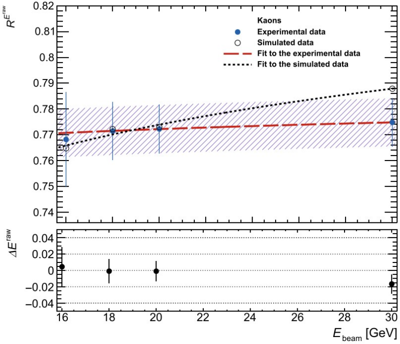


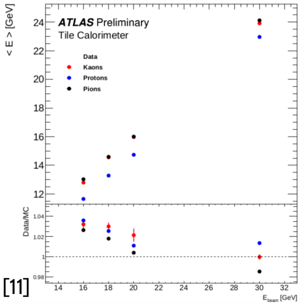
Upgrade Phase II - Test Beam Results

Hadrons

$$R^{E^{Raw}} = \frac{\langle E^{raw} \rangle}{E_{beam}} \quad \Delta\langle E^{raw} \rangle = \frac{\langle E^{raw} \rangle}{\langle E^{raw}_{MC} \rangle} - 1$$

- The response to isolated hadrons is important to validate and improve the modelling for jet and τ measurements in ATLAS
- Results for kaons are dominated by statistical errors, while, for pions, electron contamination plays an important role
- For the measured response as a function of the energy beam, the response is larger for pions and kaons than for protons





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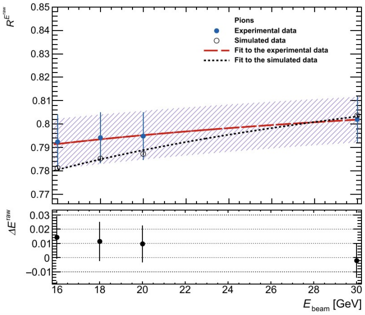

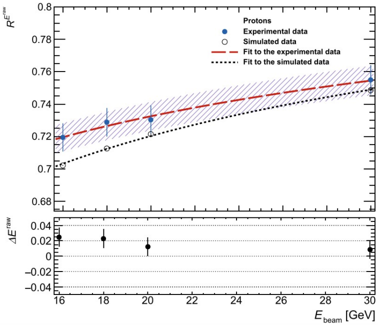

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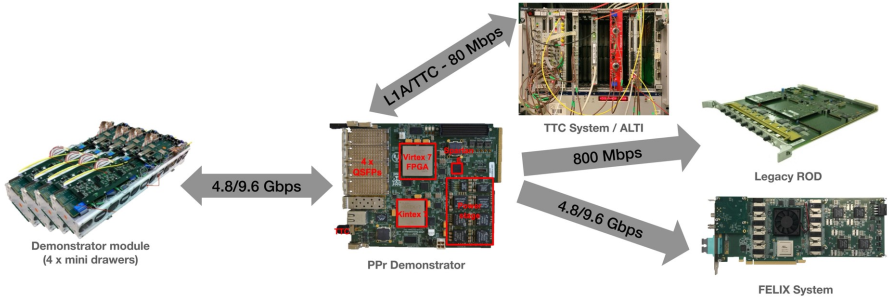
Upgrade Phase II - Demonstrator in TileCal

- A hybrid electronic module was inserted in TileCal (2019)
- It is backward compatible with the current TDAQ system (legacy RODs at 800 Mbps) and Phase-II system (FELIX at 4.8/9.6 Gbps)
- Very useful complement to the testbeam to prepare and learn about the new electronics and identify problems
- This module has good performance with low noise levels wrt legacy modules



Summary and Conclusions

- The High-Luminosity phase will bring new challenges, such as higher radiation environment, pile-up and readout rates
- The TileCal team has been working on solutions to satisfy these new requirements:
  - Replace all On/Off-detector electronics and $\sim$10% of the PMTs during the long shutdown (2026 to 2028)
    - On-detector eletronics with better radiation hardness
    - Faster Off-detector electronics that will be able to have 1 MHz output rate compared to the current 100 kHz
    - PMTs with higher quantum efficiency and better stability
  - A new and easier to use mechanical structure
- The test beam campaigns have been and will continue to be useful to validate the developments of the new designs and to study the performance of the new components
- The hybrid TileCal module (demonstrator) is fully integrated with the current ATLAS TDAQ and DCS system and is taking data with good performance

Thank you

References

[1] cds.cern.ch/record/2636343?ln=fr, Accessed: 2024-07-31.

[2] hilumilhc.web.cern.ch/content/hl-lhc-project, Accessed: 2024-08-05.

[3] cds.cern.ch/record/2900788.

[4] A. Solodkov, ***The atlas tile hadronic calorimeter production, calibration and performance*,** LHC Days in Belarus 2018 Workshop.

[5] A. Collaboration, ***Technical design report for the phase-ii upgrade of the atlas tile calorimeter*,** 2018.

[6] twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileElectronics.

[7] ep-news.web.cern.ch/content/atlas-tile-calorimeter-phase-ii-upgrade-entering-production-phase.

[8] indico.cern.ch/event/1339557/contributions/5929092/attachments/2859744/5003108/HW20240521-Calor-wide.pdf.

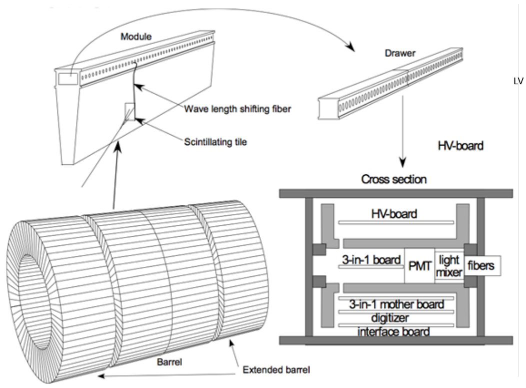
[9] twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileCalibrationLaser.

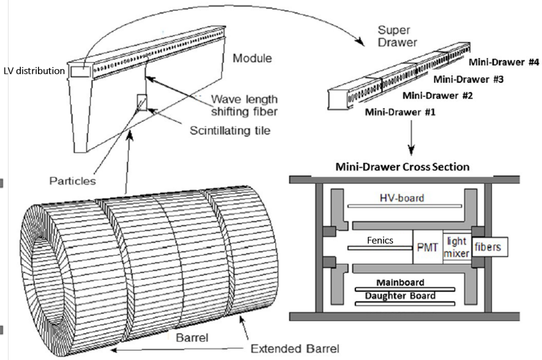
[10] indico.cern.ch/event/1264216/contributions/5548227/.

[11] twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTileTestBeamResults.

[12] J. Abdallah, S. Angelidakis, G. Arabidze, *et al.*, **"Study of energy response and resolution of the atlas tile calorimeter to hadrons of energies from 16 to 30 gev,"** *The European Physical Journal C*, vol. 81, no. 6, pp. 1–18, 2021.

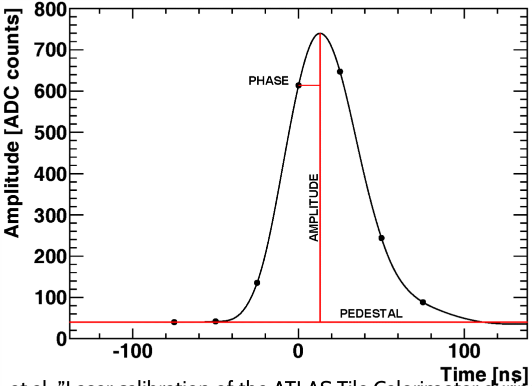
Overview on-detector





Signal Reconstruction

- The signal from the PMT undergoes shaping and is sampled (7 samples) every 25 ns
- To reconstruct the signal, the amplitude (proportional to the energy), the phase and the quality factor are determined
- The Optimal Filter is used for both for calibrations and physics runs



Agaras, M. N., et al. "Laser calibration of the ATLAS Tile Calorimeter during LHC Run 2." Journal of Instrumentation 18.06 (2023): P06023.

Mainboard

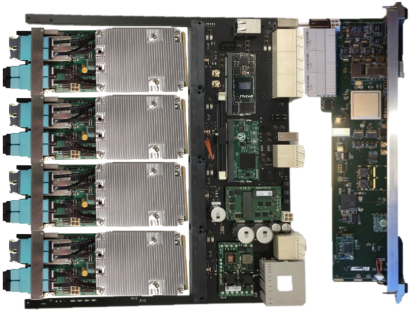
- The Mainboard is also responsible for distributing 10 V for each side independently to improve reliability
- It is divided into 4 groups, each with one FPGA that serves as a communication hub between FENICS and Daughterboard
- The PMT signals from FENICS are parallel digitised by a dual 12 bit 40 Msps ADC that are sent to the daughter board via two-bit serial bus at a speed of 560 Mbps (14 bit 40 Msps)
- All Mainboards were already produced

Daughterboard

- Collects the digitised data from the Mainboard
- It is connected to the Off-detector (TilePPR) via multi-gigabit optical links (4.8 Gbps)
- The data transmissions to PPR are at a rate done over 9.6 Gbps
- Redundant optical fibers and electro-optic modules are used for protection against single-link failures for each side independently

Tile PreProcessor

- The TilePPr needs bi-directional communication
  - Uplink to transfer the detector data to the PPr (higher bandwidth than downlink) → 4096 each at 9.6 Gbps
  - Downlink to transmit the LHC clock and control and configuration commands → 2048 each at 4.8 Gbps
- The Carrier Base Board distributes power to up 4 Compact Processing Modules (CPM)
- Interface and monitoring with ATLAS DCS system via TileCoM
- Allows the communication of CPM and TDAQi
- Each CPM is able to process the data from 8 MiniDrawers (2 Tile modules) → clock distribution, operation and readout
- Online energy and time reconstruction at 40 MHz per channel
- Triggers selected events to FELIX at 1 MHz
- GbE switch provides communication to all components in the board
- 32 PPr will be needed to readout the entire detector

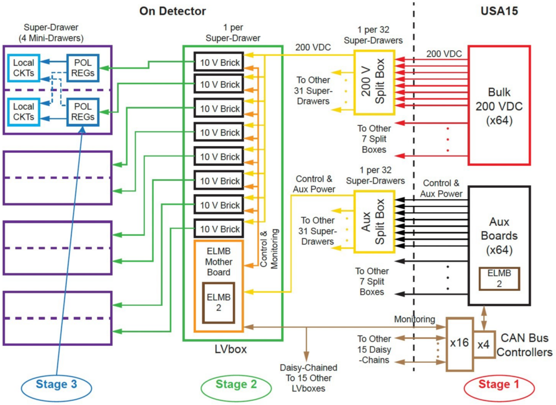


TDAQi

- The TDAQi interfaces the trigger and ATLAS DAQ
- Receives cell calibrated energy and time for every bunch crossing through low latency links
- Processes and transmits trigger primitives to the ATLAS Trigger system
  - Uplink to transfer the detector data to the PPr (higher bandwidth than downlink) $\rightarrow$ 4096 each at 9.6 Gbps
  - Downlink to transmit the LHC clock and control and configuration commands $\rightarrow$ 2048 each at 4.8 Gbps
- The Carrier Base Board distributes power to up 4 Compact Processing Modules (CPM)
- Interface and monitoring with ATLAS DCS system via TileCoM
- Allows the communication of CPM and TDAQi
- Each CPM is able to process the data from 8 MiniDrawers (2 Tile modules) $\rightarrow$ clock distribution, operation and readout
- Online energy and time reconstruction at 40 MHz per channel
- Triggers selected events to FELIX at 1 MHz
- 32 PPr will be needed to readout the entire detector

Low Voltage

- The Bulk distributes 200 V DC power to the LVPS Brick
- The Brick converts the high voltage and low current into low voltage (10 V) needed by various circuits in the front-end electronics
- The ELMB interfaces the LVPS Bricks with the Aux board/CAN Bus controller
- The CAN Bus tunes the output voltage and monitors the input and output currents and voltages but also the Bricks temperature
- The Auxboards provide auxiliary power and send control signals to LVPS



High Voltage

- The high voltage power supply control system must provide high voltage to all PMTs, control the settings for each tube individually and monitor the applied voltage reporting them to the Digital Control System
- The HV Bus is responsible for distributing the HV to the PMTs (up to 12 PMT each (896 in total))
- 100 meters long cables will connect the HVremote board to the HV Bus (256 units)
- The HV remote board are responsible for regulating and control the the HV supplied by the HV module (256)