LHC Upgrades

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Overview

- Motives for upgrades
- Requirements for machine
- Timing
- Changes to the experiments
 - limited time, so selected "highlights"
 - omitting ALICE (apologies!)

- There is now a lot of material on upgrade plans
 - talks, proposals, official documents,... available for consultation

Motives for upgrades

- No shortage of physics yet to be discovered
 - when it is, the detailed ATLAS/CMS objectives should be much more precise
 - meanwhile strongest arguments are for increasing sensitivity by adding statistics
 - LHCb hopes to characterise NP by (greater) precision measurements
- LHC operational conditions becoming clearer
 - about half the integrated luminosity to 2020 will be delivered at twice the design value, possibly with 50ns bunch spacing
 - detectors were not designed for this (remember LHC was a challenge!)
- Age and experience go together
 - real detectors will be imperfect and may degrade
 - technology is constantly improving and performance can be enhanced
- Profit from the huge investment over more than two decades
 - obvious that future developments will be equally lengthy and challenging

Physics goals of sLHC

Main ATLAS Physics goals:

Higgs discovery: Mass and understanding electro-weak symmetry breaking

Unification of forces, gravity, SUper SYmmetry, extra dimensions

New forces (W', Z')

Flavour: why 3 families, neutrino mass, dark matter

Whatever is discovered at the LHC will need a lot of data to understand exactly what has been discovered: characterising the discoveries.

In addition, the sLHC can extend the discovery potential, to higher masses or lower cross-sections. While the LHC aims at ~300 fb⁻¹ per experiment, the sLHC aims for 3000 fb⁻¹ of data, opening up new possibilities for channels limited by statistics at the LHC

There are many measurements where extending the LHC data set is important, including:

- 1. Higgs couplings
- 2. Triple gauge-boson couplings
- 3. Vector boson fusion at ~1 TeV
- 4. SUSY discovery or spectroscopy
- 5. New forces: W', Z' to higher limits

SLHC Physics: Extra gauge bosons



J. Nash CMS Upgrade Plans 8 March 2011

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SUSY searches - measurements

Here we need a lot of Integrated Luminosity, but needs to be high quality. Lower pile-up may be important.

- SLHC statistics will be vital in reaching understanding of complicated SUSY channels
 - Sparticles seen, but statistics for reconstruction limited at LHC
- Performance of the detector here is vital
 - B-tagging
 - Lepton id



LHCb $B_s \rightarrow \mu^+ \mu^- Roadmap$

Will take Upgrade to reach SM sensitivity



Objectives for the accelerator

- Increase the energy and luminosity to the design values
 - should be achieved after 2013 shutdown
- Further increase the luminosity to about twice design level
 - following a second shutdown around 2017
- Still some uncertainties about how this will be achieved
 - 25ns or 50ns bunch spacing? N_p /bunch, electron cloud, no. bunches, ...
 - what new machine challenges remain to be overcome?
 - imperfections and reliability
- but now building on very promising early performance demonstrating how well the LHC design is delivering
 - emittances, β^* , steady progress in extending performance
- Long term goal, after 2021
 - Run to ~2030 and provide 3000 fb⁻¹ with ~ $5x10^{34}$ cm²s⁻¹ levelled luminosity

Draft 10 year plan

[Outcome Chamonix 2011 presented @ LMC 81 - draft]



ACES 2011 Workshop, CERN, March 2011

Oliver Brüning BE-ABP

Summary Performance Reach:

Performance Reach of the LHC

-Existing LHC & injectors can reach nominal performance with 25ns and 50ns beams: $L = 1 \ 10^{34} \text{ cm}^{-2} \text{ sec}^{-1}$

-Small emittance option with 50ns operation can reach: $L = 1.7 \ 10^{34} \ cm^{-2} \ sec^{-1}$

@ half nominal total beam current for 50ns beam option -Nominal machine with LINAC4 and 50ns operation can reach: $L = 2.5 \ 10^{34} \ cm^{-2} \ sec^{-1}$

with approximately nominal total beam current

-Full upgrade can reach:

 $L \ge 5 \ 10^{34} \ cm^{-2} \ sec^{-1}$

with geometric reduction factor!

→ CC & LRBB wires are ideal tool for leveling!

Implications for the experiments

- In this decade pile-up could be x2, or even x4 at 50ns, worse than designed for
 - experiments are just beginning to encounter multiple events/crossing
 - tracking performance, calorimeter isolation for trigger, forward detectors
- Next decade requirements
 - higher granularity
 - greater radiation tolerance
 - improvements to trigger to constrain L1 rate
 - rejuvenation of accessible detector components, eg electronics
 - longevity of existing detector systems which can't change much
- Constraints
 - experiments can't be rebuilt and not complete freedom to adapt
 - eg L1 latency, energy deposited in LAr, access to interior of experiments

Example of a constraint: CMS YB0



Power cables, optical fibres, cooling pipes on surface of solenoid vacuum tank. Major restrictions on access to interior and VERY long time needed if services were to be dismantled and redone.

Schedule

- Three main steps for CMS and ATLAS
- 2013 shutdown
 - mainly consolidation for high luminosity & 14 TeV, esp muon systems
 - possible installation of new beampipe(s) and ATLAS inner pixel layer
- 2017 shutdown
 - completion of any high lumi consolidation
 - new beampipes, reducing radius if not done earlier
 - CMS pixel replacement, L1 trigger upgrade, HCAL photosensors, DAQ,...
 - ATLAS forward calorimeter, muon upgrades, DAQ,...
- 2021
 - replace tracking detectors with new systems
 - trigger upgrades
 - other improvements to muons, calorimeters, electronics, DAQ

Pixel detector upgrades

- Being so close to the beam, radiation damage was expected to degrade innermost layers within first decade
 - CMS pixels are removable to permit replacement or repair
- Exceeding L= 10³⁴ degrades performance
 - buffer depth of inner layers is limited, which leads to inefficiency
- ATLAS
 - insert inner layer with smaller pixels, aiming for 2013
 - choose between 3D silicon, planar silicon or diamond pixel sensors
 - new 130nm FE ROC is at an advanced stage
- CMS
 - replace whole detector with more layers but less material in 2017
 - new cooling, power and data links required
 - extend buffers in ROC but keep existing design (0.25µm CMOS)



IBL Detector





System overview



a fatter and	Value	Units
Number of staves	14	
Stave length	706	mm
Modules per stave	16	
Pixel size (phi, z)	50×250	µm²
Module active size	40.8×20.4	mm²
Coverage in η	η < 3.0	degree
IBL nominal radius	33.25	mm
IBL outer envelope	38.3	mm
IBL inner envelope	31.0	mm
Stave tilt angle	14 degree	
Sensor thickness:		
Planar silicon	150÷250	μm
3D silicon	230	μm
Diamond	400÷600	μm
Radiation length at z=0	1.54	% of X_0



Sensor technologies for IBL



Planar silicon

- Slim edge n-in-n
- Thin n-in-p
- Prototyping with CiS, HLL, HPK





3D silicon

- Active edge single sided and double sided
- Prototyping with CNM, Sintef/SLAC, FBK







Motivation for Speed-up

- FE-I4 success push up optimism:
 - First version of the chip is guite successful, planar sensor with FE-I4 measured on test beam at DESY, 3D sensors with FE-I4 just start testing.
- LHC shutdown schedule:
 - Machine has moved LHC next shutdown into 2013/14. phase I shutdown delayed (2017 or later)
 - Installation in 2013 simplified by low activation of beam pipe.
- nSQP project
 - If Pixel detector is brought to surface IBL installation is further simplified.
- Physics profit earlier of better tracking performance.



Shift material budget out of tracking region





η<2.2 : weight = 16.9 Kg (3 layer)



 η <2.2 : weight = 6.5 Kg (4 layer)



 $\eta \sim 1.5$: γ -conversion for H $\rightarrow \gamma\gamma$ from 22% to 11% for new 4 Layer Pixel System

BPIX / FPIX Envelope Definition & Insertion into CMS





Impact Parameter of old / new Pixel System





Beam pipe r<23mm : 16 faces to 12 faces → reduce MS term by ~0.75 → total 0.75x0.6 = 0.45 !

Upgrade of Pixel Readout Chain





Present ROC for 1 st Layer:			
<u>Luminosity</u>	bx-spacing	Data Loss	
1x10 ³⁴ cm ⁻² s ⁻¹	25nsec 50nsec	<mark>4%</mark> 16%	
2x10 ³⁴ cm ⁻² s ⁻¹	25nsec 50nsec	15% ~ <mark>50%</mark>	
50nsec operation of LHC <u>was not planned</u> in original ROC architecture in 1998.			





Other changes in Phase I 2017 include...

- LHCb
 - present limit of 1fb⁻¹/y can be increased to 5 fb⁻¹/y
 - read out all data at 40MHz and generate trigger off-detector
 - trigger decision can be more sophisticated using data from all sub-detectors
 - upgrade significant detector elements, especially VELO
- ATLAS trigger
 - add tracking information in L2 hardware processing
- CMS L1 trigger
 - improve isolation selection in calorimeters
 - architecture may be foundation for future tracking trigger



LHCb sub-systems





Electronics architecture

Front-end electronics: transmit data from every 25ns BX



VELO upgrade data rate challenge

- Electronics has to digitise, zero suppress and transmit event data at 40 MHz
- By pixel standards the occupancy of the VELO is miniscule, but the data rate is HUGE
- 1 chip has to transmit 10-20 Gbit / second
- Our current granularity, occupancies = ok but FE electronics and DAQ are not







Pixel (baseline) option

VeloPix chip: 256 x 256 array, 55 x 55 μ m pixels

- Strong overlap with TimePix2 (under design)
- 3 or 4 bits TOT
- Architecture to minimise bandwidth (hottest chip = 12 Gbit/s)
- Serial readout





Trigger Improvements

 Detailed studies of system latency show scope for L1 improvements and additional functionality: E_T^{miss}, topological trigger combining multiple trigger objects



- L2 improvements: include FTK to improve efficiencies combine tracks early with trigger objects
- Explore new technologies for HLT (eg GPUs)

Phil Allport: ATLAS Upgrade

Level-2 fast track finder, FTK (before the SD)

Two time-consuming stages in tracking

Pattern recognition – find track candidates with enough Si hits



- 10⁹ prestored patterns simultaneously see each silicon hit leaving the detector at full speed.
- Track fitting precise helix parameter & χ^2 determination
 - Equations linear in local hit coordinates give near offline resolution:

 $p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$ a & b are prestored constants; VERY fast in FPGA

March 4, 2011

FTK Status Report



Key Principles of the Upgrade



- Hold the Level 1 Accept Rate at 100kHz
 - (plus side) Avoids as much as possible rebuilding front end and readout electronics
 - (minus side) Puts more pressure on the DAQ to deal with increased data size
- Employ full granularity of detectors in trigger
 (0.087 x 0.087 in η–φ)
- Rely on powerful modern FPGAs with huge processing and I/O capability to implement more sophisticated algorithms
- Use state of the art telecom technology to support increased bandwidth requirements

Also will achieve some hardware standardization

CMS Time-Multiplexed Trigger: Concept



- The key problems of triggering remain the same as in 1995
 - Concentration of dataflow into a single processor
 - Limitations on algorithms due to internal bandwidth limits
 - Understanding and optimising what is going on



CMS Upgrade Architecture: µTCA



- Advanced Telecommunications
 Computing Architecture ATCA
- µTCA derived from AMC std.
 - Advanced Mezzanine Card
 - Up to 12 AMC slots
 - 10-11 Processing modules
 - 1-2 Controller Modules
 - 10 GB/s point-to-point links
- Dramatic increase in computing power and I/O.
- Possible to built a trigger based on a single µTCA card → reduce
 - Complexity
 - Maintenance + Manpower costs



Single Module μ TCA card 75x180



CMS GCT Matrix Card 75x180 mm (2009)

2021: Phase II

- ATLAS and CMS will insert completely new trackers
 - yet to be fully defined
 - technologies to achieve the radiation tolerance and performance are still under development
 - many challenges and promising ideas, some of which will be developed during Phase I (CO2 cooling, DC-DC & serial powering, advanced links...)
 - but must not sacrifice performance conflicts between power and material needs care
- L1 trigger will be a particular challenge
 - consensus seems to have emerged that tracking information will be needed
 - new types of module are needed but time is short

CMS – Studies of new tracker layouts



Studying several potential layouts for a new outer tracker

Want to increase granularity as well as minimize material in future tracker

- Need to understand how many triggering layers (in red at left), and where they need to be located in order to provide adequate triggering capability
- No final decision on layout of tracker until final requirements determined

CBC: CMS Binary Chip for outer tracker

- New 130nm ASIC, descended from APV25 philosophy
 - now working and module prototyping beginning

volts

studies to include trigger functions

2 consecutive data frames (2 headers)1 fC signal injected on one channel





7 m

pipeline

buffers

4 mm

Strawman Layout of New ATLAS Inner Tracker

4 layers of pixels to larger radius than now 3 double-layers of short strips (SCT region) 2 double-layers of long strips (TRT region) Approx. 400 Million pixels (cf 80 Million now) Approx. 45 Million strips (cf 6.3 Million now)

4+3+2 (Pixel, SS, LS) V14-2009



Implemented in Geant, including realistic service material, to study performance and look at optimisations

Inner Tracker Sub-committee set up to further improve on this: number of layers, length of barrel, conical end-caps, maintenance



sLHC-PP Public Event

Microstrips: Modules and staves

Hybrid with front-end chips glued directly to sensor Sensor glued to cooled mechanical support - "Stave" Staves arranged in cylinders Stave can reduce material and helps assembly schedule by avoiding bottle-neck at module mounting on cylinders







March 8 2011

Nigel Hessey, Nikhef

sLHC-PP Public Even



Why tracker input to L1 trigger?

- Single μ , *e* and jet L1 trigger rates will greatly exceed 100kHz
 - Tracker data appears to be only extra info capable of improving selectivity
 - can increase latency, to 6.4 μs , but must maintain 100 kHz for compatibility



The track-trigger challenge

- Impossible to transfer all data off-detector for decision logic
 - for most of detector, at least
- Large fraction of low p_T tracks
 - not useful for trigger
 - conceptually simple to measure
 - hit density means high combinatorials
- Possible solution by correlating information from two closely spaced radial layers

several ideas for how to do this but a big challenge to implement and demonstrate in next few years



Track Trigger at L1

Several ideas for implementing a track trigger at L1. Wanted: high-PT (~20 GeV) leptons.

ATLAS EM calo has good identification, allowing a twostage trigger approach:

Calorimeter or muon system identifies a candidate high-PT lepton and gives region-of-interest

Inner tracker modules in that region are read-out, and hardware track finders confirm presence of track with matching momentum

Rol is a few % of modules so small increase in bandwidth needs --> very little increase in material

Needs additional data stream in FE chip and a lot more study, but encouraging so far





Alternatively, measure track angle to radial direction at outer edge of inner tracker - look for near radial tracks

Either with paired silicon layers or GasPix detector with 10 mm drift gap

Summary

- Too much material to do justice to
 - much has been omitted
- LHC is a huge data mine and improvements to the detectors will ensure it will be delivering physics for two decades
- Many of the changes are extremely challenging
- They will need all the ingenuity of the next generation of physicists to accomplish successfully
- The rewards will be immense

BACKUP MATERIAL

Options for Leveling:

CRAB cavities

-New technology not yet demonstrated for hadron storage rings

Wires for long range beam-beam compensation:

-New technology not yet demonstrated for hadron storage rings with long range beam-beam interactions

Operation with offsets at the IP:

-Has been difficult in other machines

Dynamic optics change during physics collisions:

-Has never been done so far in a collider plus complication of crossing angle in common beam pipes for the LHC

Summary of LHC Intensity Limits (7 TeV)



ACES 2011 Workshop, CERN, March 2011 Oliver Brüning BE-ABP