



# **HLS with Intel OneAPI on Allen algorithm**

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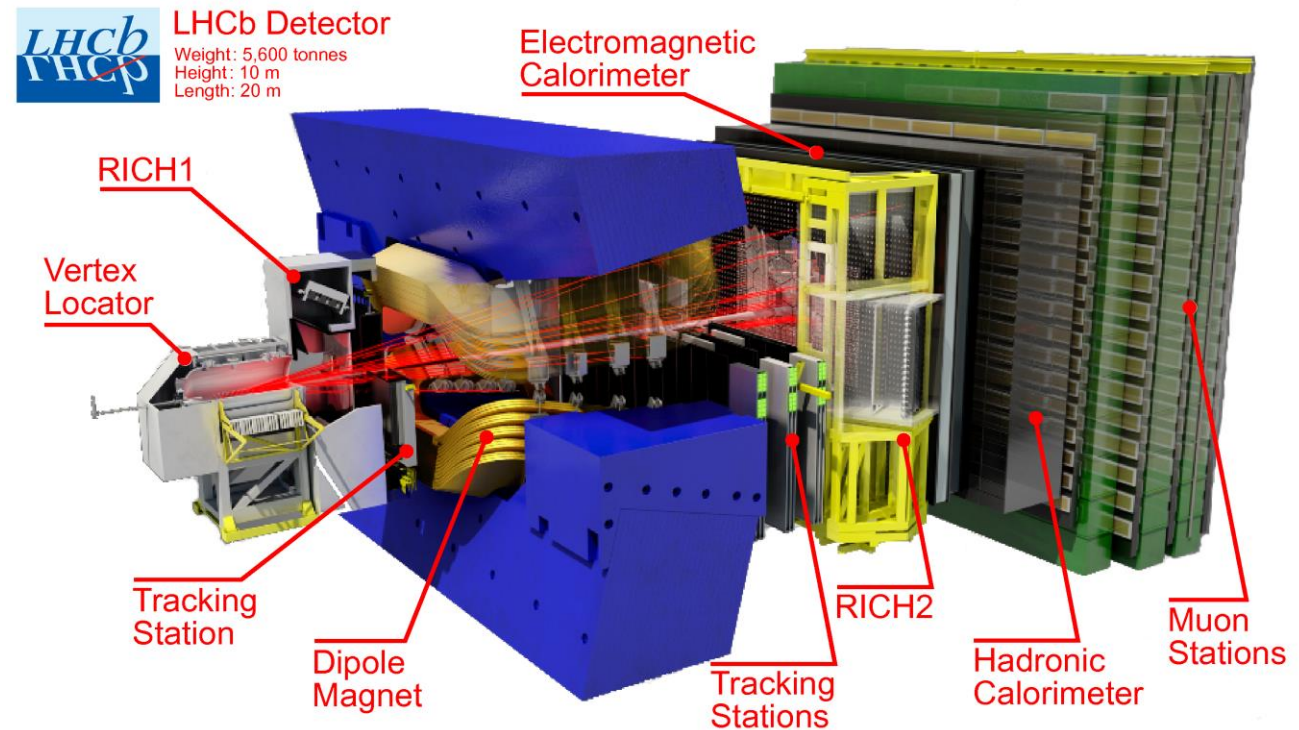
# Theoretical background

## *Defining the project*

- **Allen project**  
Specifically "masked Velo clustering" algorithm

- **Current status**
  - Allen in SYCL for GPU
  - FPGA Implementation

- **Goal**
  - Allen in SYCL for FPGA



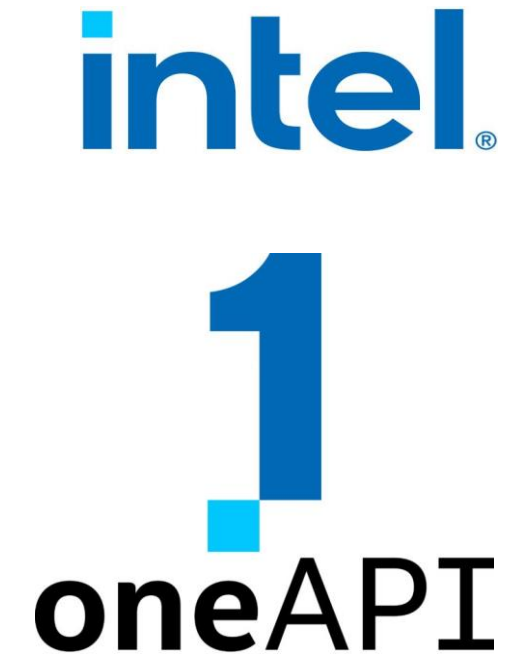
# Theoretical background

## *Defining the tools*

- **High level Sythesis:** SYCL for heterogeneous computing
  - Data Parallel C++



- **FPGA hardware**
  - custom hardware implementation for specific tasks



# Challenges

## Setting up the System

- combining the above
- getting started



## Allen size

- code volume
- compilation time



## GPU -> FPGA

- initial implementation focused on GPUs



# Methodology

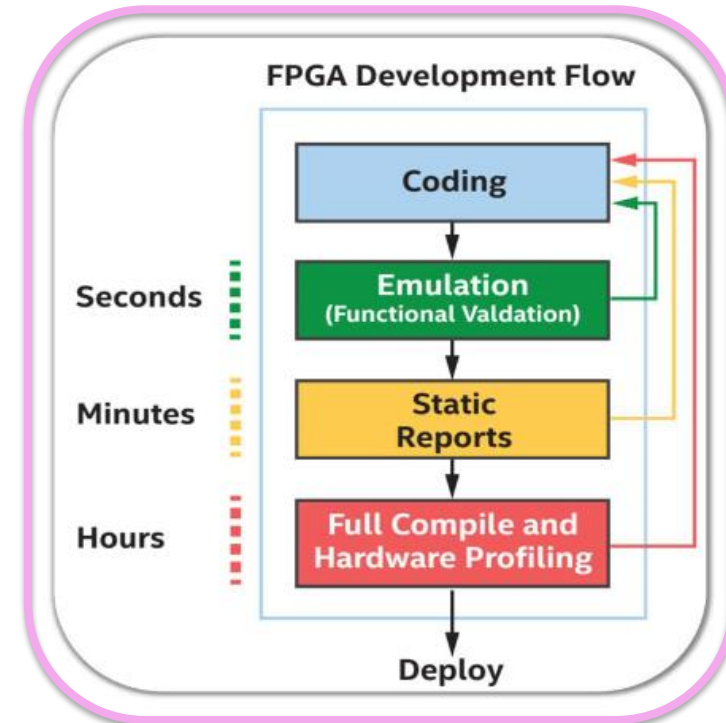
## *Experimenting on SYCL Allen*

### Setting up a SYCL kernel

- memory allocation
- queue jobs
- invoke kernel
- getting results

### OneAPI Compilation Stages

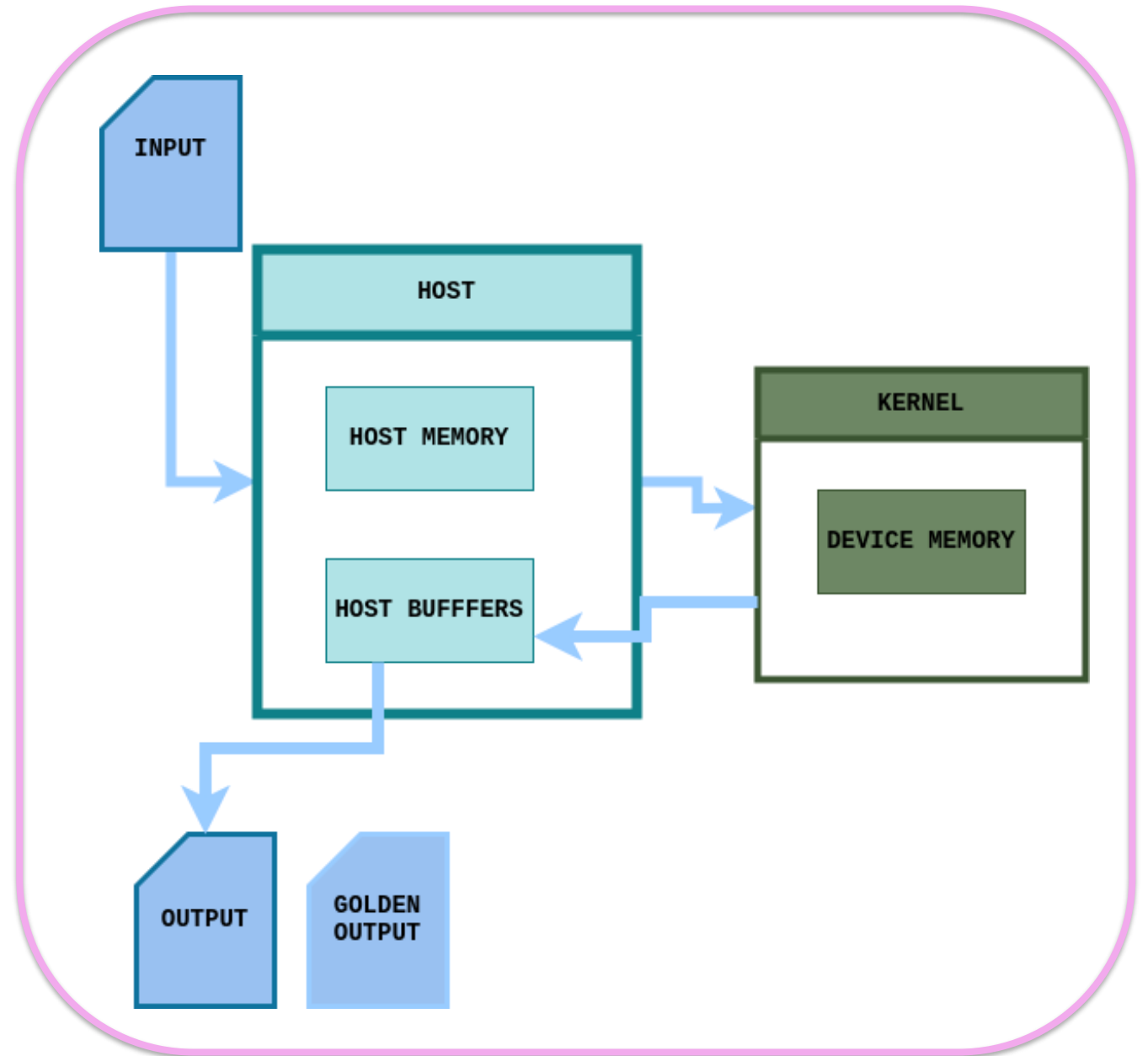
1. FPGA Emulation for verification
2. FPGA Simulation reports
3. FPGA Compilation



# Techniques

*Making specific changes*

- **Separating the algorithm**
  - sequence change
  - input/output redirection
- **Memory management**
  - memory allocation in the device
  - host buffers for device memory
- **Kernel Invocation**
  - specialized for the FPGA
  - `parallel_for` -> `single_task`



# Future work

*Experimenting on SYCL Allen*

- **Future implementation**
  - standalone implementation - further separating the algorithm
  - working more on FPGA performance specialized architecture

# THANK YOUU :) )

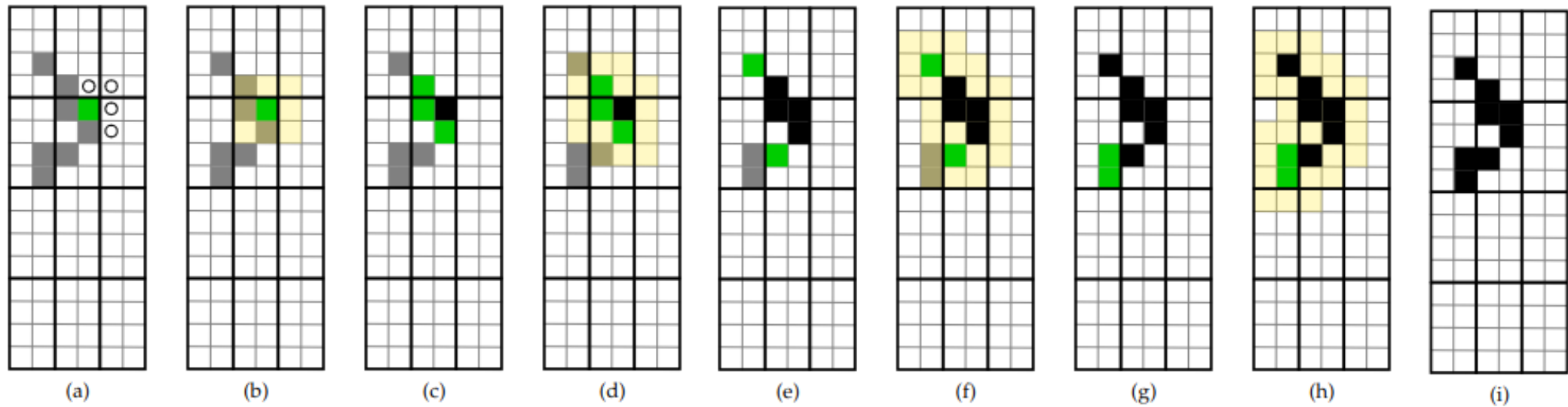
## QUESTIONS?

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# Detailed explanation

## *Masked Velo clustering logic*



Optimization of high-throughput real-time processes in physics reconstruction

Daniel Hugo Campora Perez

<http://cds.cern.ch/record/2718278?ln=en>