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Object: Hardware and software inventories, technical experiences, R&D activities expected

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Find below LLR's answers about the SLHC's R&D, as requested by F.Vasey (coordinator of Optoelectronics working group for SLHC) during the last working group phone meeting at 22.02.07.

1/ Hardware and software inventories

Measurement materials:

- Serial Data Analyzer (Real Time) 11 GHz bandwidth on 2 ch / 40 GS/s → which give the opportunity to have the analysis capability on serial link up to 6Gbps. The same material configured at 6 GHz bandwidth on 4 ch / 20 GS/s → up to 3,5Gbps capability on serial link analysis.
- Optical Electrical converter for SDA, 950 nm to 1630 nm (3.5 GHz bandwidth)
- 8B/10B symbol viewer for SDA, software to translate serial data waveform into symbol view
- Optical 1 to 8 wideband single mode coupler, ≈ 10 db insertion loss/ch, measured at 1550 nm
- Pulse pattern generator 15 MHz to 3.35 GHz dual channel, delay modulation (jitter injection), low intrinsic jitter, LVDS levels
- Function / Arbitrary Waveform generator 80 MHz, sine, square, triangle, ramp, noise, sin(x)/x, DC volts etc...

EDA software for specific purpose:

- Allegro PCB signal integrity (SPECCTRAQuest Cadence), signal integrity verification
- HyperLynx GHz (Mentor), signal integrity verification
- Seamless FPGA (Mentor), hardware/software verification for Xilinx platform with embedded PowerPC

2/ Technical experiences onto embedded serial link and FPGA programming, associated publications

- First validation of XILINX multi gigabit transceiver connected to a CERN GOL device. Results published at LHC-electronics-workshop 2002 Colmar: *Embedding deserialisation of LHC experimental data inside Field Programmable Gate Arrays*
- Latency optimization and jitter effect inside XILINX multi gigabit transceiver. Results published at LHC-electronics-workshop 2003 Amsterdam: *A solution to reduce the latency of a Multi Gigabit Transceiver (Virtex-II Pro) - Effect of clock jitter on the Bit Error Rate*

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- Test platforms for CMS ECAL electronics boards. Results published at LHC-electronics-workshop 2004 Boston: *Tests of the boards generating the CMS ECAL Trigger Primitives from the On-Detector electronics to the Off-Detector electronics system*
- Electronics test bench for testing the CMS ECAL FE boards. Results published at LHC-electronics-workshop 2004 Heidelberg: *CMS ECAL Front-End boards : the XFEST project / A real time electronics emulator with realistic data generation for reception tests of the CMS ECAL front-end boards*
- IP and simulation test bench using a XILINX multi gigabit transceiver at 1.6 Gbps with custom low latency architecture. HDL code provided and used to the CMS ECAL global calorimeter trigger (GCT) project: work not published.

3/ Activities expected, inside Working Group's R&D

The main purpose of the Opto Working Group is probably to propose, design and test a radiation hard optical transceiver. To do this a versatile test bench must be studied and used to measure any commercial and custom solutions. The platform test should be largely based on the shelf's material available in industries, but specific requests in HEP must be take in account, like latency, number of channel, type of measurement. In fine, a reference test bench can be an excellent way to precisely compare different components or solutions tested with the same platform, under the same conditions.

We propose to develop a test bench based on use of a FPGA provider test board. Generally high quality fixtures are available on FPGA board and they can be used up to 3.5 Gbps on serial links. This test bench will be used for testing optical link system at different levels of complexity.

We would have the capability to test commercial or custom optical transceivers by driving them with serial bit streams from embedded SerDes. Emitter like the receiver side should be used. It is alone necessary to design a specific PCB for each component under test and the necessary fixtures to connect it to the standard FPGA test board. We could also, construct a fast BER tester by using an opto coupler 1 to 8 and applying majority comparison scheme or by selecting a reference channel among the 8 available. The same way has been successfully applied for the reception's tests of CMS ECAL front-end boards. Parallel testing appears as an efficient solution for testing BER with components that exhibit a low transmission error count. It is also important to do the measurement of jitter margin by injecting a calibrated noise onto the emitter clock or receiver clock and what they do affect the BER.

The GBT physical transceiver part can also be tested. In a first time, this one could be tested without the ASIC supporting the protocol layer. This one is another part of the GBT's project. But a real interest is to create an IP inside FPGA that emulate the protocol layer of the GBT. FPGA with embedded SerDes could be used as a high integrated system into off-detector side if a solution is demonstrated to do this while respecting latency budget. Nevertheless this IP's should be used as testing platform for the GBT's ASIC.

Summary

We propose to develop a test bench by using commercial FPGA's board. This one can drive the optical transceiver under test with their embedded SerDes. Up to 8 optical transceivers could be drove by an optical splitting method. The GBT physical transceiver part can also be stimulated with a parallel

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interface inside the FPGA board. Finally an IP could be developed and integrated in the FPGA to emulate the protocol layer used by GBT project. This IP can demonstrate the possibility to use it as commercial high integrated solution for the receiver part of the link between On-detector and Off-detector electronics.

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