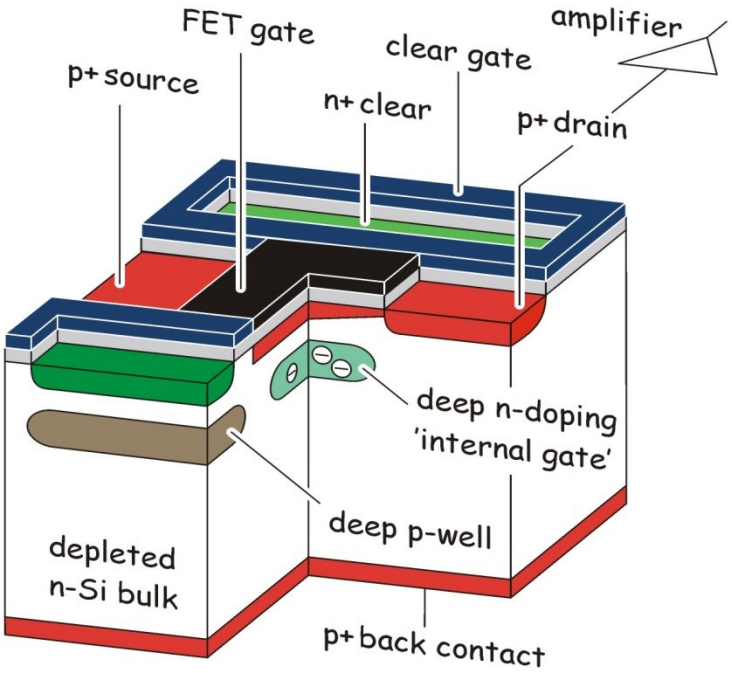
DEPFET Active Pixel Sensors (for the ILC)

- DEPFET Principle
  - Single Pixel characteristics
- An Array of DEPFETS
- Thin DEPFETs for Belle II and ILC

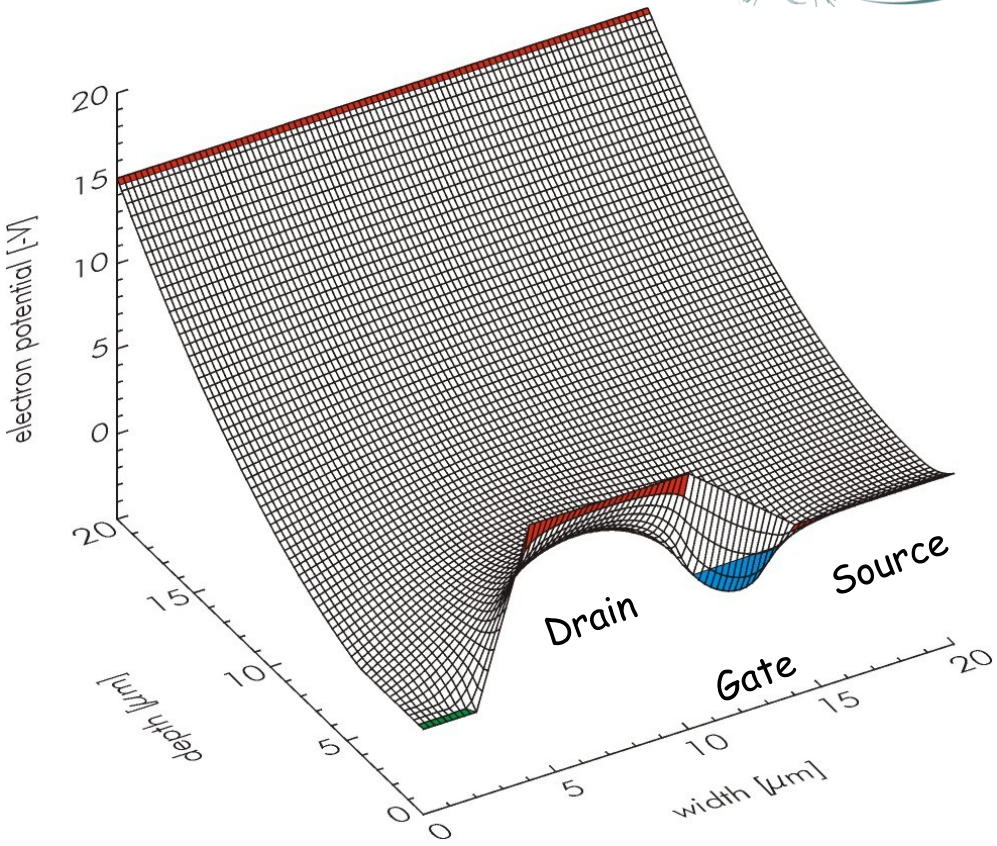
The DEPFET Collaboration … 15 Institutes, and still growing

DEPFET Principle

J. Kemmer & G. Lutz, 1987

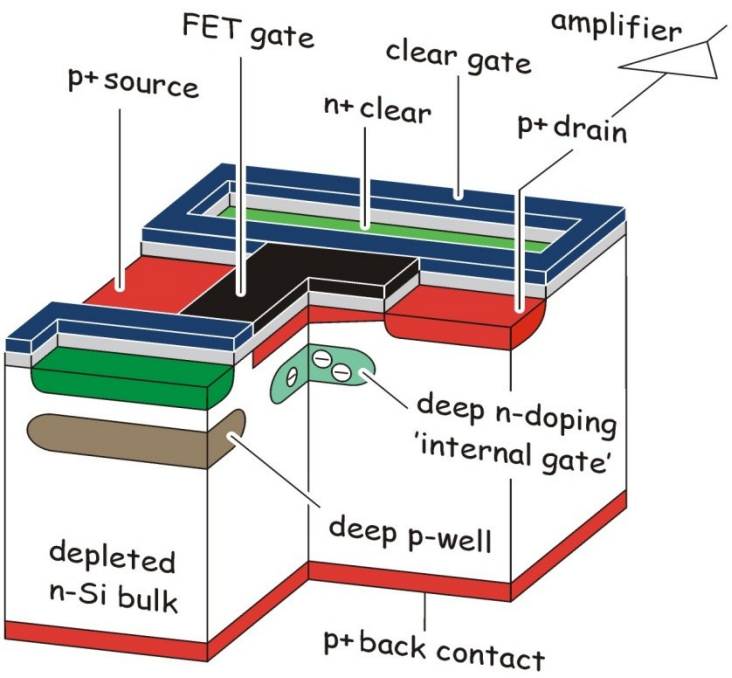


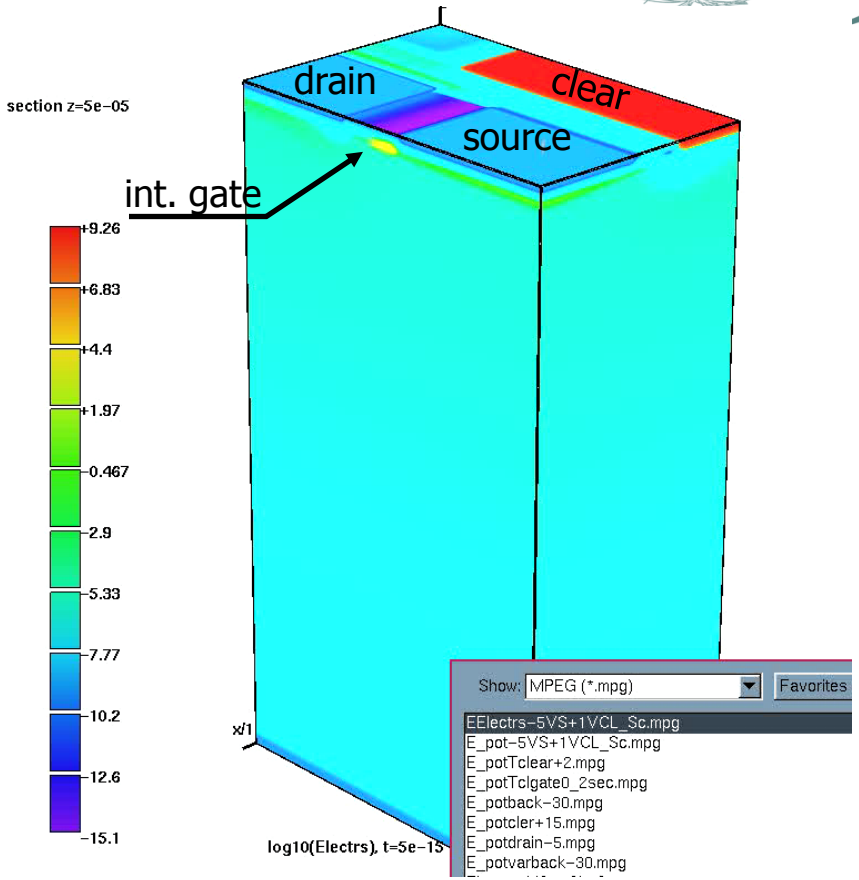
Depleted P-channel FET



- fully depleted sensitive volume, mip: ~ 80 e-h pairs/µm
- internal amplification
- Charge collection in "off" state, read out on demand

DEPFET Principle

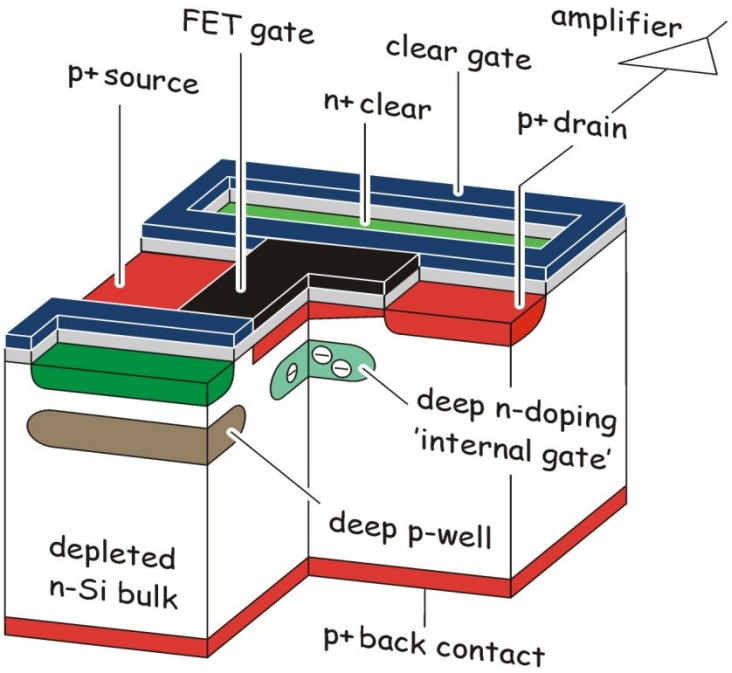


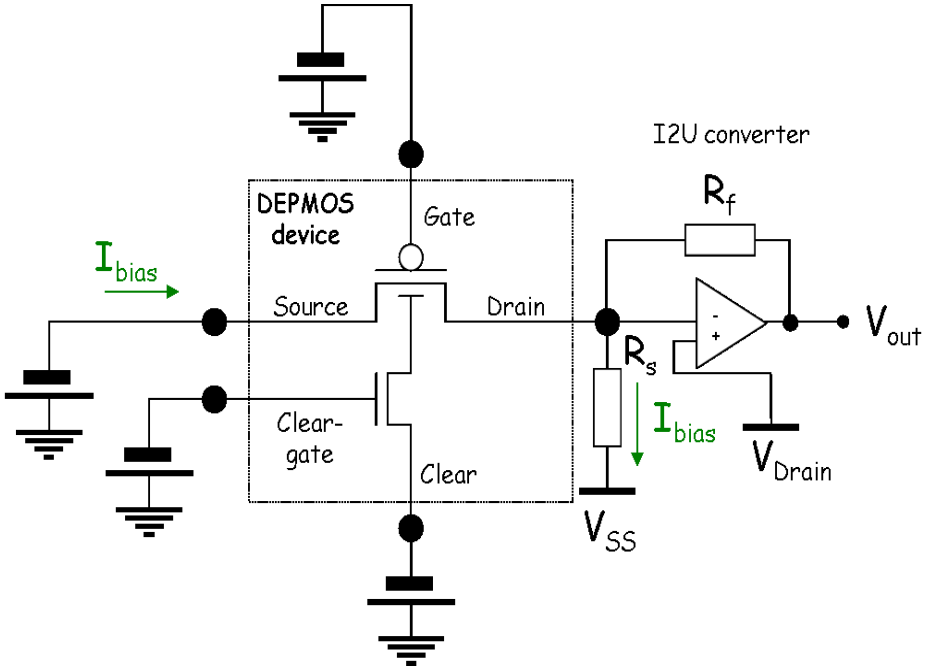


TeSCA 3D Simulation by K.Gärtner, WIAS, Berlin

- fully depleted sensitive volume, mip: ~ 80 e-h pairs/µm
- internal amplification
- Charge collection in "off" state, read out on demand

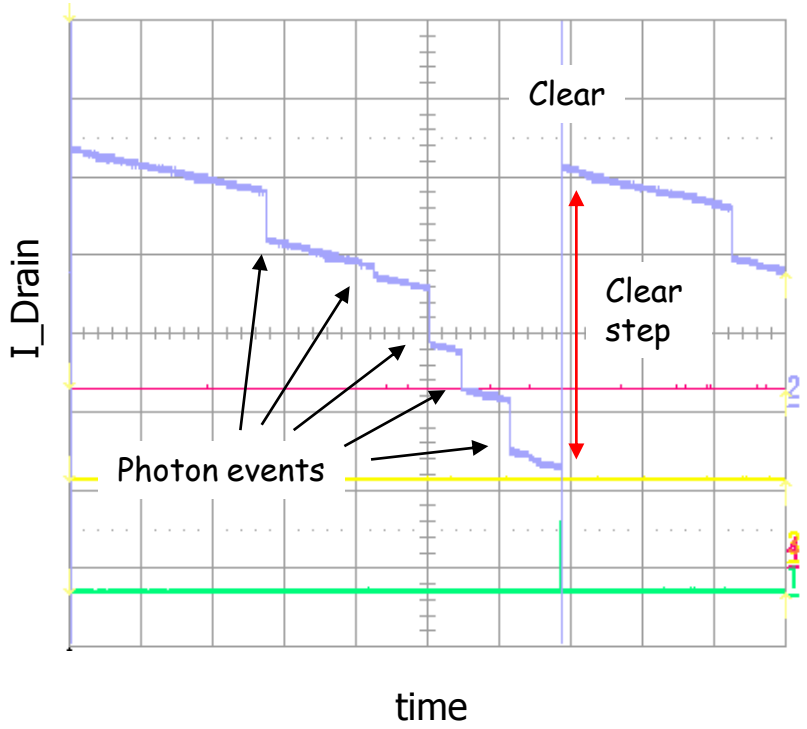
DEPFET Principle

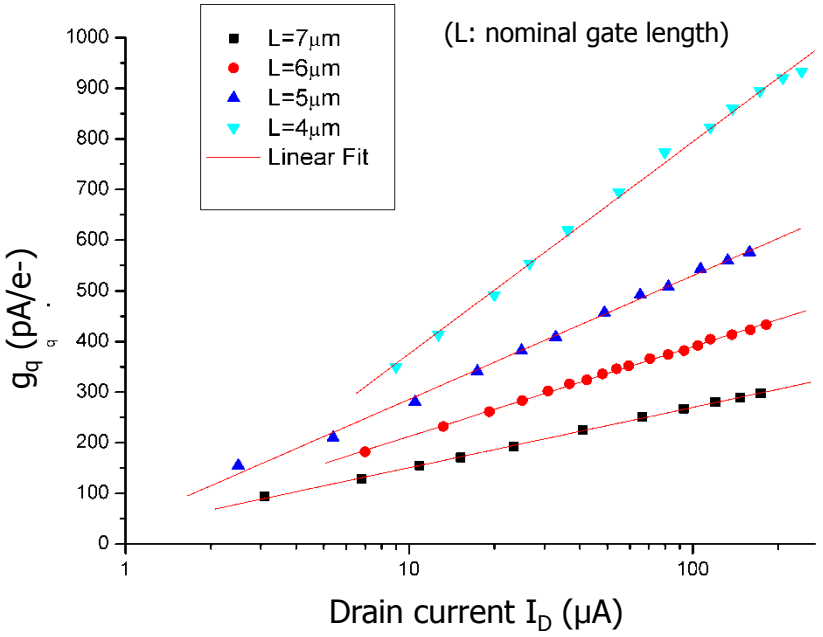




- fully depleted sensitive volume, mip: ~ 80 e-h pairs/µm
- internal amplification
- Charge collection in "off" state, read out on demand

Internal Amplification



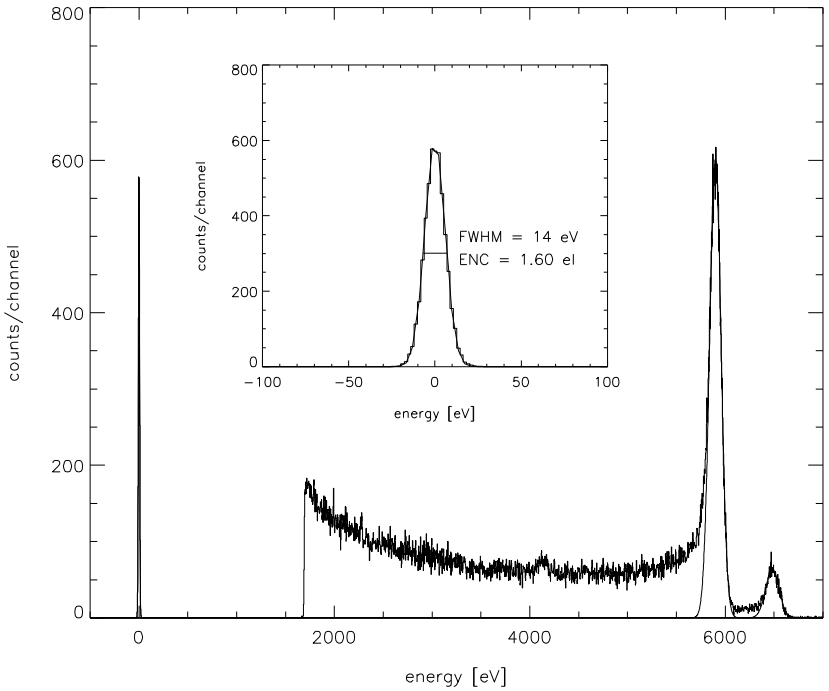


$$g_q = \frac{dI_D}{dQ} = \frac{g_m}{C_{ox}} \quad \Rightarrow \quad g_q \sim \frac{1}{L^{3/2}} \qquad g_q \sim I_D^{1/2} \qquad g_q \sim \frac{1}{W^{1/2}}$$

(Ideal transistor theory - neglecting short channel effects)

$g_q \sim t_{ox}^{1/2}$ Reduction necessary to improve radiation hardness and output IV curves

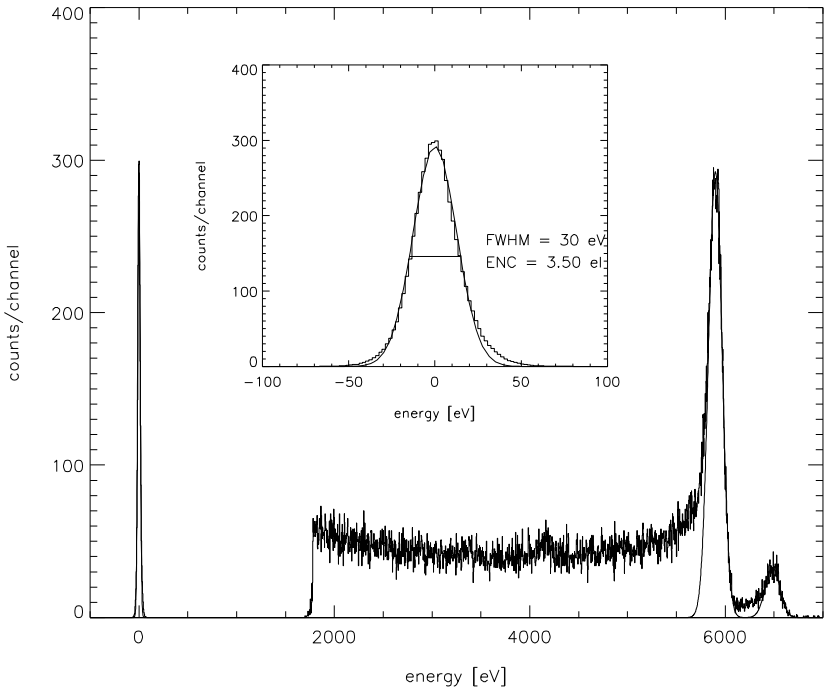
55Fe Spectrum (single pixel)



non-irradiated
V_{thresh}≈-0.2V, V_{gate}=-2V
I_{drain}=41 µA
time cont. shaping τ=10 µs

Noise ENC=1.6 e^- (rms)

at T>23 degC

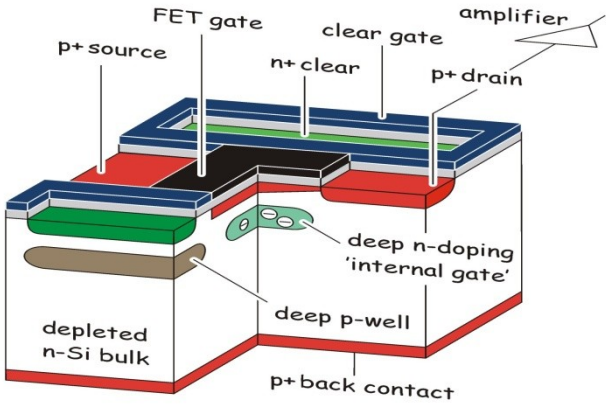


912 krad ^{60}Co
V_{thresh}≈-4.0V, V_{gate}=-6.0V
I_{drain}=40 µA
time cont. shaping τ=10 µs

Noise ENC=3.5 e^- (rms)

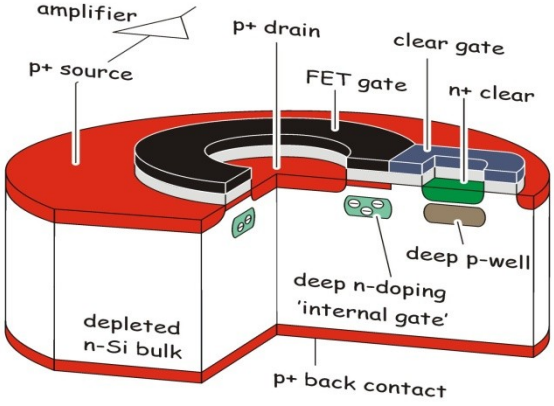
at T>23 degC

DEPFET Types and Applications



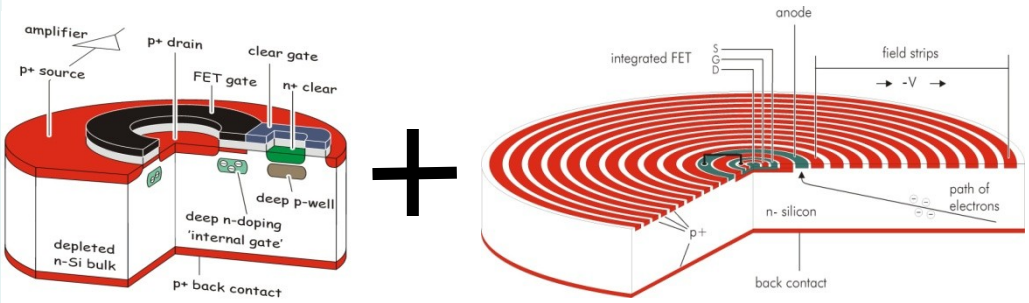
Particle tracking → vertex detector at Belle II and ILC

- pixel size: 20μm…75μm
- r/o time per row: 25ns-100ns
- Noise: ≈100 el ENC
- thin detectors: 50μm…75μm → still large signal: 40nA/μm for mip



X-ray imaging spectroscopy → **IXO (Athena)**

- pixel size: 100μm
- r/o time per row: 2.5 μs
- Noise: ≈4 el ENC
- fully depleted thick detectors better → large QE for higher E



X-ray (imaging) spectroscopy
→ **BepiColombo and XFEL**

- pixel size: 100s of μm
- For XFEL: DEPFET → DSSC

DEPFET **S**ensor with **S**ignal **C**ompression

An Array of DEPFETs – r/o ASICs

mpi halbleiterlabor

Hybrid-pixel-like approach

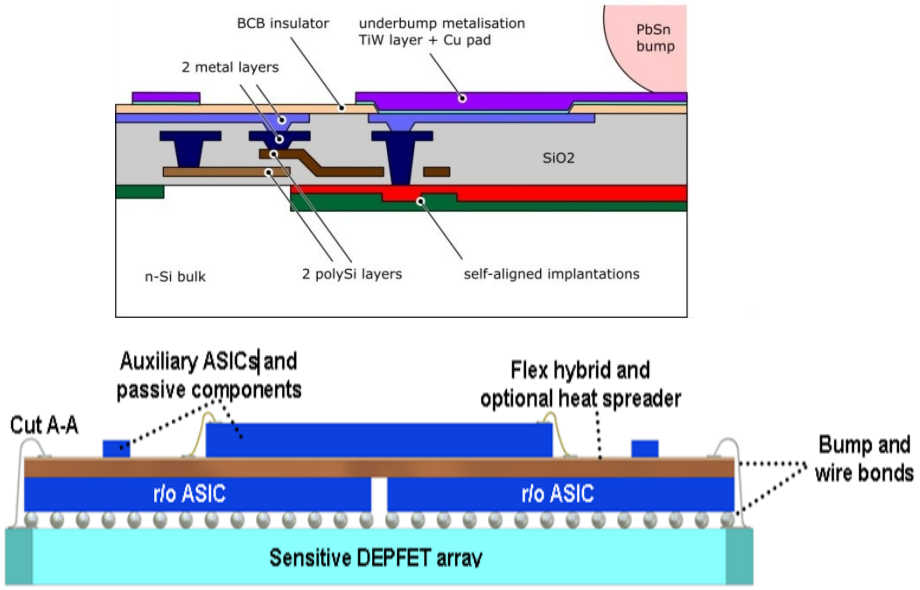
- one amp. (&ADC) per pixel, external common clear
- more challenging interconnection (bump bonding, vertical integration ..)
- high power consumption
- fast! frame rate comparable with hybrid pixels

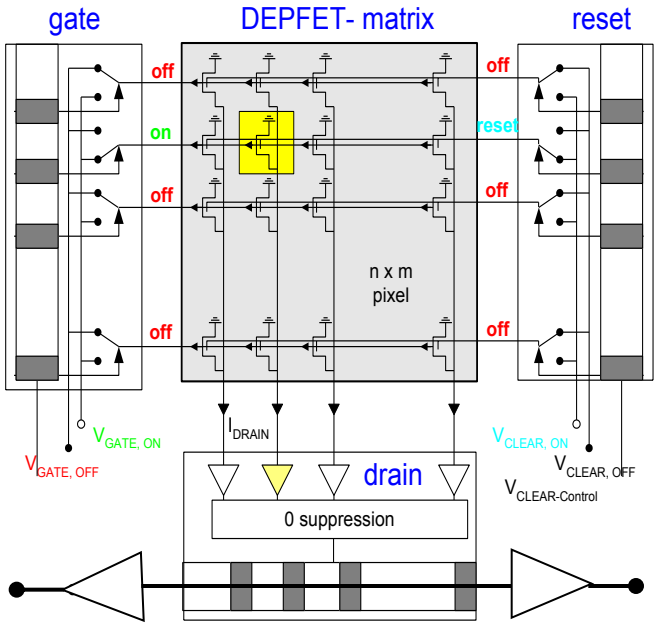
→ **European XFEL** (~5MHz frame rate)

Row wise read-out ("rolling shutter")

- select row with external gate, read current, clear DEPFET, read current again
- two different auxiliary ASICs needed, but no interconnect in sensitive area
- r/o needs time…..
- only one row active → low power consumption

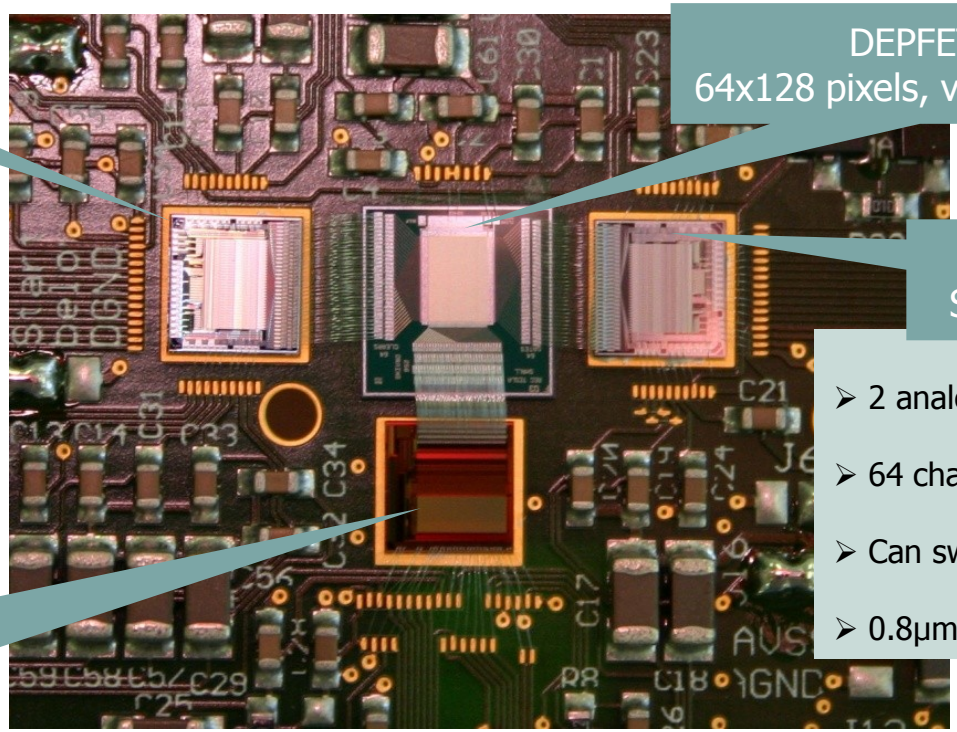
→ **Belle II, ILC, IXO, Bepi Columbo**





ILC Prototype System

Gate Switcher



DEPFET Matrix
64x128 pixels, various pixel types

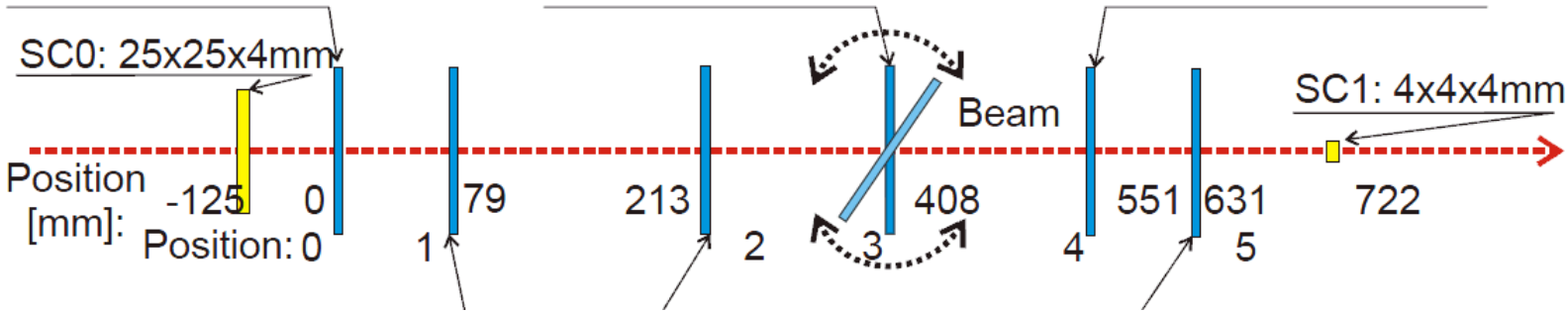
Clear Switcher

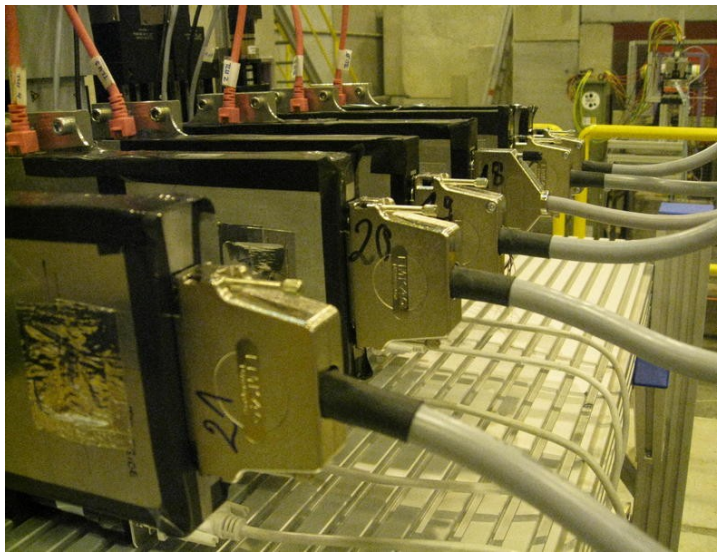
- 2 analog MUX outputs with
- 64 channels each
- Can switch up to 25 V
- 0.8µm AMS HV technology

Current Readout
CUROII

current based 128 channel readout chip
50 MHz band width in the f/e
On-chip pedestal subtraction (CDS)
Real time hit finding and zero suppression
0.25µm CMOS technology (radhard design)

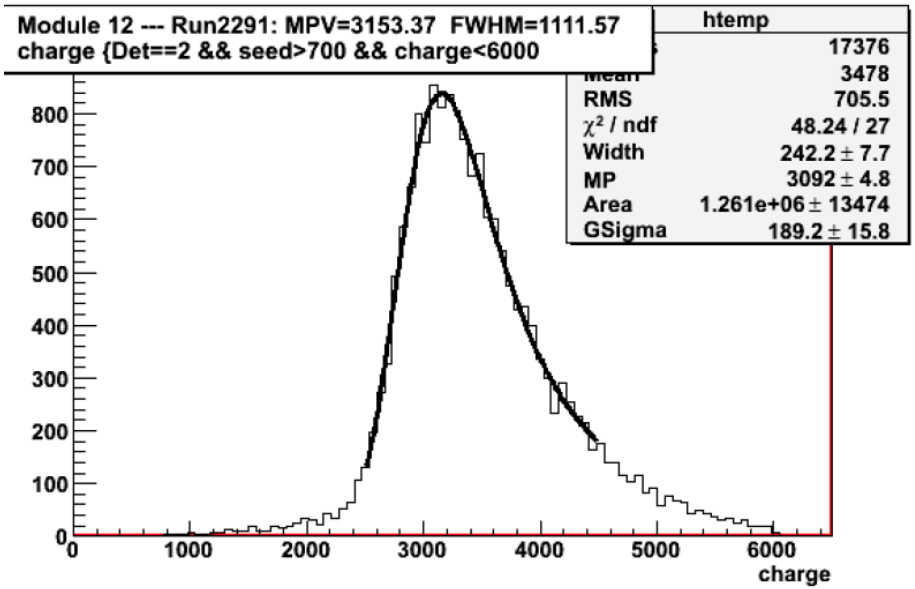
Evaluation of ILC Test Matrices: Beam Tests at CERN H6





- 5 telescope planes with "standard" DEPFET matrices, 450 µm thick
  - 24x32 µm² pixel size
  - 2008: 64x128 pixels
  - 2009: new readout board for 64x256 matrices
- one device under test (DUT) on the rotation stage
  - 2008: 64x128 pixels, 24x24 µm²
  - 2009: 64x256 pixels
    - 20x20 µm² with shorter gate length
    - capacitively coupled clear gate (…better clear)
- all devices characterized in the lab before test beam (laser, source..)
- Test beam program:
  - high statistics run for in-pixel studies
  - angular scans
  - "clear" parameter and depletion voltage scans
  - Beam energy scan
  - …

Data Analysis finished 2010, with a world record ..



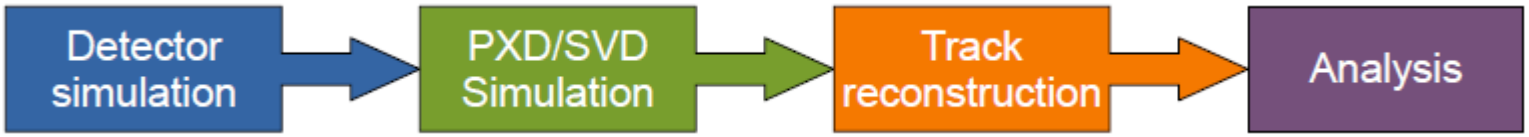
- 120 GeV pions, 90°, 20 x 20 μm² pixel
- DEPFET Gate L=5 μm
- → higher $g_q \approx 650$ pA/e⁻
- S/N ≈ 200
- **≈ 1 μm resolution!**

TABLE I

RESIDUALS AND RESOLUTIONS IN x AND y. TYPICAL ERROR OF RESIDUALS AND RESOLUTIONS IS 0.1 μM.

Resolution in [μm]	Module #0 32x24 μm		Module #1 32x24 μm		Module #2 20x20 μm		Module #3 32x24 μm		Module #4 32x24 μm		Module #5 32x24 μm	
	x	y	x	y	x	y	x	y	x	y	x	y
Residuals	2.49	2.28	1.60	1.38	1.54	1.42	1.98	1.61	2.06	1.61	3.24	2.86
Resolutions	1.65	1.45	1.15	0.90	1.10	1.00	1.60	1.20	1.65	1.20	2.00	1.80

Towards Thin Sensors



Particle gun (single event)
EvtGen (physics event)
Detector geometry
Material

E-Field in Silicon
Lorentz angle in B-Field
A/D Conv. and clustering

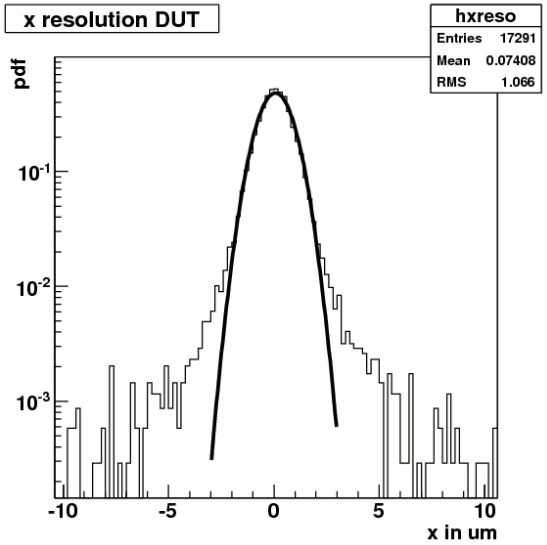
Marlin tracking
PXD+SVD+CDC

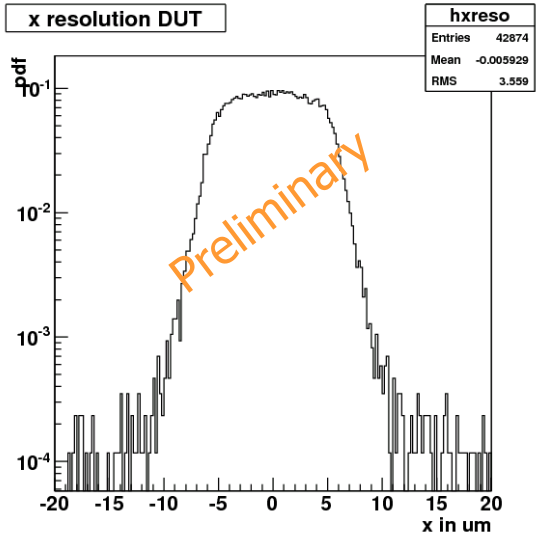
Physics channels

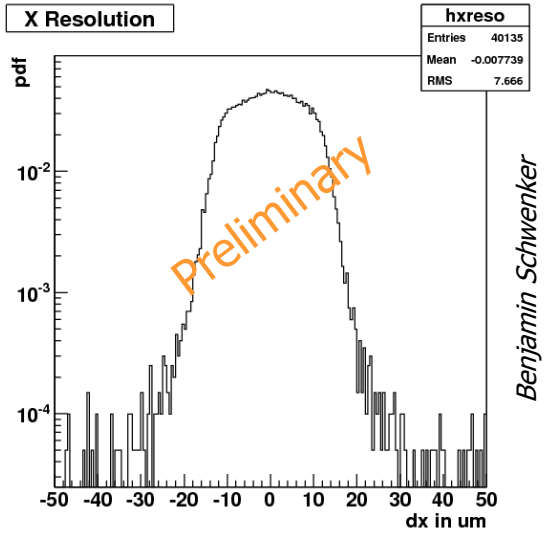
Test Beam Data
Pixel: 20x20x450 μm^3
→ σ_{sp}≈1 μm

small + thin
Pixel: 20x20x50 μm^3
→ σ_{sp}≈3.5 μm

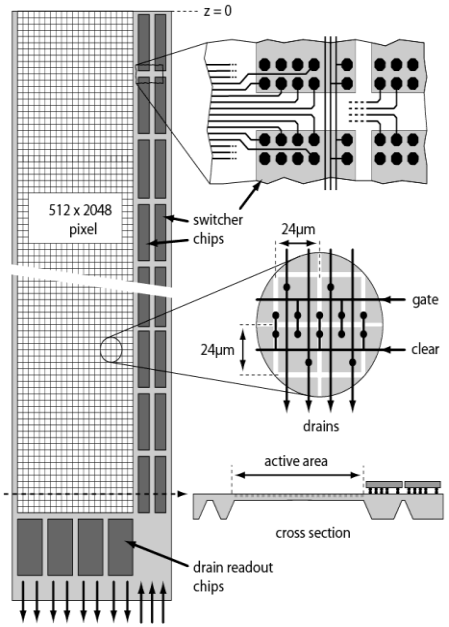
bigger + thicker + 1.5 T
Pixel: 50x50x75 μm^3
→ σ_{sp}≈7.7 μm

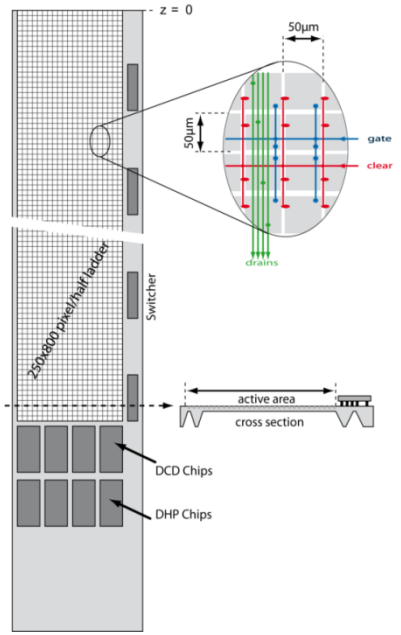






VXD vs. PXD (from a DEPFET point of view)

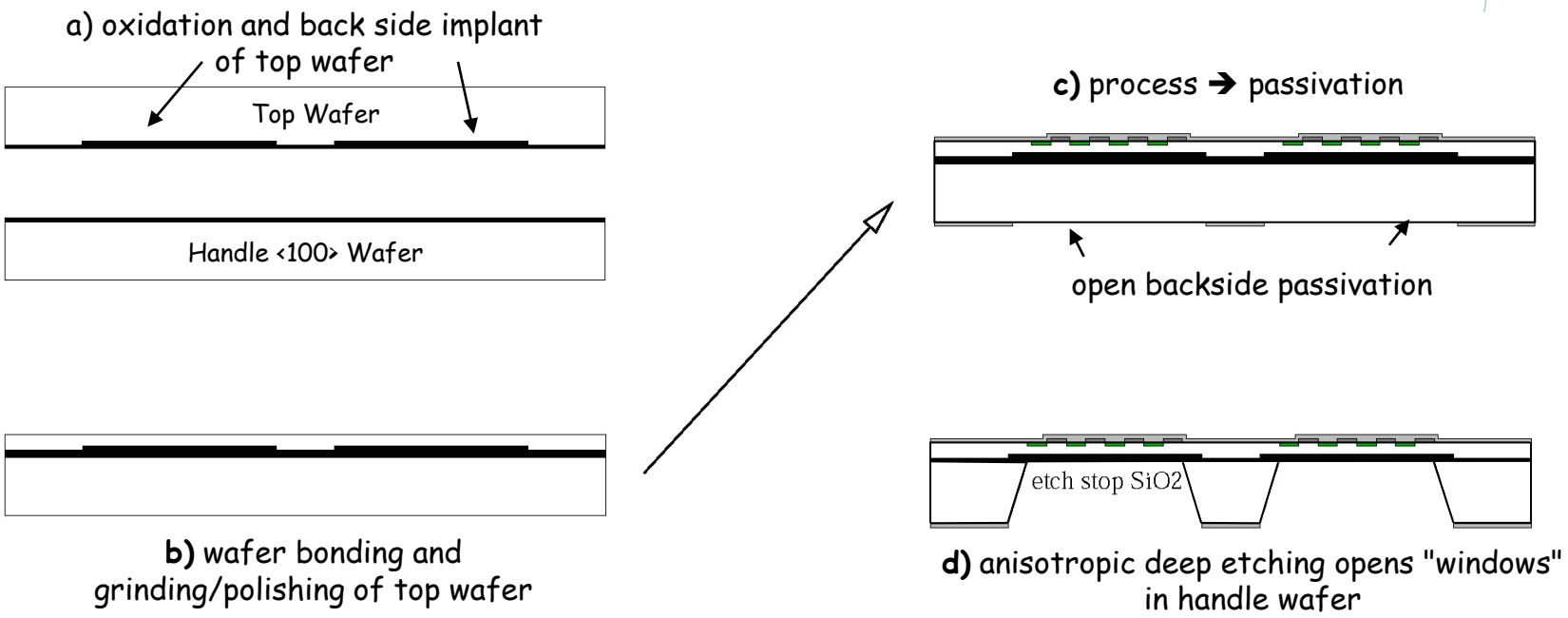


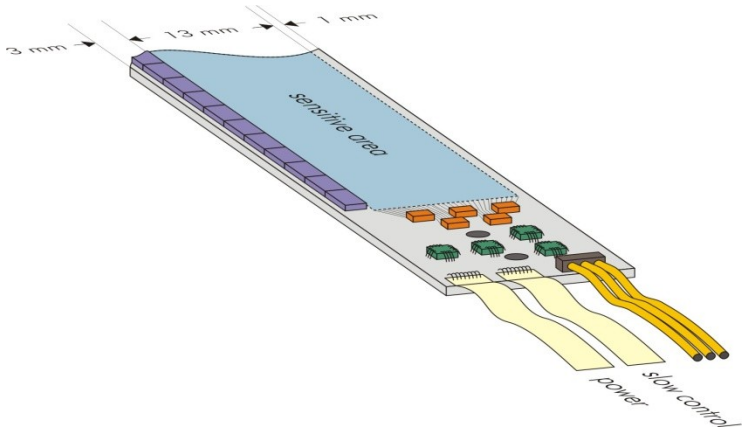


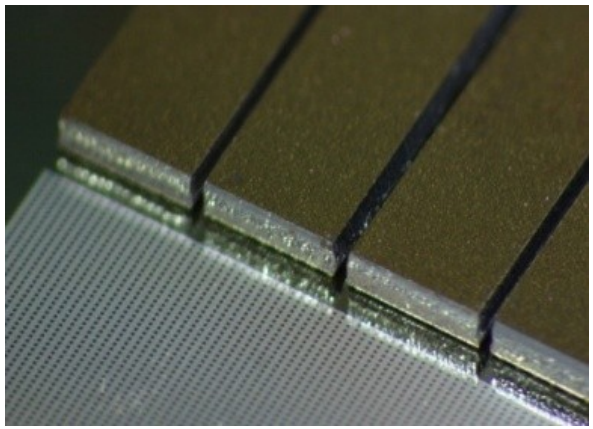
-: radii: 15, 26, 37, 48, 60 mm	14, 22 mm
-: ladder length: 125mm(L0) and 250mm(L1-4)	136 mm(L0) and 169mm(L1)
-: sensitive width: 11mm (L0), 15mm(L1), 22mm(L2-4)	12.5mm (L0, L1)
-: number of ladders: 10/11/12/16/20 → 130 sensors	8/12 → 40 sensors
-: pixel size: ≈20 µm	50x50 μm^2 (L0) 50x75 μm^2 (L1)
-: Row rate: ≈40 MHz	≈10 MHz
-: number of pixels: ≈800 Mpix	≈8 Mpix

And: minimal material for both!!!

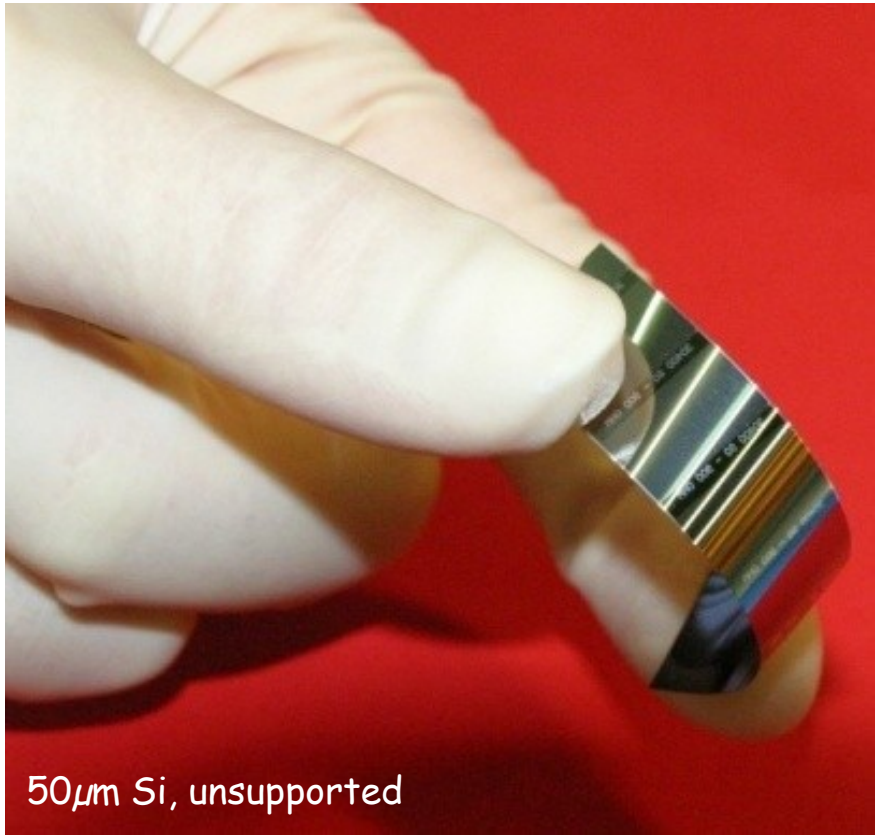
Thinning Technology – All Silicon Module







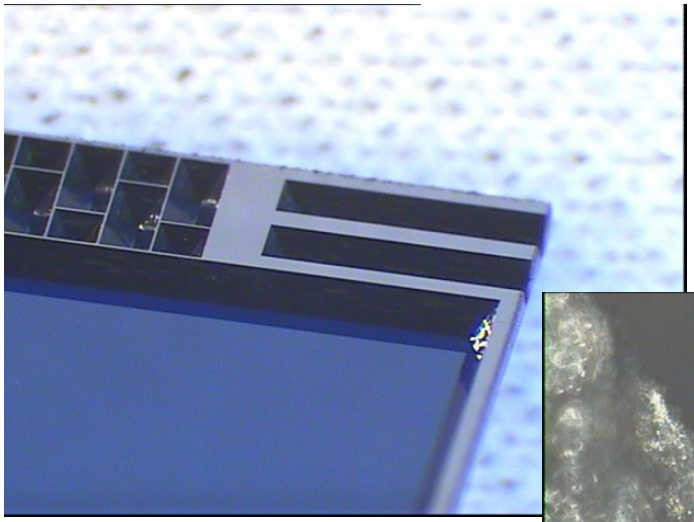
Self-supporting All-Silicon Module

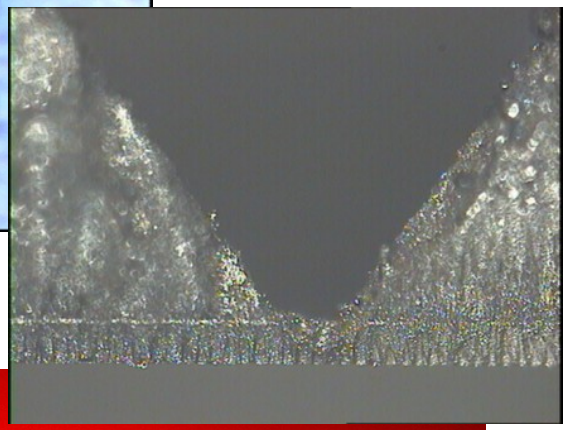


- Half-ladders (modules) are laser-cut
- Modules are supported by a monolithic silicon frame
- Two modules are assembled to one ladder
- overall length is 136 mm (inner) and 169 mm (outer)

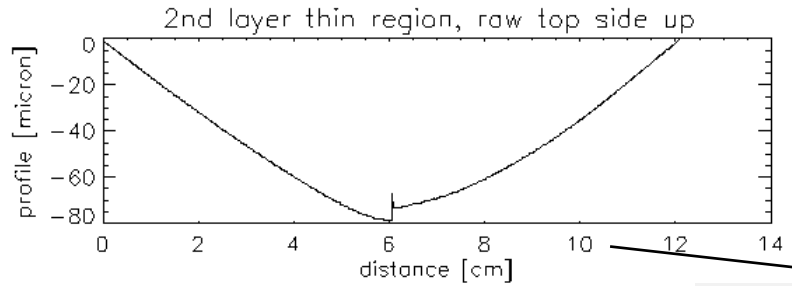
Micro joint between half-ladders

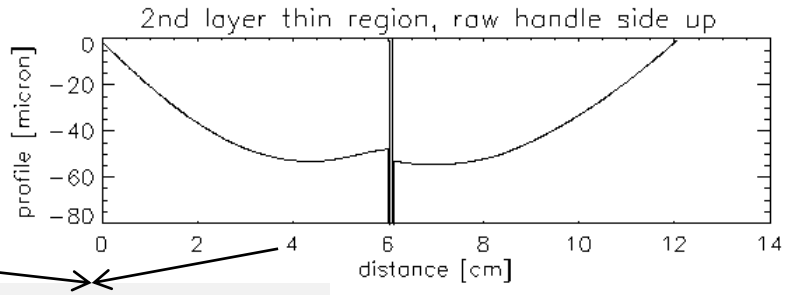
- butt-joint between two half-ladders
- reinforced with 3 ceramic inserts
- 2x300µm dead area per ladder



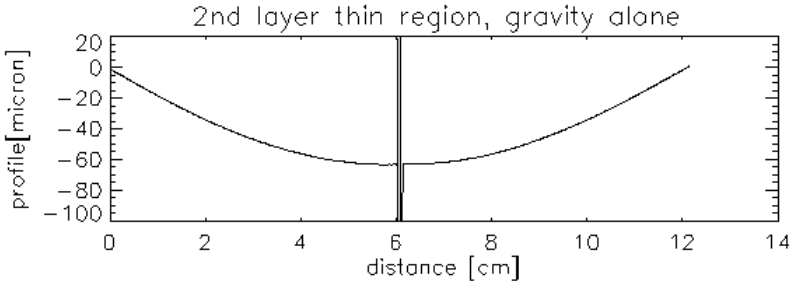


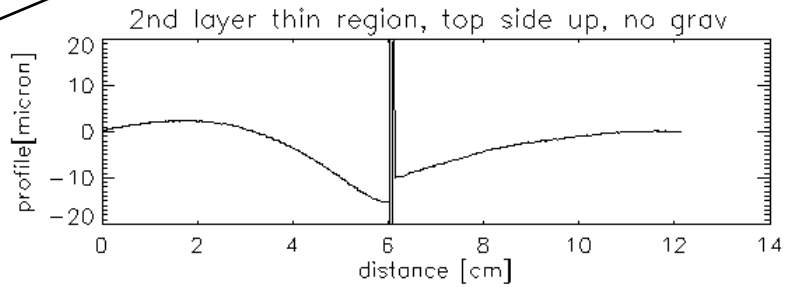
Micro joint between half-ladders

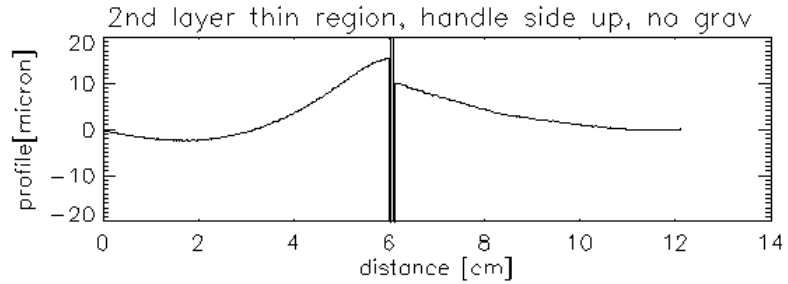




gravity effect = Δy/2

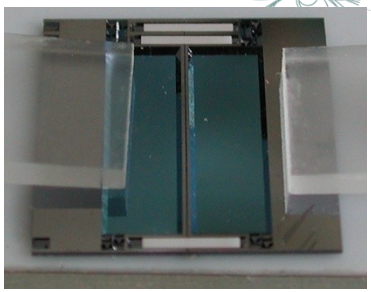


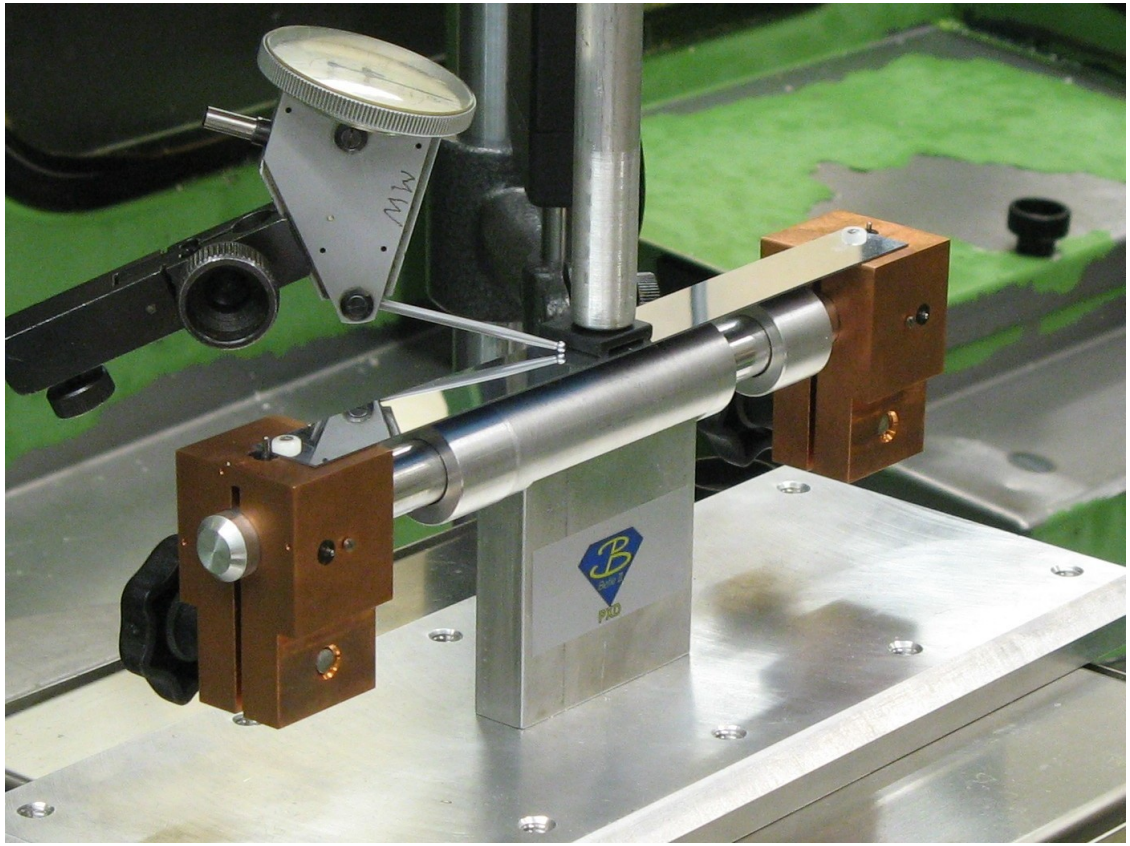




Micro joint between half-ladders

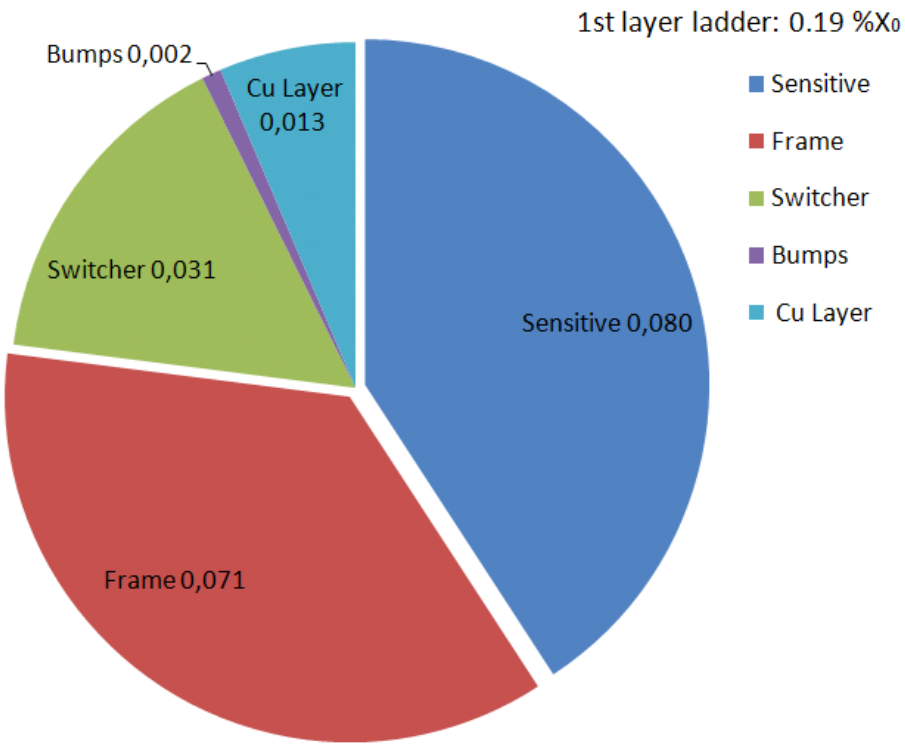
Mechanical tests → remarkably robust!!
-: Bowing: up to 1 mm sagitta (over 10 cm)
-: Tension: 40 to 60 N, then the Silicon broke





Total Material Budget within the Sensitive Volume (Belle II)

❑ sensitive area of the first layer ladder:	1.25x9.0 cm^2 (1.5x9.0 incl. frame), 75 µm thin
❑ support frame:	0.1+0.2 cm, 420 µm
❑ Switcher-Sensor Interconnect:	Gold stud bumps, one bump/connection, Φ=48 µm
❑ Cu Layer	t=3 µm, 50% coverage in acceptance
❑ Switcher dimensions:	0.15x0.36 cm^2
❑ Number of Switchers:	12 (32x2 channels per chip – gate and clear)
❑ Material reduction by frame perforation:	1/3

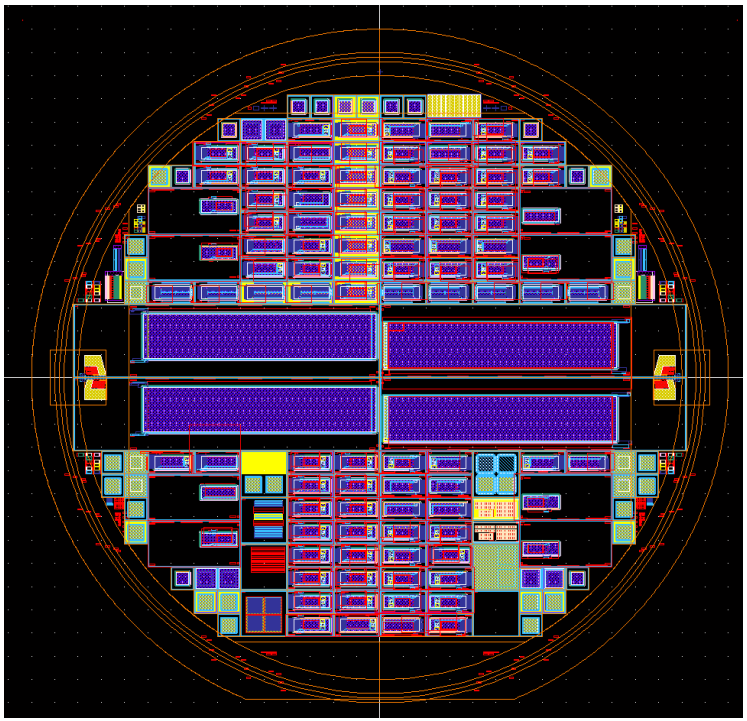


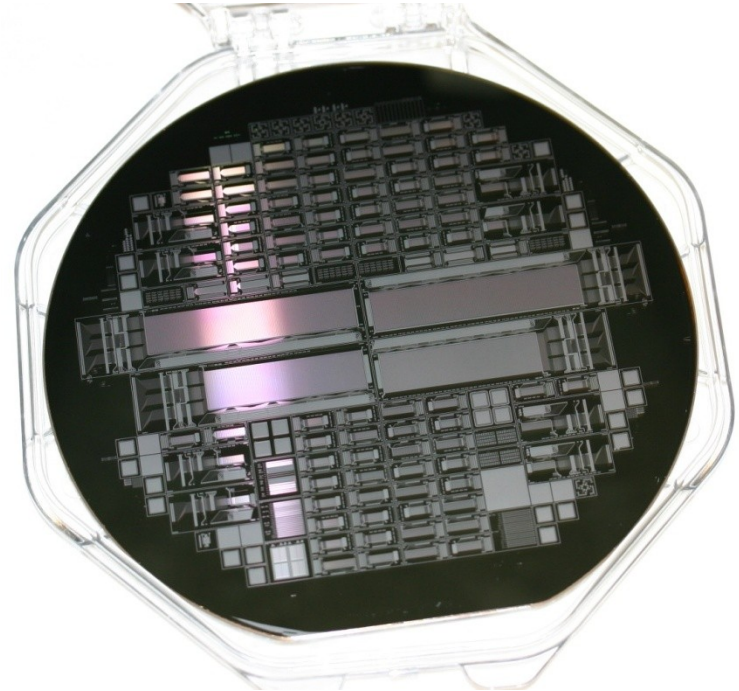
→ 0.19 %X_0 in total

Silicon contribution (0.15%) experimentally confirmed

PXD6 Batch: Prototyping for Belle II and ILC

- 8 SOI wafers (→ 50 µm in sensitive area) + 2 monitor wafers on standard thick material
- About 100 test matrices in different variations
  - pixel sizes from 20 µm to 200 µm
  - shorter gate length, improved clear structures, various field shapes..
- Technology variations on the wafer level (plasma etching)
- 4 half-ladders for Belle II with the most promising design options

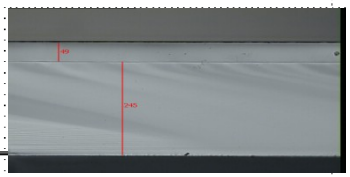


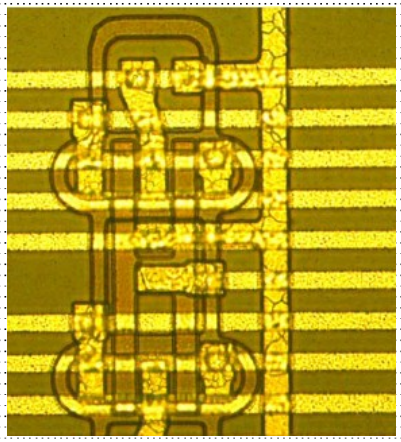


PXD6 Batch: Prototyping for Belle II and ILC

Fertigstellung DEPFET-Pixelproduktion pxd-5-3 — ges. 07.Mai.2008

Nr.	Vorgangsname	Dauer
1	**Oxidation, alin/alip, Nitrid1, ps0n, nd0n**	21 Tage
2	Oxidation, 230nm	3 Tage
3	Litho ALIN/ALIP	6 Tage
4	Justagemarken anätzen	3 Tage
5	Lithographie POXP/POXRP	6 Tage
6	Implantation	3 Tage
7	**Waferbonden Fa. Tracit**	21 Tage
8	Waferbonden	21 Tage
9	**Oxidation, Justagemarken**	12 Tage
10	Feuchte Oxidation, 180nm	2 Tage
11	Litho ALIP, MA-IR, Entwicklungslabor	3 Tage
12	Justagemarken anätzen, auf 50nm	2 Tage
13	Litho ALIN, MA-VS/RS, RR	3 Tage
14	Justagemarken anätzen, auf 90nm	2 Tage
15	**Poly1-Ebene, deep-Implante, NOXN**	56 Tage
16	LPCVD-Nitrid1 30nm	2 Tage
17	Implantation ME	3 Tage
18	LPCVD-Nitrid2 10nm	2 Tage
19	LPCVD-Poly1, 550°C, 600nm	1 Tag
20	LPCVD-LTO1, 100nm	1 Tag
21	3. Implantation Poly1, n-Seite, 140keV, 8E15cm-2	3 Tage
22	Rekristallisation, EANN-900, 1h	2 Tage
23	2. Lithographie PO1N	5 Tage
24	Strukturierung LTO1 n-Seite, SEZ	2 Tage
25	Strukturierung Poly1 n-Seite, SEZ	2 Tage
26	LTO1 beidseitig abätzen, SEZ	1 Tag
27	3. Lithographie PSHN	4 Tage
28	P-Kanal Implantation	3 Tage
29	4. Lithographie PDPN	4 Tage
30	5. Deep P-Implantation	3 Tage
31	Oxidation Poly1, FOX2-900, 215nm	2 Tage
32	Nitrid1 durchätzen, n-Seite, davor 2min HF-Dip	2 Tage
33	5. Lithographie ND1N	4 Tage
34	6. Deep N-Implantation	3 Tage
35	7. Lithographie NOXN	4 Tage
36	8. N+ Implantation, P 180keV, 1E15, Strombegrenzung!	3 Tage
37	**Poly2-Ebene, POXN**	32 Tage
38	LPCVD-Nitrid3, 730°C, 30nm	2 Tage
39	LPCVD-Poly2, 550°C, 500nm	1 Tag
40	LPCVD-LTO2, 100nm	1 Tag
41	9. Implantation Poly2, n-Seite	3 Tage
42	Rekristallisation, EANN-900, 1h	2 Tage
43	8. Lithographie PO2N	5 Tage
44	Strukturierung LTO2 n-Seite, SEZ	2 Tage
45	Strukturierung Poly2 n-Seite, SEZ	2 Tage
46	LTO2 beidseitig abätzen	1 Tag
47	Poly2, p-Seite abätzen, SEZ	2 Tage
48	Poly2 FOX-900, 215nm	2 Tage
49	Nitrid2 durchätzen, beidseitig, davor 2min HF-Dip	2 Tage
50	9. Lithographie POXN	4 Tage
51	8. P+ Implantation	3 Tage
52	**Poly p-Seite entfernen**	12 Tage
53	Polyoxid1 p-Seite abätzen, SEZ	2 Tage
54	Poly1 p-Seite abätzen, SEZ	2 Tage
55	defreckle p-Seite	2 Tage
56	LPCVD-LTO3, d=300nm	2 Tage
57	LTO3 abätzen, p-Seite	1 Tag
58	Nitrid1 p-Seite abätzen	2 Tage
59	Annealing NITDANN+H2T-450	1 Tag
60	**Kontakte ätzen, Metallebene 1**	25 Tage
61	Lithographie KO1N	5 Tage
62	LTO3+Oxide durchätzen, n-Seite	3 Tage
63	Metallisierung hot alu, n-Seite	2 Tage
64	11. Lithographie AL1N	5 Tage
65	Hotalu strukturieren n-Seite	3 Tage
66	Litho FRECN	3 Tage
67	Defreckle-etch n-Seite	2 Tage
68	LPCVD-LTO4 zmi, 600nm	2 Tage
69	**Kontakte ätzen, Metallebene 2**	18 Tage
70	Lithographie KO2N	5 Tage
71	LTO4 strukturieren, n-Seite, padetch	3 Tage
72	Metallisierung cold alu, n-Seite, softetch!	2 Tage
73	Lithographie AL2N	5 Tage
74	Alu2 strukturieren n-Seite	3 Tage
75	**Rückseitenprozedur**	40 Tage
76	Lithographie WINP, p-Seite	4 Tage
77	600nm lto4-zmi + 180nm th. Oxid durchätzen, p-Seite	3 Tage
78	TMAH-Ätzung, p-Seite	5 Tage
79	Litho WINPF	4 Tage
80	LTO4-zmi- + th. Oxid-Überhang entfernen	3 Tage
81	Litho KONP	4 Tage
82	th. Oxid p-Seite durchätzen	3 Tage
83	Sputtervorreinigung, Schutzlack n-Seite, LM-Reinigung	2 Tage
84	Metallisierung cold alu, p-Seite	2 Tage
85	12. Lithographie ALUP	3 Tage
86	Alu strukturieren p-Seite	2 Tage
87	H2T-400, inkl. Messen vorher/nachher	3 Tage
88	Endreinigung, Endkontrolle	2 Tage
89	cut	0 Tage

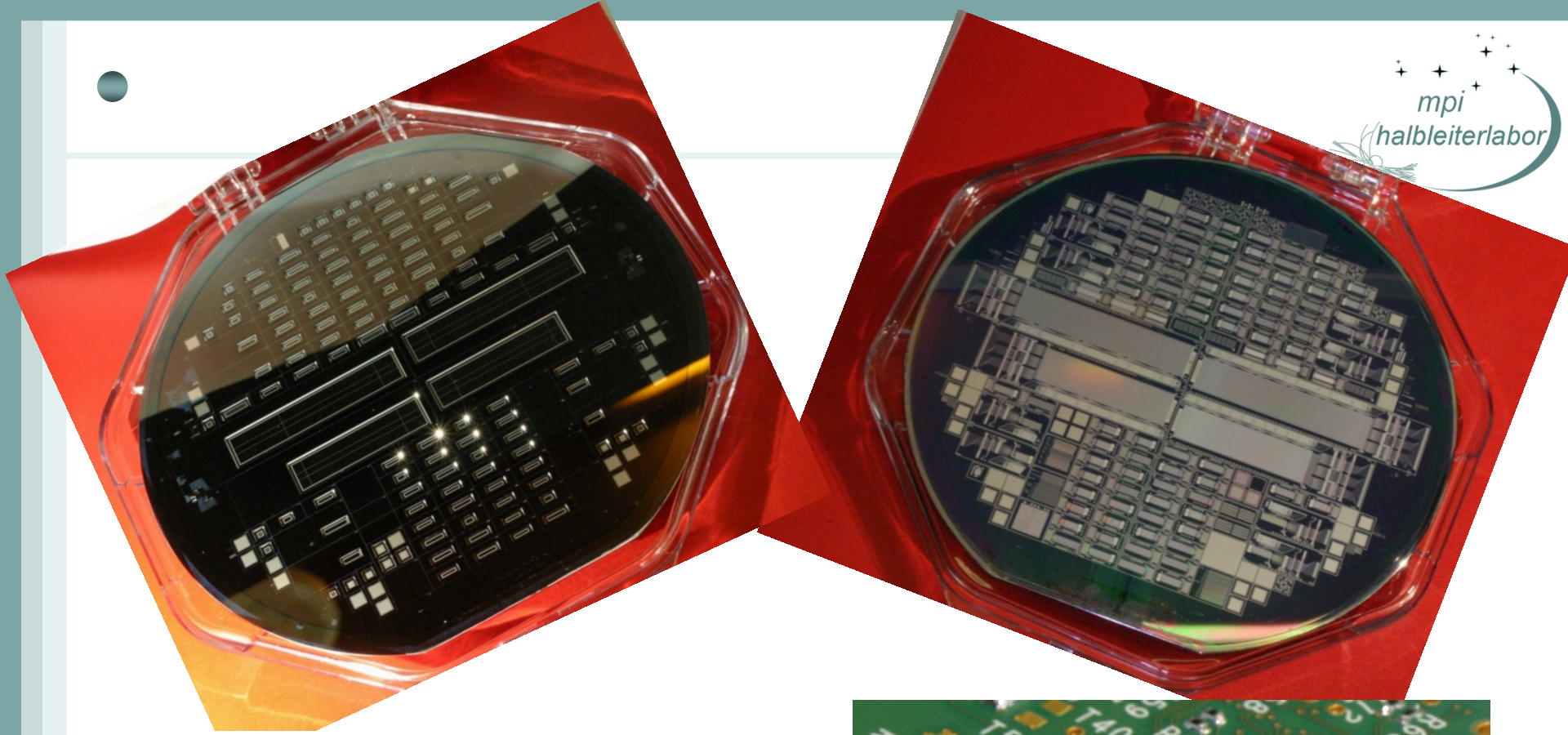


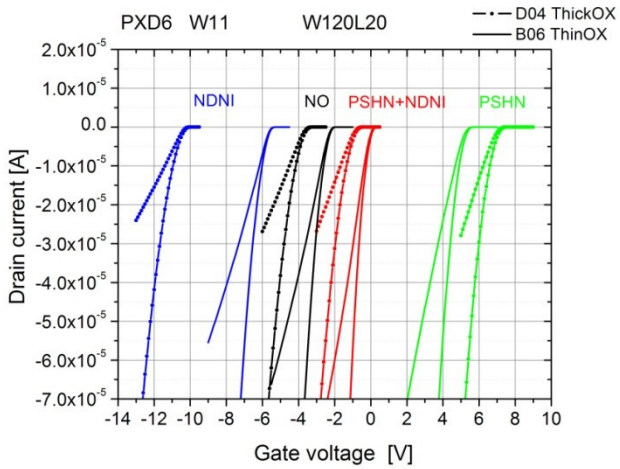


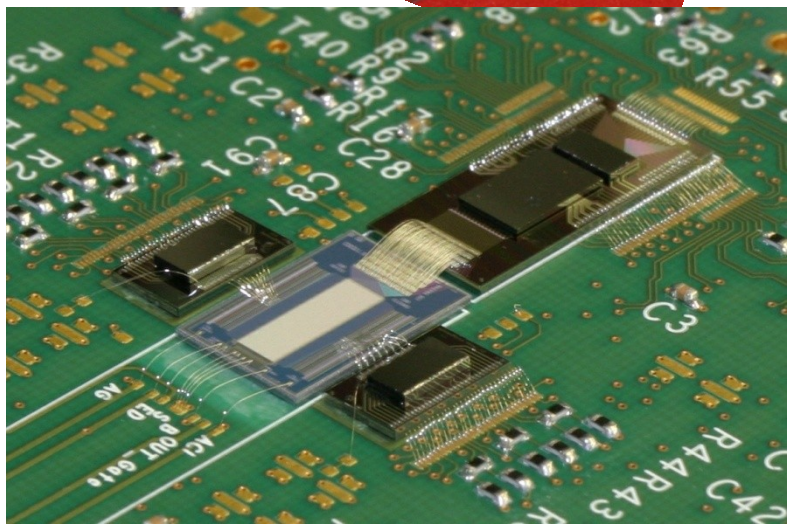
- 9 Implantations
- 19 Lithographies
- 2 Poly-layers
- 2 Alu-layers
- sums up to 89 steps with 1-5 WD each
- in between:
  - a lot of inspection steps!
  - process control, dummy wafer production..

→ **19 months processing time (16 after SOI pre-processing)**

We are now here – it's done ☺ (almost..)




PXD6 W11 W120L20
D04 ThickOX
B06 ThinOX
NDNI
NO
PSHN+NDNI
PSHN
Drain current [A]
Gate voltage [V]
2.0x10-5
1.0x10-5
0.0
-1.0x10-5
-2.0x10-5
-3.0x10-5
-4.0x10-5
-5.0x10-5
-6.0x10-5
-7.0x10-5
-14 -12 -10 -8 -6 -4 -2 0 2 4 6 8 10



In Summary: Achievements and Status and Future

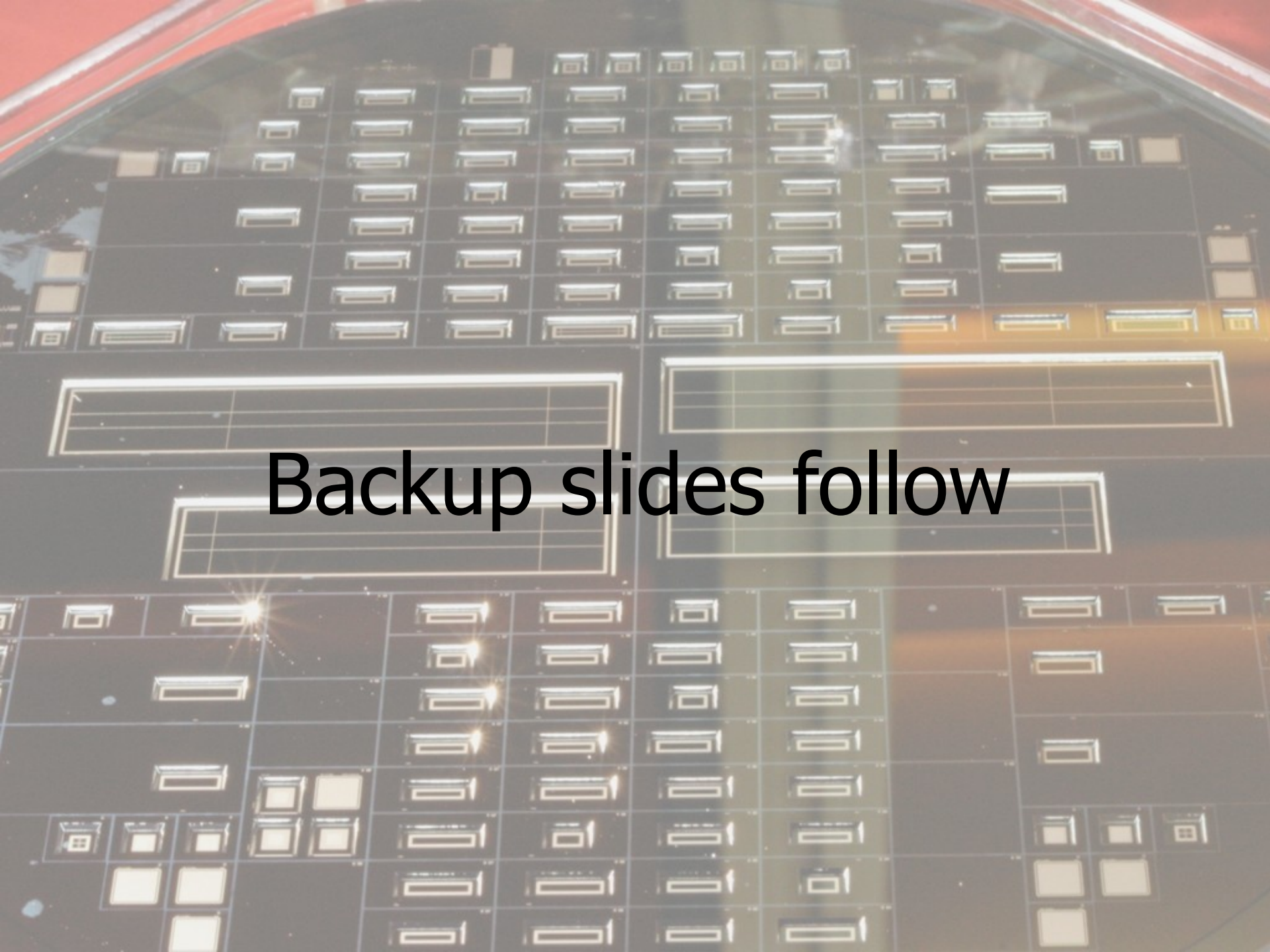
DEPFETs for the ILC VXD

- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ many test beams @ CERN:
  - ✓ S/N≈200 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. with 20 µm pixels: 1.0 µm @ 450 µm ←→ goal ≈ 4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm),

  design goal 0.11 % X_0
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad (static measurements up 8 Mrad) and ~10^{12} n_{eq}/cm^2

The Future

- DEPFET PXD @ Belle II gave a strong push to the project!!
- First thin DEPFETs are now being tested (ILC **and** Belle II)
- ILC and Belle DEPFETs are very similar, Belle II as "prototype" for ILC DEPFETs
- Read-out system design and detector simulation is now focusing on Belle II. We need to increase our effort at in least in the field of detector simulation to stay competitive in the ILC community.


Backup slides follow

ILC: The generic VXD at ILD

-: radii 15, 26, 37, 48, 60 mm

-: ladder length 125mm(L0) and 250mm(L1-4)

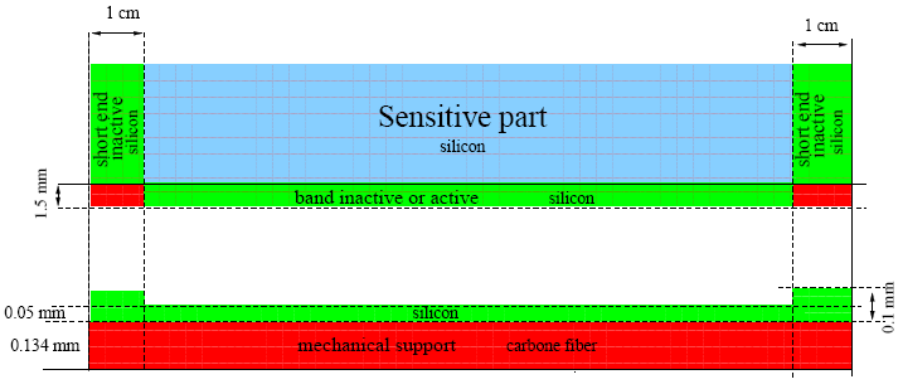
-: sensitive width 11mm (L0), 15mm(L1), 22mm(L2-4)

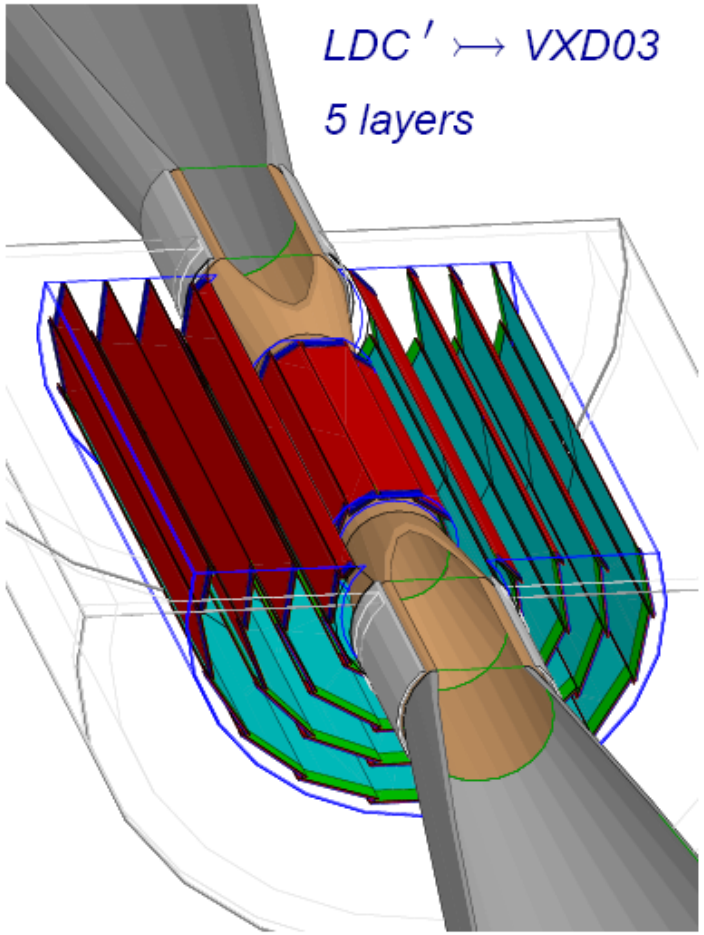
-: number of ladders: 10/11/12/16/20 → 130 sensors

-: acceptance $|\cos\theta| = 0.97$

-: pixel pitch ≈20 μm

-: number of pixels: ≈800 Mpix





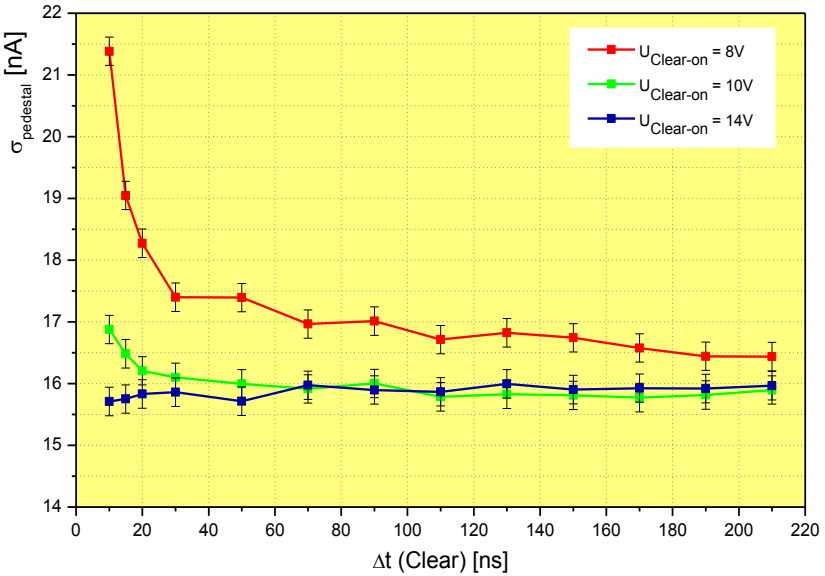
Minimal Material Contribution: 0.11% X_0 per layer

Fast Clearing

o Study clear efficiency for short clear pulses

Device with common clear gate

$U_{Clear\text{-}off}$ = 3 V



Complete clear in only 10-20 ns @ ΔV_{clear} = 11-7 V

Module Concept/Power Consumption

Total power consumption of the vtx-d in the active region (TDR design, 25 μm pixel)

DEPFET matrix only:

1st layer : 2 rows active, 30 μA · 5V · 650 · 2 · 8 = 1.6 W

2nd .. 5th layer: 1 row active, 30 μA · 5V · 1100 · 1 · 112 = 18.5 W

Steering chips: assuming 0.15 mW for an inactive, 300 mW for an active channel

1st layer : [(4998 · 0.15 mW)+(2 · 300mW)] · 8 = 10.8 W

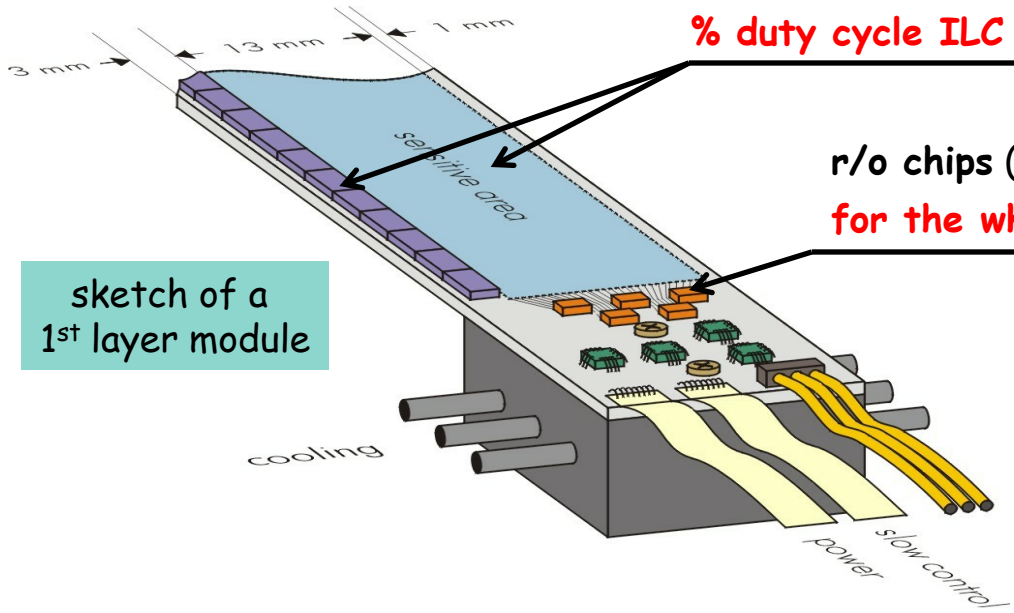
2nd ..5th layer: [(6249 · 0.15 mW)+(1 · 300mW)] · 112 = 138.6 W

Σ active region ≈ 170 W

% duty cycle ILC 1/200 → ≈ 0.9 W

r/o chips (current version):2.8 mW/chn.

for the whole vtx-d: ≈ 2W



sketch of a 1st layer module