R&D ACTIVITIES AT USC FOR FUTURE LINEAR COLLIDERS

VI Jornadas sobre la participación española en futuros aceleradores lineales

Daniel Esperante on behalf of the USC group

USC
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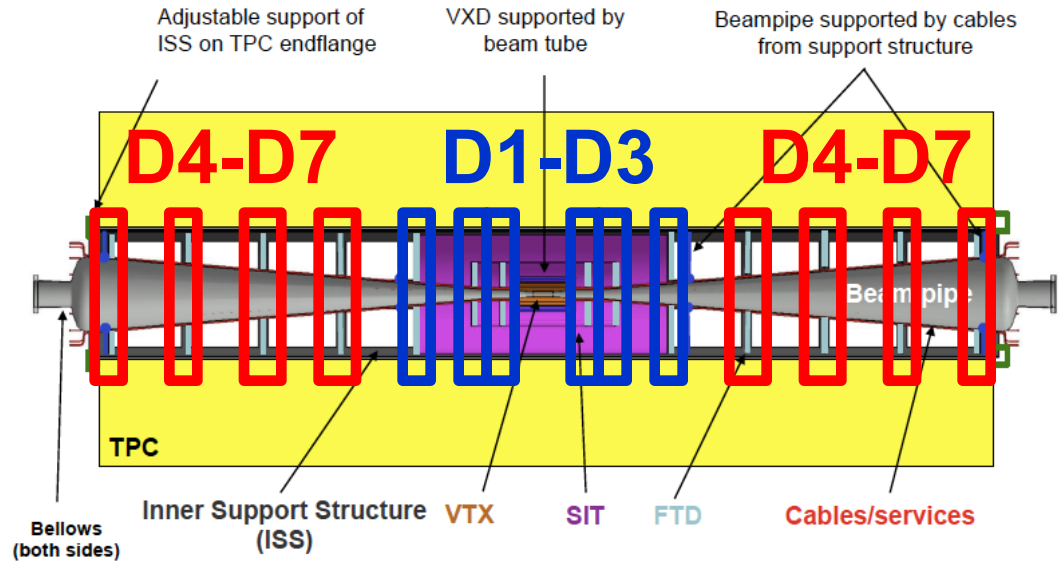
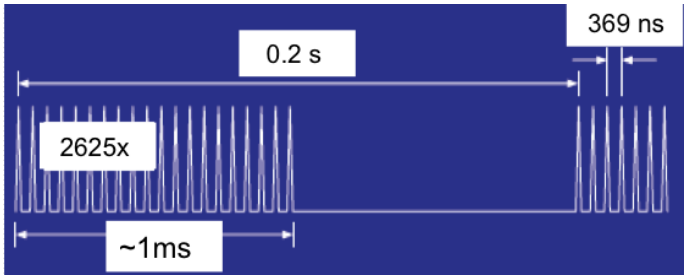
USC R&D FOR THE FORWARD TRACKER DETECTOR IN FUTURE LINEAR COLLIDERS

- Working approach in the USC for the FTD:
  - Active pixel thin sensors close to the IP D1-D3 disks
  - Fine-pitch thin microstrip sensors option in D4-D7 disks



Time structure of ILC



USC R&D ONGOING TASKS

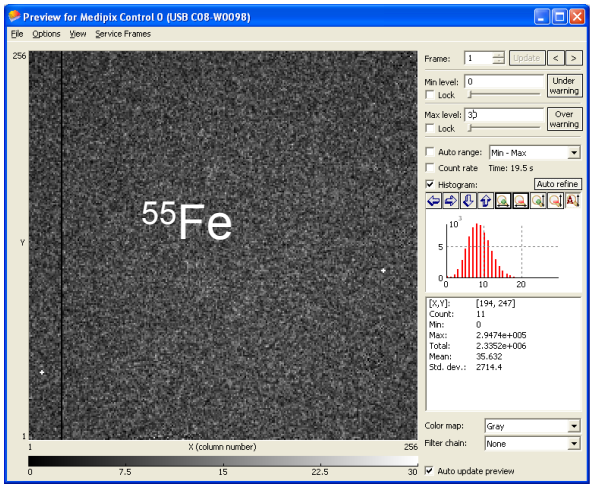
- Regarding to FLC project:
  - Active pixels:
    - Sensors:
      - Thinning of 2D-pixel (55x55 µm) sensor from 300 µm down to 200, 150, 100 µm, p-on-n & n-on-p (with CNM)
      - 1X3 ASIC-sensor assemblies and guard-ring studies (with CNM)
    - New assemblies with Medipix and Timepix and results
    - Next steps: characterization in lab, test-beams, and also irradiations and CVD cooling
  - R-ϕ silicon micro-strip fine-pitch technology:
    - Prototypes: new sensors (Hamamatsu), p-on-n, 200 µm thick, with 30 µm minimum pitch
    - Assemblies with D0 sensors (200 µm thick, 60 µm pitch with 30 µm intermediate strips), old R sensor, pitch adapter
    - Next steps: characterization in lab and test-beams
- Side developments:
  - High-speed readout copper link
  - Telescope Trigger Logic Unit (AIDA)

PIXEL TECHNOLOGY

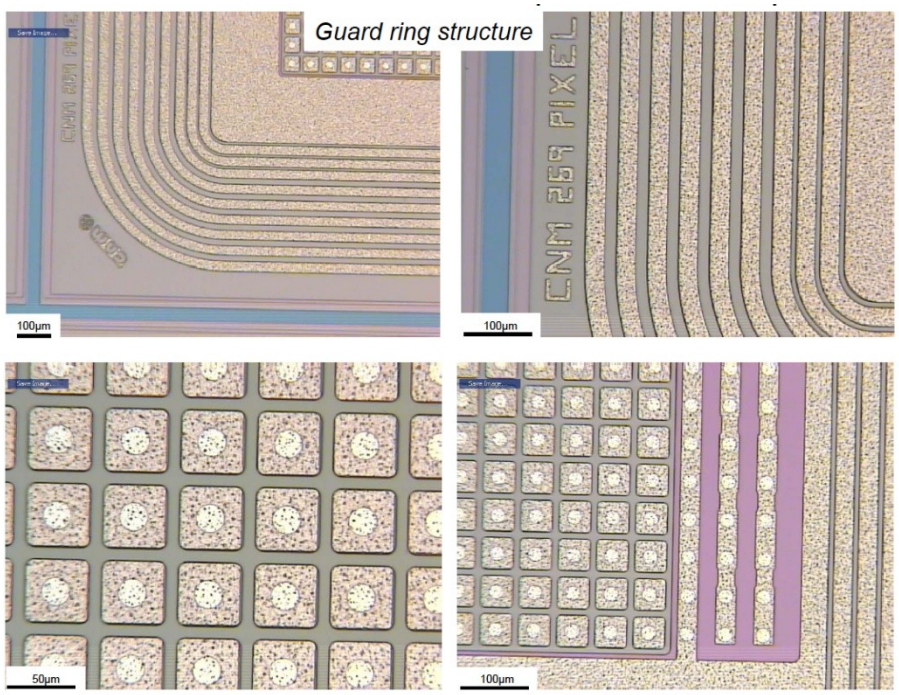
- Design driven parameters:
  - Low material budget (0.25 RL[%], first 3 disks of FTD)
  - Low power FEE
  - High resolution ~7 μm in R-φ
- R&D activities:
  - Optimization of pixel sensor geometry:
    - Sensor substrate thinning down to 100-150 μm
    - Bump bonding of thinned sensors onto the readout electronics (Timepix)
    - Minimal guard ring design, edgeless sensors
    - Characterization of the assemblies in the Lab (X rays, Laser, radioactive sources) and test with particles in beams
    - Module/Tile with 3 sensors/chips. This would be a prototype of a module to be installed in the first 3 disks of the FT
- R&D planned for the future:
  - Thinning of the read-out ASICs (Timepix-like) and bump bonding onto thin sensors, characterization in the Lab and test beams
  - Validate Timepix2 and evolutions:
    - ToT and ToA modes running simultaneously in each pixel
    - Data driven readout
    - Power cycling leading to a 70% reduction on the time the ROC

SENSOR THINNING (WITH CNM)

- Collaboration with CNM to thin 2D-pixel (55x55 µm) sensor from 300 µm down to 200, 150, 100 µm, p-on-n & n-on-p
- Readout with Timepix and Medipix3 ASIC (radiation hardness studies)
- Goal: measure the resolution, efficiency, rad-hardeness … of a thin sensor:
  - Minimal guard ring design
  - Production of thinned module/ladder with 3 ASICs

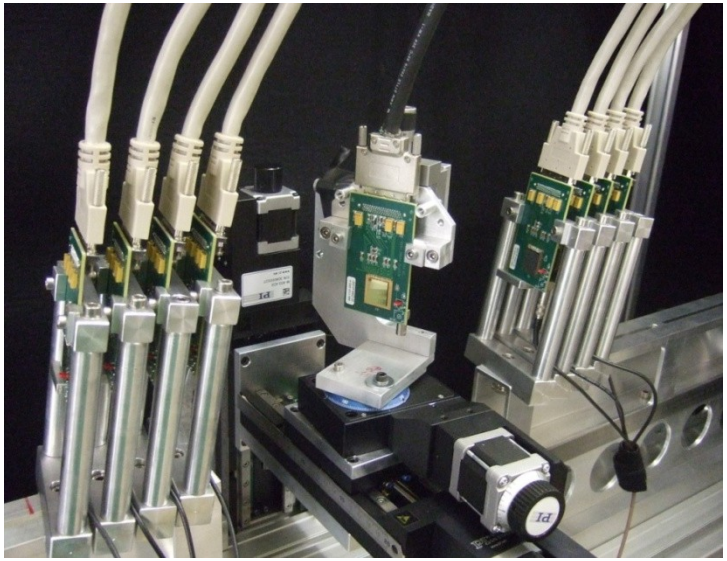


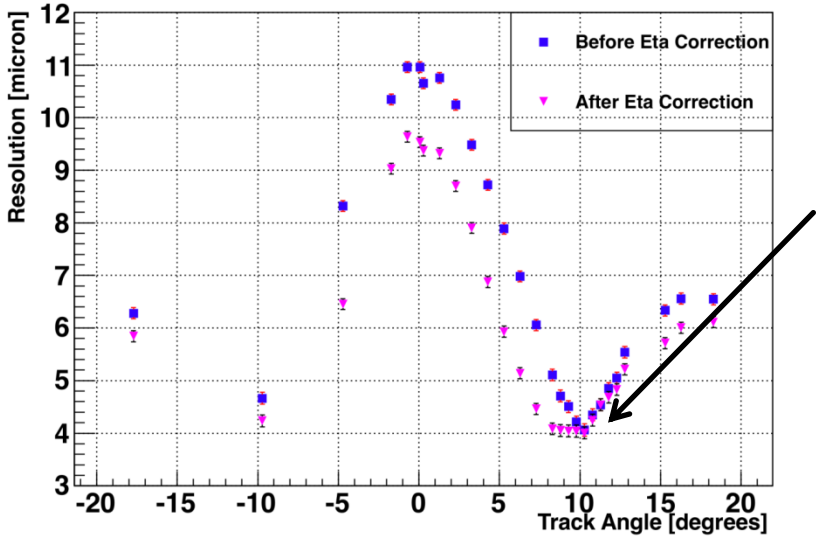
150µm



TEST-BEAMS: SENSORS AND TIMEPIX (WITH CERN)

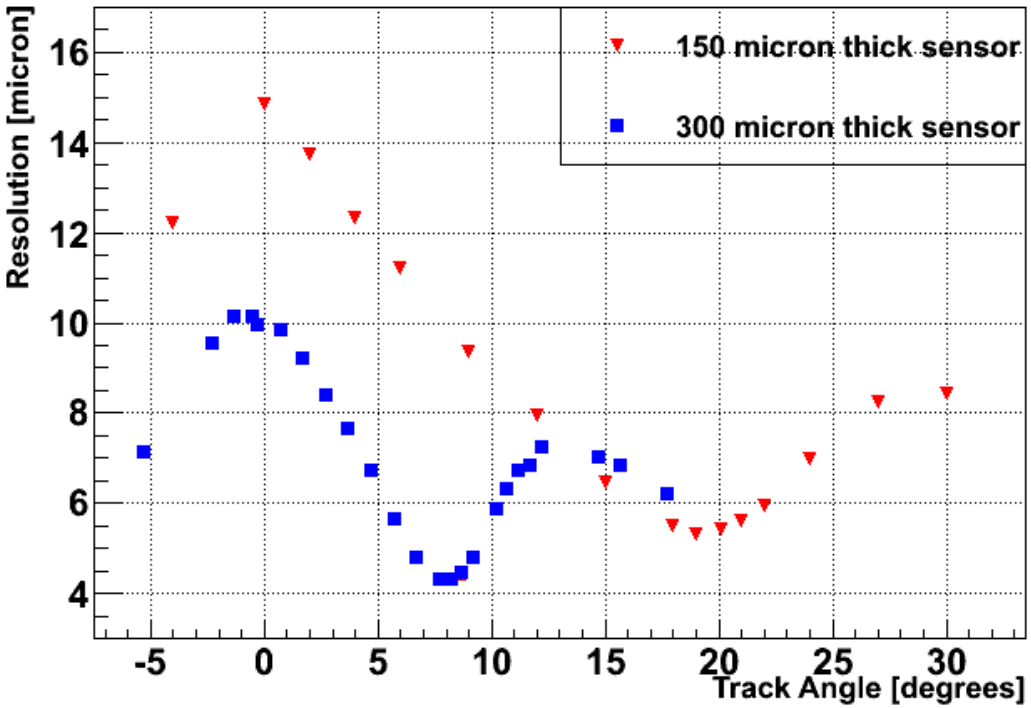
- Several testbems with Timepix telescope:
  - 55 x 55 μm pixels
  - 1.5 μm spatial resolution at DUT
  - 1 ns timing resolution
  - Up to 5kHz track rate
  - >1Mhz instantaneous beam rate
- Main measurements:
  - Resolution vs. Angle
  - Resolution vs. Threshold
  - Resolution vs. Silicon Bias
  - Efficiency vs. Threshold
  - Efficiency vs. Bias
  - Timewalk



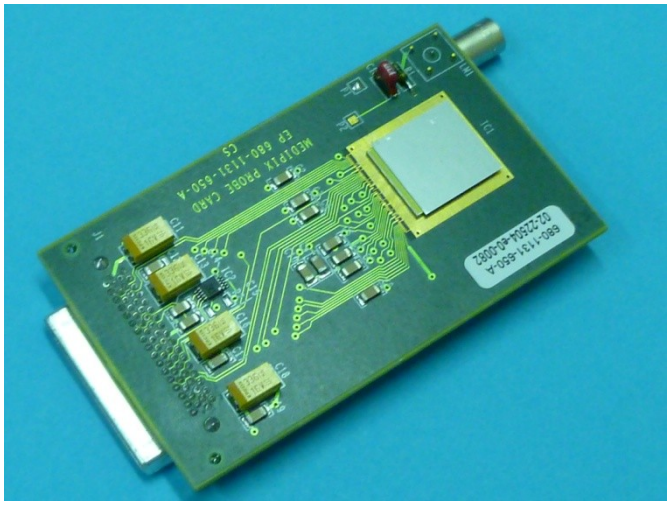


Operating point of Telescope planes

THINNED SENSOR RESULTS: 150 µM P-ON-N

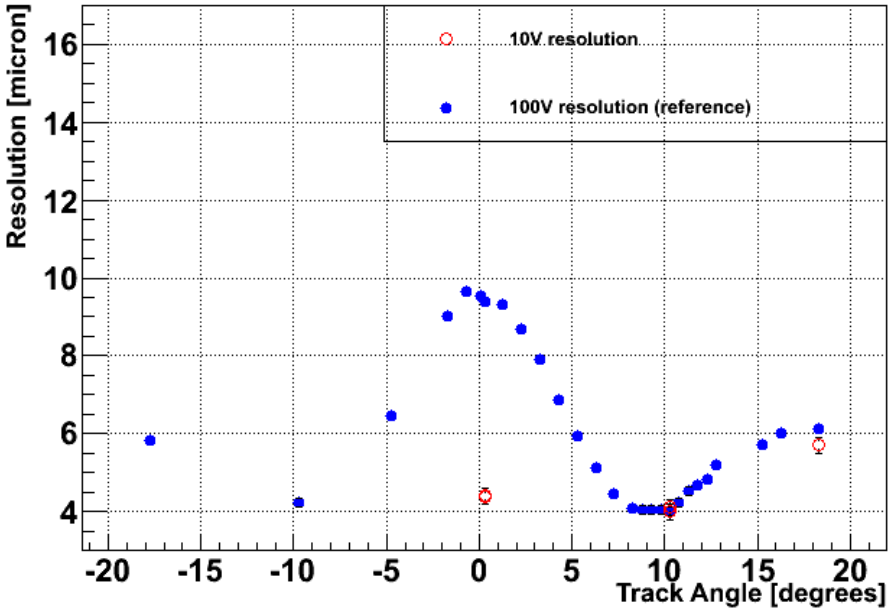


150 µm assembly characterized in the testbeam



- Resolution below 6 µm for the 150 µm sensor
- With a 150 µm sensor the optimum resolution point is at twice the angle of a 300 µm.

A HIGHLIGHTED RESULT WITH 300 µM SENSOR

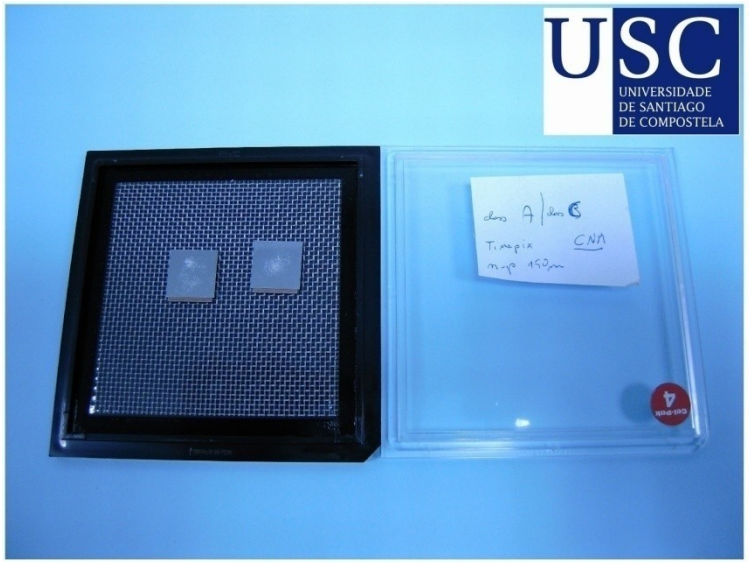


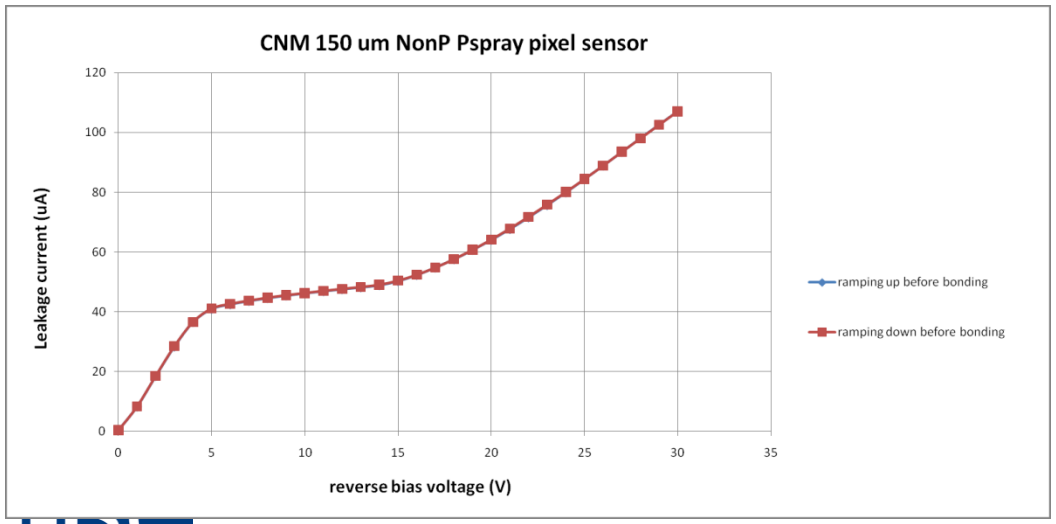
- Important result that implies that we can be close to optimum resolution without being at optimum angle:
  - 10V data (close to depletion)
  - 100V data (over-depleted)
  - There is an enormous gain at lower voltage

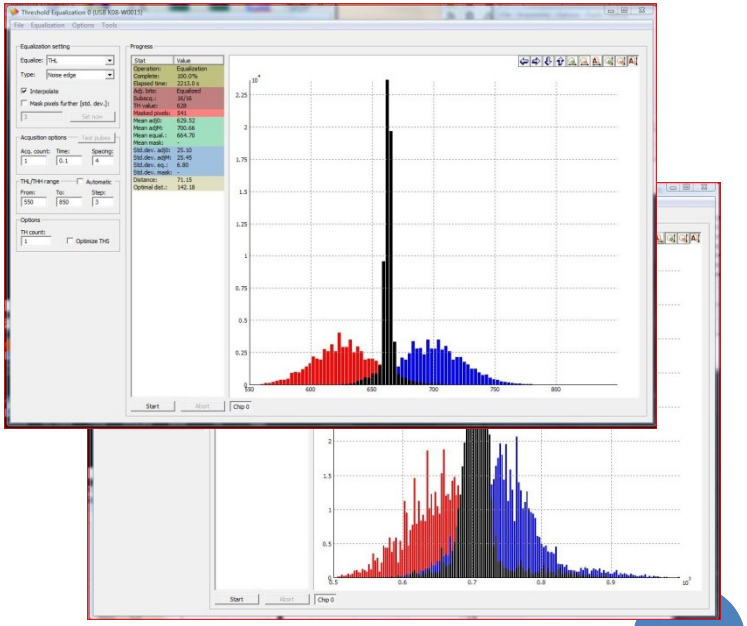
- We want to investigate this with the thinned sensor

NEW ASSEMBLIES (WITH CNM)

- Timepix sensors:
  - n-on-p, **150 µm**, 55x55 µm pixels
  - P-spray not completely tuned by CNM
  - To be characterized in lab:
    - Equalization scans and I-V curves already performed
    - Characterization with laser (after opening a window in the metallization)
    - Energy calibration with radioactive sources
  - To characterize also in test beam





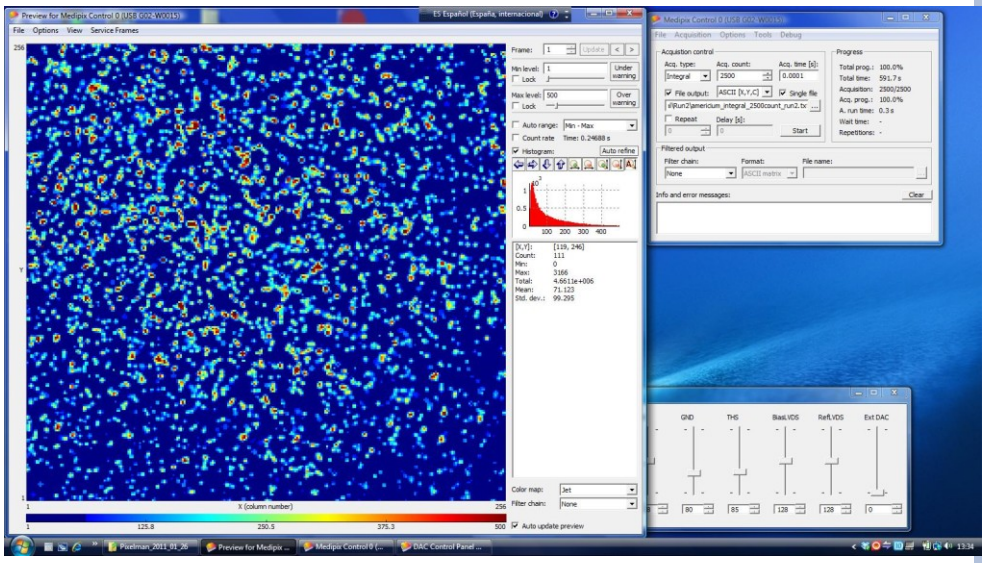


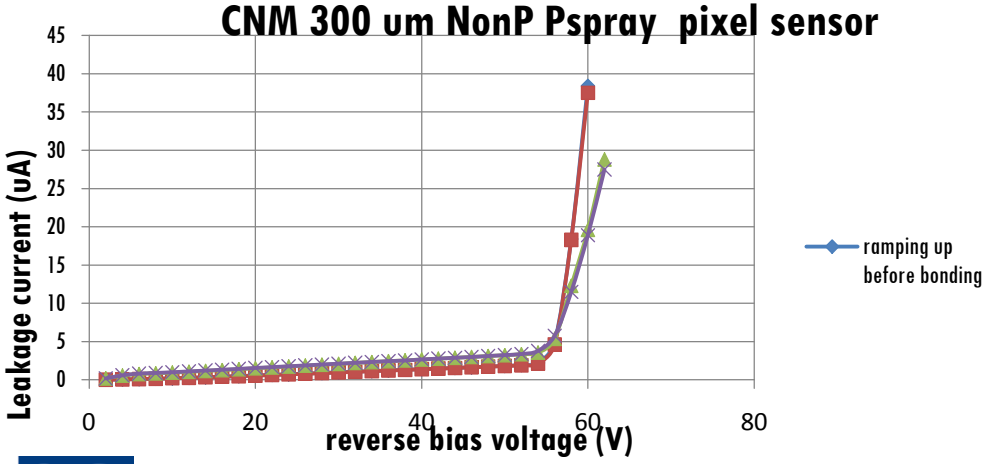
Threshold equalization

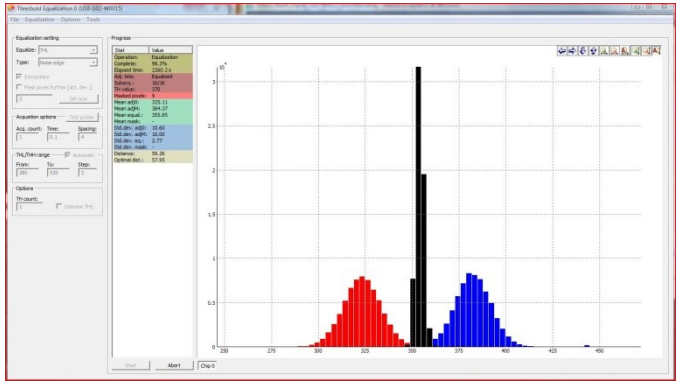
NEW ASSEMBLIES (WITH CNM)

- Timepix sensors:
  - n-on-p, **300 µm**, 55x55 µm pixels
  - P-spray not completely tuned by CNM
  - To be characterized in lab:
    - Equalization scans and I-V curves already performed
    - Characterization with laser (after opening a window in the metallization)
    - Energy calibration with radioactive source

Pixel-map with source after opening 2x2 mm window in the metallization



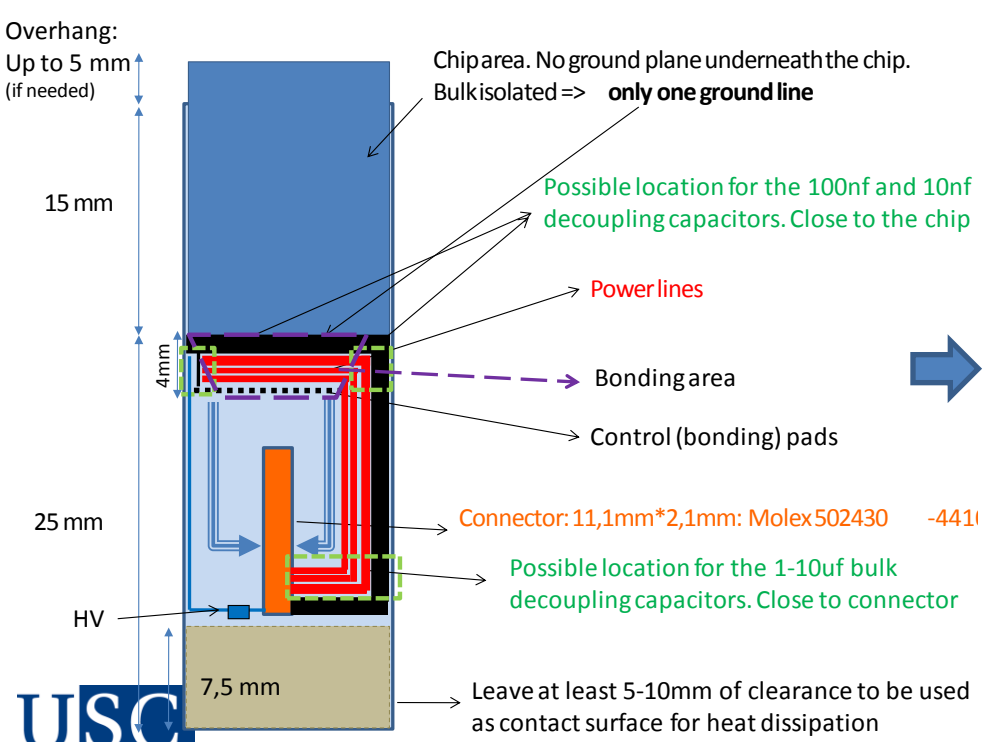




Threshold equalization

IRRADIATIONS AND CVD COOLING (WITH CERN)

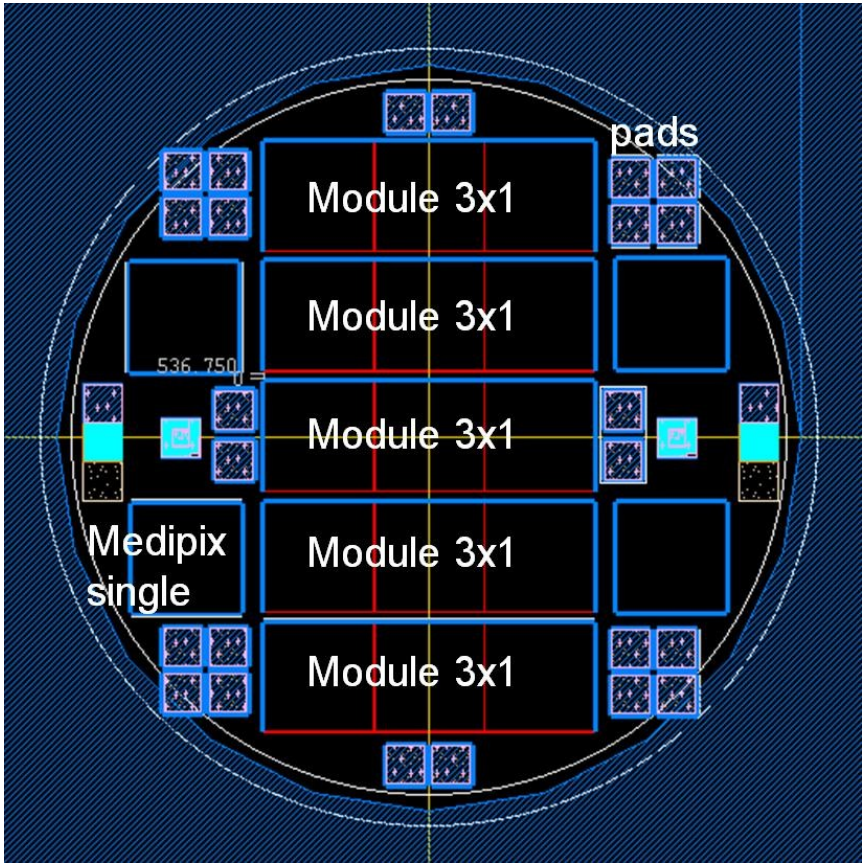
- Irradiate assembly with Medipix3 + 'n-on-p' sensor
- Heat dissipation is an issue:
  - Research CVD diamond support with lithography



Molex slimstack connector
1mm mated height

NEW 1X3 MODULES (WITH CNM)

- Build 1x3 tiles with standard guard-ring:
  - Try bump-bonding in large structures
- Build test structures to optimize guard-ring:
  - Minimal guard-ring to reduce dead areas
- Study p-stop and p-spray pixels guarding



(Preliminary mask by G. Pellegrini)

TIMEPIX AND TIMEPIX2 (WITH CERN)

Timepix

- Square Pixel size (55 μm x 55 μm)
- IBM 250 nm CMOS process
- Low occupancy is suited to ToT measurement, with no loss from 1 us deadtime
- Changes needed
  - Replace shutter based readout/acquisition scheme by continuous, dead-timeless operation
  - Sustained readout of pixels with maximum flux 5 particles /cm2/25 ns
  - Reduced ToT range and resolution
  - Add bunchtime identification good within 25 ns

Timepix2

- Timepix2 is an important step forward
  - 130 nm process
  - Improved (faster) front end
  - Fast column bus
  - Data driven readout
  - Simultaneous Time Over Threshold and Time of Arrival measurements
- Timepix2 by end 2011
- Evolutions from 2012 on in 130, 90 and 65 nm and faster readout

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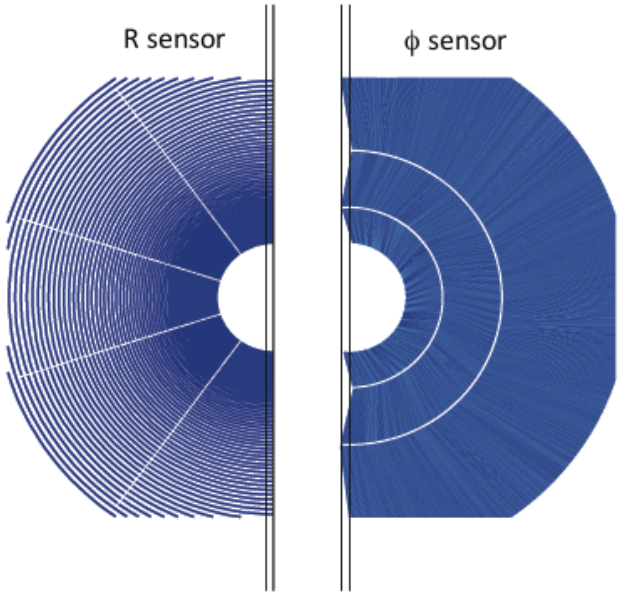
STRIP TECHNOLOGY

- Design driven parameters:
  - Low material budget (0.65 RL[%], last 4 disks of FTD)
  - Low power FEE
  - High resolution ~7 μm in R-φ
- R&D planned:
  - Optimization of sensor parameters:
    - Minimum pitch 25-30 μm
    - Sensor thickness (~200 μm)
    - Strip length, routing scheme of readout strips
    - Removal of pitch adapter (SNR issues)
    - Design of edgeless sensors
  - Construction of first prototypes standard thickness, evaluation of resolution:
    - 40 μm pitch, 300 μm already instrumented with Beetle ASICs
    - 30 μm pitch design to be sent to Hamamatsu for production
  - Characterization of prototypes in particle beams with Beetle readout chip

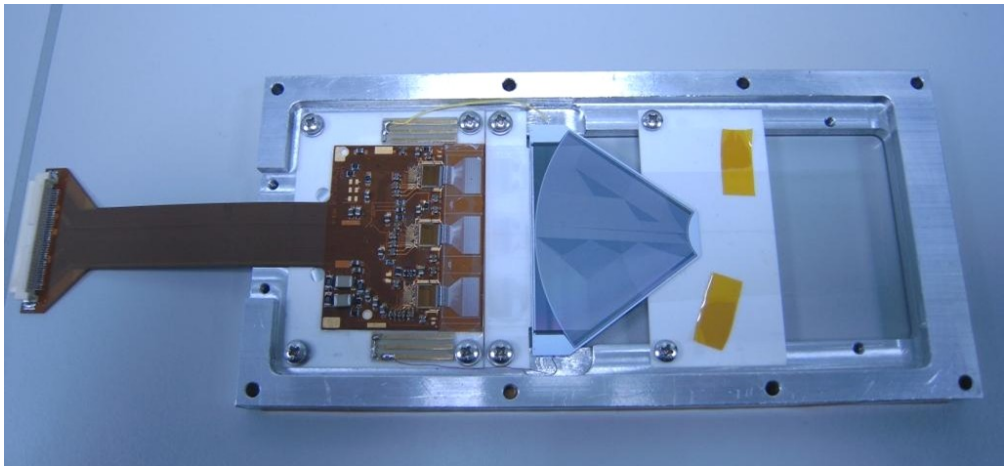
R-PHI SENSOR (GLASGOW, CERN, USC)

- New R-Phi sensor prototypes:
  - Order sent to Hamamatsu
  - P-on-n, 200 µm thick, with 30 µm minimum pitch
  - The USC will take care on the assembly of prototypes
  - Also in the testing in lab with LHCb TT-Hybrid (Beetles), Alibava and modified DB and in test-beam with Timepix telescope and Beetle-TELL1 readout



MICRO-STRIPS, PR01

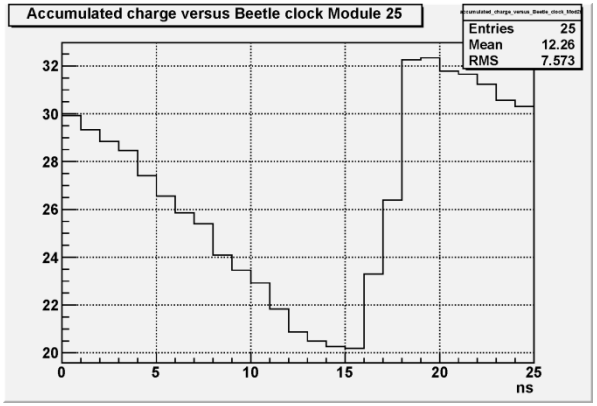
- This is an old Hamamatsu sensor:
  - (n^+n) sensor p-stop,
  - 300 µm thickness
- We have instrumented with an IT-hybrid (3 Beetle chips)
- We have also setup the need readout and trigger electronics and software as well as worked in the development of the Timepix telescope
- The aim is to measure eta and resolution for fine pitch with fast electronics, tested in test beam May 2010

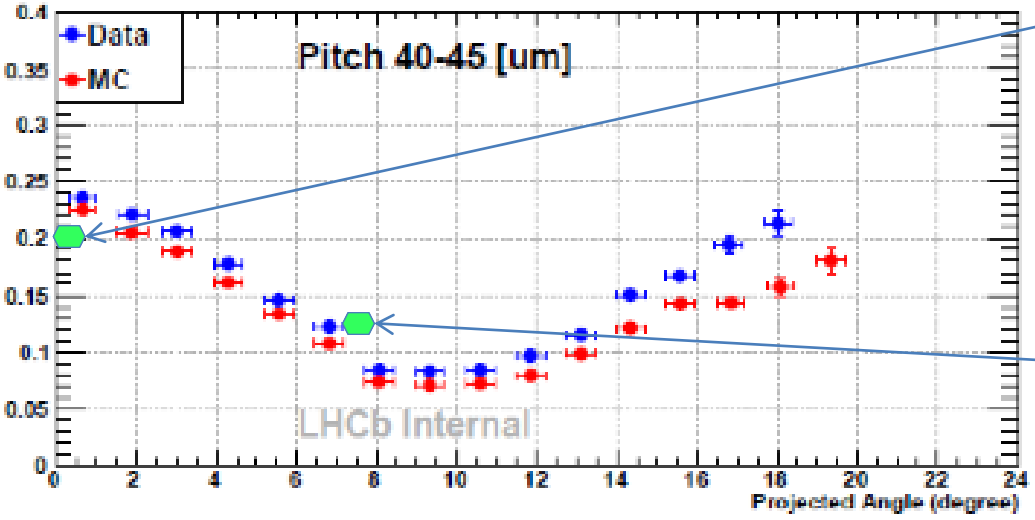


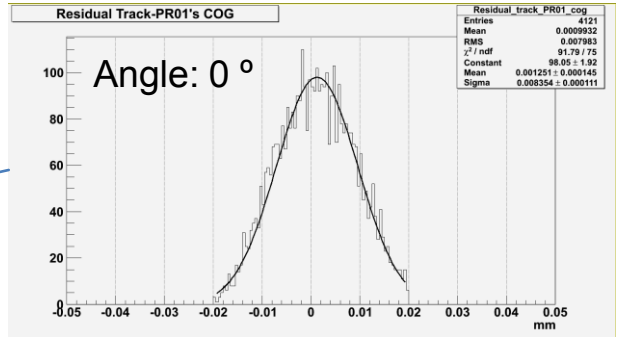
MICRO-STRIPS, PR01 RESULTS

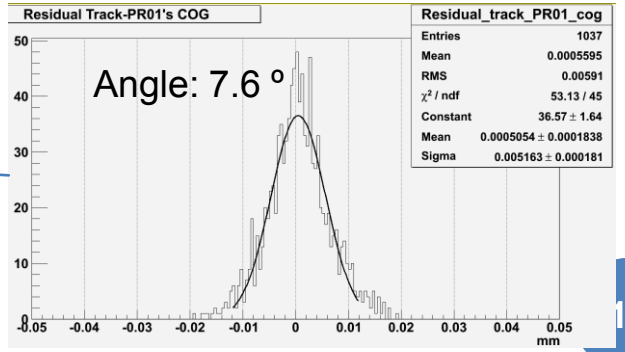
- Currently analyzing the results. We did not achieve the optimum results yet, but we are close. We are working on it:
  - At 0º it seems that we get a resolution a bit better than expected (8.3 = 0.207*(pitch))
  - At 7.6º , is slightly worse, but we know that this is due to a lack of charge that we observe in the pulseshape

Pulseshape, 25ns window



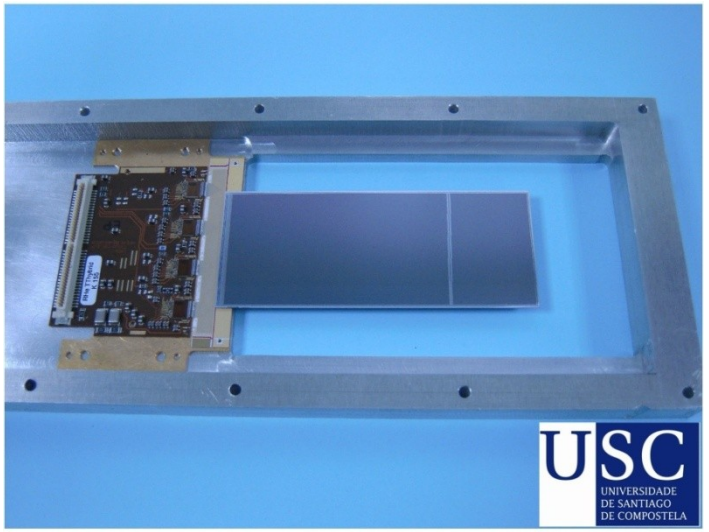




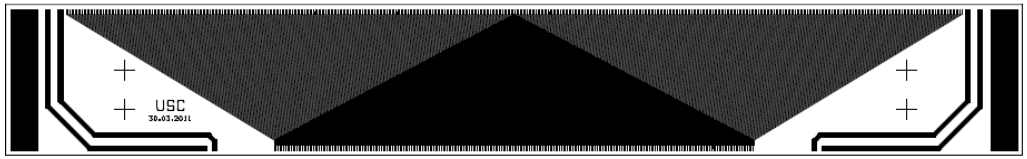


OTHER MICRO-STRIP ASSEMBLIES

- D0 sensors with fast readout:
  - TT hyhbrid, 4 Beetle chips
  - Sensors: p-on-n, 200 µm thick, 60 µm pitch with 30 µm intermediate strips)
  - Tests in lab and test-beam



- Pitch-adapters:
  - Try to build it in Santiago
  - Two options:
    - Based of metallized cristal substrate from Optimask
    - Or ceramic substrate



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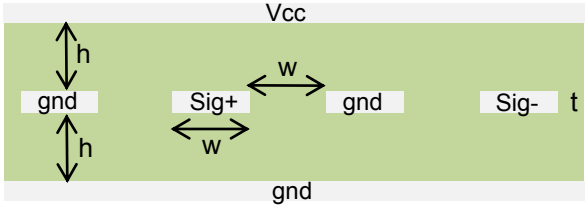
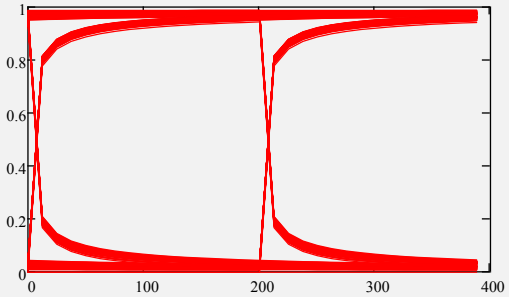
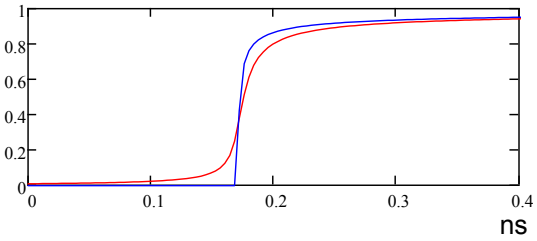
HIGH SPEED LINK (WITH CERN)

- Read-out speed is a concern in current high-density pixel detectors since effective data Tx rate goes above Gbits. Typical issues:
  - Zero suppresion needed in the chip
  - Local copper interface to a high speed opctical link
- Problems to face:
  - Skin effect in conductor and dielectric losses
  - Control the cable mechanical parameters to achieve the desired electrical performance
  - Signal compensation needed if distances above several tens of cm
- USC activity:
  - Prototype cable to asses the performance of a high-speed flex cable 'Pyralux® AP-PLUS' from 'Dupont'
  - Characterize radiation hardness and high frequency behavior of different configurations:
    - With network analyzer
    - FPGA high speed custom system





Eye diagram for R_0, L=65 cm and 5Gbit/s.
Skin effect only.



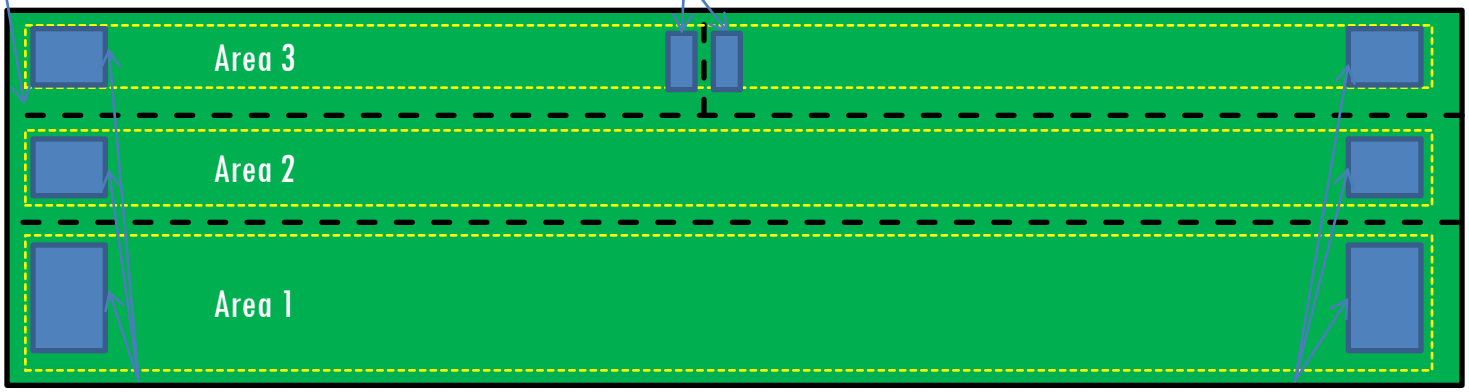
Step response L=65 cm and LCP:
Blue = skin-effect only.
Red = including dielectric loss.

HIGH SPEED LINK (WITH CERN)

Cable assembly:

Cut-out lines

Male-female
miniature connectors

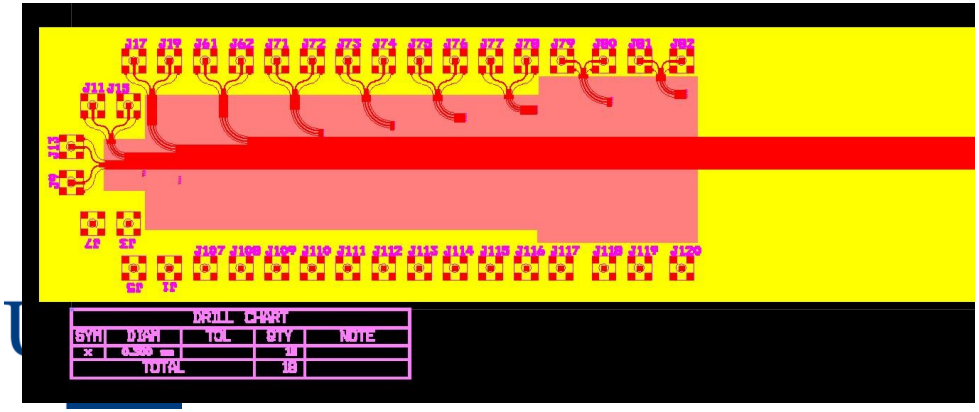


SMC connectors

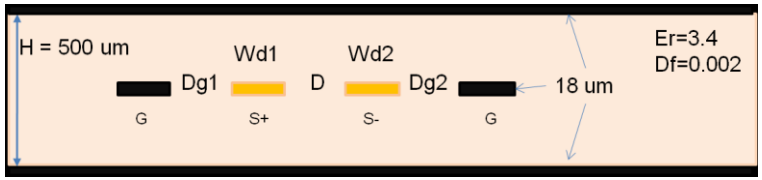
SMC connectors

- Area1: to study parameters of coupled differential lines
- Area2: to study parameters of decoupled strip-lines
- Area3: to place a miniature fine pitch connector and test a Tx line with the connector. This area is cut-off in two pieces out of the rest of the assembly.

Layout development:



Parameters to scan:

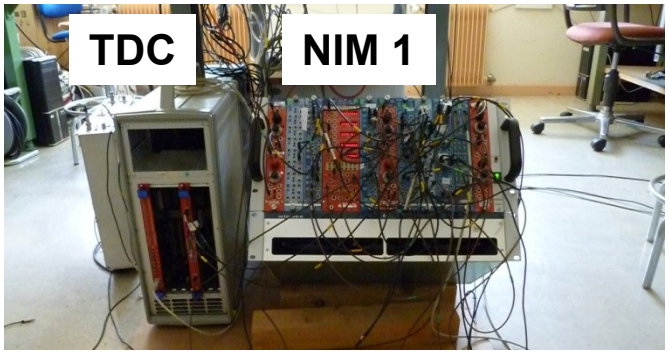


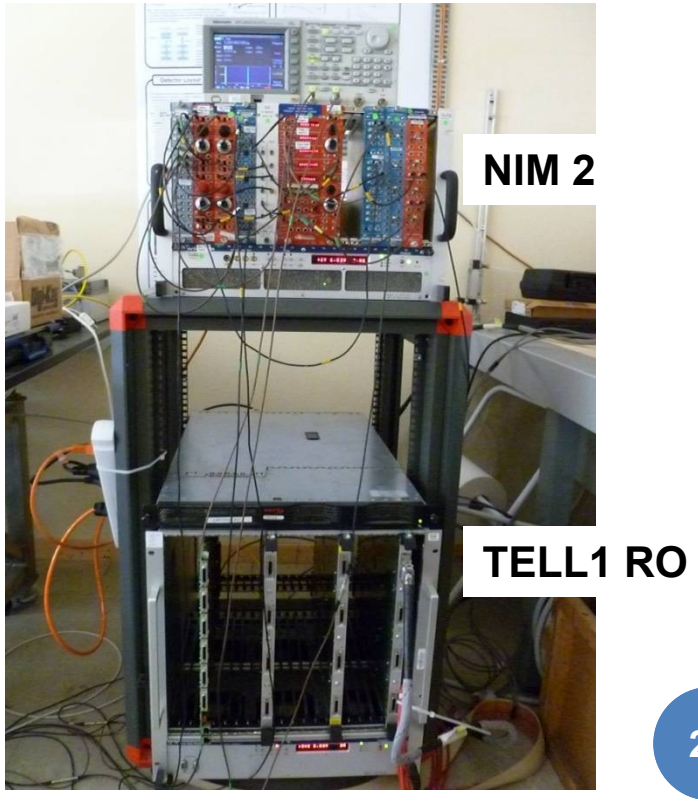
TRIGGER LOGIC UNIT (TLU) (LINKS TO AIDA PROJECT)

- Timepix Telescope arm is a AIDA Deliverable

- Trigger Logic Unit: currently we use 2 NIM crates and a VME TDC to perform timing tasks
  - Controlling the Shutter – eg selecting X particles per frame
  - Providing triggers to external systems
  - Measuring the phase between synchronised and unsynchronised triggers

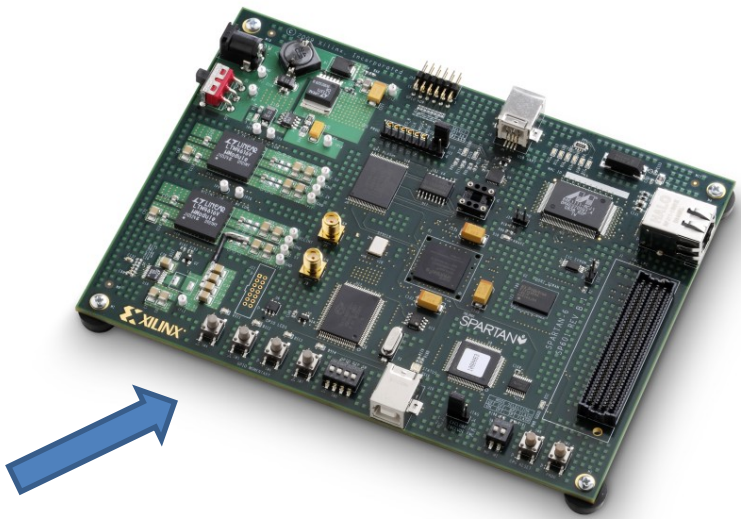
- The development of a trigger logic unit common to the EUDET and Timepix telescope under considaration. Already got in touch with David Cussans (developer of previous EUDET TLU) to build a portable based TLU replacement





TLU (LINKS TO AIDA PROJECT)

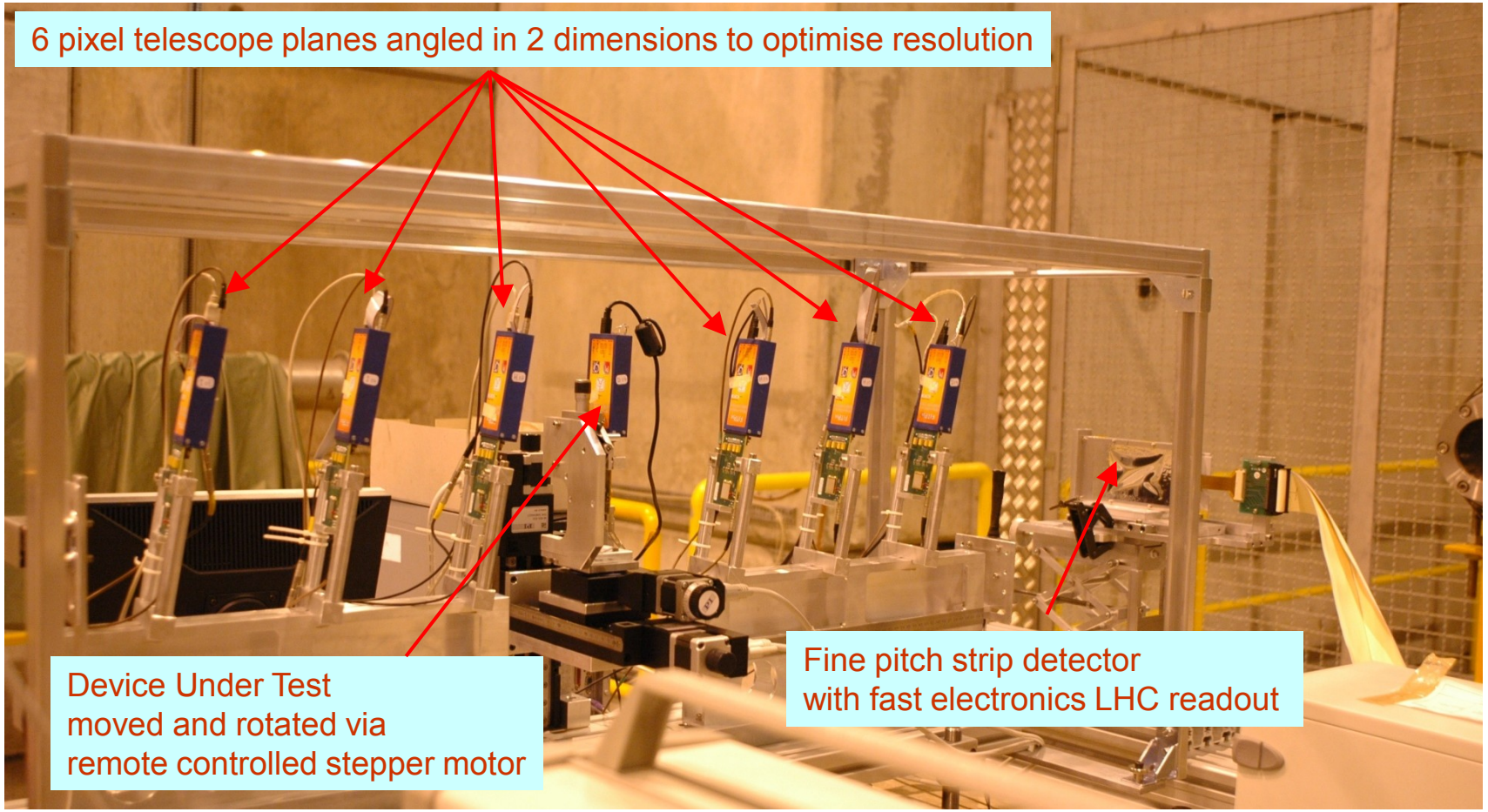
- The first idea was to build a TLU only for the Timepix telescope design based on VHDL and Altera (Stratix II) development board:
  - Embedded system, remote configurable, GBE data output, several on-chip TDCs…
  - A solution was presented to the collaboration
- But, finally, the idea to converge to a common TLU has prevailed:
  - Moved to Xilinx SPARTAN-6 FPGA development board, the same as the future EUDET TLU
  - Currently studying how to integrate both systems



SUMMARY

- USC is focused on sensor R&D for the FTD in future linear colliders:
  - Thin pixel sensors are being evaluated with Timepix-like readout for the inner part:
    - Spatial and time resolution, S/N and radiation hardness
  - Fine pitch thin microstrip sensor in R-Phi geometry for the outer region:
    - Spatial resolution, S/N and radiation hardness
- Tile-module prototyping ongoing:
  - Develop the technique to produce large area detectors
- High speed copper link for high throughput data readout
- Work on test infrastructure: Trigger Logic Unit for the AIDA telescope
- Several test-beams ahead with the different prototypes
- Also open to collaborate in the APD irradiation campaign

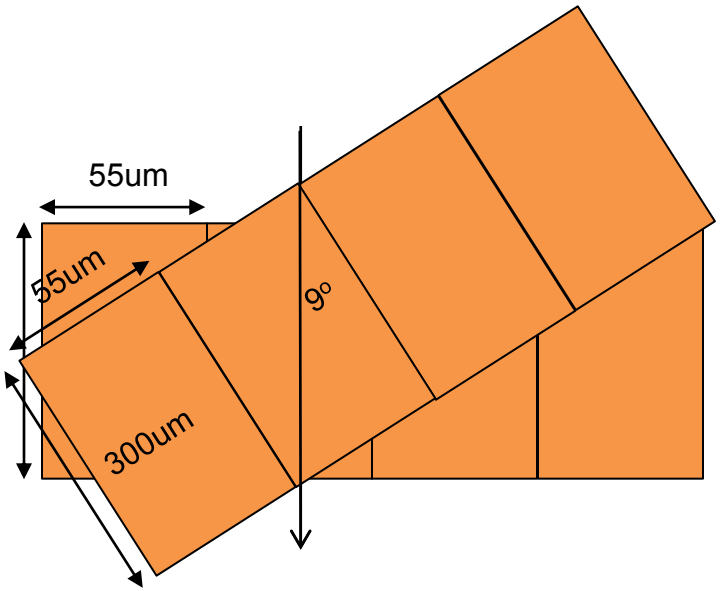
2010 TIMEPIX TELESCOPE



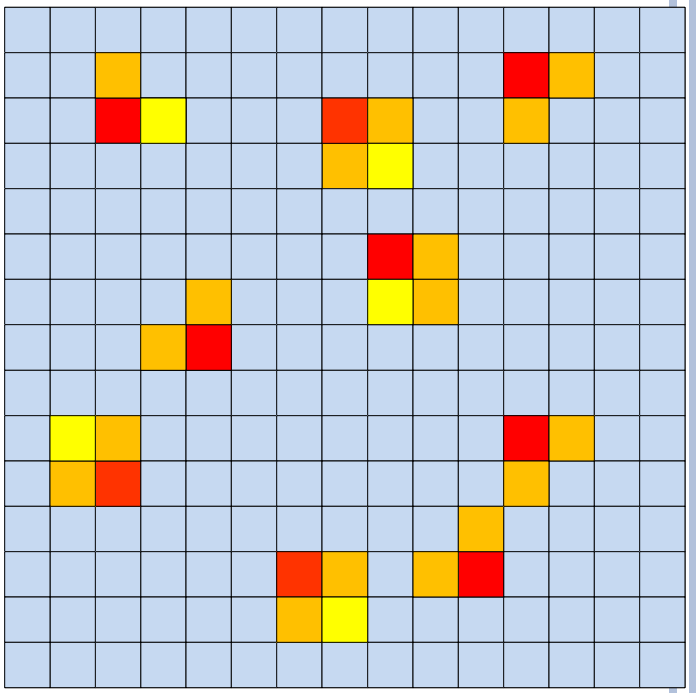
ANGLED PLANES TO BOOST RESOLUTION

Hits that only affect one pixel have limited resolution (30um region in 55um pixel)

Tilting the sensor means all tracks charge share and use the ToT information in centroid, CoG calculations



Perp ~10um resolution
9º<4um resolution



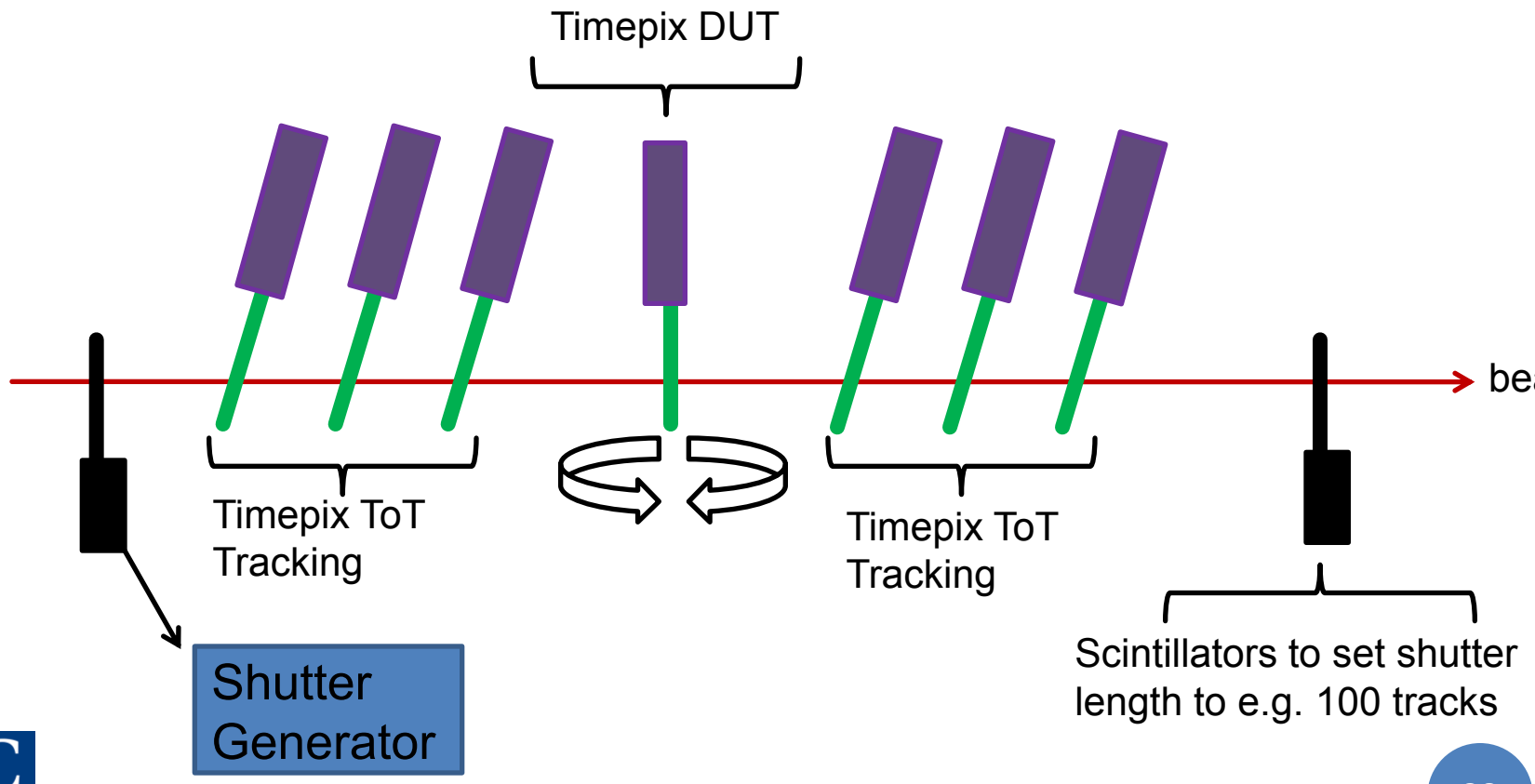
Indicative Timepix events

2010 TELESCOPE IN TIMEPIX DUT CONFIGURATION

In this configuration the telescope was optimized for running with a Timepix DUT

The USB2 readout allowed a 7 frame per second readout rate (700Hz track rate)

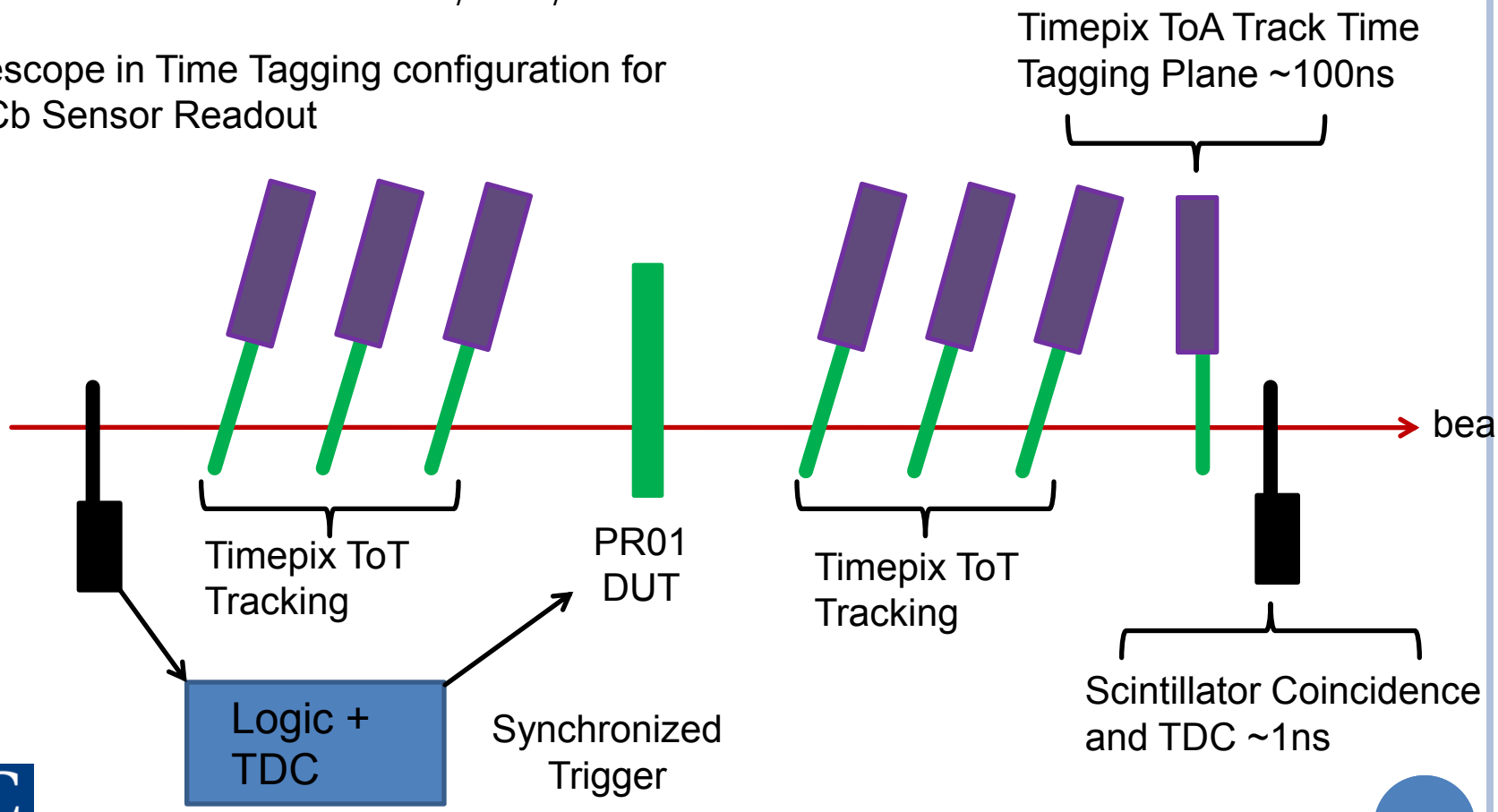
The all angled six Timepix telescope gives a ~2.0μm Track Extrapolation Error



TIME RESOLUTION FOR LHC READOUTS

- Asynchronous SPS beam not suited to LHC systems designed for 25ns bunch structure
- Implemented a TDC which with Timepix ToA mode gives us ~1ns per track time stamping
- Able to provide and record synchronised triggers to 40MHz readout systems (TELL1)
- Allows software reconstruction and analysis of asynchronous tracks

Telescope in Time Tagging configuration for LHCb Sensor Readout

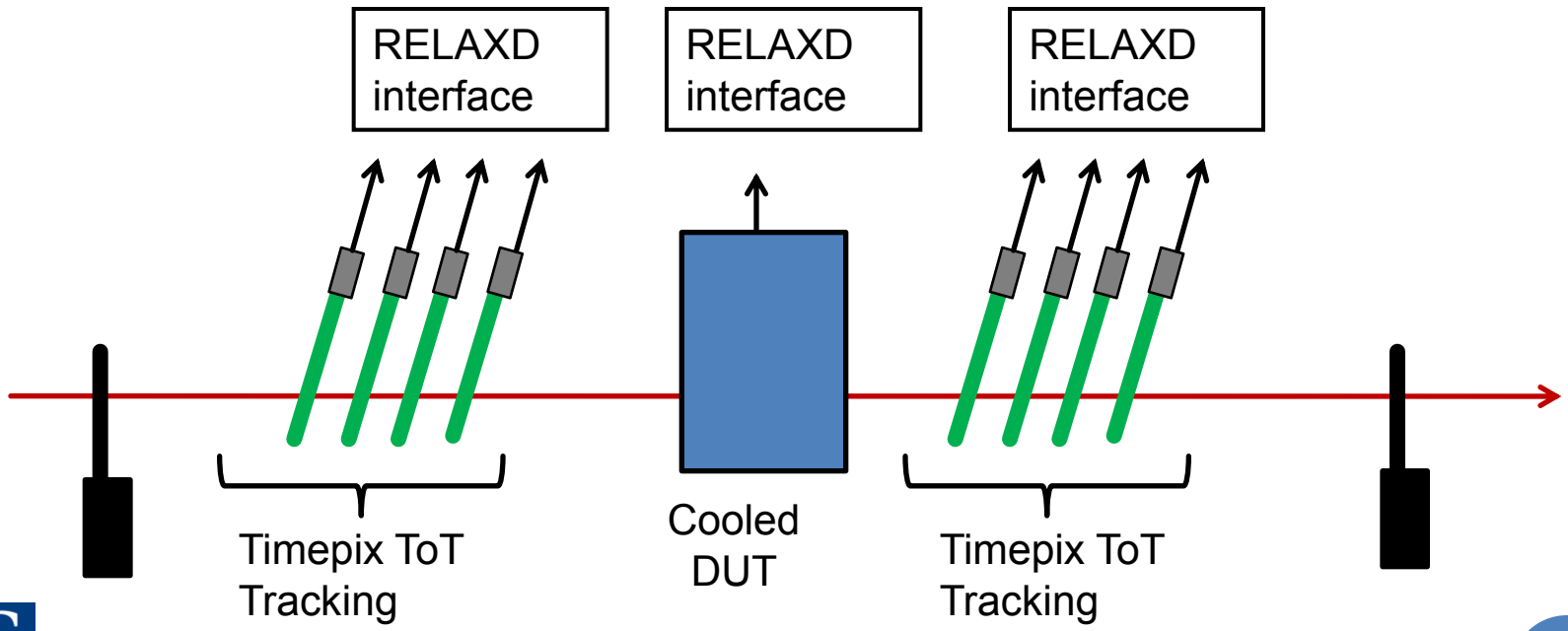


AUGUST 2010 TELESCOPE – TIMEPIX DUT

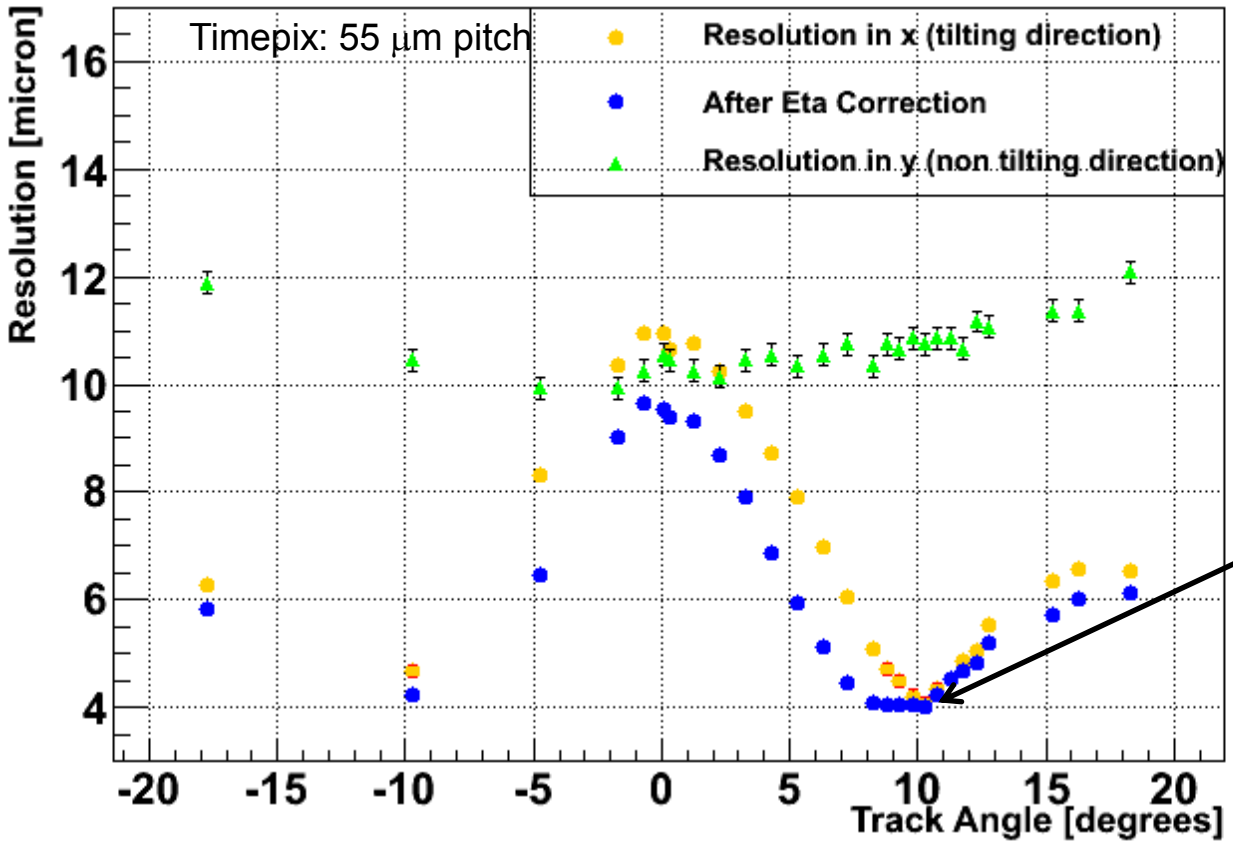
RELAXD system allowed 55 frames per second readout (~2,500 tracks per second)
Each 100,000 point measurement now takes 4 minutes

Eight angled Timepix tracking planes gives a ~1.67um Track Extrapolation Error

Closer tacking planes reduce multiple scattering effects



TIMEPIX TELESCOPE – RESOLUTION PER PLANE



Operating point of Telescope planes

Resolution measured at Testbeam

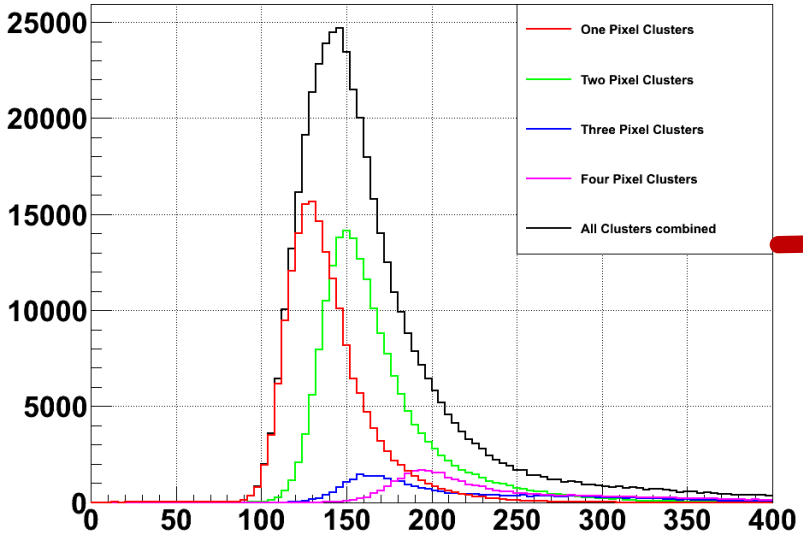
Resolution per plane 4um

Resolution at Device Under Test (with 8 planes) 1.6um

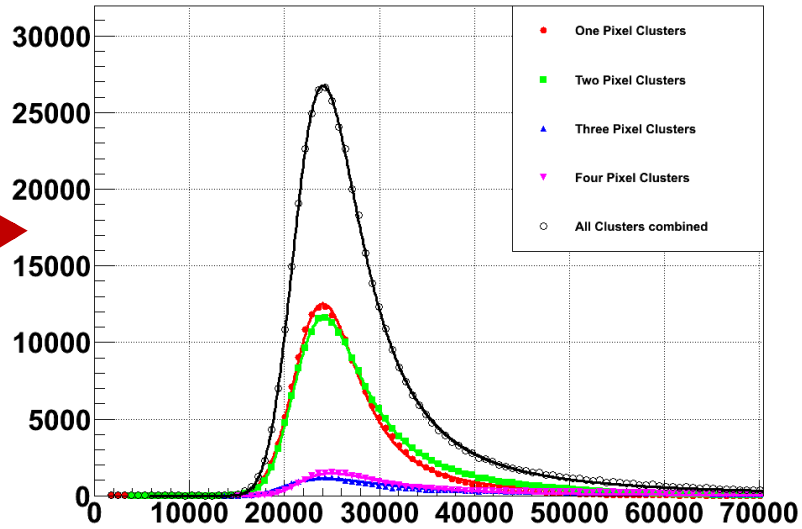
TIMEPIX DATA ANALYSIS

- Calibration of chip under excellent control
- Many lessons learned for Timepix2 design and necessary useful features for calibrating final chip
- 1st paper submitted: http://arxiv.org/abs/1103.2739

Before Calibration

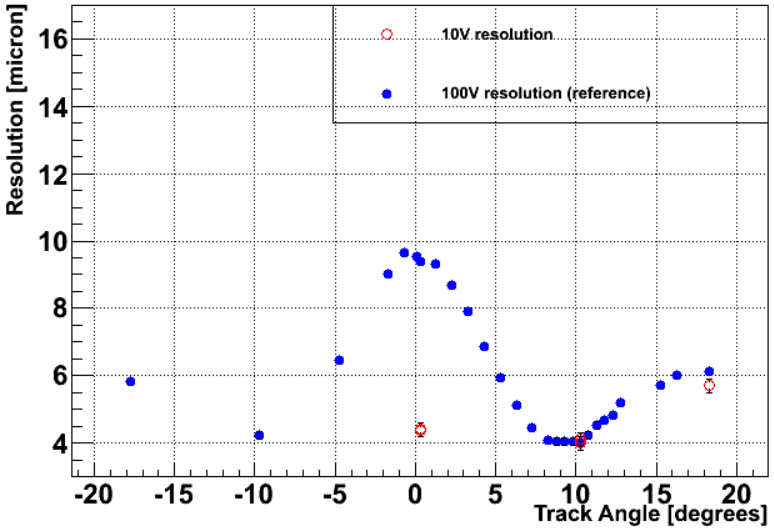


After Calibration



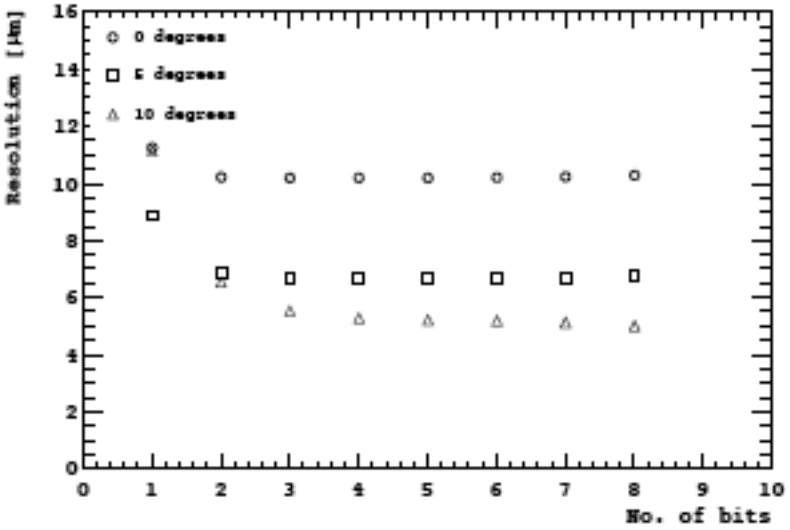
A FEW HIGHLIGHTED RESULTS:

Resolution as a function of angle



10V data (close to depletion)
100V data (overdepleted)
There is an enormous gain at lower voltage
Possible advantage for VELO under investigation

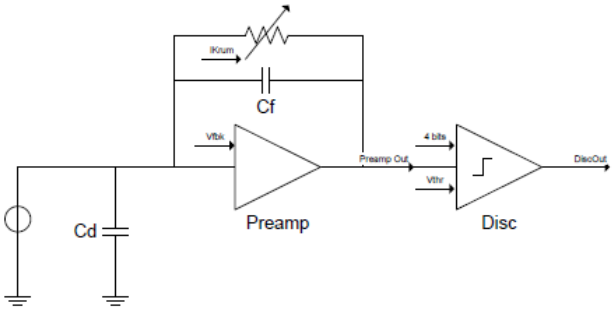
Resolution as a function of # bits

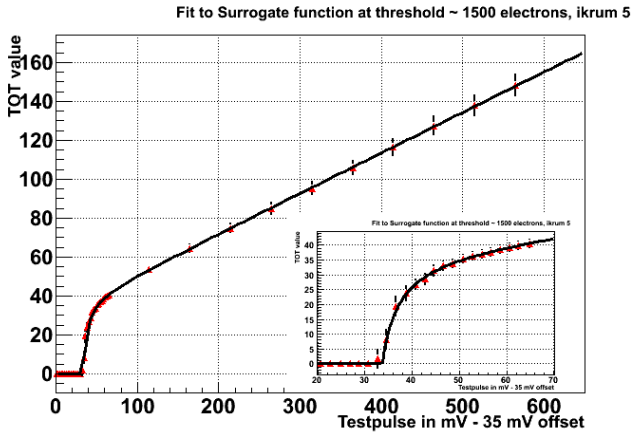


Resolution as a function of number of bits (shown for three different angles)
Input to Timepix2/Velopix design
4 bits and above are safe
3 bits is close to resolution degradation

VELOPIX: ANALOG FRONT-END REQUIREMENTS.

- Reduce timewalk: <25 ns @ 1ke$^-$ threshold.
  - Faster preamplifier and discriminator of Timepix2 covers and exceed this requirement
- I_{krum} range 5 . . . 40nA
  - ⇔ sensitivity 750 . . . 6000 e$^-$/25ns.
  - ⇔ 20 ke$^-$ signal returns to baseline in 660 . . . 83 ns
- Reduced non-linearity near threshold.
- Analog power consumption <10 uW/pixel.
- Higher preamplifier gain (~50mV/ke$^-$).
  - reduced ENC, lower detectable charge (~500 e$^-$)
  - reduced linear range (30 ke$^-$) : better suited to Si -tracking
- Design by X.Llopart(CERN) and V.Gromov (NIKHEF) very advanced.





VELOPIX:

- Digital :
  - Simultaneous 4 bit Time-over-threshold and time identification (12 bit).
  - Data loss must be kept < 0.5% in worst conditions (6kHz pixel hit-rate).
    - Limit ToT< 400ns.
    - Adequate buffering & bus speeds.
  - Data driven readout.
  - SEU protection of logic & registers.
  - multi-Gbit/s output links : 4 x 3.2Gb/s#
  - Design of superpixel, column bus and EOC logic very advanced (TuomasPoikela).
- Total power budget <3W full chip.
- Radiation hardness TID 400Mrad.

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DATA RATES

- Numbers at highest occupancies:
  - average particle rate per 'hottest' asic ~ 5 particles/25ns = 200MHz
  - average pixel cluster size ~2: (pessimistic assumption, 200um Si)
- Information bits per hit pixel : 32
  - 4 bit : Time over Threshold value.
  - 12 bit : bunch identification
  - 16 bit : pixel address.

=> Single asic data rate can reach 13 Gbit/s !

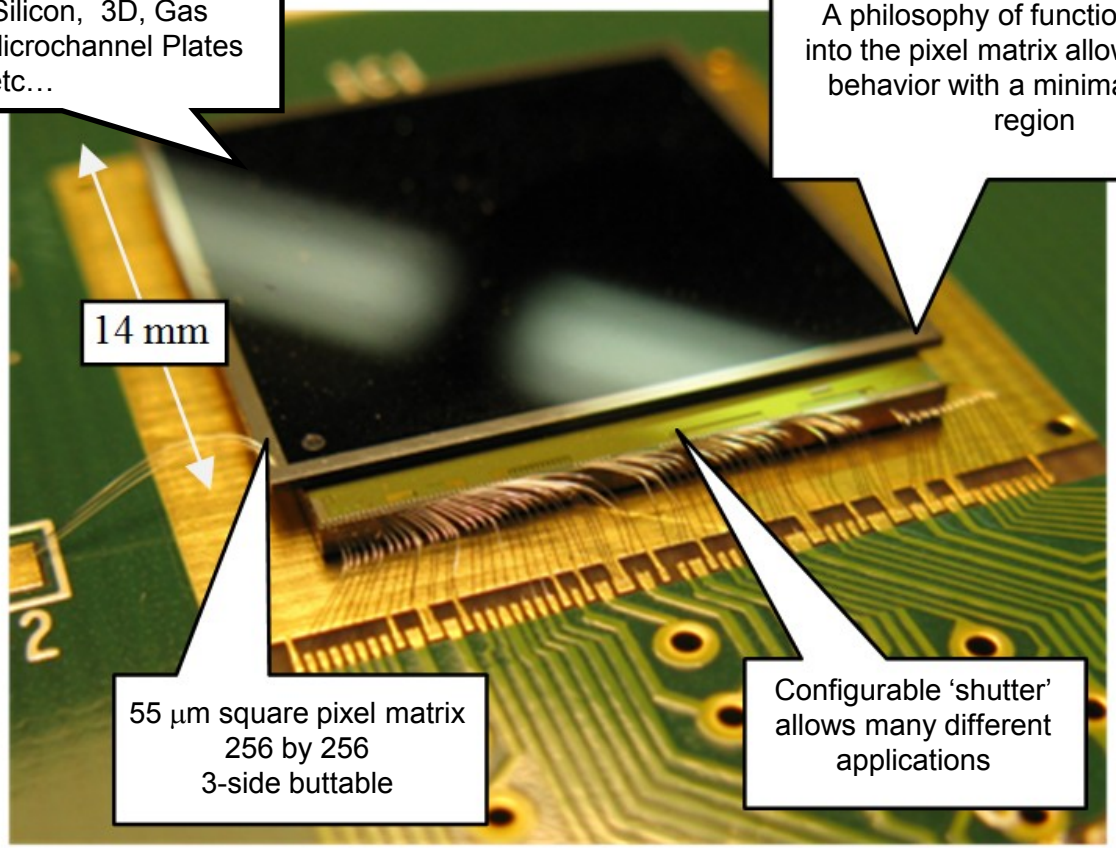
- 30% data reduction can be achieved by 'clustering' data:
  - share the bunch id (12bit) and address bits between neighbor pixels.
  - must be done before column readout, i.e. inside pixel array !
  - most efficiently done in units of 4x4 pixels = "Super pixel"

Average #particles/event

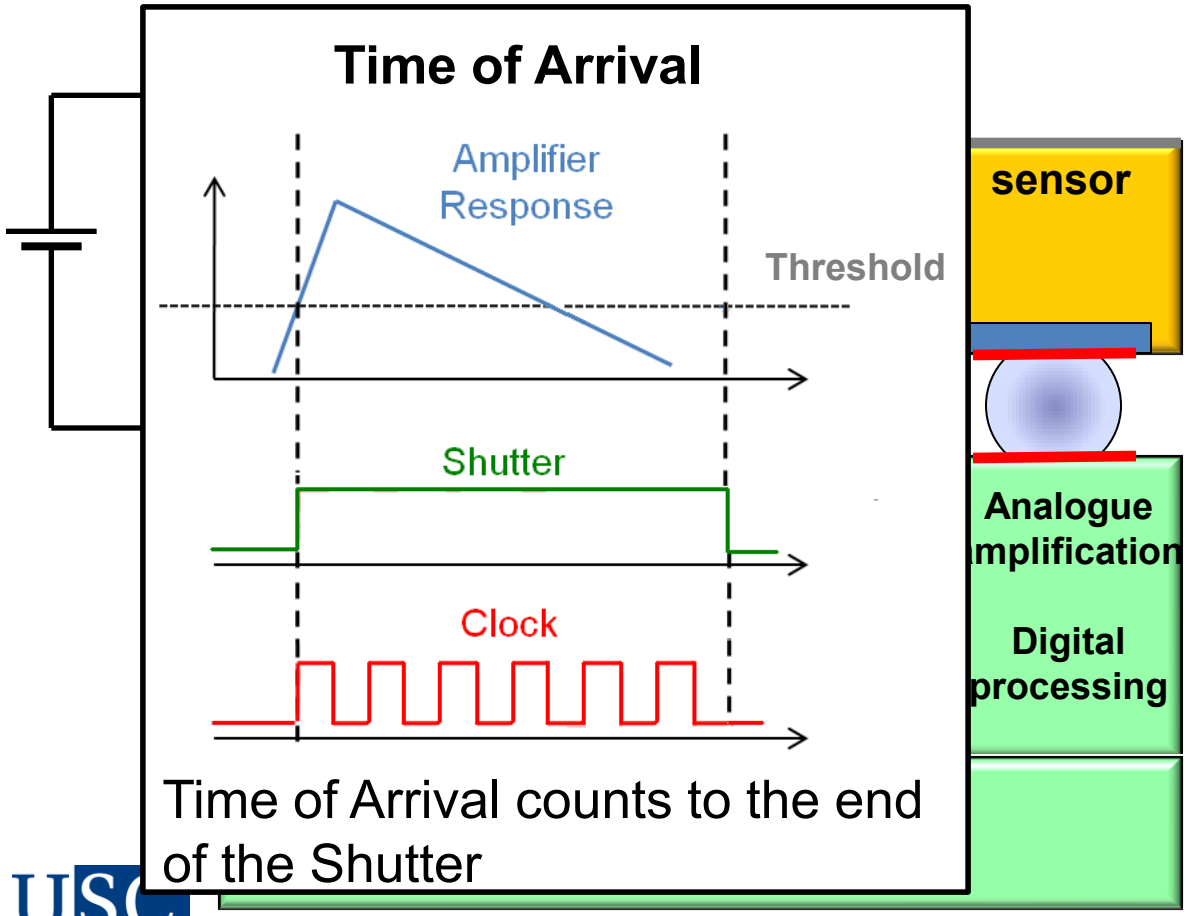
1.3	1.0	0.6
5.3	2.6	1.0

5.3	1.3	
2.6	1.0	
1.0	0.6	

ACTIVE PIXELS: TIMEPIX/MEDIPIX



TIMEPIX (2006)



Timepix design requestedand funded by EUDET collaboration

Conventional Medipix2 counting mode remains.

Addition of a clock up to 100MHz allows two new modes.

Time over Threshold

Time of Arrival

Pixels can be individually programmed into one of these three modes

DEVELOPMENT HISTORY AND FUTURE

Medipix1	**1μm SCAMOS** 64 by 64 pixels Photon Counting Demonstrator (1997)
Medipix2	**250nm IBM CMOS**, 256 by 256 55μm pixels Full photon counting (2002)
Timepix	Analogue (ToT) and Time Stamping (ToA) (2006)
Medipix3	**130nm IBM CMOS** Photon Counting, Spectroscopic, Charge Summing, Continuous Readout (2009)
Timepix2	Fast front end, Simultaneous ToT and ToA (2011)
VELOpix	**130nm/90nm/65nm** Future LHCb readout – Data driven 40MHz ToT 12Gb/s per chip (2013)
Timepix3 CLICpix	**130nm/90nm/65nm** Future Hybrid Pixel Time tagging layer for the LCD project (20??)

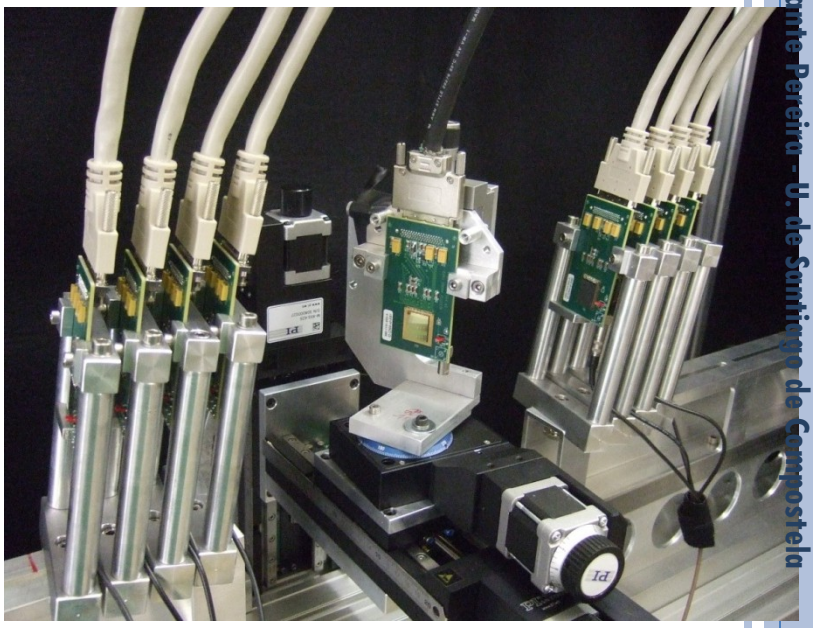
TIMEPIX2 MAIN REQUIREMENTS

- Lots of different applications → Very demanding specs !

Pixel size	55 µm x 55 µm
Pixel matrix array	256 x 256
Sparse readout	YES
PC, TOA or TOT recorded simultaneously	YES (2 at a time)
Minimum detectable charge	≤ 500 e-
TOA resolution	>1.5ns (25ns/16) 4bits (Gossipo3 style)
Peaking time	< 25 ns
TOT resolution	<5% channel to channel spread
Technology	IBM 130nm DM 3-2-3
Power consumption	<1.5W/cm^2 (~45 µW/pixel) @1.2 V
Target floorplan	3 sides buttable and minimum periphery
TSVs possibility	YES. Multi-dicing scheme as Medipix3

TELESCOPE COMPARISONS

Telescope	Pixel	Resolution	Time Tag	Rate
Timepix 2009	55μm	2.3μm	100ns	100Hz
Timepix 2010 (May)	55μm	2.0μm	~1ns	350Hz
Timepix 2010 (Aug)	55μm	1.7μm	~1ns	2.8kHz
EUDET (Low res)	18μm	~2μm	100us	990Hz
EUDET (High res)	10μm	~1μm	-	300Hz?



EUDET. Telescope