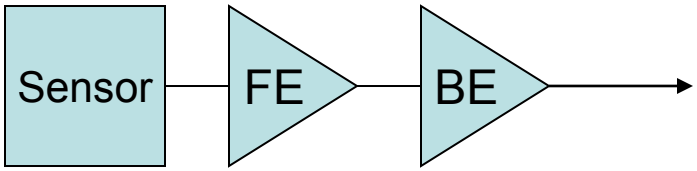
High performance sensor interfaces: Efficient system architectures and calibration techniques

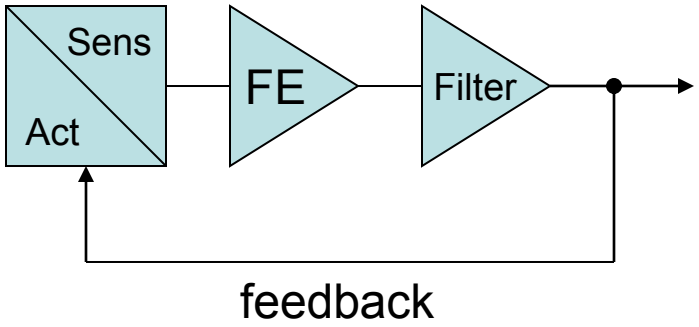
Marc Pastre – 2011

Outline

- Sensor interfaces
  - System architectures
    - Open-loop vs. Closed-loop
    - Continuous-time vs. Sampled
  - Frontends
    - Voltage-, current-, charge-mode
- Case studies
  - Hall sensor
  - MEMS-based accelerometer
- Digital calibration
  - Successive approximations
  - M/2^{+}M Sub-binary DACs for successive approximations
- Conclusion

Open-loop vs. Closed-loop





- Straightforward implementation
- Analog output
- Sensitive to sensor non-linearity

- Directly compatible with a $\Delta\Sigma$ loop
- Digital or analog output
- Insensitive to sensor non-linearity
- Sensitive to actuator non-linearity
- Feedback loop stability
- Bandwidth

Continuous-time vs. Sampled systems

- Continuous-time:
  - Straightforward
  - Low power consumption
  - High bandwidth
  - Not really compatible with continuous-time calibration
- Sampled systems directly compatible with:
  - Closed-loop $\Delta\Sigma$ modulators
  - Switched capacitor circuits
  - Digital calibration

Voltage-, current-, charge-mode

- Voltage-mode:
  - Hi-Z $\Rightarrow$ Instrumentation amplifier, Op-Amp (+ input)
  - Low-Z $\Rightarrow$ Op-Amp circuit, switched capacitor
- Current-mode:
  - Transimpedance amplifier
    (based on common-source transistor, Op-Amp, …)
  - Switched capacitor circuit used as integrator
  - Virtual ground @ input
- Charge-mode:
  - Transimpedance integrator
    (based on common-source transistor, Op-Amp, …)
  - Switched capacitor

Case studies

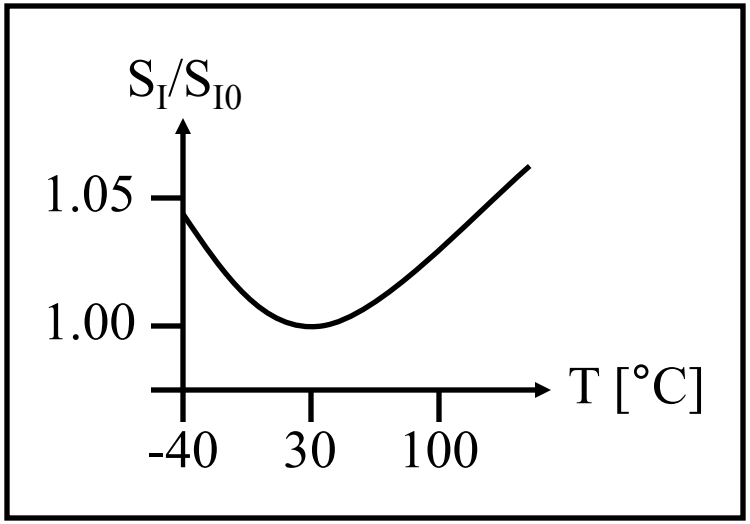
- Hall sensor microsystem:
  - Open-loop
  - Voltage-mode
  - Sampled
  - Continuous-time sensitivity calibration
- MEMS-based accelerometer:
  - Closed-loop
  - Voltage-/Charge-mode
  - Sampled
  - Sensor included in a $\Delta\Sigma$ loop

Hall sensor microsystem

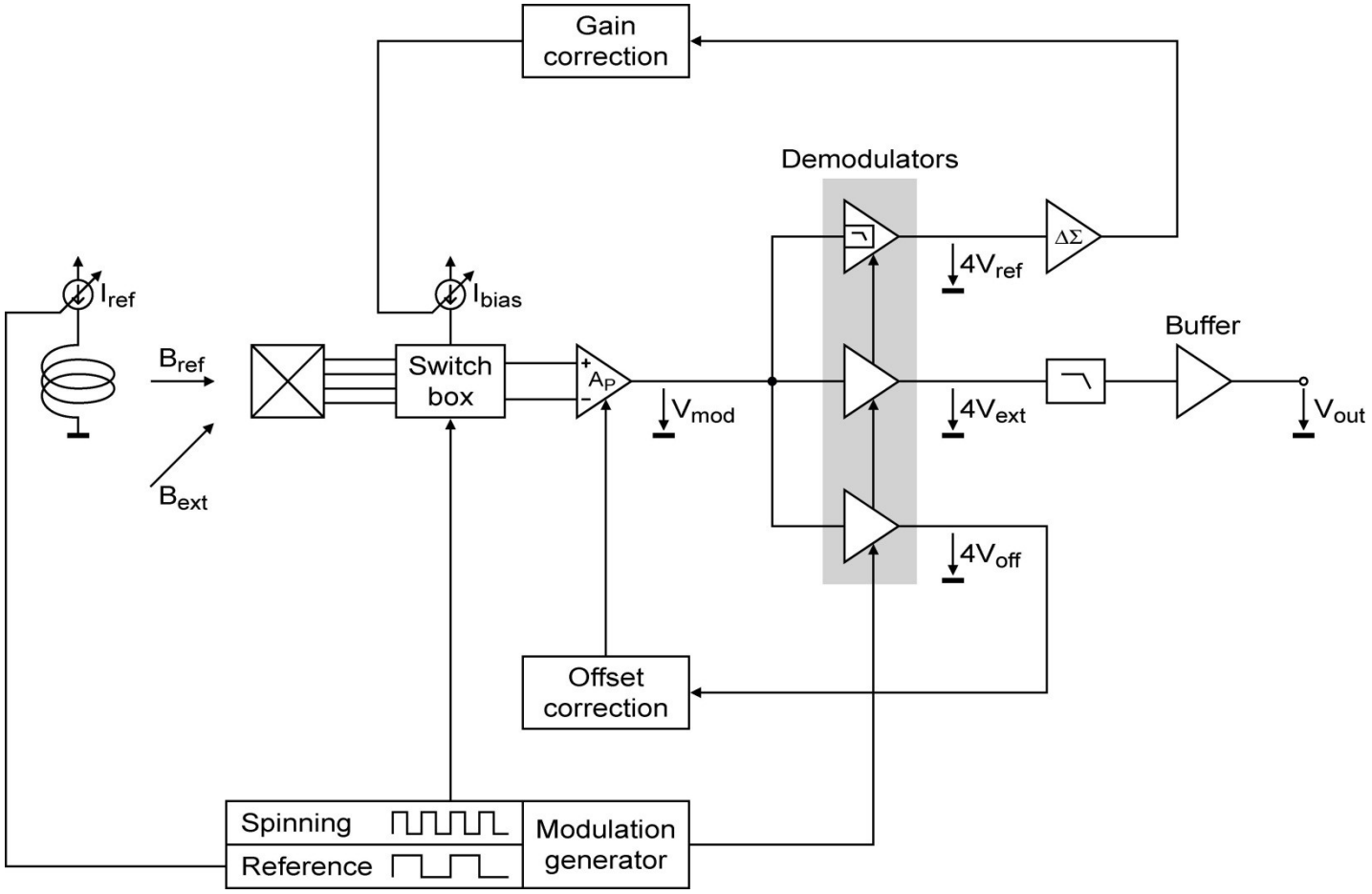
- Continuous-time sensitivity calibration
- Reference field generated by integrated coil
- Combined modulation scheme mixes up reference and external signal
- Parallel demodulation schemes allow continuous background sensitivity calibration
- Compensation of any cause of drift (temperature, mechanical stresses, ageing)

Sensitivity drift of Hall sensors

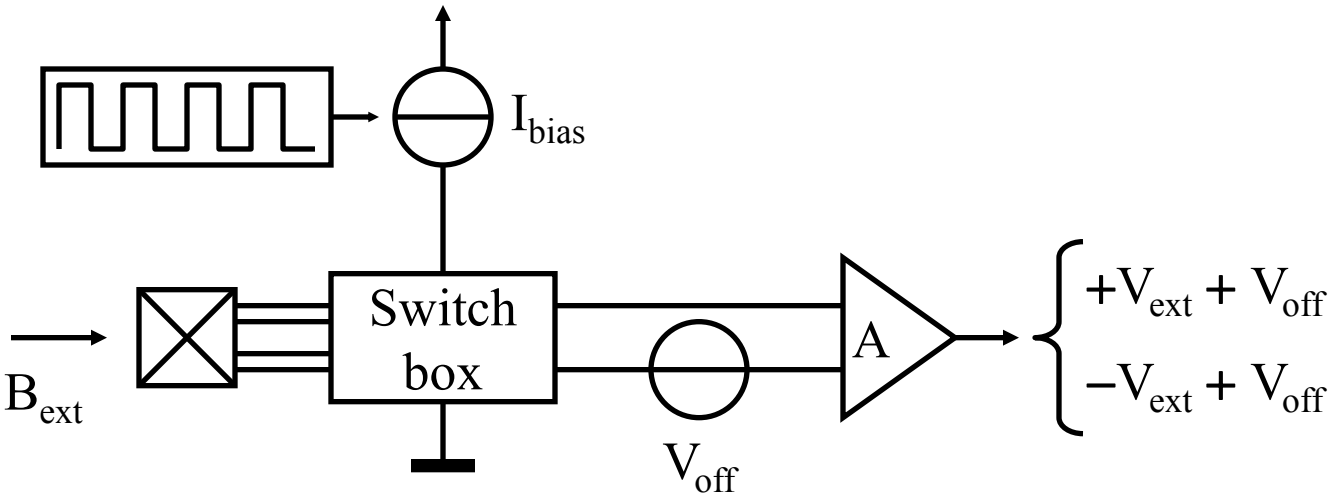
- Drift due to
  - Temperature
  - Mechanical stresses
  - Ageing
- Typical temperature drift
  - 500 ppm/°C uncalibrated
  - 300 ppm/°C with 1st order correction
- Typical ageing drift
  - 20’000 ppm (2 %)



System architecture

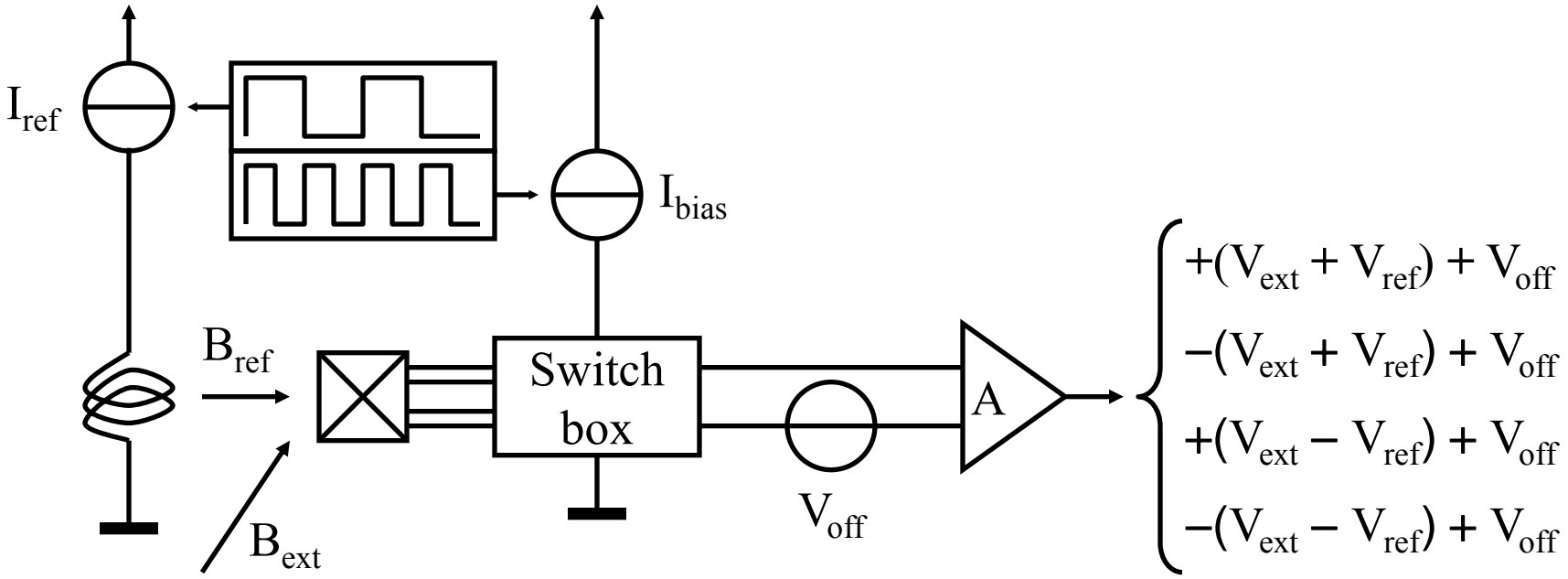


Spinning current modulation



- 2 modulation phases
- Modulated signal, constant offset
- Offset-free signal extracted by demodulation

Combined modulation



- 4 modulation phases
- Modulated signal & reference, constant offset
- Modulation frequency of 1 MHz

Demodulation schemes

	Modulation			Demodulation		
Phase	Spin.	Coil	Amplifier output	Sig.	Ref.	Off.
1	+	+	$+(V_{ext} + V_{ref}) + V_{off}$	+	+	+
2	-	+	$-(V_{ext} + V_{ref}) + V_{off}$	-	-	+
3	+	-	$+(V_{ext} - V_{ref}) + V_{off}$	+	-	+
4	-	-	$-(V_{ext} - V_{ref}) + V_{off}$	-	+	+
				$4V_{ext}$	$4V_{ref}$	$4V_{off}$

- 3 different demodulation schemes
- Offset-free signal & reference demodulation, using synchronous switched-capacitor circuits

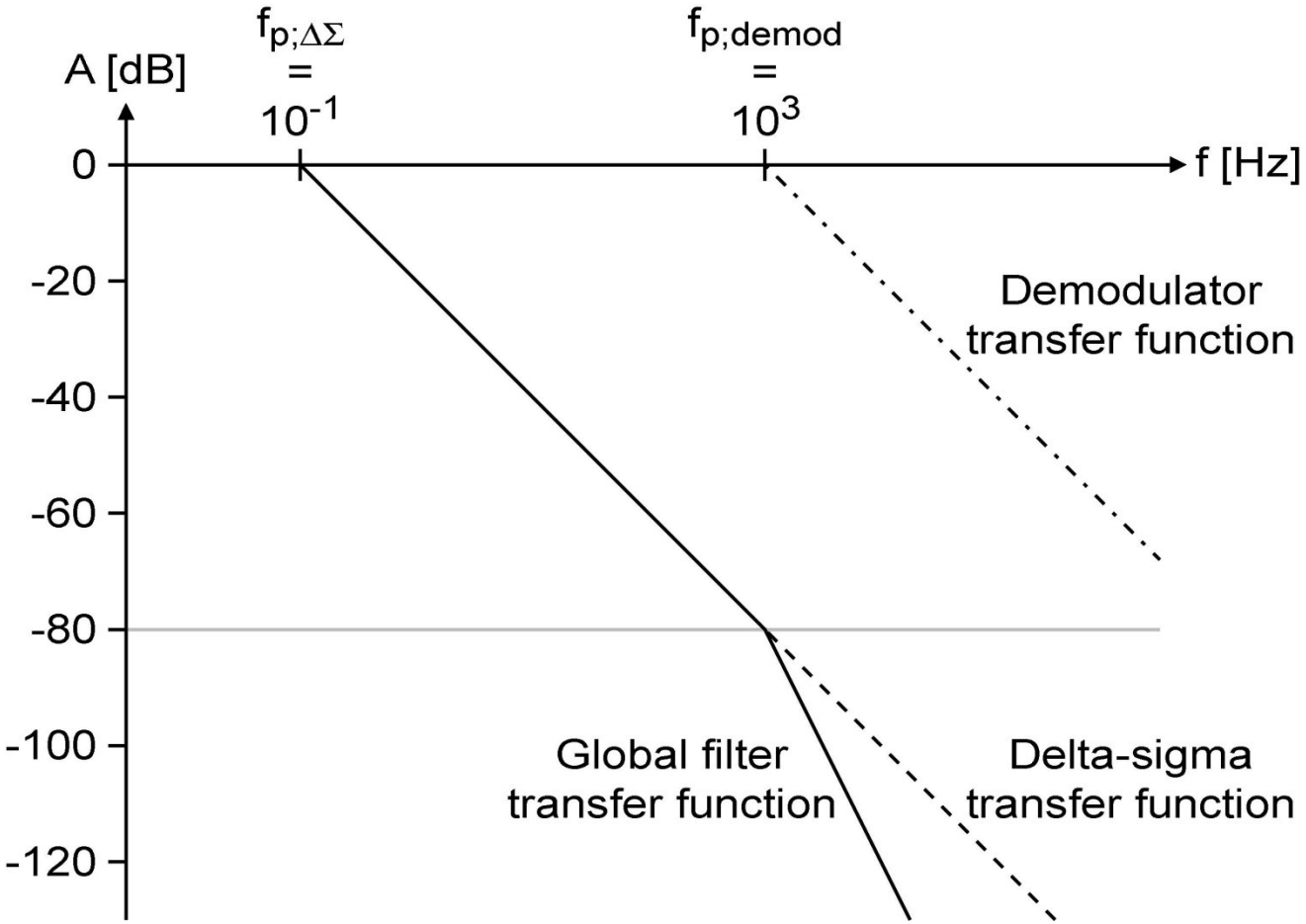
Reference signal demodulation

- 2 limitations for precise reference signal extraction:
  - Low reference signal level
    - $V_{Hall;ref} = (S_{I;Hall} \cdot I_{bias}) \cdot (E_{I;coil} \cdot I_{ref}) = 40\ \mu V$
    - $V_{Hall;ref} \cdot 0.1\% = 40\ nV$
    - Input-referred noise = 20 nV/√Hz @ 1 MHz
  - External signal aliasing
    - $V_{ext;max} = 100 \cdot V_{ref}$
    - High-pass parasitic transfer function
- Solution: Reference signal filtering

Reference signal filtering

- Filtering combined with reference signal demodulation and analog-to-digital conversion
- Second-order low-pass filtering
- Demodulator pole @ 1 kHz
  - Feedback path in the switched-capacitor demodulator
- Delta-sigma pole @ 0.1 Hz
  - Long integration period

Filtering transfer function

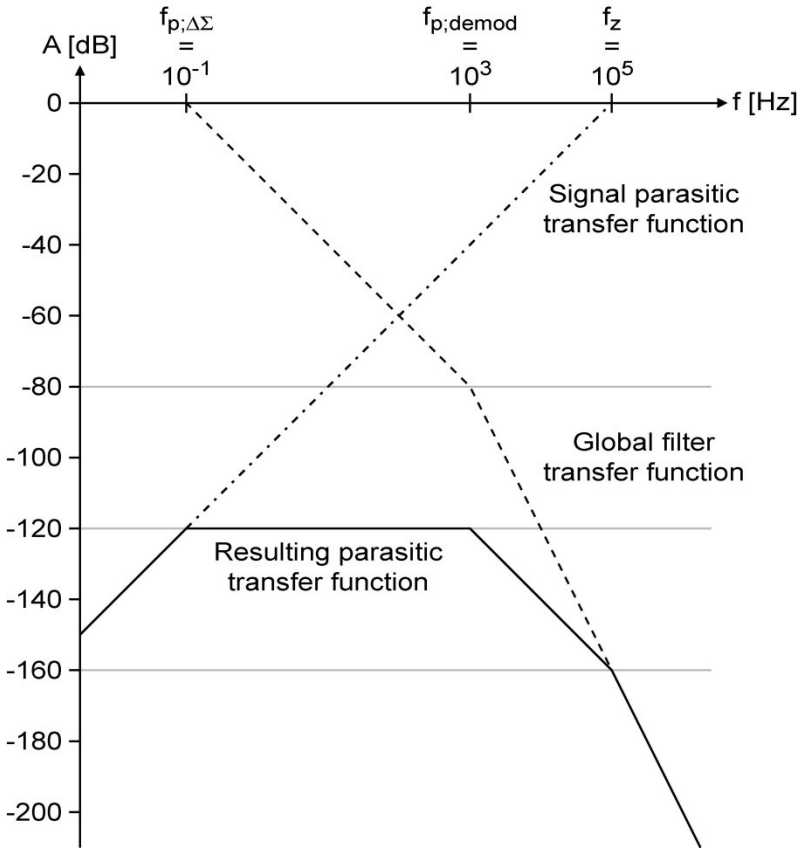


External signal aliasing

$$+[+(V_{ext;1} + V_{ref}) + V_{off}]$$
$$-[-(V_{ext;2} + V_{ref}) + V_{off}]$$
$$-[+(V_{ext;3} - V_{ref}) + V_{off}]$$
$$+[-(V_{ext;4} - V_{ref}) + V_{off}] = 4V_{ref} + \underbrace{[(V_{ext;1} + V_{ext;2}) - (V_{ext;3} + V_{ext;4})]}_{\text{Parasitic term}}$$

- Variation of the external signal between the reference demodulation phases $\Rightarrow$ alias
- Derivative effect $\Rightarrow$ high-pass transfer function
- Zero @ 100 kHz

Effect of filtering on alias

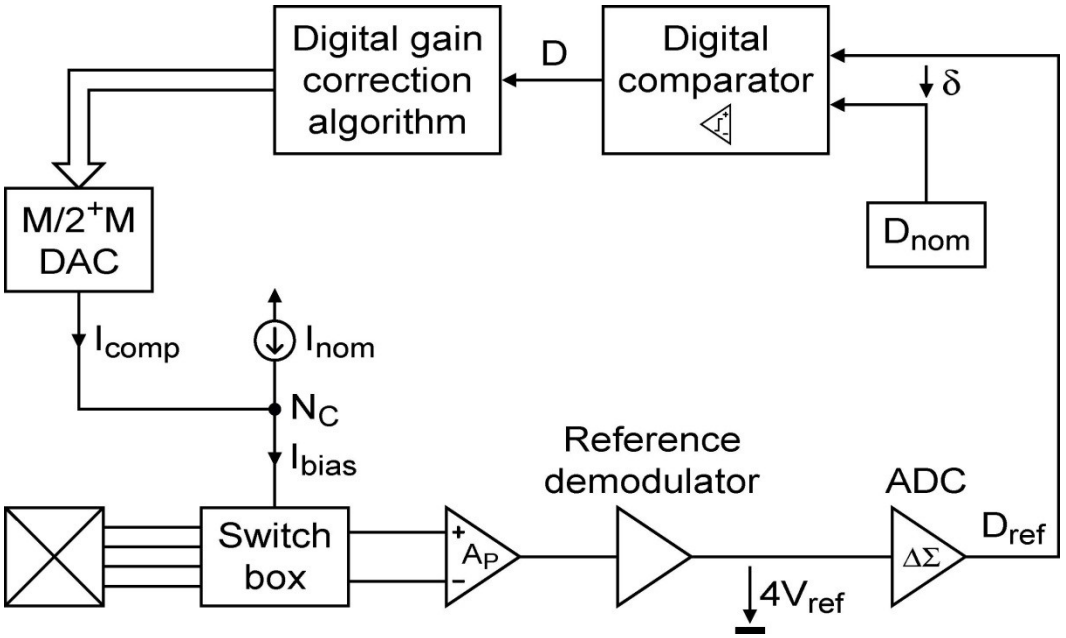


- Minimum attenuation of 120 dB

Effects of filtering

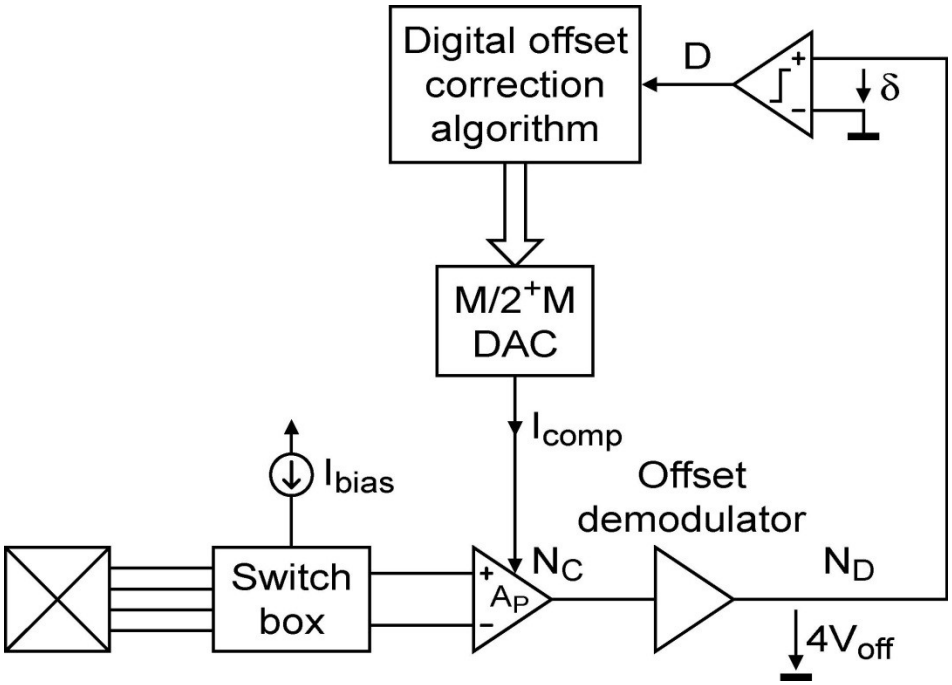
- On noise
  - Bandwidth limited to less than 1 Hz
  - White noise integrated in limited bandwidth
  - Total input-referred RMS noise < $V_{Hall;ref} \cdot 0.1\% = 40$ nV
- On aliased external component
  - Minimum attenuation of 120 dB
  - $V_{ext;max} = 100 \cdot V_{ref}$ attenuated to $100 \cdot V_{ref} / 10^6 = V_{ref} \cdot 0.01\%$
- Extraction of $V_{ref} \cdot 0.1\%$ possible $\Rightarrow$ sensitivity calibration with 1'000 ppm accuracy

Sensitivity drift compensation



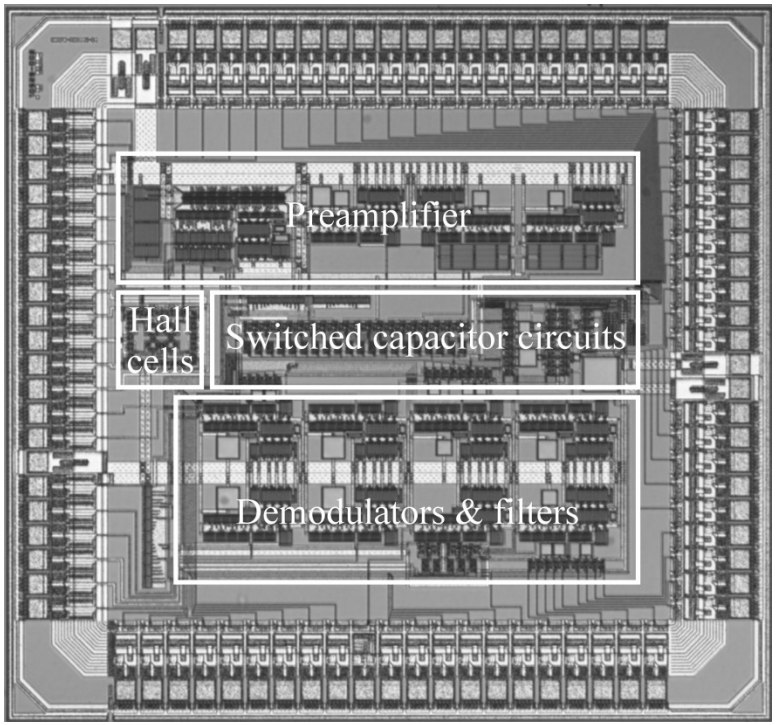
- Sensitivity compensated by sensor bias current adjustment
- $V_{Hall} = (S_{I;Hall} \cdot \mathbf{I_{bias}}) \cdot B$

Offset compensation



- Compensation current injection into preamplifier
- Demodulator can be optimized (low-pass filter)

Circuit micrograph



- 11.5 mm^2 in AMS 0.8 μm CXQ
- Hall sensors & coils integrated

Measurement results

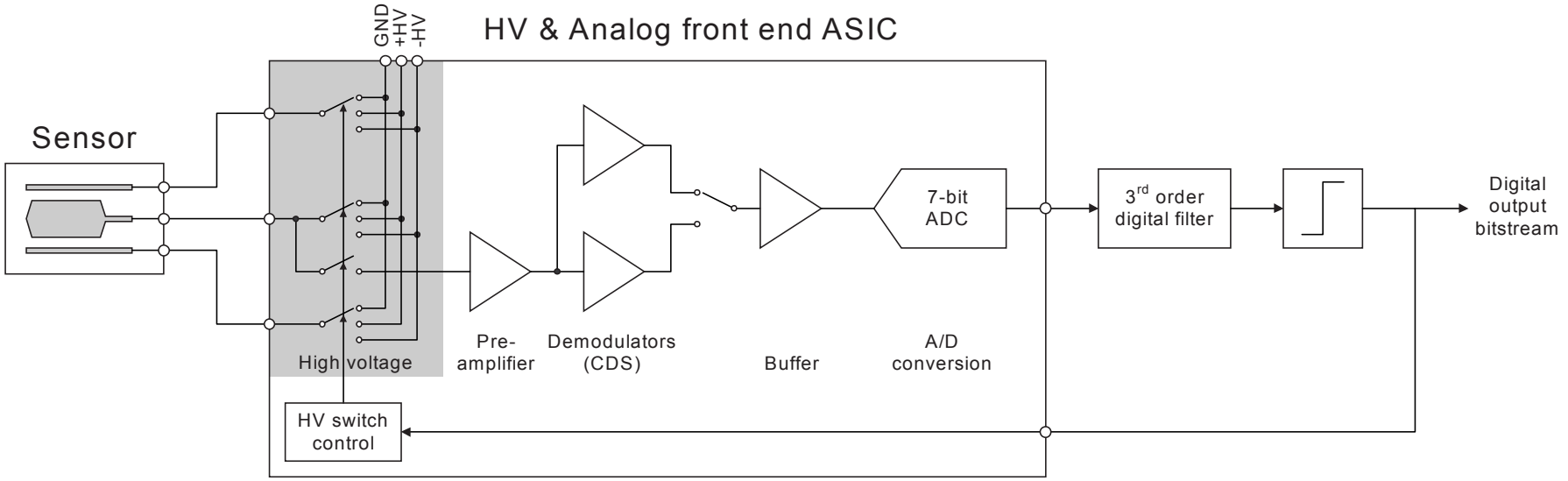
Supply voltage	5 V
Sensitivity	35 V/T
Full scale	± 50 mT
Bandwidth	500 kHz
Non-linearity	< 0.1 %
Gain drift	< 50 ppm/°C

- Compared to state of the art:
  - High bandwidth
  - Low gain drift (6-10 times better)

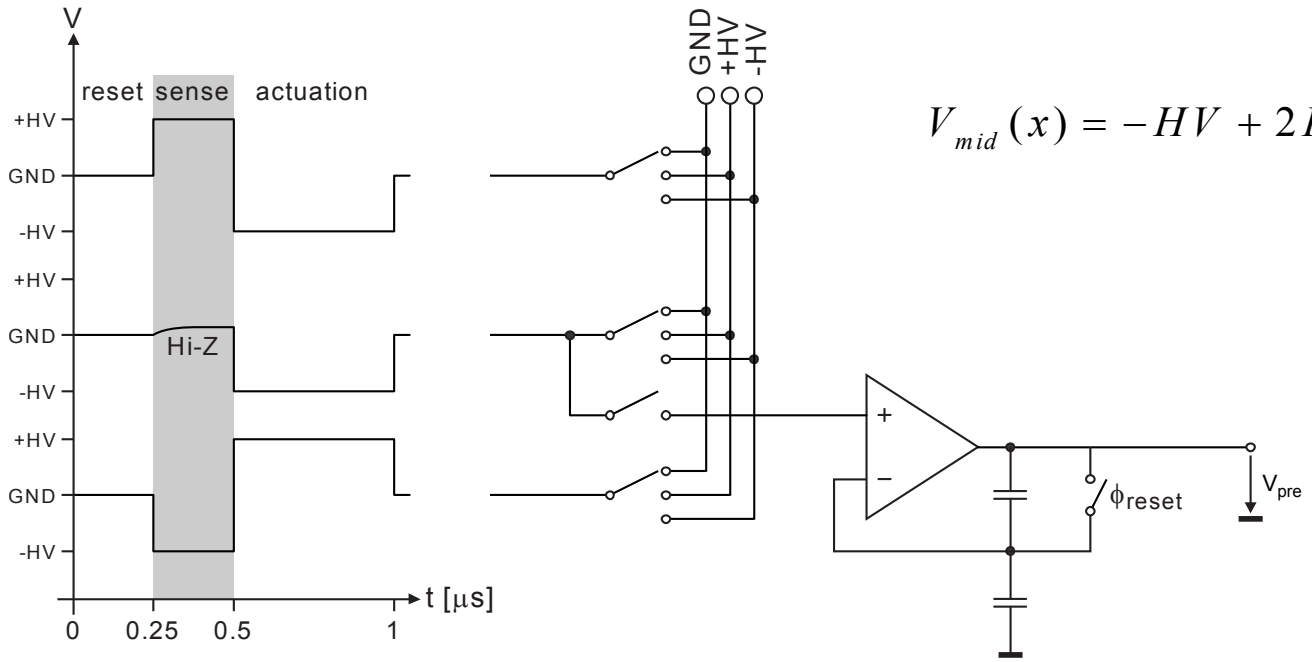
MEMS-based accelerometer

- Closed-loop system
- 5th order $\Delta\Sigma$ loop: Sensor (2nd order) + Filter (3rd order)
- Low-precision front-end (7 bits)
- Internally non-linear ADC
- Digital filter (3rd order)
- Versatile and reconfigurable system, yet featuring high performances

System architecture



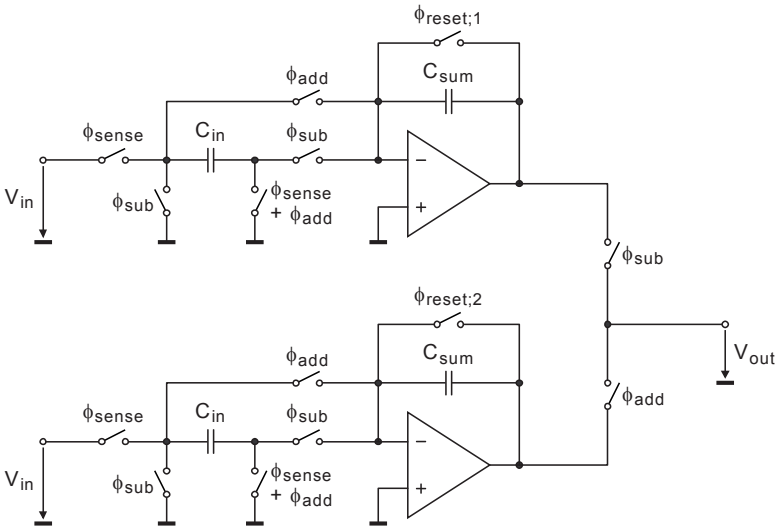
Frontend

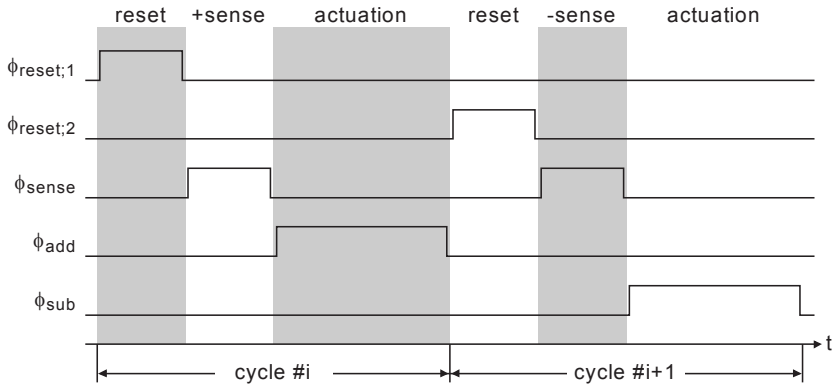


$$V_{mid}(x) = -HV + 2HV \frac{C_t(x)}{C_t(x) + C_b(x)}$$

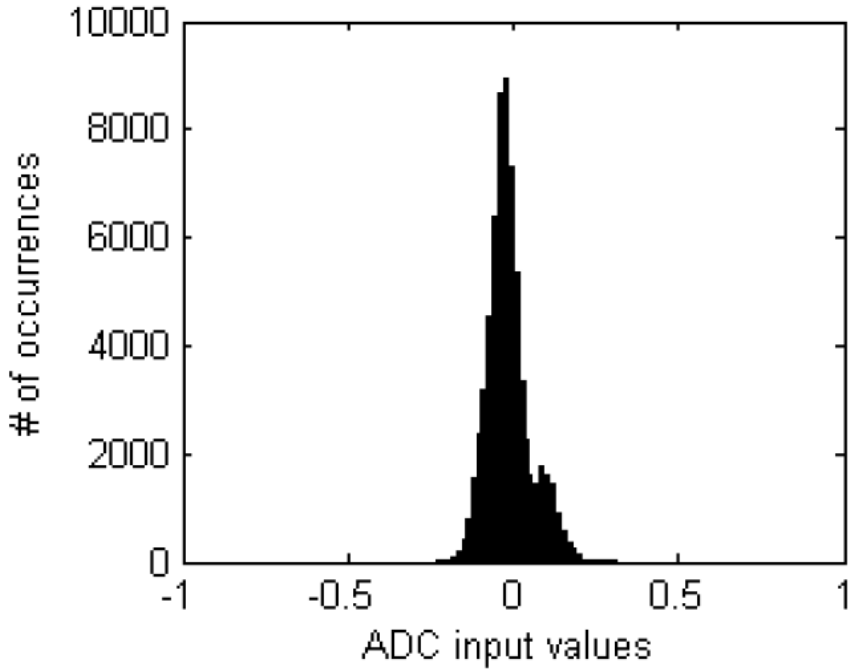
- 11.5 mm² in AMS 0.8 µm CXQ
- Hall sensors & coils integrated

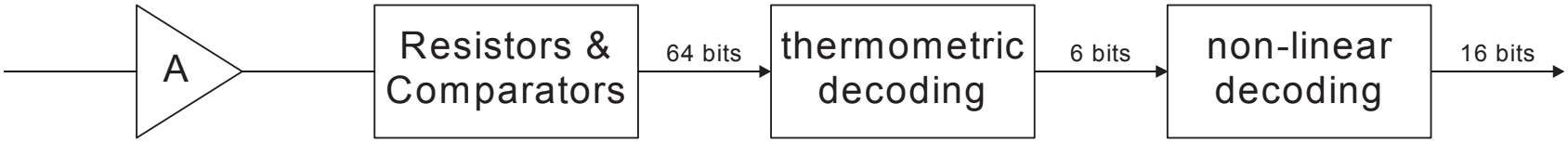
Time-interleaved CDS



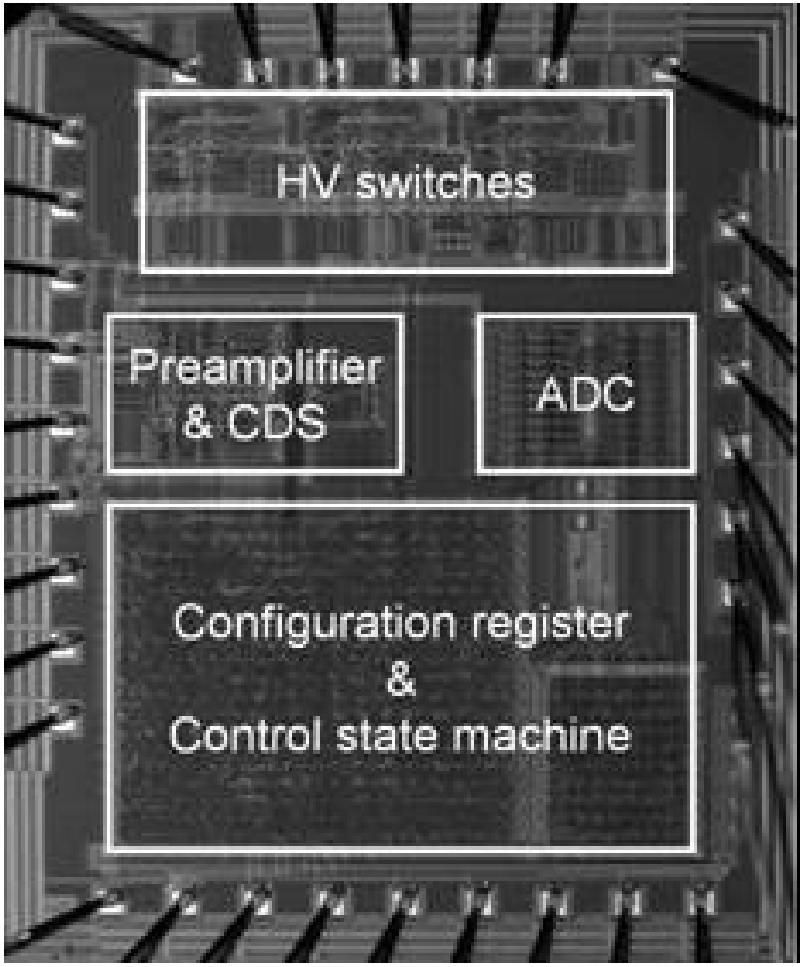


Internally non-linear ADC



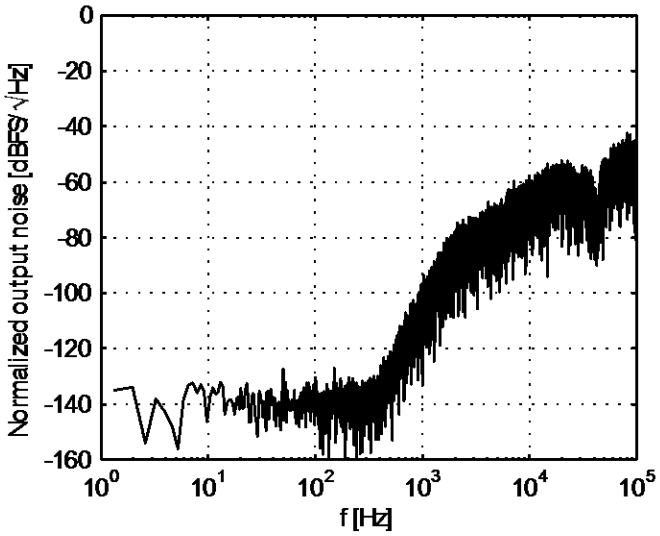


Circuit micrograph

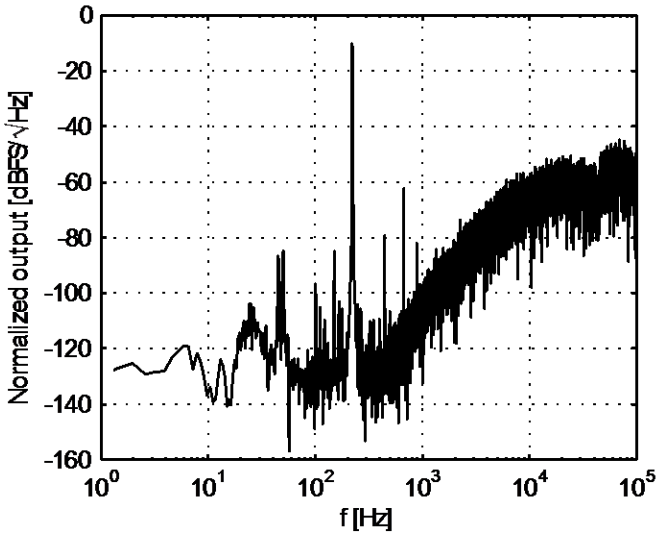


Measurement results

Without signal



8g @ 222Hz



- Compared to state of the art:
  - High bandwidth
  - Low noise

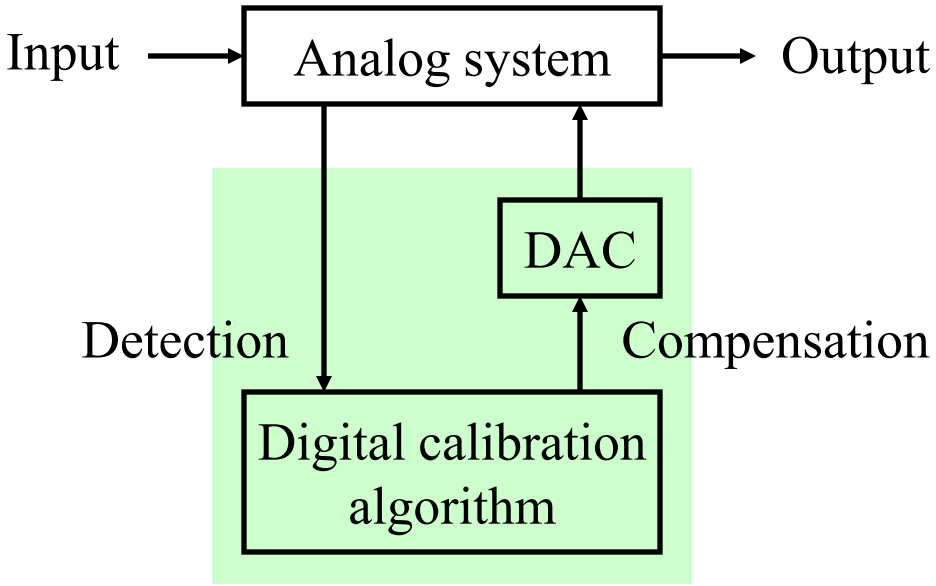
Measurement results

Supply voltage	3.3V / ± 9V
Sampling frequency	1 MHz
ΔΣ loop order	2 + 3 = 5
Full scale	11.7 g
Bandwidth	300 Hz
Input noise	1.7 μg/√Hz
Dynamic range (300 Hz)	19 bits
SNR (300 Hz)	16 bits

Digital calibration

- Digital compensation of analog circuits
- Successive approximations:
  - Algorithm
  - Working condition
- Sub-binary DACs for successive approximations:
  - Resolution
  - Radix
  - Tolerance to component mismatch
  - Architectures
  - Design

Digital compensation



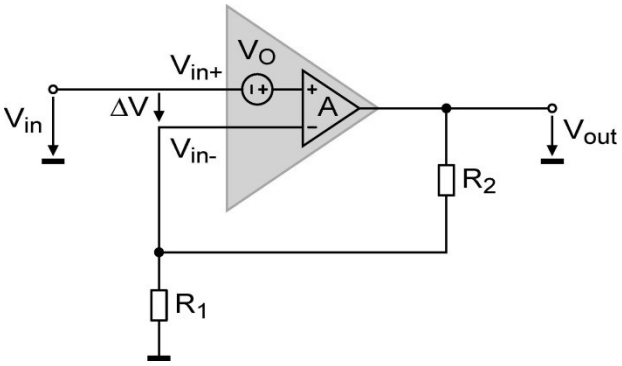
- High-precision calibration of low-precision circuits
- Alternative to intrinsically precise circuits (matching & high area)

Compensation methodology

- Detection configuration
  - Continuous: normal operation configuration
  - Interrupted: special configuration
- Detection node(s)
  - Imperfection sensing
  - Usually voltage-mode
- Compensation node(s)
  - Imperfection correction
  - Current-mode

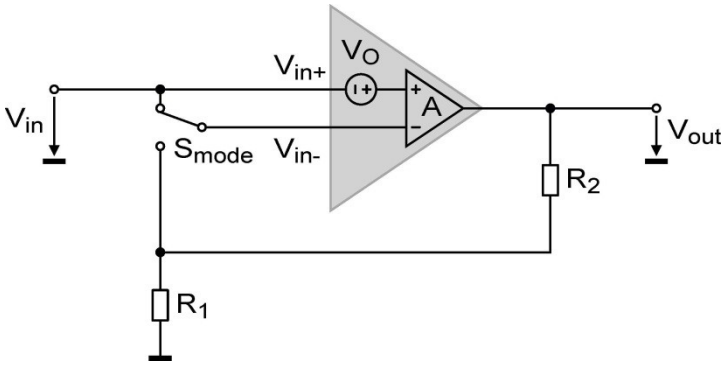
Offset cancellation in OAs

Closed-loop



$$\Delta V \cong -V_O$$

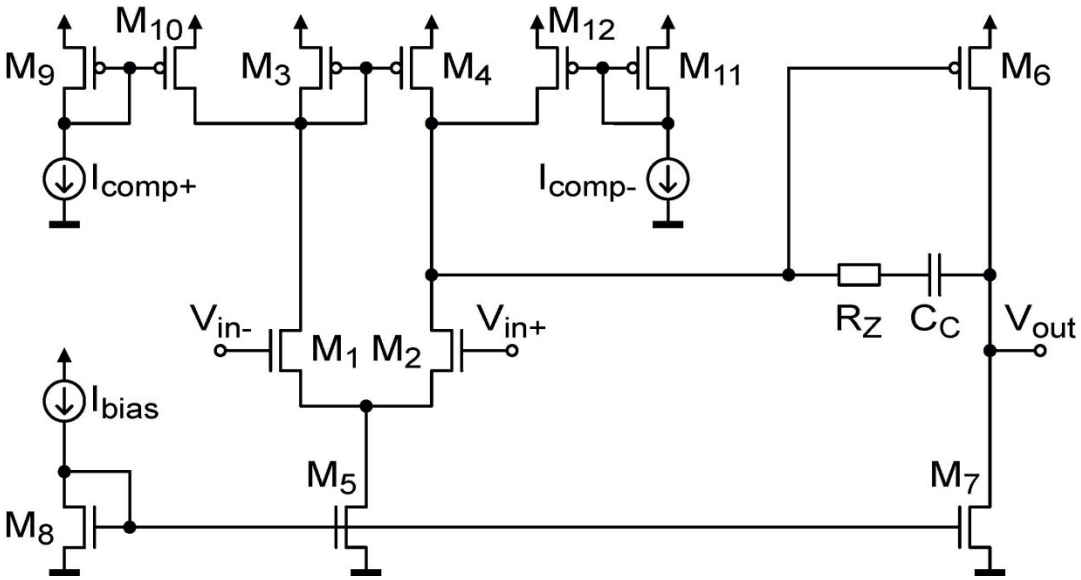
Open-loop



$$V_{out} = AV_O$$

- Closed-loop: calibration during operation possible
- Open-loop: higher detection level

Offset compensation in OAs

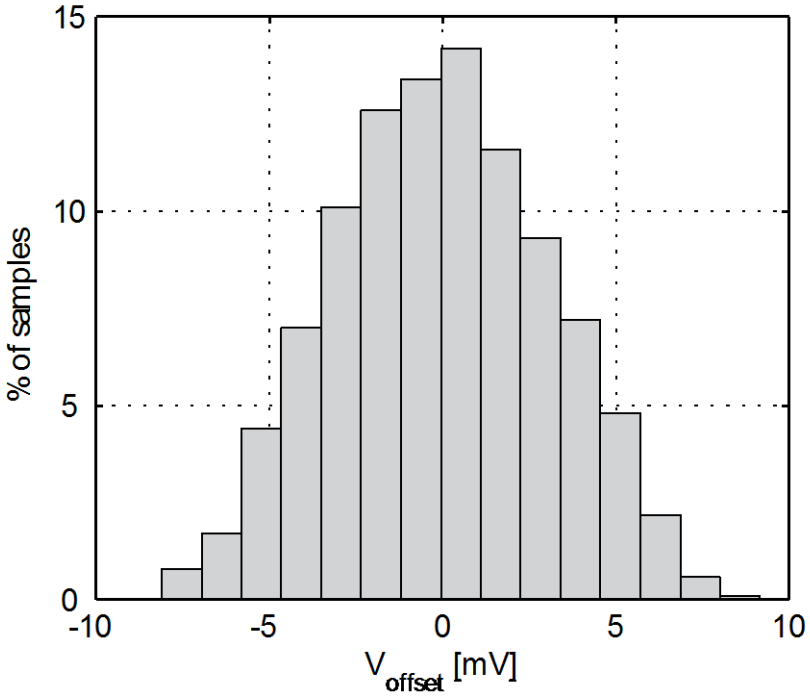


- Compensation by current injection
- Unilateral/bilateral
- Compensation current sources: M/2^{+}M DACs

Choice of compensation node(s)

- Compensation current corrects imperfection only
- Current injected by a small current mirror, taking into account:
  - Channel length modulation
  - Saturation voltage
- Connection of the current mirror does not affect the compensation node characteristics:
  - Impedance
  - Parasitic capacitance
  - System parameters linked to parasitics

Offset distribution before compensation

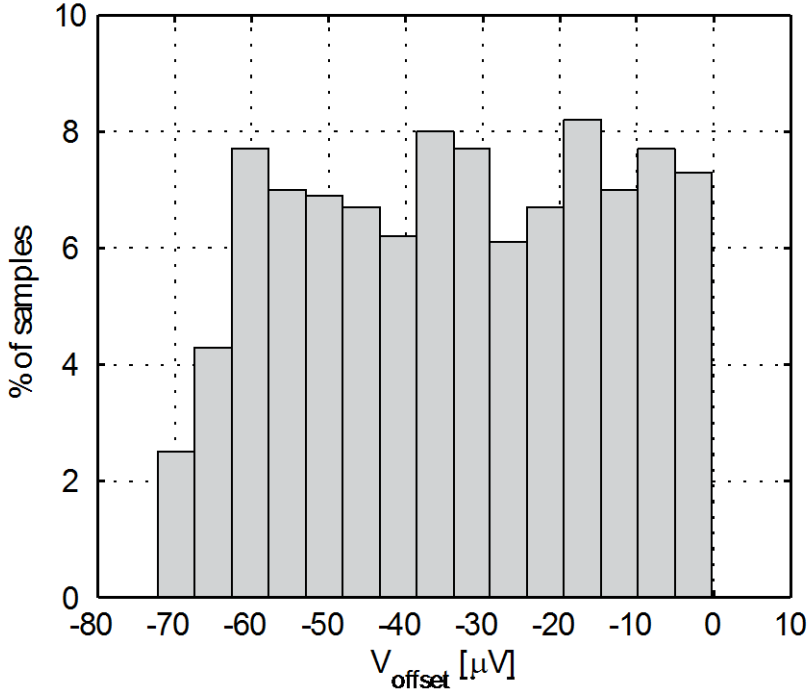


- Gaussian distribution
- Depends on component matching

Offset reduction

- Offset can be reduced by:
  - Matching $\Rightarrow$ Increase area
  - Digital calibration
- Digital calibration circuits can be made very small
- In deep sub-micron technologies:
  - Design analog circuits with reasonable performance
  - Enhance critical parameters by digital calibration
- Mixed-signal solution is optimal in terms of global circuit area

Offset distribution after digital compensation



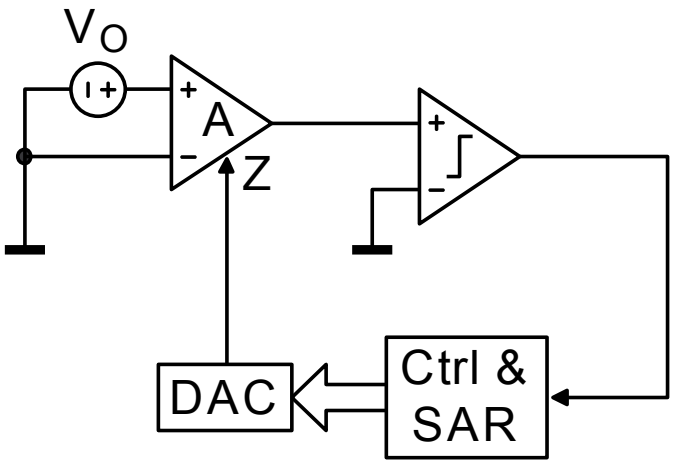
- Uniform distribution (in a 1 LSB interval)
- Residual offset depends on DAC resolution

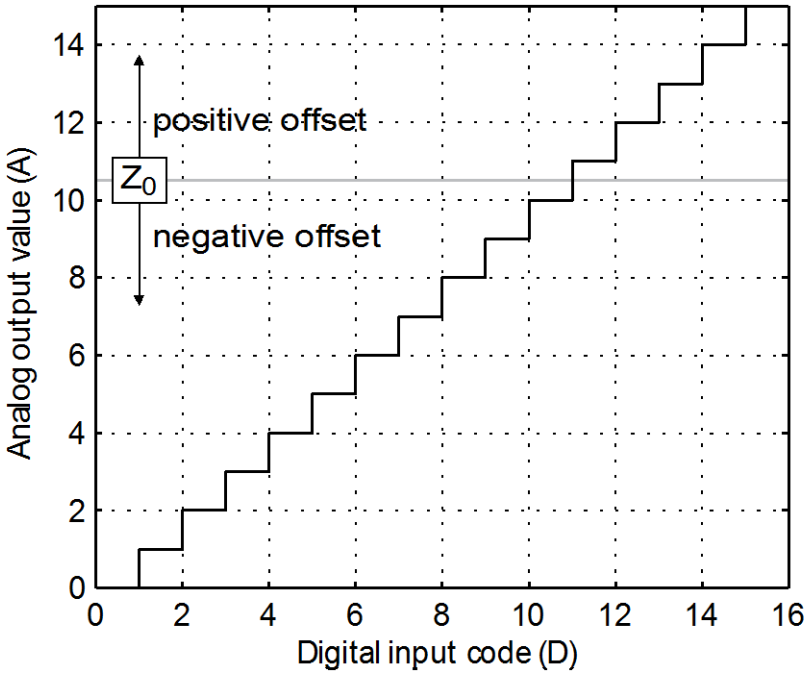
Successive approximations

```
reset all d_i = 0
for i = n downto 1
   set d_i = 1
   if C_out > 0
      reset d_i = 0
   end if
end for
```

- The algorithm decides on the basis of comparisons
- A comparator senses the sign of the imperfection
- Working condition: $b_i \leq b_1 + \sum_{j=1}^{i-1} b_j$ (i ∈ [2, n])

Offset compensation: Target

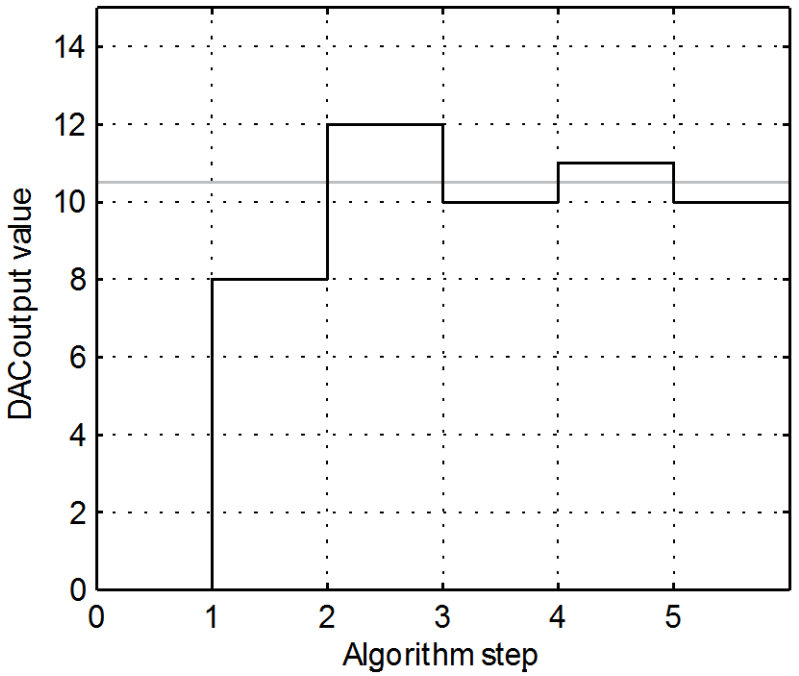




- Z_0: Correction value that perfectly cancels the offset
- $A < Z_0$: Resulting offset negative
- $A > Z_0$: Resulting offset positive

Offset compensation: Algorithm execution

```
reset all d_i = 0
for i = n downto 1
   set d_i = 1
   if C_out > 0
      reset d_i = 0
   end if
end for
```



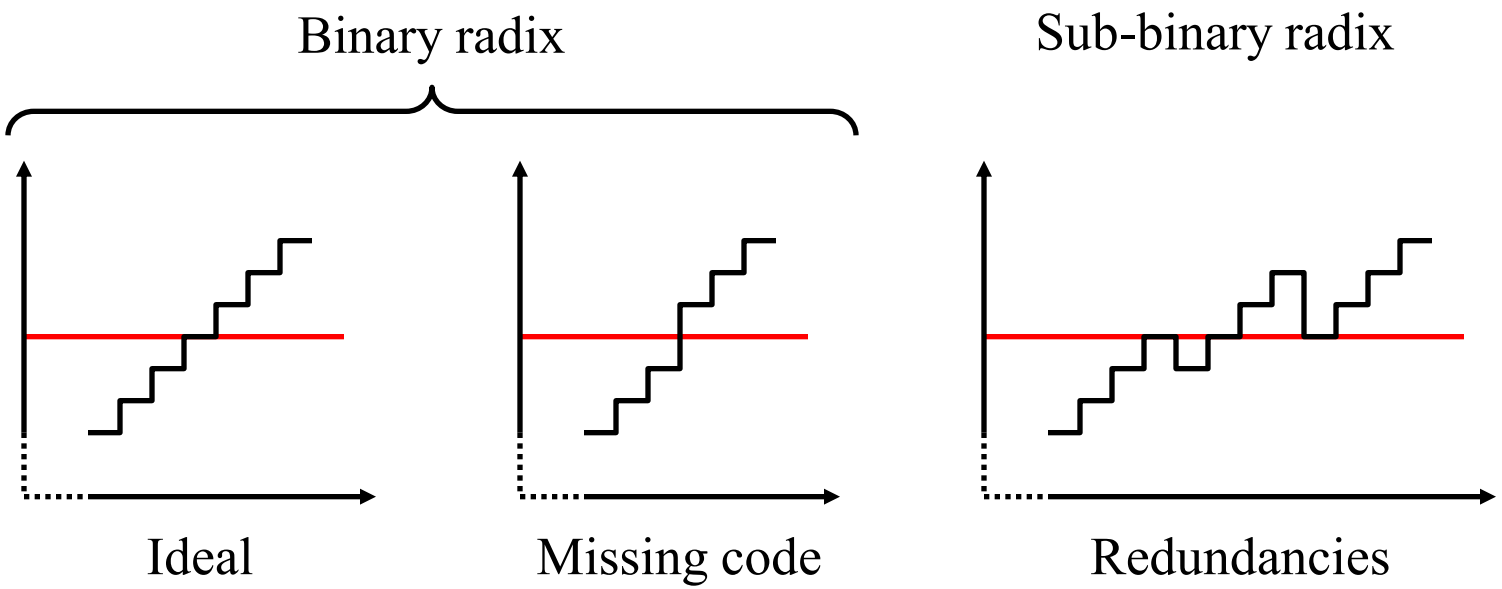
- From MSB to LSB
- Bit kept if compensation value insufficient

DAC Resolution

$$Resolution = \frac{FullScale}{LSB} \leq \frac{V_{offset;uncompensated;\max}}{V_{offset;compensated;\max}}$$

- Full scale chosen to cover whole uncompensated offset range
- Resolution corresponds to residual offset achieved after compensation

DACs for successive approximations



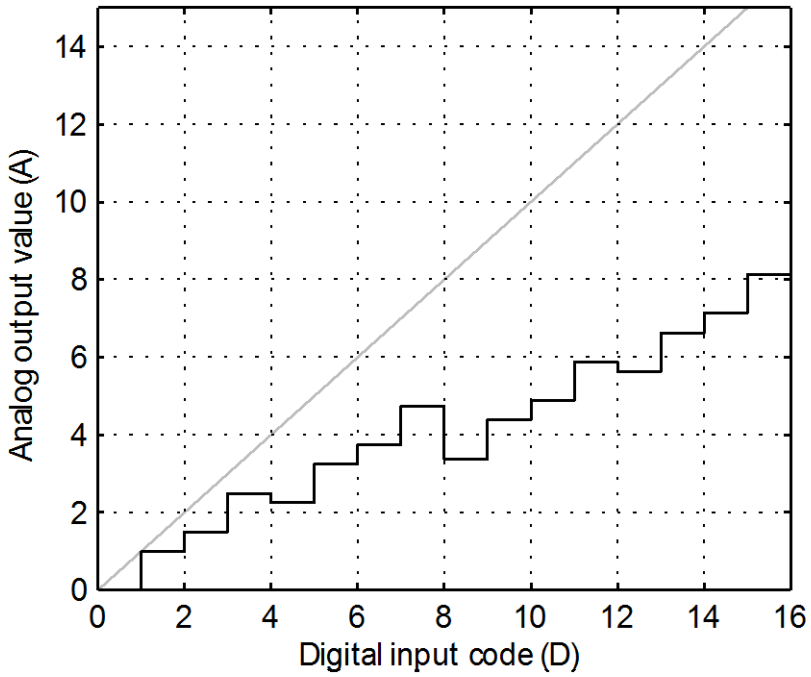
- Imperfections in DACs for compensation
  - Missing codes are problematic
  - Redundancies are acceptable

Sub-binary radix DACs

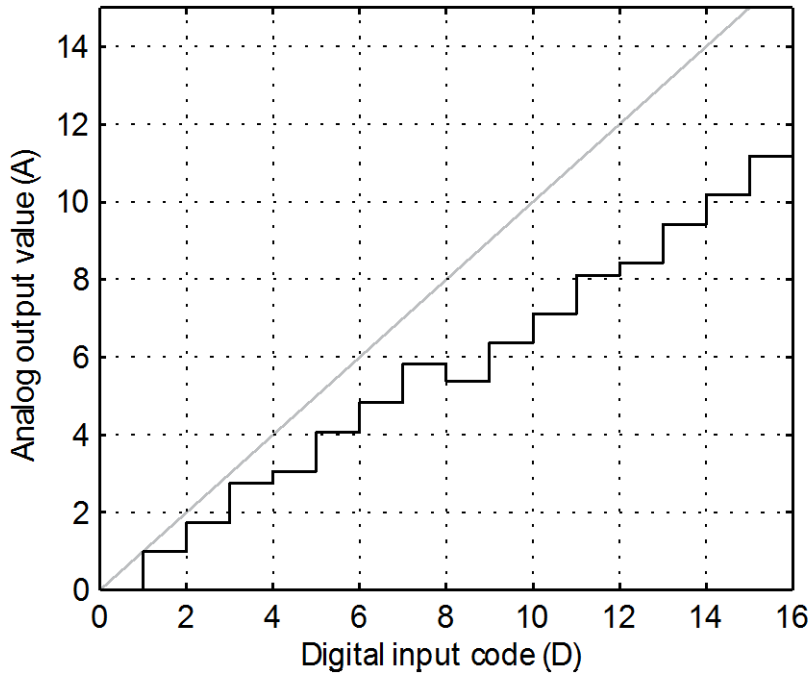
- Code redundancies are voluntarily introduced to:
  - Account for variations of component values
  - Avoid missing codes
- Arbitrarily high resolutions can be achieved without exponential increase of area
- For successive approximations:
  - Precision is not important
  - Resolution is the objective
- **Sub-binary DACs are ideal in conjunction with successive approximations**
  - **Very low area**

Sub-binary DACs: Radix

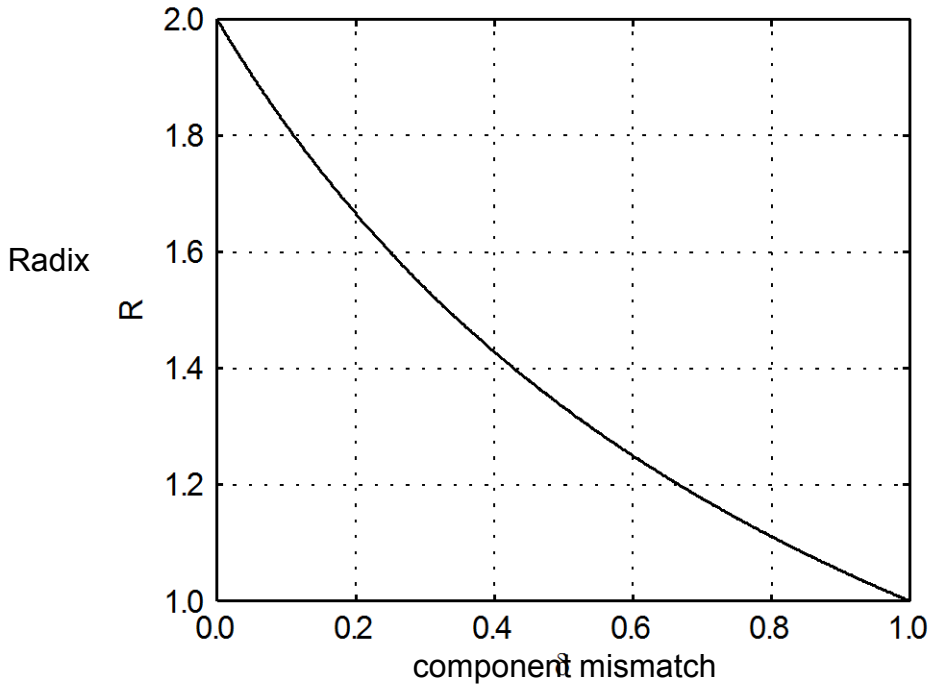
Radix = 1.5



Radix = 1.75

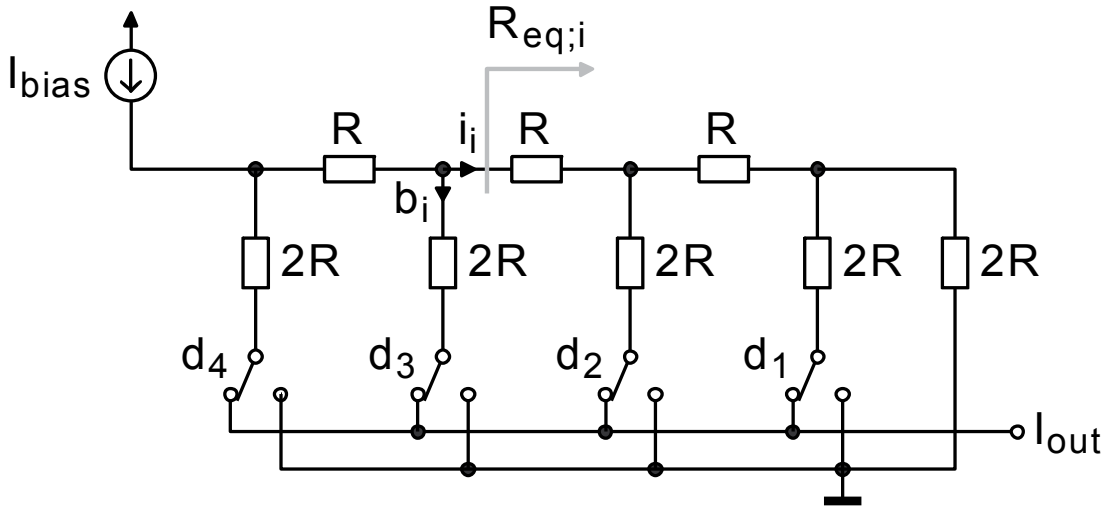


Radix: Tolerance to component mismatch



- Radix-2 tolerates no mismatch!
- 100 % mismatch ⇒ thermometric DAC (radix-1)

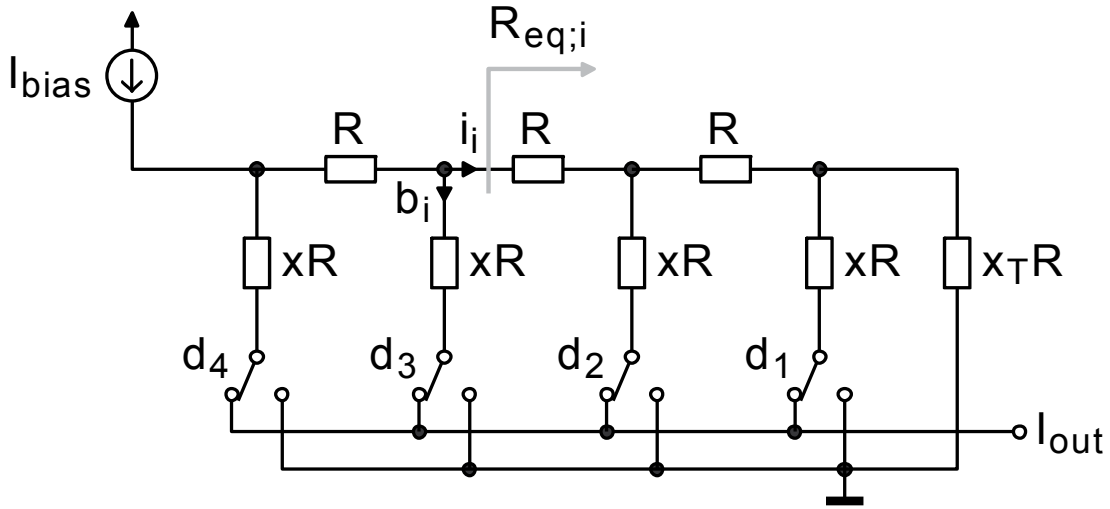
Implementation: Current-mode R/2R converters



$$b_i = b_1 + \sum_{j=1}^{i-1} b_j$$

- $R_{eq;i}$ = 2R ($\forall$ i)
- Current divided equally in each branch ($i_i = b_i$)
- Component imperfection $\Rightarrow$ current imbalance $\Rightarrow$ missing code (or redundancy)

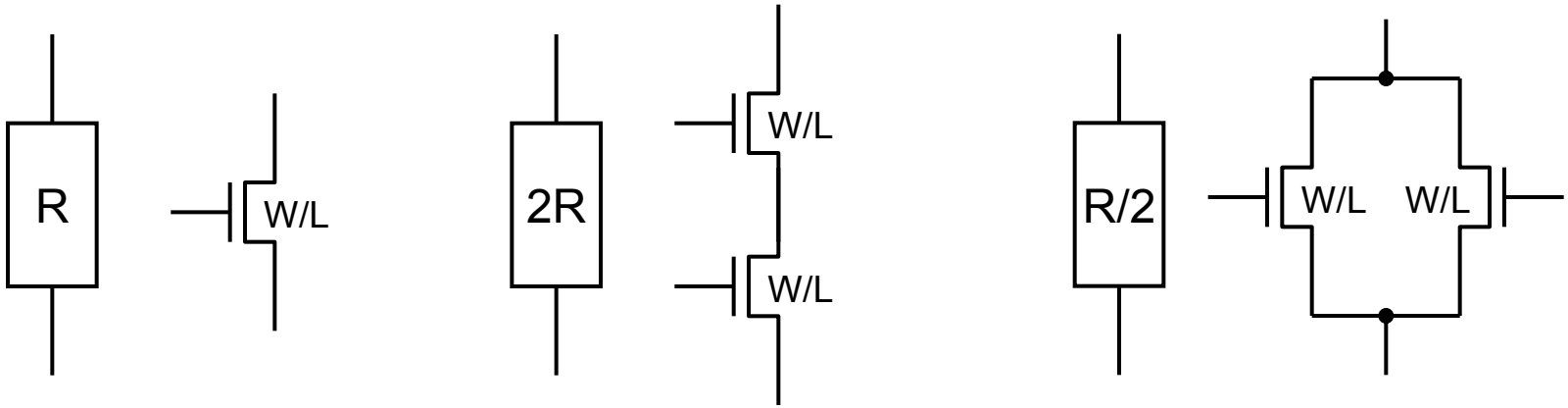
R/2+R converters



$$b_i < b_1 + \sum_{j=1}^{i-1} b_j$$

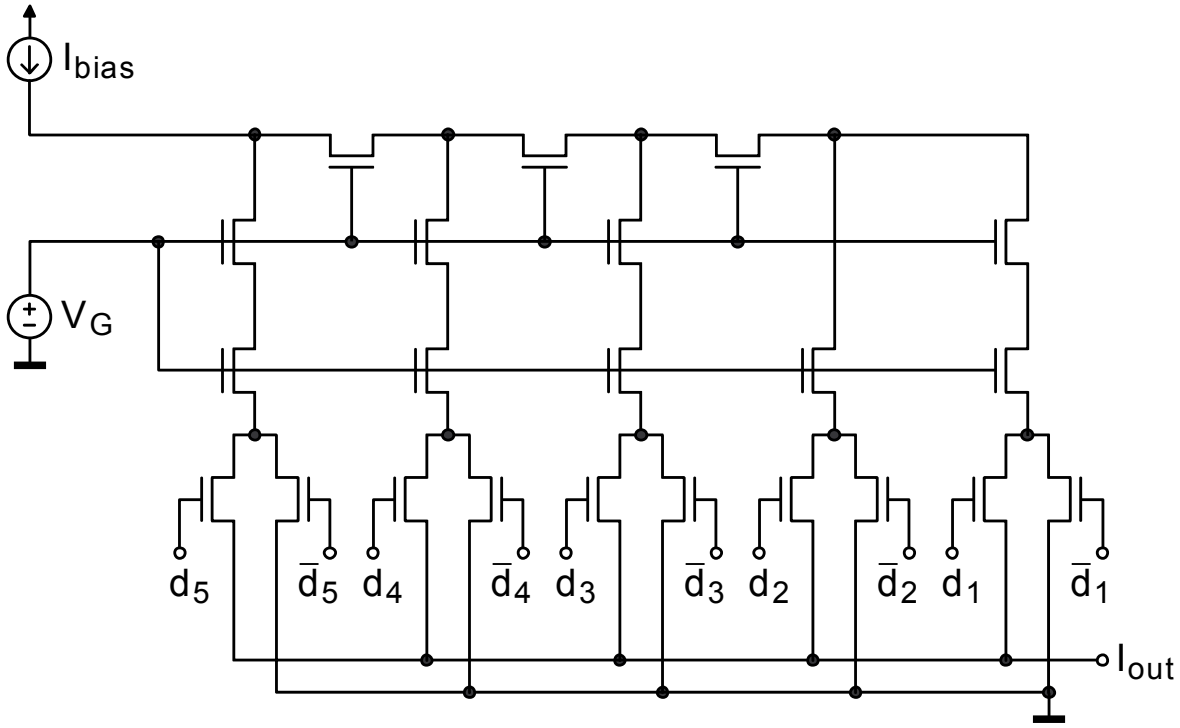
- $x > 2$; $R_{eq;i} < xR$; $i_i > b_i$
- Current division voluntarily unbalanced
  - Radix < 2 (sub-binary)
  - Code redundancies

R/2+R converters: Pseudo-MOS implementation



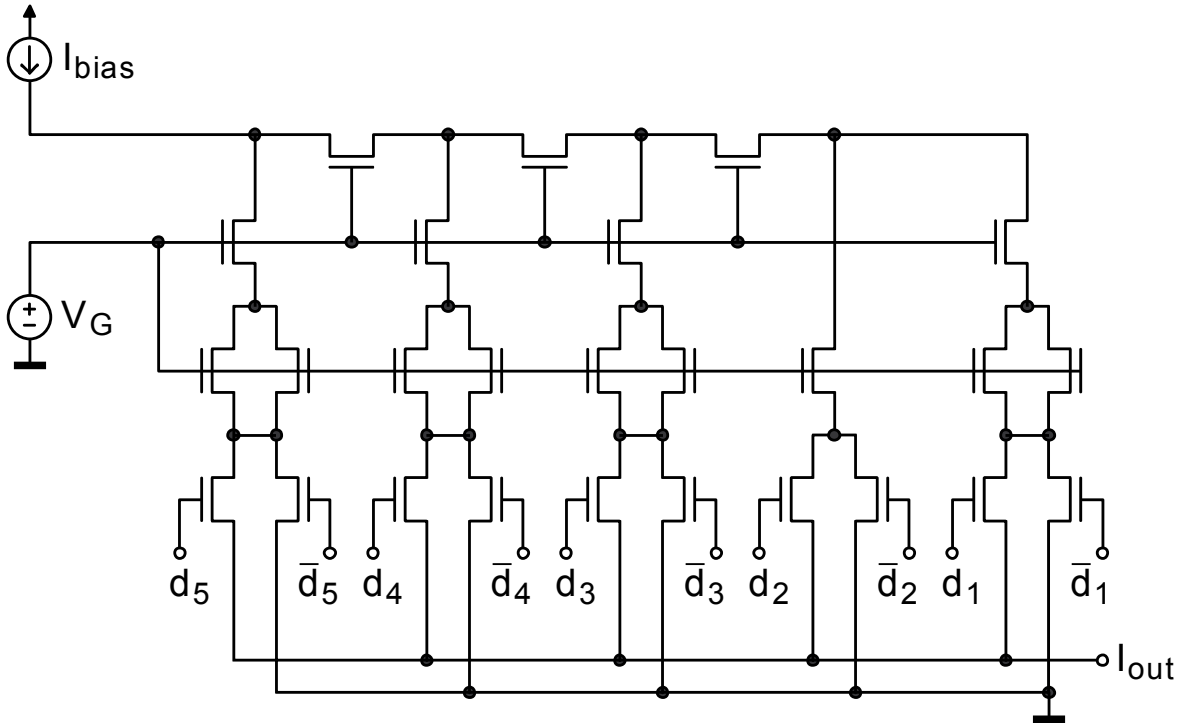
- Resistors can advantageously be replaced by transistors to implement the current division
- Unit-size device with fixed W/L implements R
- Unit-size devices are put in series (2R) or in parallel (R/2)
- Unit-size transistors are kept very small
- Condition: V_G identical for all transistors

M/3M converters



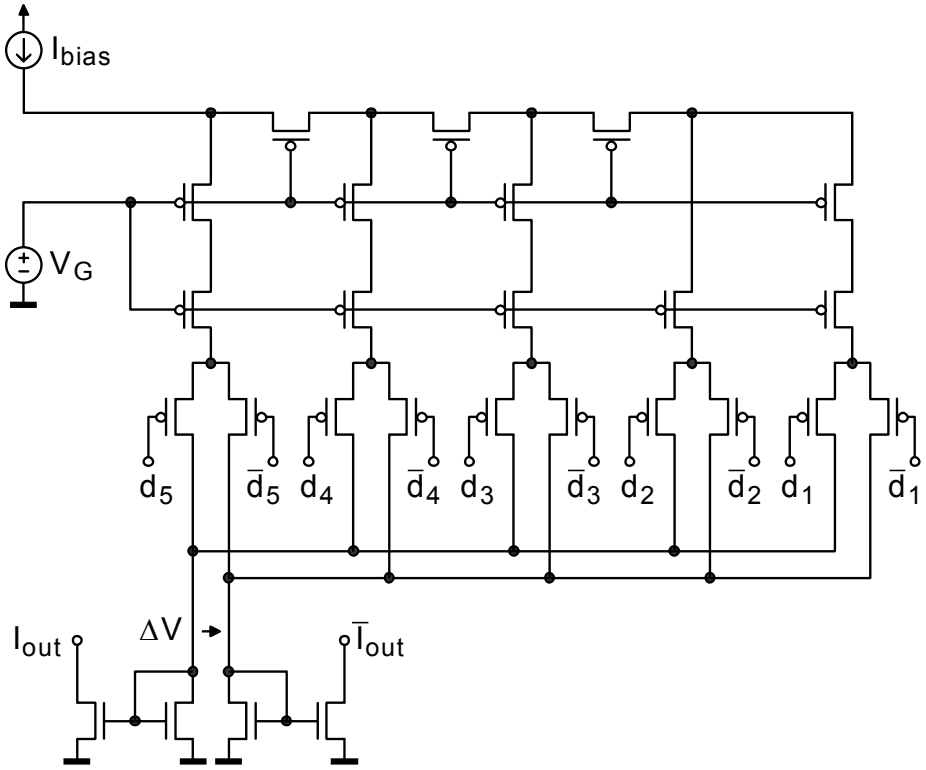
- Radix 1.77 ; maximum mismatch 13 %
- $V_G = V_{DD}$ allows driving d_i directly with logic

M/2.5M converters



- Radix 1.86 ; maximum mismatch 7.3 %
- $V_G = V_{DD}$ allows driving d_i directly with logic

Current collectors & Output stage



- Current mirrors simple to implement
- ΔV is not problematic

Conclusion

- Closed-loop systems are less sensitive to imperfections
- Calibration can be included transparently in sampled systems
- It is advantageous to include sensors in $\Delta\Sigma$ loops
- Switched capacitor circuits enable flexible and reconfigurable systems
- Calibration is necessary in deep sub-micron technologies to reach high performances
- Improve analog performance with digital calibration:
  - Design analog circuits with reasonable performance
  - Enhance critical parameters by digital calibration
  - Mixed-signal solution optimal in terms of global circuit area

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