A 20-b accelerometer-based front-end for instrumentation

Enrico Sentieri – STMicroelectronics
Andrea Baschirotto – Univ. Milan-Bicocca

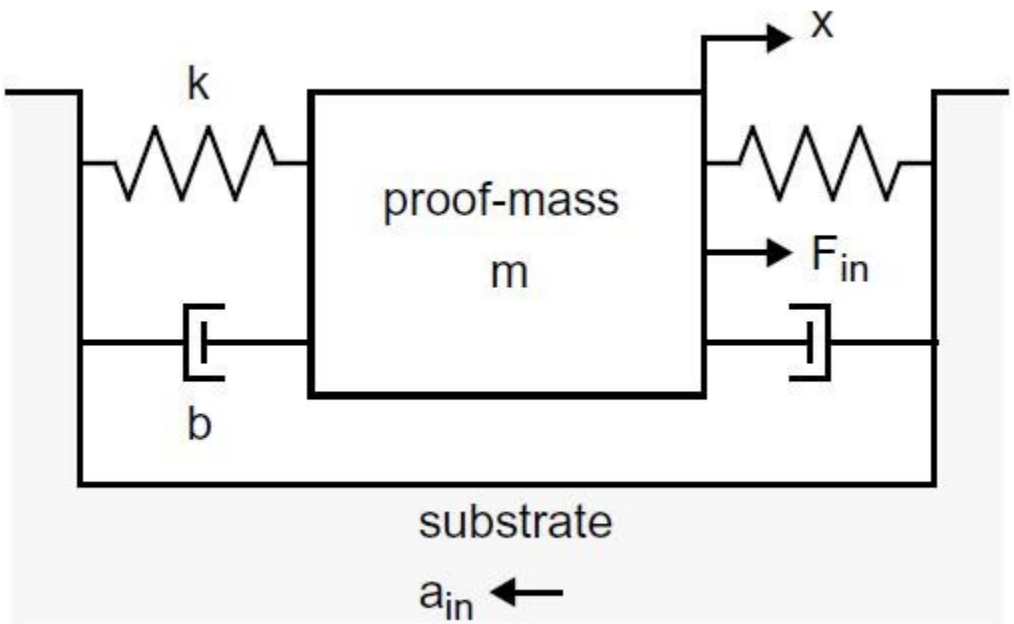
Microelectronics Users eXchange MUX-2011
CERN, June, 9th, 2011

Introduction

- Introduction
- Design Objectives
- Noise Budget Partitioning
- Architecture
- ADC Architecture

Sensor Accelerometers (1)

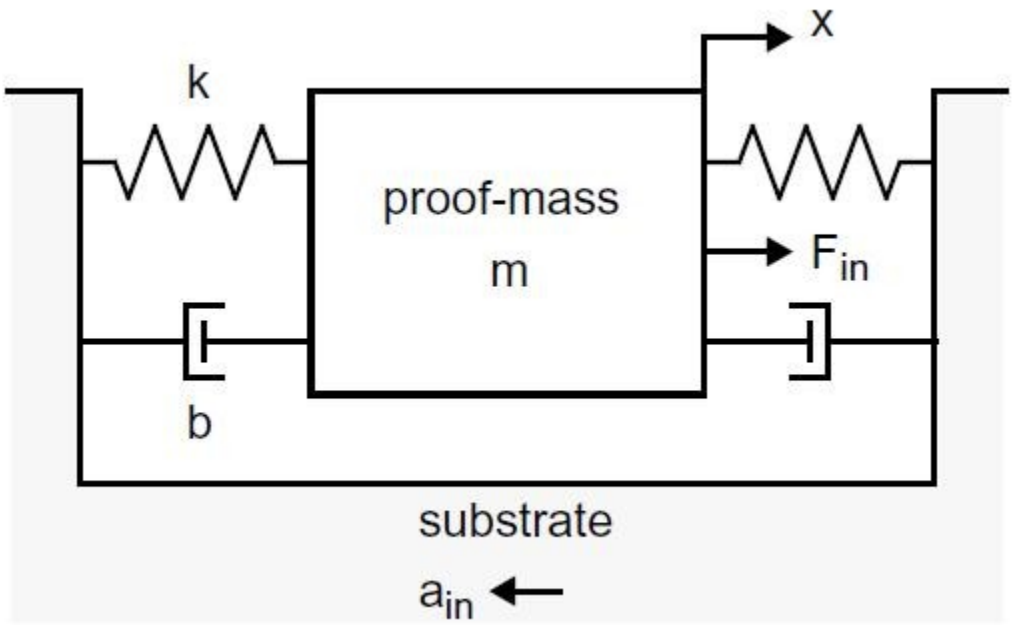
- Displacement accelerometers measure the displacement (**x**) of a suspended proof mass (**m**) in response to an input acceleration (**a**)



$$x = \frac{m}{k} \cdot a_{in}$$

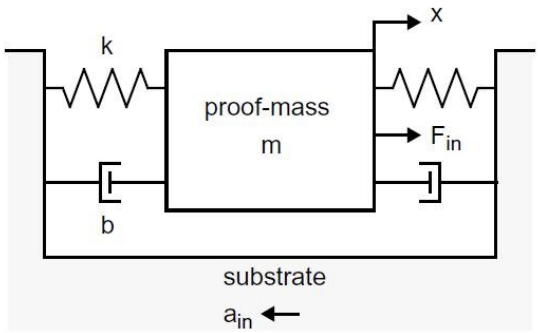
Sensor Accelerometers (2)

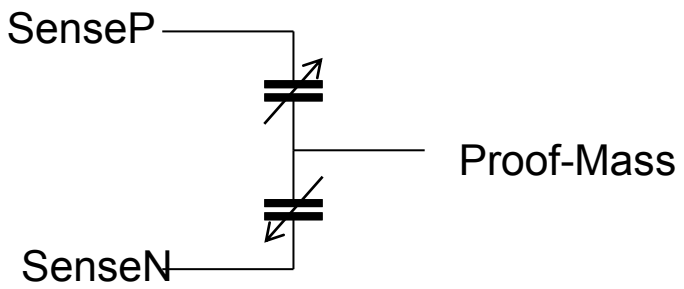
- Displacement capacitive sensors are widely used in several systems
  - Accelerometers
  - Pressure sensors
  - Microphone
  - etc…



Sensor Accelerometer (3)

- Most popular technique to measure the proof mass displacement
  - ➔ ***Capacitive Position Sensing***
  - Different Sensor-Capacitive-Bridge topologies
  - Example:
    - Two nominally equal-sized capacitor are formed between the electrically conductive proof mass and stationary electrodes
    - When the substrate undergoes acceleration
      - ➔ the proof mass displaces from the nominal position
      - ➔ capacitive half-bridge unbalacement



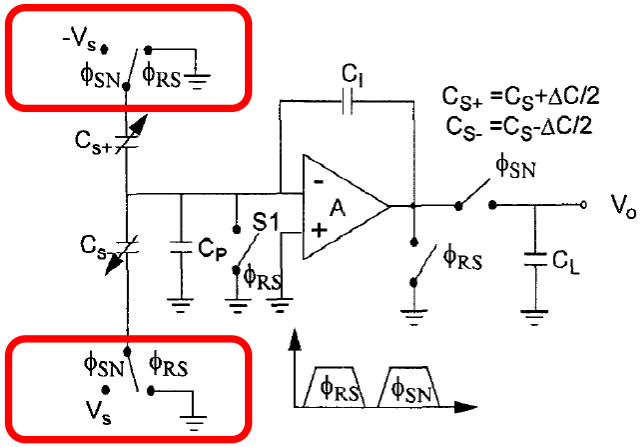


Sensor Accelerometer Interface (1)

- Capacitors sense AC signals
  - ➔ AC modulation sources for capacitive sensing
  - The sensed signal is an Amplitude Modul. Signal
  - The acceleration signal modulates a HF carrier
- To extract the envelopment
  - ➔ The sensed signal need to be demodulated or sampled
- Accelerometer sensitivity ≈ modulation carrier amplitude

Sensor Accelerometer Interface (2)

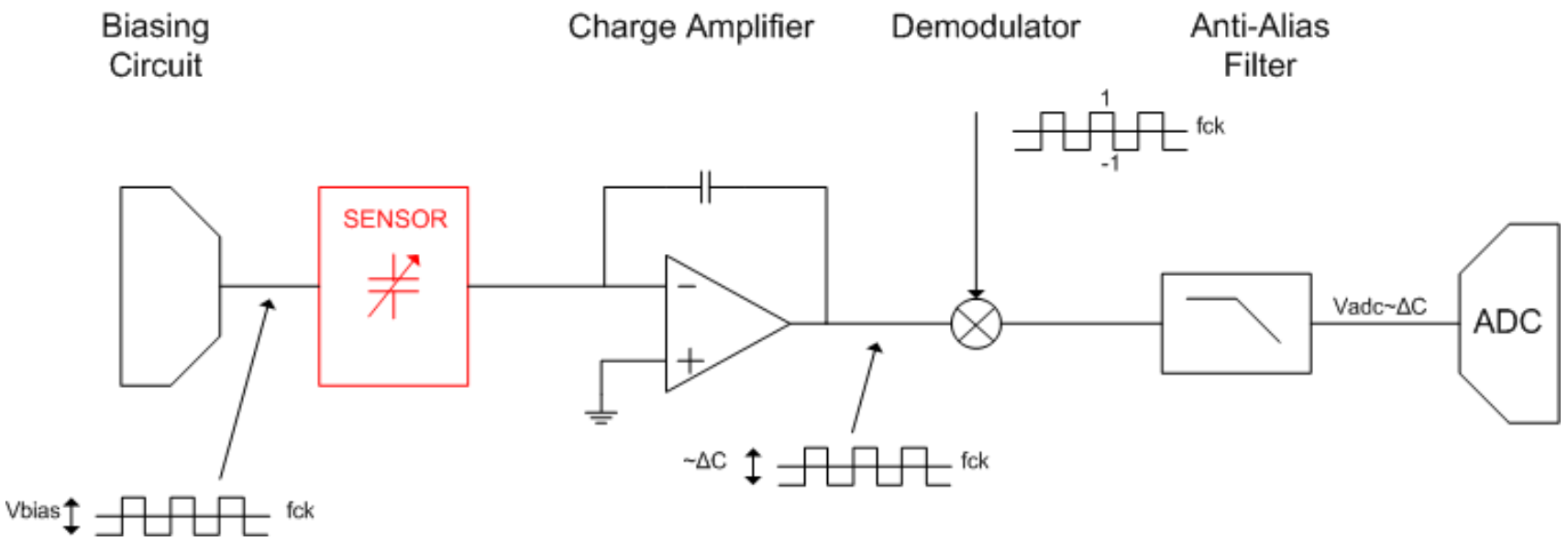
- SC Architectures are very popular



  - MOS switches to connect the sensor and the circuit input.
    - The thermal noise of MOS switches (kT/C noise)
  - SC circuits are sample data systems
    - It is not possible to insert an Anti-Alias filter between reading circuit and sensor
    - ➔ the input wide band noise is folded in base band
      - SC have much higher noise

Modulation/Demodulation

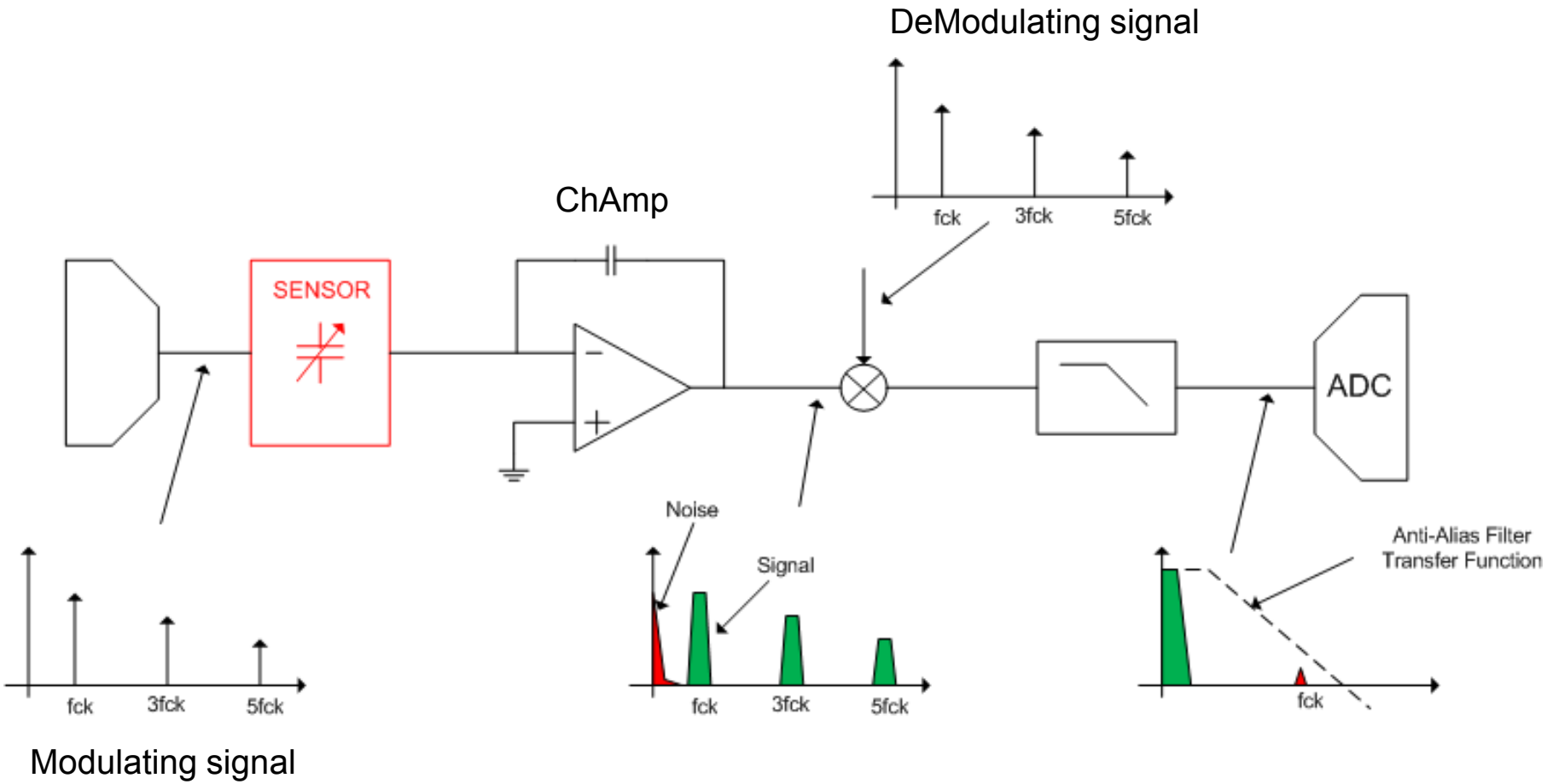
- Time Domain Signal Processing



Modulating signal

Modulation/Demodulation

- Frequency Domain Signal Processing



Gain Error due to Op-Amp band limited (1)

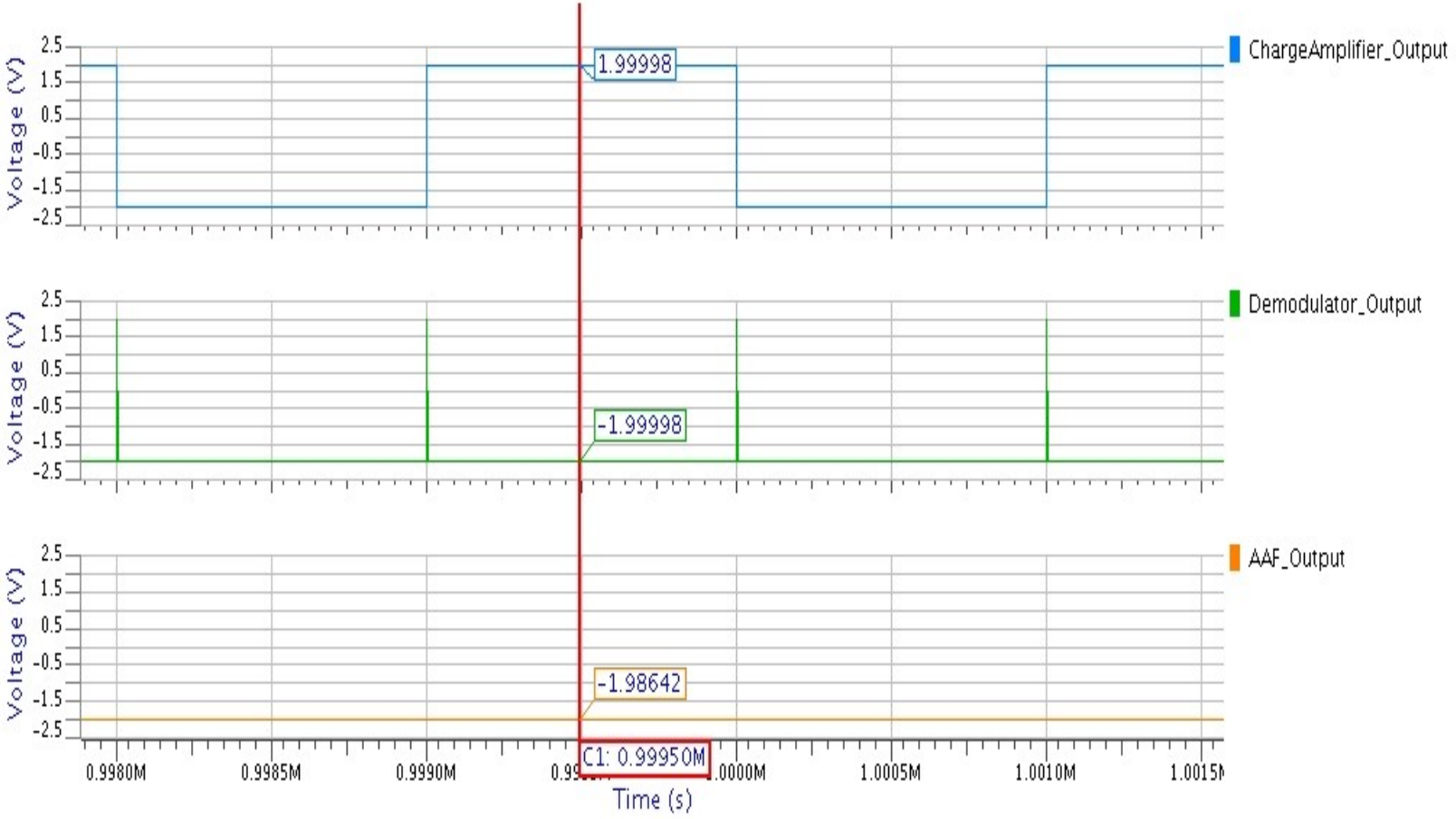
- Modulation ➔ the acceleration is transposed to the odd harmonics frequencies of the Modulation signal

$$X_{2k+1} = \frac{4 \cdot V_0}{\pi} \cdot \frac{1}{2k+1}$$

- The ChAmp *transfer-function* shapes the modulated signal frequency spectrum
  - High-frequency component attenuation
  - ➔ The Demodulated signal amplitude is affected by ChAmp Bandwidth
    - ➔ Gain Error
      - Gain error depends on process and temperature variations

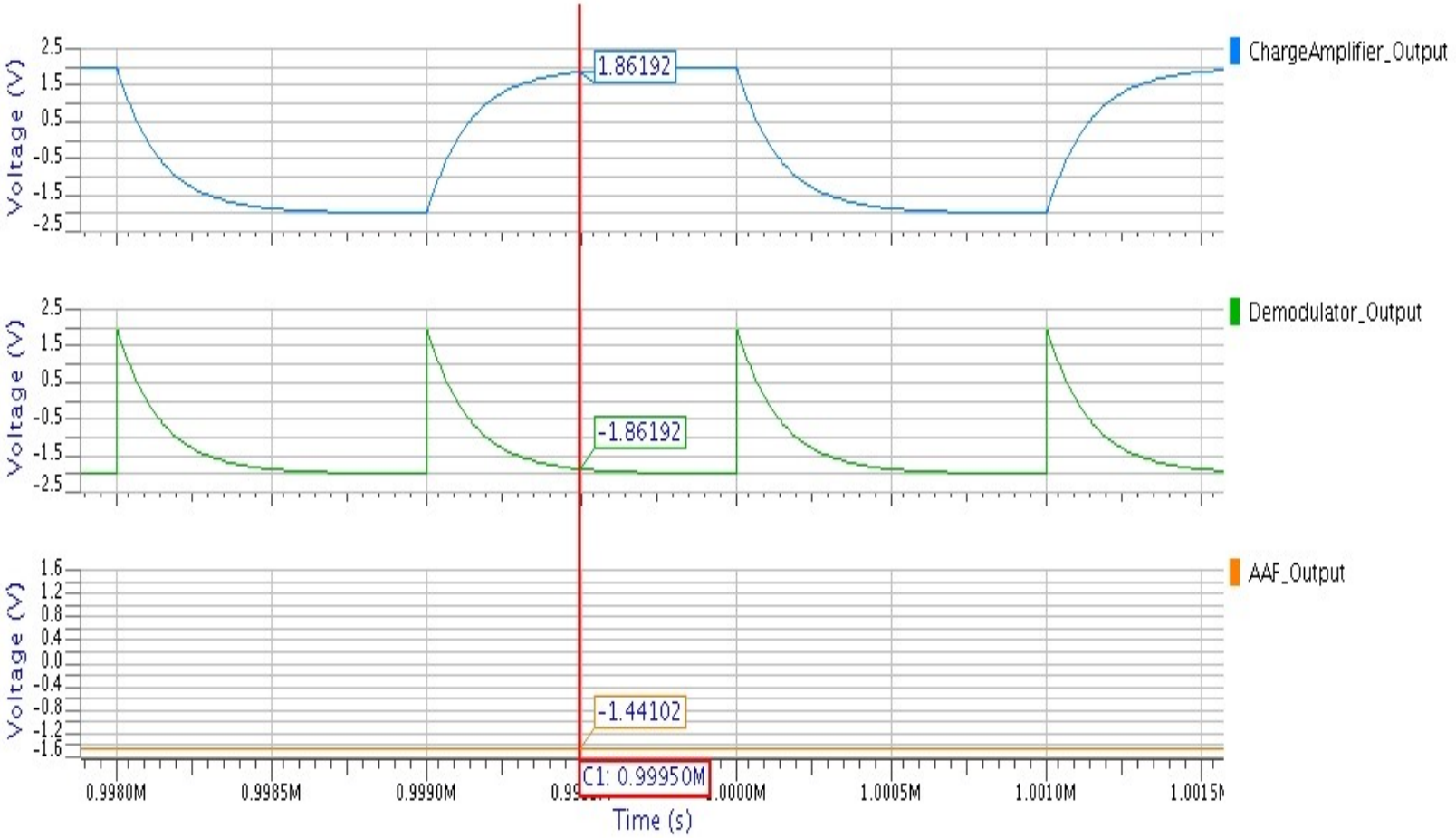
Gain Error due to opamp limited band (2)

Ideal Op-Amp (GBW=1GHz)



Gain Error due to opamp limited band (3)

Ideal Op-Amp (GBW=1MHz)



Mod/Dem-Freq vs. Power Consumption

- Higher Mod/Dem-Freq
  - ☺ In CMOS circuit, the electronics low frequency ***flicker-noise*** which often extends to low MHz
  - ☹ Larger opamp Gain-Bandwidth
    - ➔ Higher Power Consumption
    - ➔ trade-off between performances and power consumption
  - Typically the Mod/Dem-Freq (f_m) is from some tens of kHz to MHz
    - ➔ f_m = 100kHz

Design Objectives

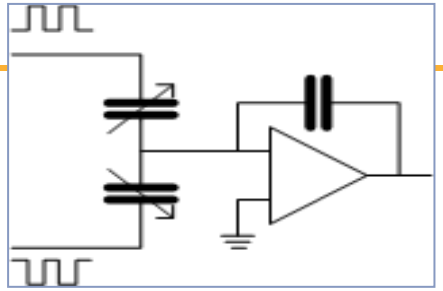
- Introduction
- Design Objectives
- Noise Budget Partitioning
- Architecture
- ADC Architecture

Design Objectives (1)

- Design a digitizing accelerometer interface that uses the full bandwidth and dynamic range of the sensor
  - ➔ The Sensor Signal Full-Scale is ±2G
  - ➔ The total equivalent acceleration noise < 2.5μG
    - sensor + electronic

$$SNR = 20 \cdot \log_{10}\left(\frac{2G}{\sqrt{2}} \cdot \frac{1}{2.5\mu G}\right) = 115dB$$

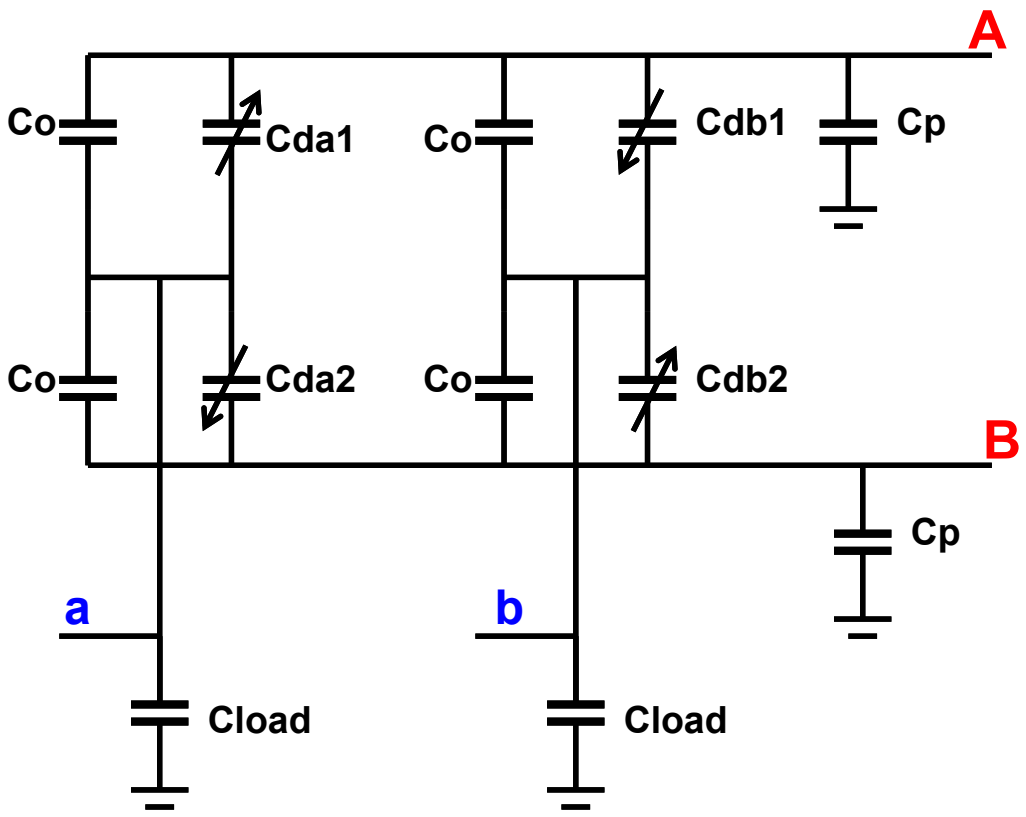
Design Objectives (2)



- Low power consumption
  - Architecture choice
    - ➔ Open-Loop Capacitive sensor Interface
  - Interface Topology
    - ➔ Charge Sensitive Amplifier with modulated input and synchronously demodulated output
  - The capacitive bridge is driven (modulated) by a squared wave voltage
    - Gain error (due to Sensor and Integrated Circuit process variation) has to be compensated
  - Bias Voltage Amplitude ➔ 10b resolution programmable

Capacitive Sensor

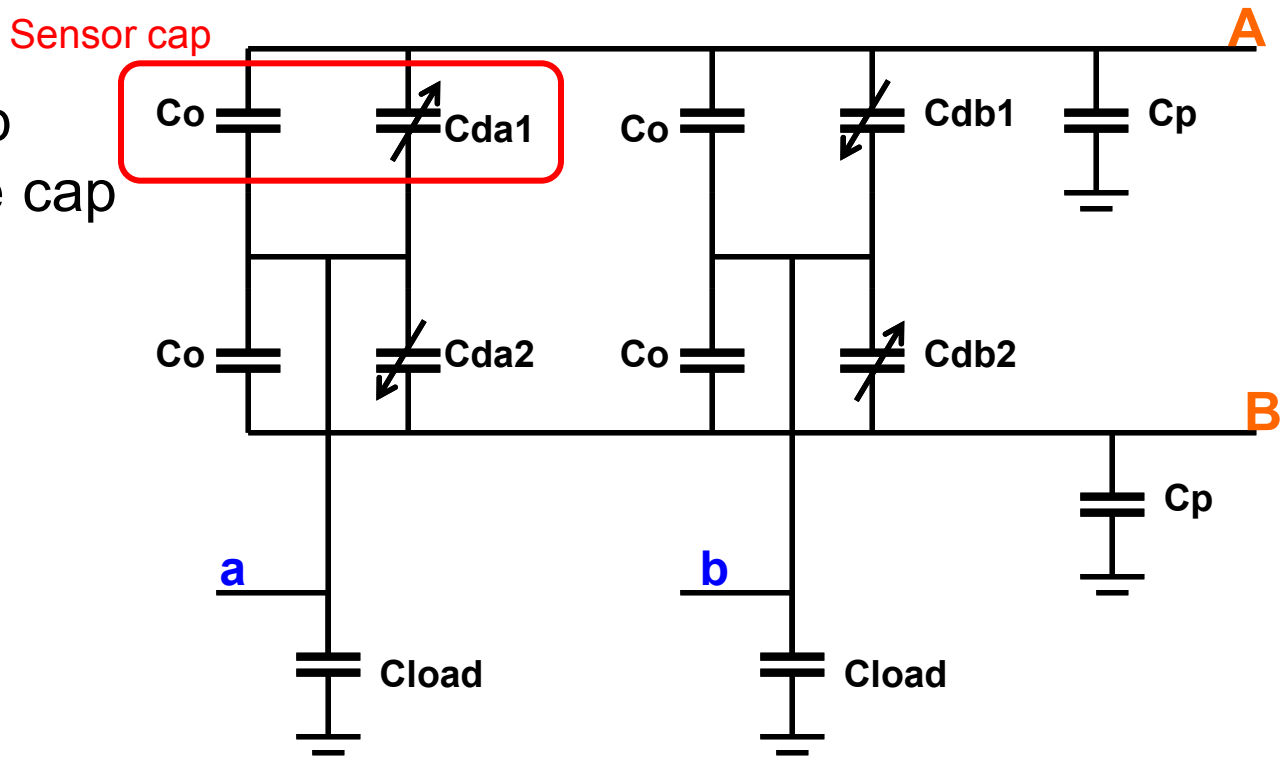
- The Capacitive sensor
  - ➔ fully-differential
  - The bridge is driven by a differential signal **a** & **b**
  - With an acceleration ➔ the capacitive bridge is unbalanced ➔ a differential charge is injected in the pins **A** & **B**



Differential charge ≈ acceleration

Capacitive Sensor Equivalent electrical Model

C_o ➔ fixed cap
C_{dxx} ➔ variable cap



a&b ➔ Modulating Sensor Pin

A&B ➔ Reading Sensor Pin

$$Cda1 = Cdb2 = -Cda2 = -Cdb1 = SF \cdot a$$

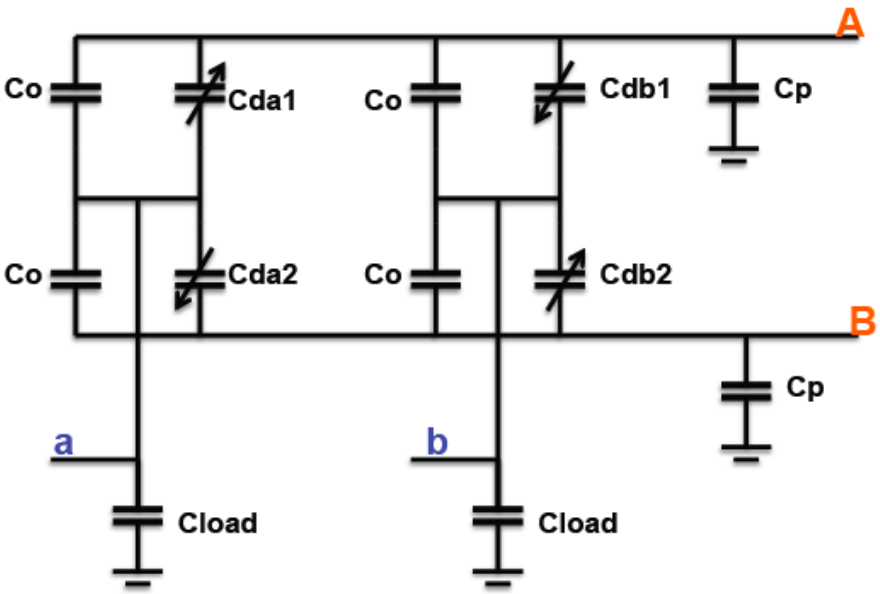
SF : Scale Factor [F/g]

a: acceleration [g]

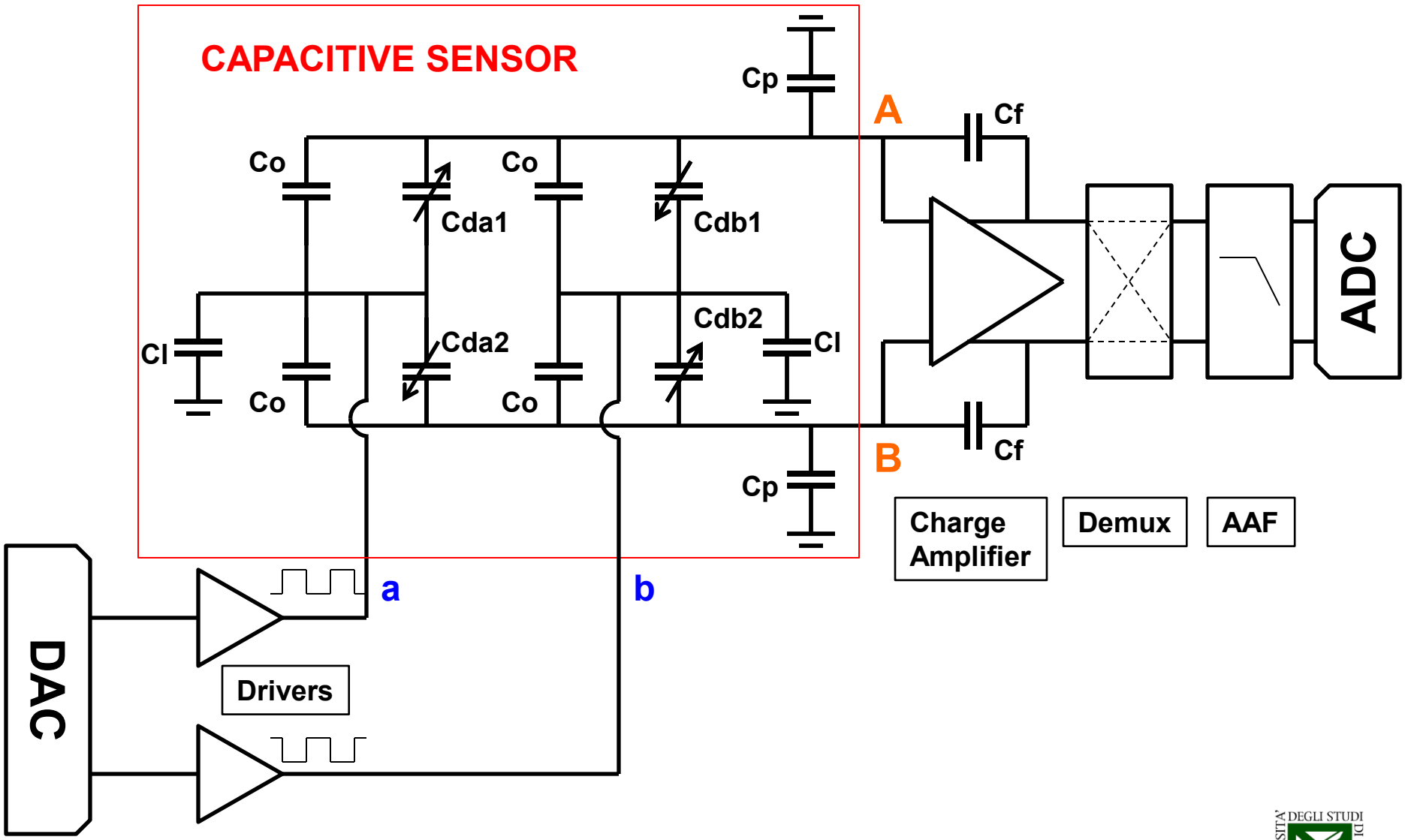
Sensor Topologies: Jiangfeng Wu. "Sensing and Control Electronics for Low-Mass Low-Capacitance MEMS Accelerometers", Department of Electrical and Computer Engineering, Carnegie Mellon University,Spring 2002.

Capacitive Sensor Parameters

- Sensor Input and Interconnection Capacitance
  - ➔ C_p=12pF
- C_{load}=20pF
- Sensor cap
  - C_o=1pF
- Scale Factor
  - ➔ SF = 300fF/G
- Sensor Dynamic Range
  - ➔ ±2G ➔ S=2G
- Sensor Noise Density
  - ➔ a_{sn}=100nG/sqrt(Hz)
- Sensor Bandwidth
  - ➔ BW=300Hz



Ideal Sensor Accelerometer Interface



Technology Choice(1)

- The technology choice driven by:
  - Performance
  - Cost
  - Process Maturity
  - Analog Option Required

Technology Choice (2)

- Standard CMOS technology with double thick oxide
- A rough system analysis
  - ➔ more than 90% device area is used for analog blocks
  - ➔ No need to use technology with high level of integration density
  - ➔ The technology choice is driven by analog requirement
- A Mature technology with two different thick oxide MOS has been selected:
  - 70Å (3.3V gate, 0.350µm minimum channel length)
  - 120Å (5.0V gate, 0.500µm minimum channel length)
  - The 5.0V MOS slower and noisier than 3.3V MOS
- Two power supply domains (5.0V & 3.3V) are available

Technology Choice (3)

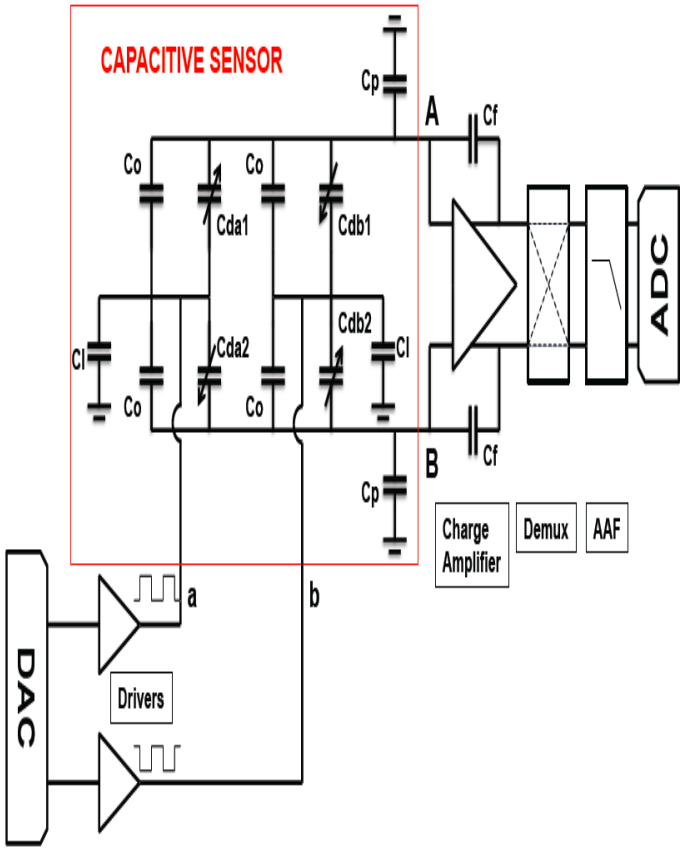
- Resistors
  - Linear Resistor (Doped-Poly resistor)
  - Diffused Resistor
    - poor linearity
    - no flicker noise compared to the poly resistor
  - HIPO (High resistance poly) resistor
    - higher sheet resistance compared to poly resistor.
    - extra mask ➔ higher cost
- Capacitor
  - High-linearity caps required for the Charge Amplifier feedback capacitor and ADC (Switched Capacitor) ➔ Metal to metal capacitor is the best choice
    - MIM (Metal Insulator Metal)
      - Thin oxide ➔ High density level
      - Extra Masks ➔ Higher Cost
    - Fringed Capacitor
      - Lower density
      - No extra mask

Noise Budget Partitioning

- Introduction
- Design Objectives
- Noise Budget Partitioning
- Architecture
- ADC Architecture

Noise Budget Partitioning (1)

- Starting from high level specifications
  - ➔ define the specification for each blocks of the system
  - ➔ identify critical blocks
  - ➔ roughly definition of a suitable architecture of each block
- Simplifications
  - This preliminary analysis should be done not considering mod/dem effects



Noise Budget Partitioning (2)

- The **Noise Budget partitioning** is an iterative design process
- Some design specifications are defined based on preliminary analysis/assumptions
  - ➔ the required performances for each block are evaluated
    - in case of any issue, the assumptions will be modified
- It's quite impossible, at the first run, to identify all the critical design parameter

Noise Budget Partitioning (3)

- Target: Total noise ➔ a_{n_rms}= 2.5μG
- Two different main Noise contributors:
  - Sensor Noise (Brownian Noise) ➔ a_{sn_rms}
  - Electronic Noise ➔ a_{en_rms}
    - Quantization Noise, Thermal Noise, & Flicker Noise

  - Sensor Noise (a_{sn_rms}):

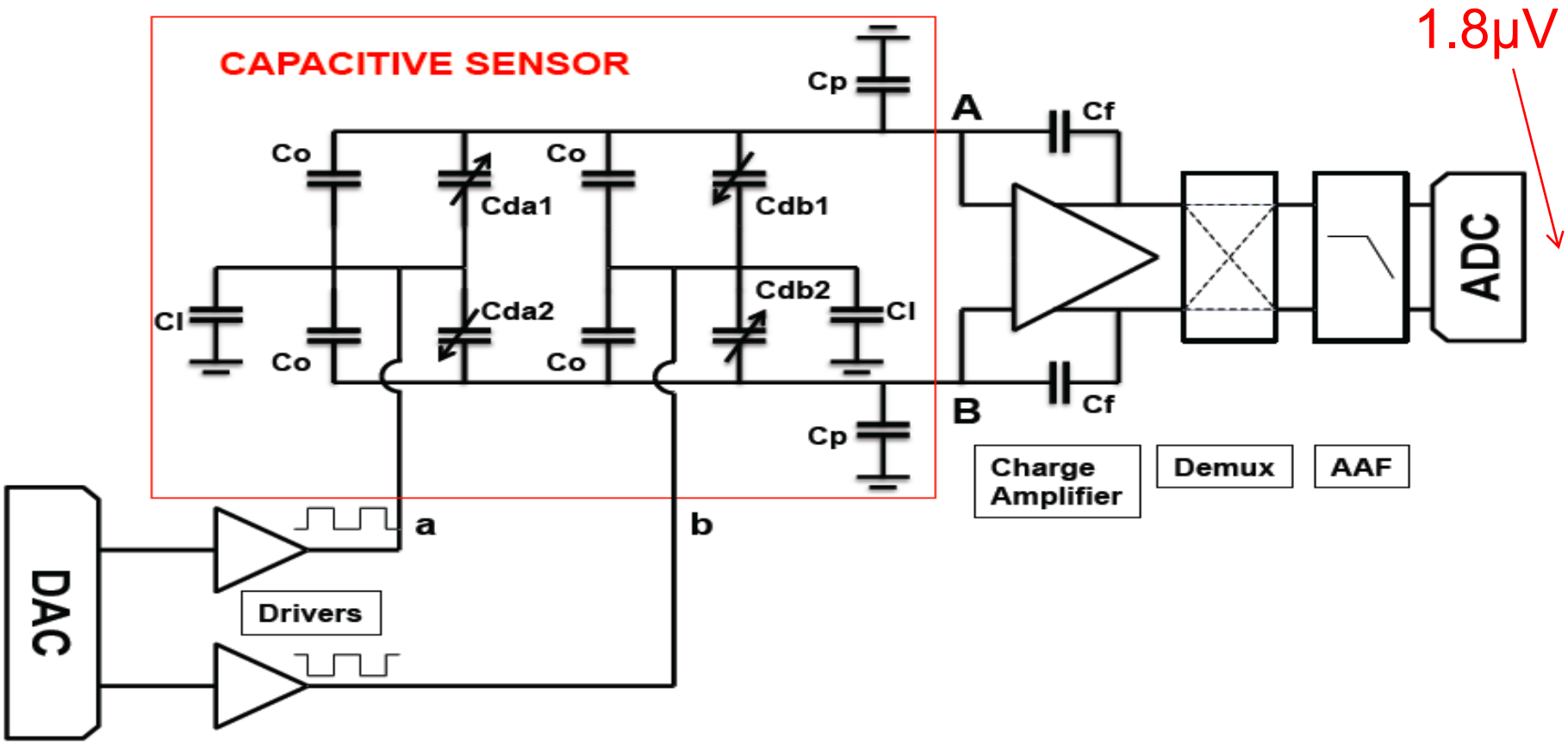
$$a_{sn\_rms} = a_{sn} \cdot \sqrt{BW} = 100nG/\sqrt{Hz} \cdot \sqrt{300Hz} = 1.73\ \mu G$$

  - Electronic Noise ➔ Equivalent Acceleration noise is evaluated to match the design Objectives:

$$a_{en\_rms} = \sqrt{a_{n\_rms}^2 - a_{sn\_rms}^2} = 1.81\mu G$$

Noise Budget Partitioning

- Assuming no-noise sensor



Noise Budget Partitioning (4)

- SNR due to the only electronic Noise evaluated at Sensor level:

$$SNR_e = 20 \cdot \log_{10}\left(\frac{S}{\sqrt{2}} \cdot \frac{1}{a_{en\_rms}}\right) = 117.9dB$$

- ➔ First design specification,
  - the SNR @ADC-output > 117.9dB
    - ➔ ADC resolution has to be:

$$ENOB_{ADC} > \frac{SNR_e - 1.76}{6.02} = 19.3bit$$

ADC Performances (1)

- ADC resolution >19.3 bit
  - SC-ΣΔ Architecture
    - ➔ the only one to satisfy this challenging design specifications.
    - Oversampled ADC architecture ➔ Relaxed the Anti-Alias Filer requirements specification
  - The small signal bandwidth
    - Critical opamp flicker-noise
    - ➔ the ADC with *Correlated Double Sampling* or *Chopper Stabilization* technique

ADC Performances (2)

- Which Power Supply?
  - ADC under 5V supply domain
    - ➔ higher reference voltage compared to 3.3V supply domain
    - ➔ Sample capacitor reduction (less area) and/or reduce the Oversampling Ratio (smaller opamp bandwidth)

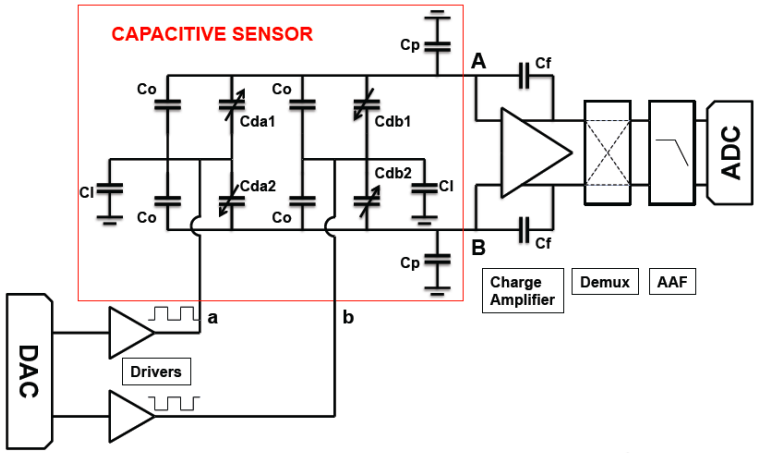
$$V_{signal} \propto V_{ref}$$

$$V_{noise} \propto \sqrt{\frac{K_b \cdot T}{C_s \cdot OR}}$$

V_{ref}: ADC reference Voltage
K_b: Boltzmann Constant
T: Temperature
C_s: Sampling Capacitor
OR: Oversampling Ratio

ADC Performances (3)

- Which Power Supply?
  - 5.0V MOS have *higher 1/f noise* than 3.3V MOS
    - Increased oxide thickness ➔ Increased trap number in the silicon oxide interface.
  - If the ADC is designed under 5.0V domain
    - ➔ The Charge-Amplifier to be designed under the same supply domain to use all the available ADC dynamic range



ADC Performances (4)

- Both solutions have some advantages (larger signal @5V) and some drawbacks (larger 1/f noise @5V)

- The best compromise performance vs. power consumption has been achieved supplying ***the ADC and Charge Amplifier at 3.3V***

ADC Performances (5)

Assumptions:

- ADC Differential Reference Voltage ➔ $2.5V_{peak}$
  - Possible under 3.3V domain
- Maximum ADC Input signal ➔ $2.0V_{peak}$
  - To avoid Modulator Saturation issue
    - ~2dB of margin
- ADC resolution required 20 bit

ADC Performances (6)

- Total Noise at ADC output

$$V_{n_{@ADCoutput}} = \frac{S_{in\_ADC_{max}}}{\sqrt{2}} \cdot 10^{-\frac{SNR_e}{20}} = \frac{2}{\sqrt{2}} \cdot 10^{-\frac{117.9}{20}} = 1.8\ \mu V$$

- ADC Noise
  - Assuming dominant quantization noise

$$V_{nADC} = \frac{LSB}{\sqrt{12}} = \frac{V_{in\_ADC_{max}}}{2^{(nbit-1)}} \cdot \frac{1}{\sqrt{12}} = \frac{2}{2^{19}} \cdot \frac{1}{\sqrt{12}} = 1.1\ \mu V$$

Biasing and Reading Noise partitioning

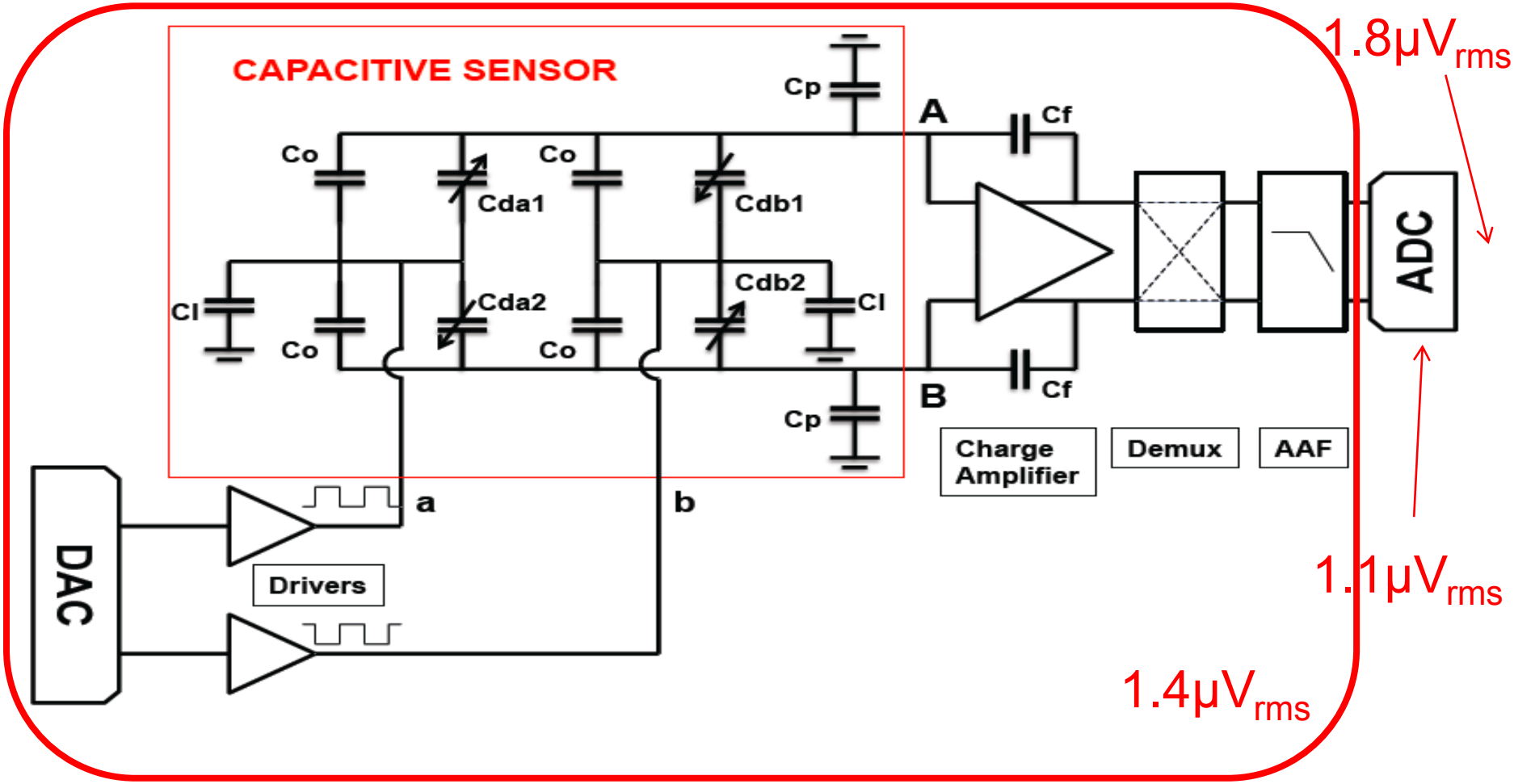
$$V_{nBiasRead} = \sqrt{V_{n\_@ADCout}^2 - V_{nADC}^2} = 1.42\ \mu V$$

- The system is divided in to two different macro blocks:
  - Reading (Charge Amplifier and AAF)
  - Biasing (DAC and Driver)

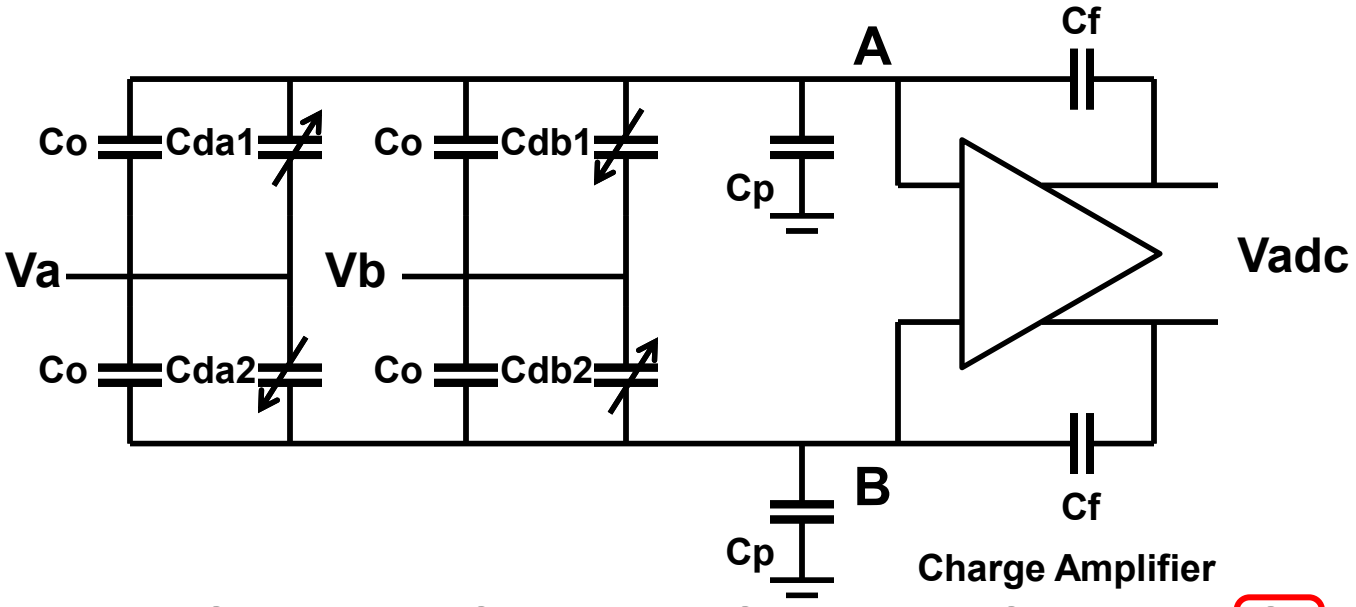
	Noise Biasing/Noise Reading				
	3/1	2/1	1/1	1/2	1/3
Noise Biasing V_{nBias}	1.35μV	1.27μV	1μV	0.63μV	0.45μV
Noise Reading V_{nRead}	0.45μV	0.63μV	1μV	1.27μV	1.35μV

Noise Budget Partitioning

- Assuming no-noise sensor



Sensor Transfer Function



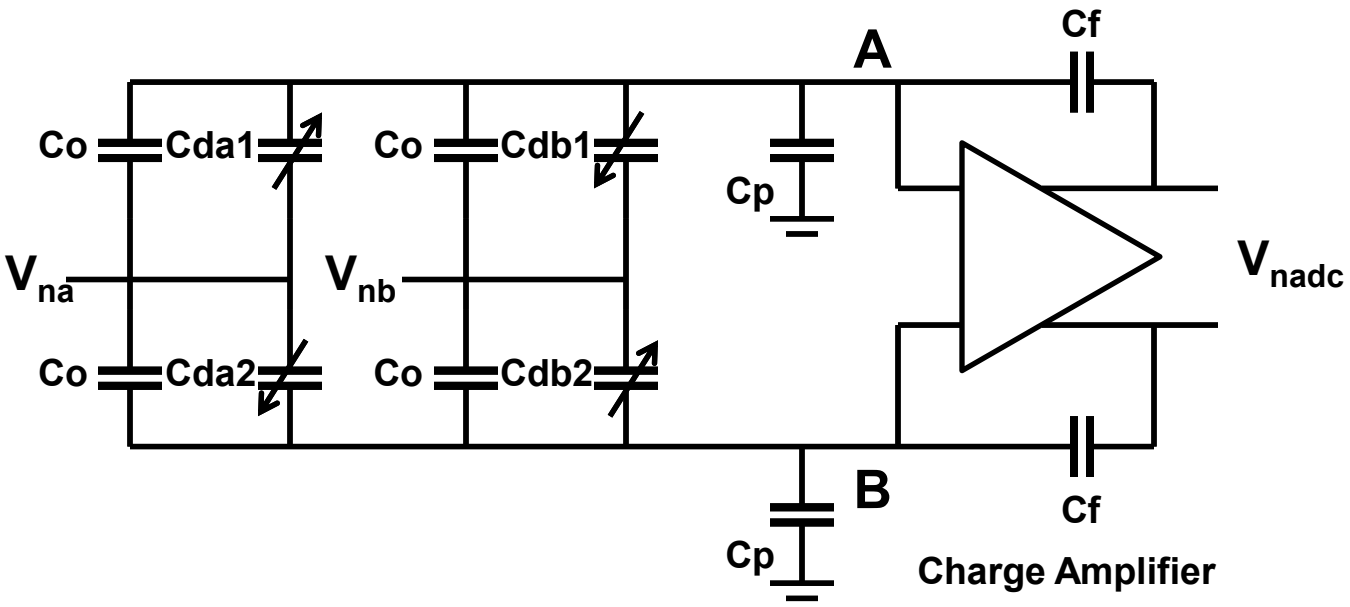
$$V_{s@ADCinput} = V_a \cdot \frac{C_{da1}}{C_f} + V_b \cdot \frac{C_{db1}}{C_f} - V_a \cdot \frac{C_{da2}}{C_f} - V_b \cdot \frac{C_{db2}}{C_f} = 2 \cdot \frac{C_d}{C_f} \cdot (V_a - V_b)$$

$$V_{s@ADCinput} = 2 \cdot \frac{SF \cdot a}{C_f} \cdot V_{bias}$$

V_{bias} is the differential Voltage applied to the sensor

$$\frac{V_{s@ADCInput}}{a} = 2 \cdot \frac{V_{bias}}{C_f} \cdot SF$$

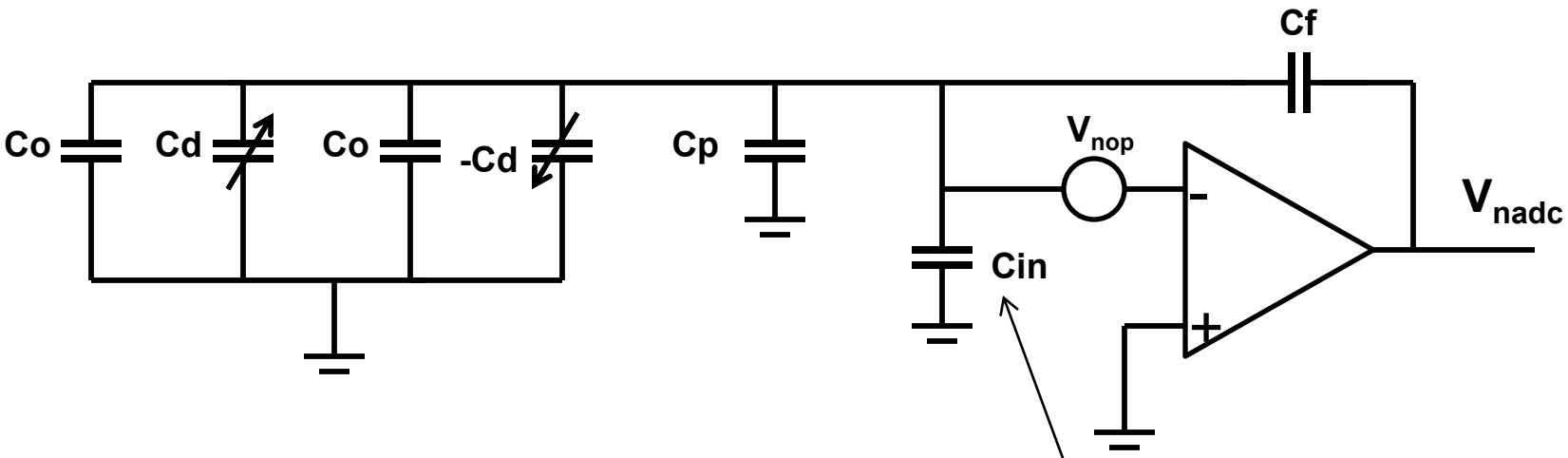
Biasing Noise Gain



$$V^2_{na@ADCinput} = V^2_{na}\left(\frac{2\,C_d}{C_f}\right)^2 + V^2_{nb}\left(\frac{2\,C_d}{C_f}\right)^2$$

$$V_{na@ADCinput} = \frac{2 \cdot C_d}{C_f}\sqrt{V^2_{na} + V^2_{nb}} = \frac{2\,SF\,a}{C_f}\cdot\sqrt{V^2_{na} + V^2_{nb}}$$

Charge Amplifier Noise Gain



$$V_{nop@ADCinput} = V_{nop}\left[1 + \frac{2 \cdot C_o + C_p + C_{in}}{C_f}\right]$$

$$NG_{ChAmp} = 1 + \frac{2 \cdot C_o + C_p + C_{in}}{C_f}$$

C_{in} ➔ Charge Amplifier Input Cap

Biasing Voltage (1)

$$\frac{V_{s@ADCInput}}{a} = 2 \cdot \frac{V_{bias}}{C_f} \cdot SF \qquad NG_{ChAmp} = 1 + \frac{2 \cdot C_o + C_p + C_{in}}{C_f}$$

$$V_{nBias@ADCInput} = \frac{2 \cdot SF \cdot a}{C_f} \cdot \sqrt{V_{na}^2 + V_{nb}^2}$$

- To maximize the ADC input ➔ two possibilities:
  - Increase the Bias Voltage
  - Decrease the ChAmp feedback cap (C_f)
    - ➔ Increase the Charge Amplifier Gain
    - C_f ↓ ➔ the (ChAmp & BiasCircuit) ADC input noise ↑
      - ➔ No effect on the overall SNR

Biasing Voltage (2)

- To optimize SNR
  - ➔ V_{bias} has to be maximized
  - ➔ The Sensor Drivers has to be realized under 5.0V Supply Domain
- Considering Supply Variation & Driver Output MOS headroom

➔ V_{bias}=4.5V

Charge Amplifier Feedback capacitor

- ➔ V_{bias}=4.5V

- The feedback cap (C_f) is evaluated to maximize ADC DR when the maximum acceleration (a_{max}) is applied to the sensor

$$V_{ADC} = 2 \cdot \frac{SF \cdot a}{C_f} \cdot V_{bias}$$

$$C_f = 2 \cdot SF \cdot a_{max} \cdot \frac{V_{bias}}{V_{ADCmax}} = 2 \cdot 300fF/G \cdot 2G \cdot \frac{4.5V}{2V} = 2.7pF$$

Biasing and Reading Noise partitioning (2)

- Read-out noise ➔ Charge Amplifier noise

$$NG_{ChAmp} = 1 + \frac{2\,C_o + C_p + C_{in}}{C_f} > 1 + \frac{2\,C_o + C_p}{C_f} = 1 + \frac{2 + 12}{2.7} = 6.2$$

  - The Charge Amplifier Input Noise is amplified

- Bias Noise Gain

$$NG_{Biasmax} = \frac{\Delta C_{max}}{C_f} = \frac{2 \times SF \times a_{max}}{C_f} = \frac{2 \times 300fF/G \times 2G}{2.7pF} = 0.44$$

  - The Bias Input Noise is amplified

Biasing and Reading Noise partitioning (3)

- Reading Noise is more critical than Biasing Noise due to Charge Amplifier Noise Gain
  - Strategy: Increasing the Reading Noise Budget compared to the Biasing Noise Budget
    - 1/2 may be the best compromise to increase the reading Noise Budget
    - 1/3 small improvement for Reading and bigger worsening for the Biasing Noise Budget

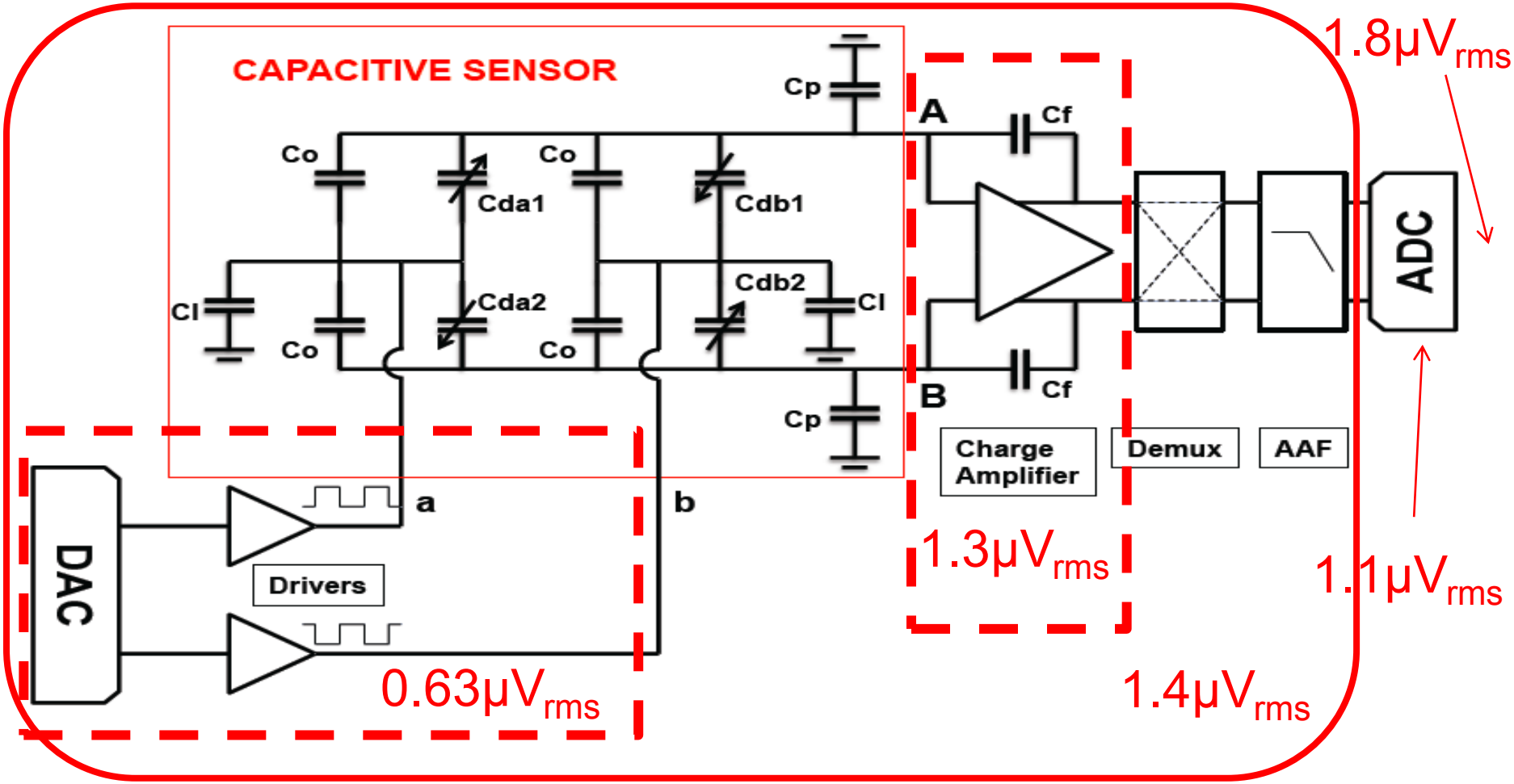
	Noise Biasing/Noise Reading				
	3/1	2/1	1/1	1/2	1/3
Noise Biasing V_{nBias}	1.35μV	1.27μV	1μV	0.63μV	0.45μV
Noise Reading V_{nRead}	0.45μV	0.63μV	1μV	1.27μV	1.35μV

$$V_{n\,Read\,@\,ADCInput} = 1.27\mu V$$

$$V_{nBias\,@\,ADCInput} = 0.63\ \mu V \quad \square \quad V_{nBias\,@\,DriverOutput} = \frac{0.63\ \mu V}{0.44} = 1.43\mu V$$

Noise Budget Partitioning

- Assuming no-noise sensor



Noise Budget Partitioning Conclusion

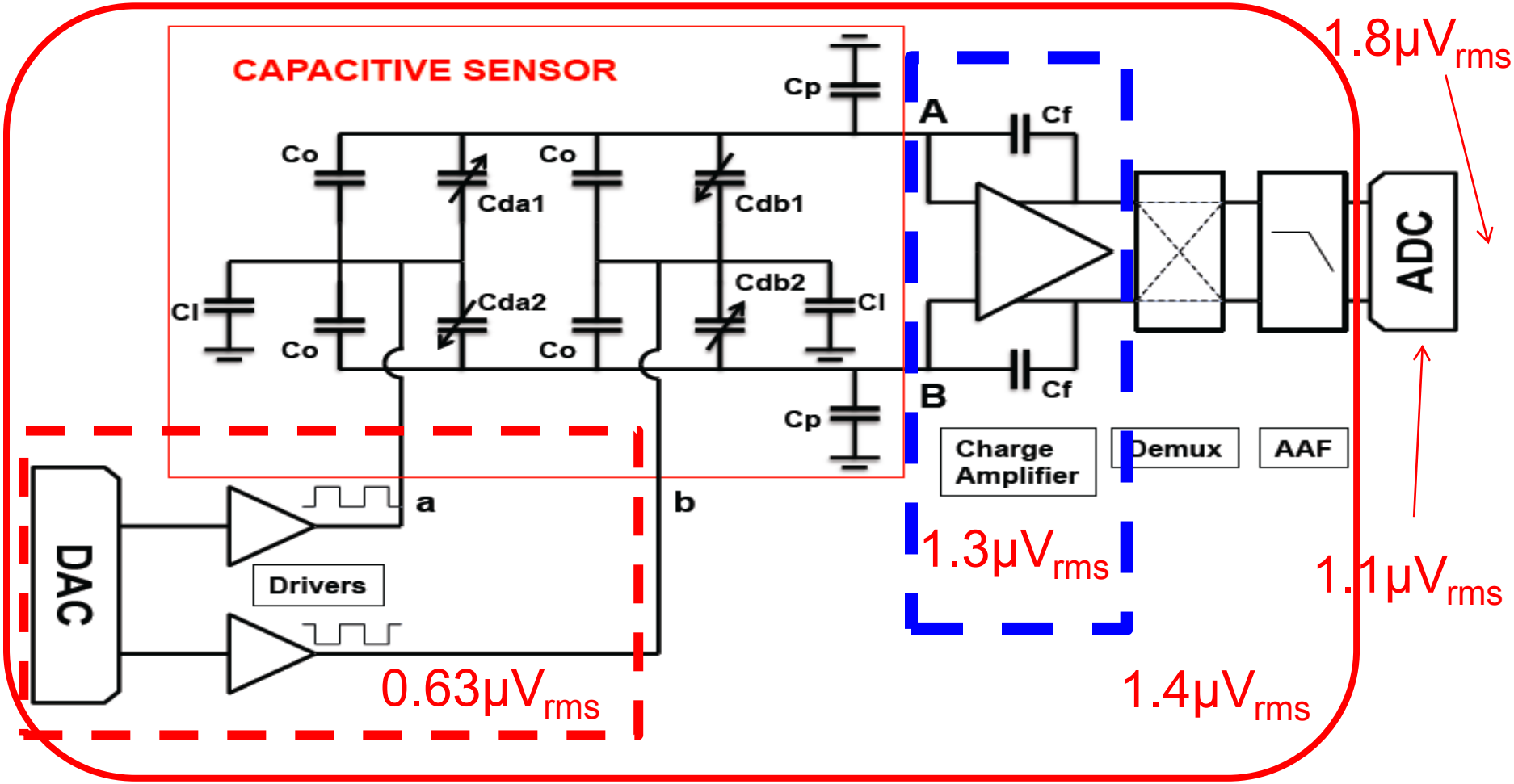
- Starting from the high level system specifications
  - ➔ a preliminary noise breakdown
- To descend the hierarchy, it is necessary to define the architecture of each block
  - ➔ Next step ➔ defining the circuits architecture and their noise budget
- It is mandatory to take into account the mod/dem effects

Architecture

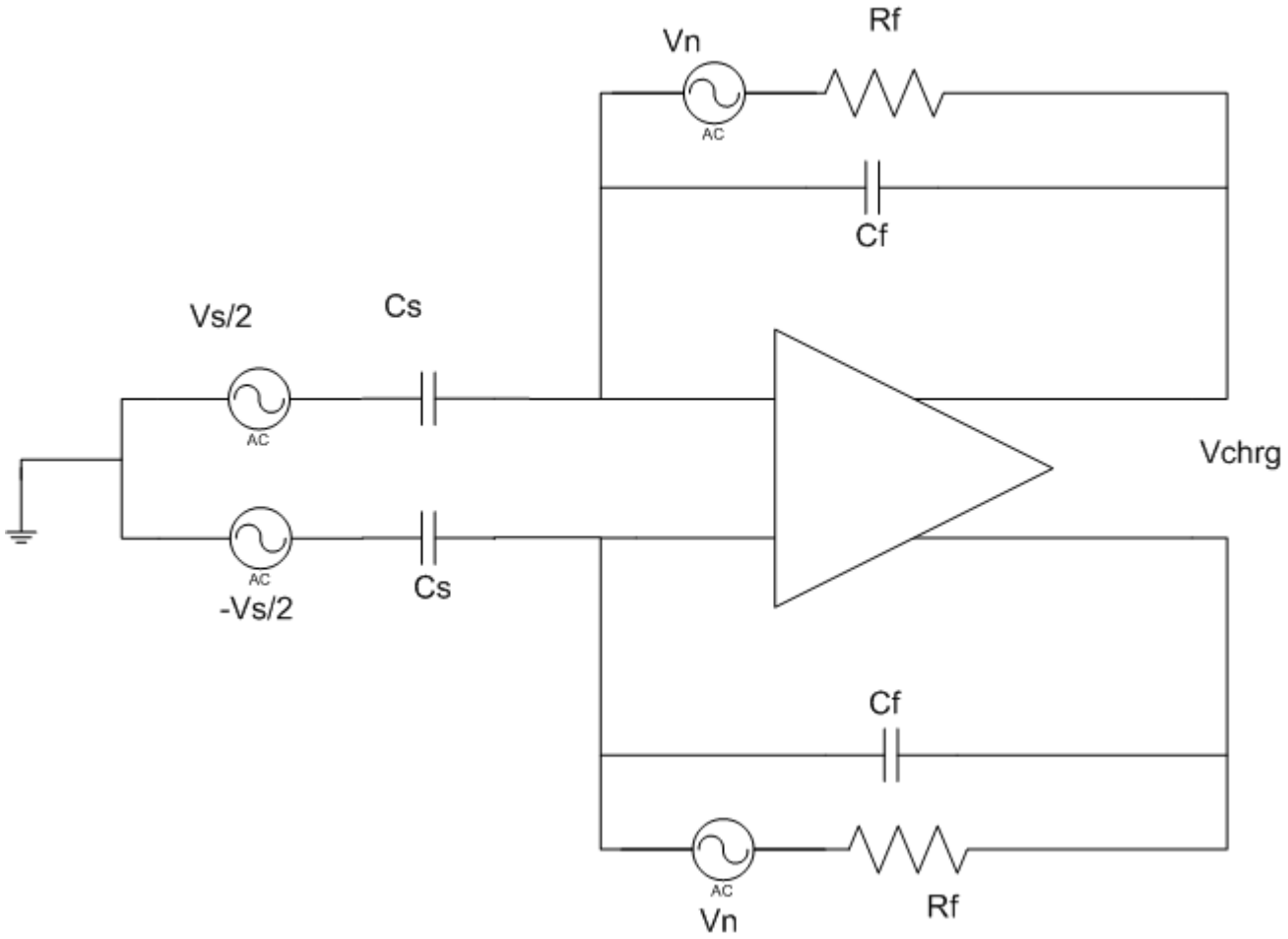
- Introduction
- Design Objectives
- Noise Budget Partitioning
- Architecture
- ADC Architecture

Charge Amplifier

- Assuming no-noise sensor



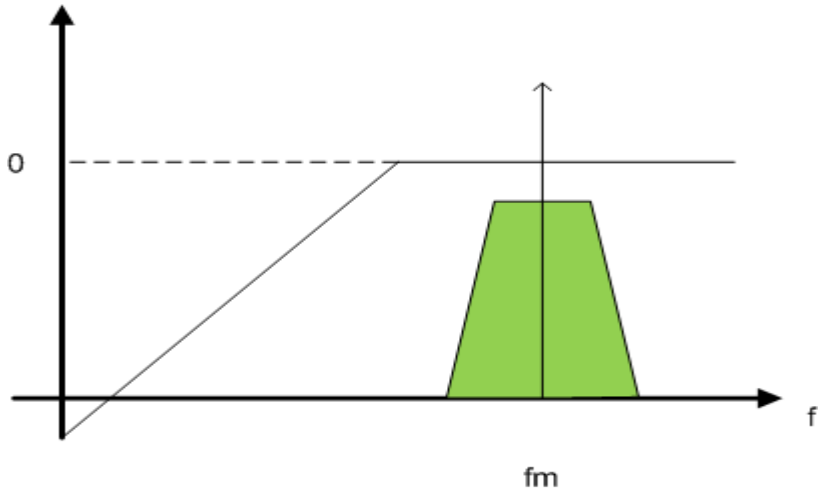
Charge Amplifier (1)

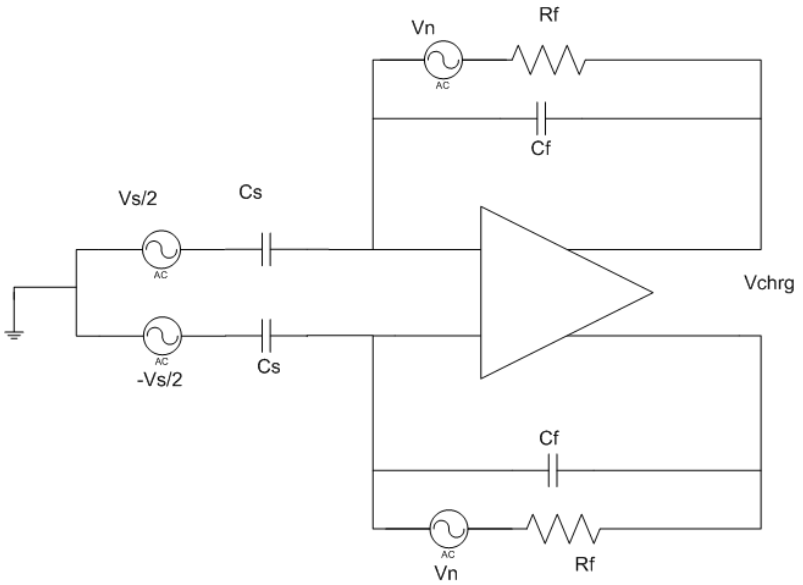


- Charge Amplifier needs a opamp input DC polarization

Charge Amplifier (2)

$$\frac{V_{ChAmp}}{V_s} = \frac{R_f \cdot C_s \cdot s}{1 + R_f \cdot C_f \cdot s}$$





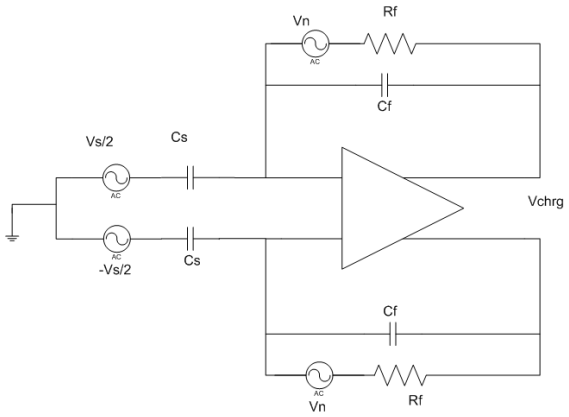
- The Charge Amplifier Signal is Amplitude Modulated
  - Carrier frequency ➔ f_m
- To reduce the Charge Amplifier gain error
  - The pole frequency has to be lower than modulation frequency

Charge Amplifier (3)

$$V_n^2 = 4 \cdot k_b \cdot T \cdot R_f$$

$$V_{nChAmp} = \frac{V_n}{1 + C_f \cdot R_f \cdot s}$$

$$V_{nChAmp\ @f=f_m} = \sqrt{\frac{2 \cdot 4 \cdot k_b \cdot T \cdot R_f}{1 + (2 \cdot \pi \cdot f_m \cdot R_f \cdot C_f)^2}} \cdot \sqrt{\frac{2 \cdot k_b \cdot T}{R_f \cdot (\pi \cdot f_m \cdot C_f)^2}}$$



- R_f ↑ ➔ Output Noise density (due to R_f) ↓

Charge Amplifier (4)

- The noise spec ➔ $V_{nRead} = 1.27\mu V$
- Assumption:
  - R_f-Noise ≈ 1/3 of the to Total Noise (negligible effect in the noise power budget)
- The ChAmp Output Noise density due to feedback resistor is:

$$\frac{1.27\mu V}{3\sqrt{300}} = 24nV / \sqrt{Hz}$$

- Assumption: Modulation frequency f_m=100kHz

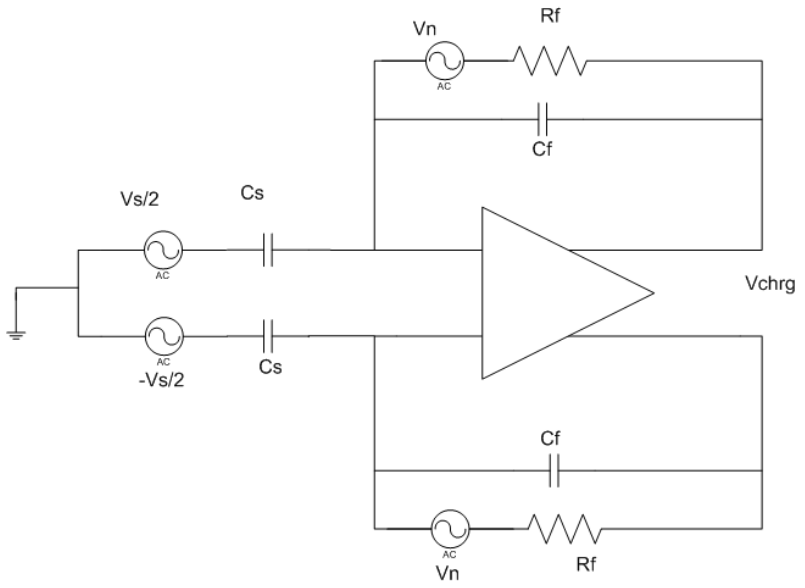
$$R_f = \frac{2 k_b T}{V_{n\_ChAmp@f=f_m}^2 (\pi f_m C_f)^2} = 20M\Omega$$

$$f_{pole} = \frac{1}{2\pi R_f C_f} = 3kHz << f_m$$

Charge Amplifier (5)

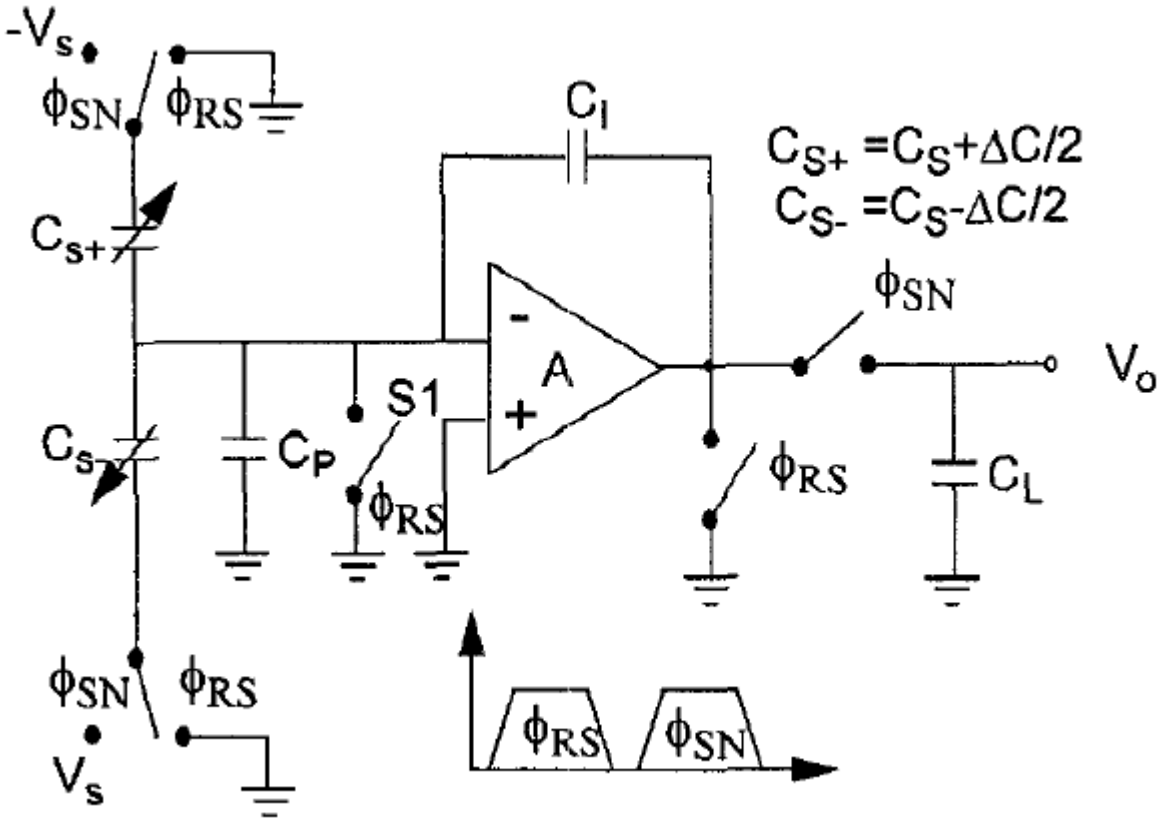
- Large R_f's
  - are difficult to be integrated in standard CMOS process
  - require large Area

  - Switched Capacitor
  - MOS operating in triode
  - Integrated Resistor



Charge Amplifier (6)

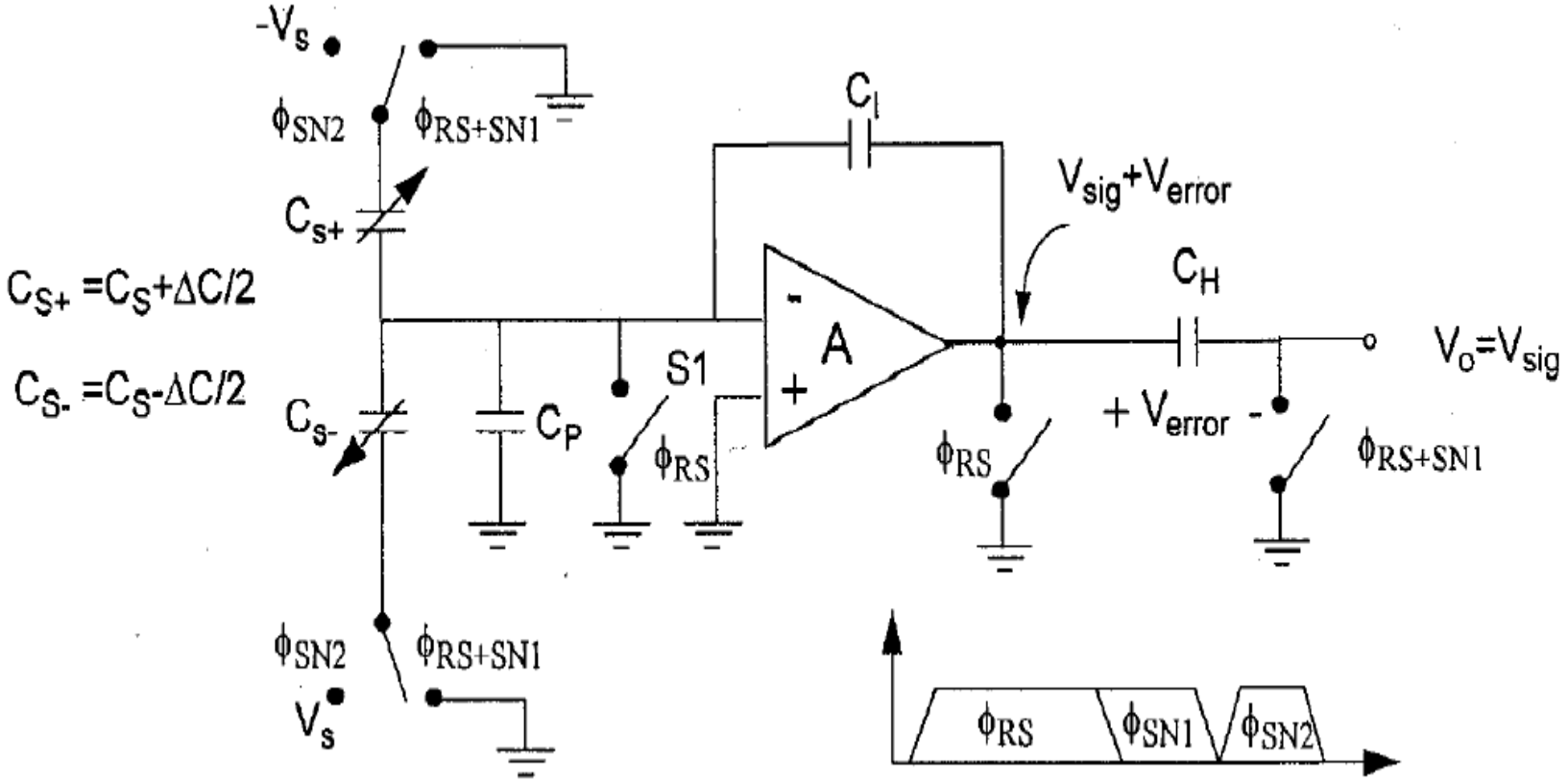
- Switched Capacitor capacitance sensing



"Correlated Double Sampling in Capacitive Position Sensing Circuits for Micromachined Applications" Wongkomet, N.; Boser, B.E.;1998

Charge Amplifier (7)

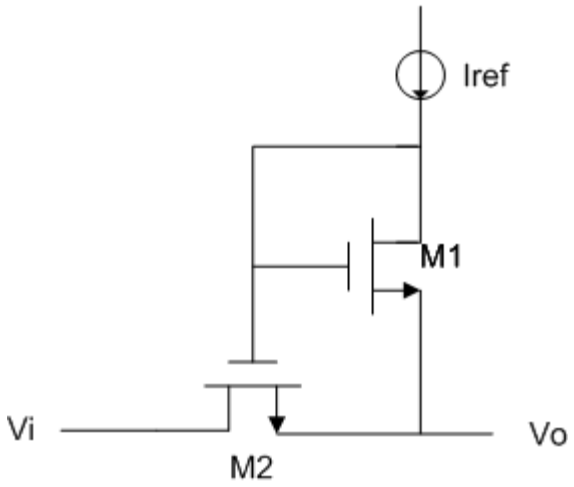
- Switched Capacitor capacitance sensing with CDS



"Correlated Double Sampling in Capacitive Position Sensing Circuits for Micromachined Applications" Wongkomet, N.; Boser, B.E.;1998

Charge Amplifier (8)

- MOS operating in Triode region



$$R = \frac{(W/L)_1}{(W/L)_2} \cdot N \cdot R_{ref}$$

"Single-Chip Surface Micromachined Integrated Gyroscope with 50°/h Allan Deviation"
J.A. green, S. J. Sherman, J.F. Chang and S.R. Lewis - 2002

- Good operation with small (V_o-V_i) to keep M2 in triode
  - ➔ Same ChAmp Input and Output
  - ➔ This solution is mainly used when a pre-Amplifier is inserted after the Charge Amplifier

Charge Amplifier (9)

- Integrated Resistor
  - ☺ No Noise Folding
  - ☺ Better Linearity/No dynamic limitation
  - ☺ Better Noise Performance
  - ☹ Huge Area increments
- Roughly Area Estimation
  - **Doped Poly Typical** Rs(Ω/sq)=300 ➔ area for 2x 20MΩ & W=1µm

$$A = \frac{2 \square 20M\Omega}{300} = 0.13mm^2$$

  - **HIPO** Rs(Ω/sq)=1000 ➔ area for 2x 20MΩ & W=1µm

$$A = \frac{2 \square 20M\Omega}{1000} = 0.04mm^2$$

Charge Amplifier (10)

- Diffused Resistor have Rs higher or equal to HIPO resistor
  - ☺ Standard process (no extra mask)
  - ☹ Linearity Issue
  - ☹ Junction Leakage at the high Impedance Input of the Charge Amplifier

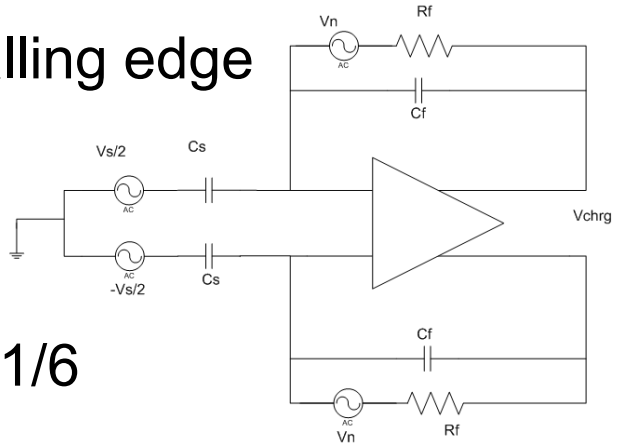
Charge Amplifier (11)

- The choice between **HIPO** and doped Poly depends on cost evaluation (mask/process vs. area)

- The real area used for the feedback resistor is higher than first roughly estimation
  - Distance between modules
  - Active area density

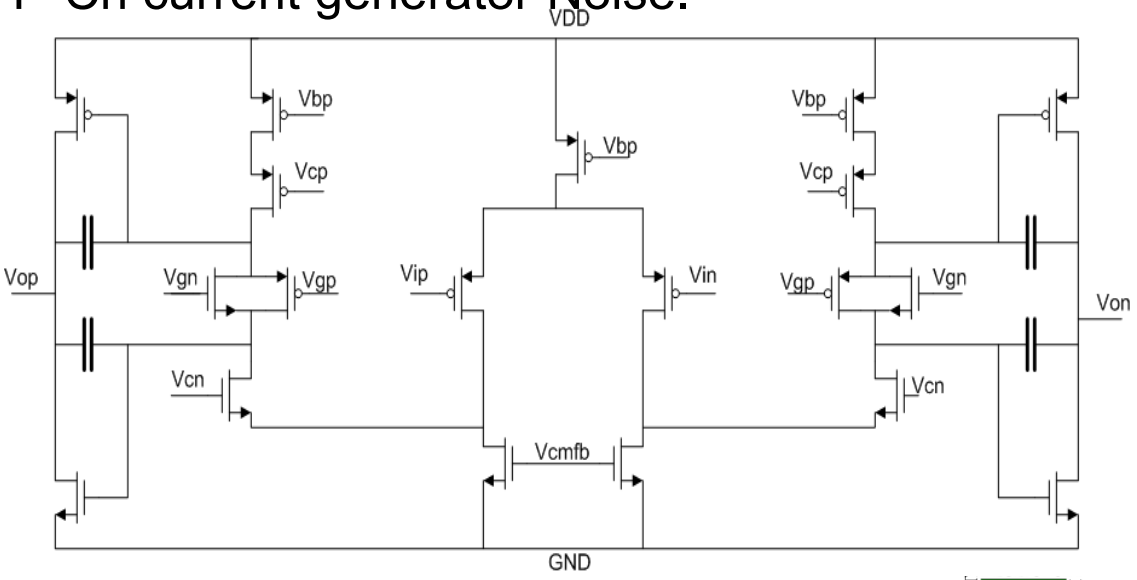
Charge Amplifier (12)

- ChAmp opamp
  - Output swing & Anti-Alias Filter Resistive Load
    - ➔ Two-Stage topology
  - High current during the carrier rising/falling edge
    - ➔ Class-AB output stage
  - Overall gain error reduction
    - ➔ Closed-Loop gain-gandwidth > 10x f_m
  - ChAmp feedback factor ≈ $1/NG_{ChAmp} = 1/6$
  - Opamp noise is chopped
    - ➔ Thermal noise dominates
    - ➔ Thermal noise reduction
      - Large differential pairs and current generator MOS
        - ➔ high parasitic capacitor
        - ➔ stability Issue



Charge Amplifier (13)

- Usually LN ➔ PMOS input differential pair (PMOS have lower 1/f noise than NMOS)
- Recent technologies have small difference between P-Ch and N-Ch flicker noise ➔ Op-Amp with N-Ch differential pair can achieve better Noise performance
- The advantages of N-Ch differential pairs:
  - Higher g_m ➔ Lower thermal noise
  - Higher rejection of the P-Ch current generator Noise.
- Opamp noise is choppered



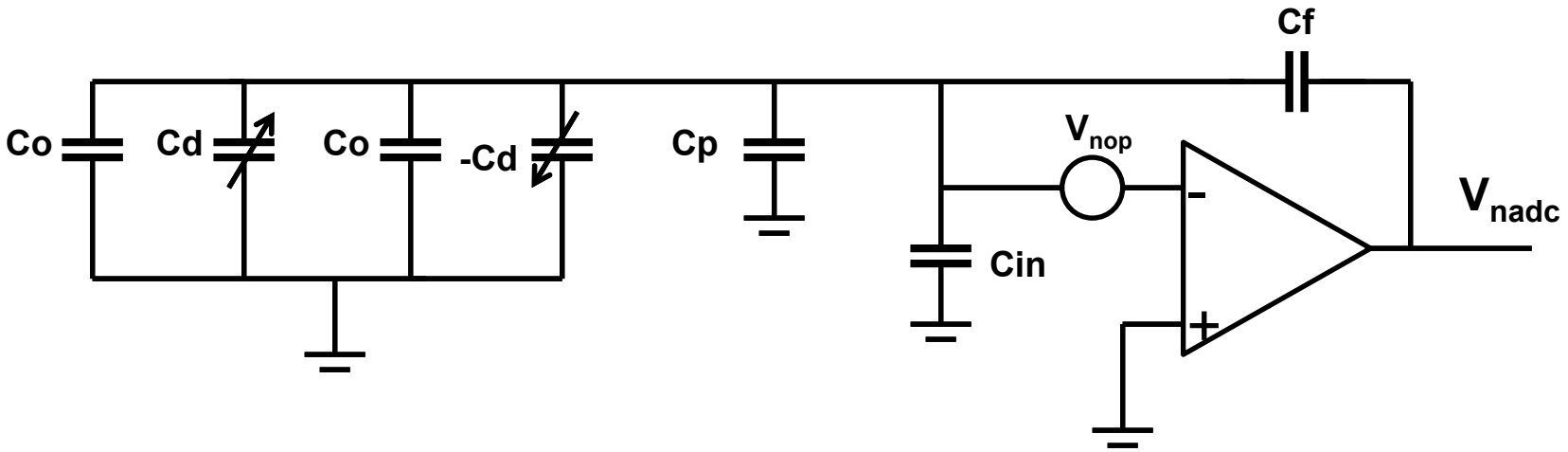
Charge Amplifier (14)

- Low Noise circuits design
  - large transistor
    - ➔ large channel width and MOS area
    - ➔ thermal and 1/f noise reduction
- In case of capacitive sensing

$$NG_{ChAmp} = 1 + \frac{2 \cdot C_o + C_p + C_{in}}{C_f}$$

  - Large Transistor
    - ➔ Large gate capacitance
      - Increased Charge Amplifier Noise Gain

Charge Amplifier (15)



- For dominant thermal noise (chopper)
- Minimum noise for $C_{in} \leq C_{sensor} + C_{interconnect}$

$$NG_{ChAmp} = 1 + \frac{2 \cdot C_o + C_p}{C_f} = 6.2$$

$$\frac{V_{nRead@ADCInput}}{NG_{ChAmp} \cdot \sqrt{BW}} = \frac{1.27\mu V}{6.2 \cdot \sqrt{300Hz}} \cdot 11nV / \sqrt{Hz}$$

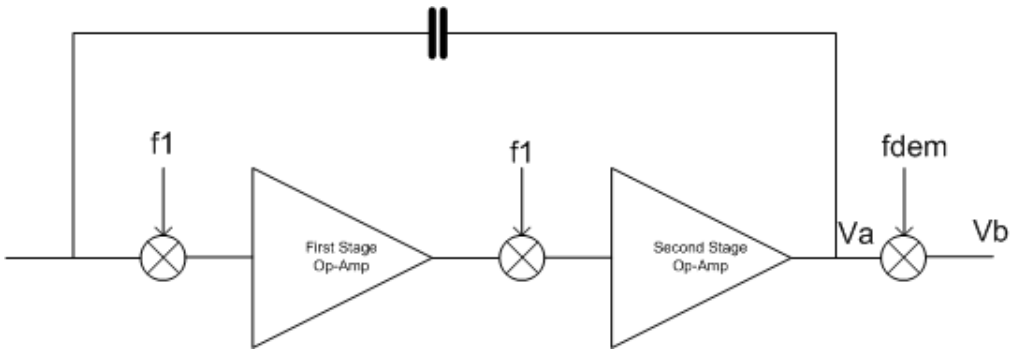
Charge Amplifier (16)

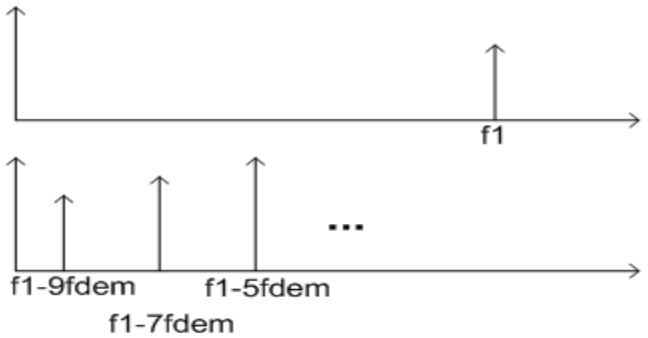
- This rough result is useful only to understand the challenge of the Charge Amplifier opamp design
  - ➔ 11nV/√Hz is an aggressive input noise target

- To reduce the noise
  - Sol1 ➔ mod/dem frequency (f_m) increase
    - ➔ f_m > opamp flicker corner frequency
    - ➔ higher power consumption (the Mod/Dem frequency effects all the circuits specifications)
    - Complexity in circuits Implementation
  - Sol2 ➔ chopper opamp

Charge Amplifier (17)

- The opamp 1/f noise is modulated by the Choppered square wave at frequency f_1 (Odd harmonics)
- The opamp modulated output signal is down converted by the demodulation clock (f_{dem})
- F_1 defined avoid that its odd harmonics are down converted in base band by the demodulation square wave
- Ex.: f_1=1000kHz & f_{dem}=100kHz

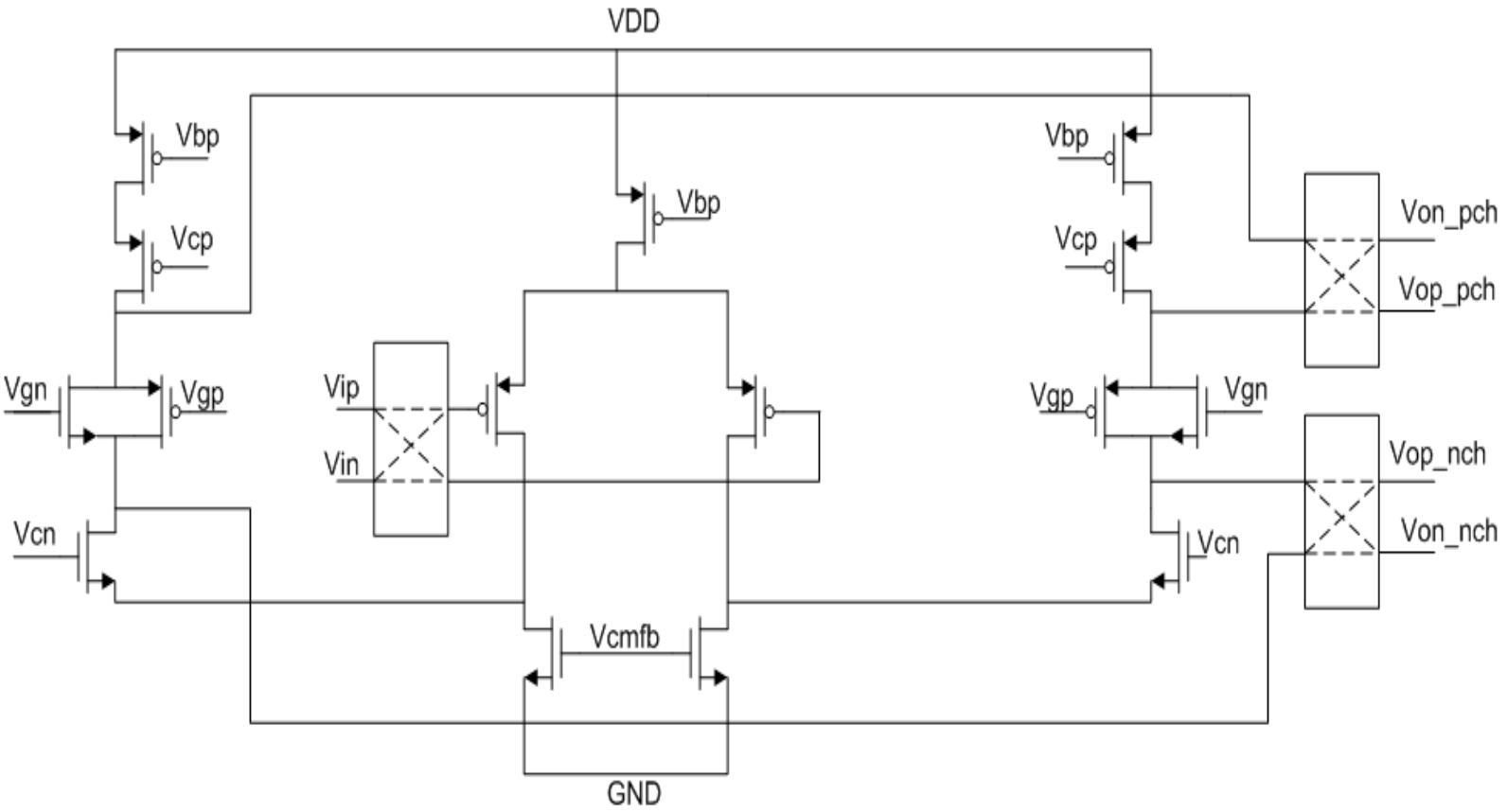




$X_{2k+1}=(4*V0)/(pi*(2k+1))$

Charge Amplifier (18)

First Stage of the Chopper Charge Amplifier Op-Amp



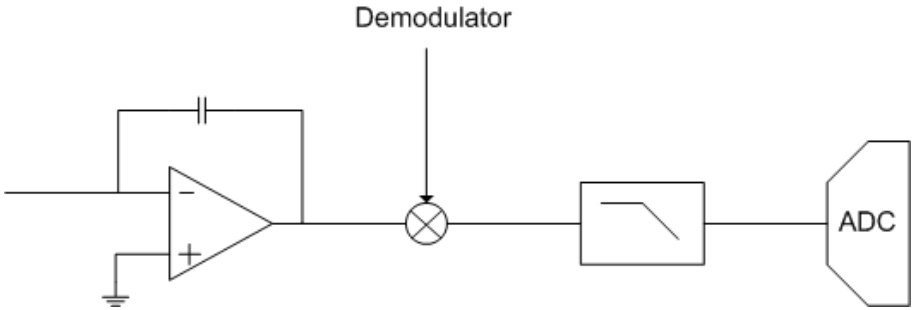
Charge Amplifier (19)

- Both solutions (Choppered and CT) have been designed and compared.
- CT solution performs the best results with the in term of:
  - Power consumption
  - Performances
  - Linearity
  - Development time

- Op-Amp specification:
  - GBW ≈ 10MHz
  - Input referred Noise ≈ 11nV/√Hz
  - Current Consumption ≈ 2.2mA ➔ 7.3mW@3.3V

Anti-Alias Filter (1)

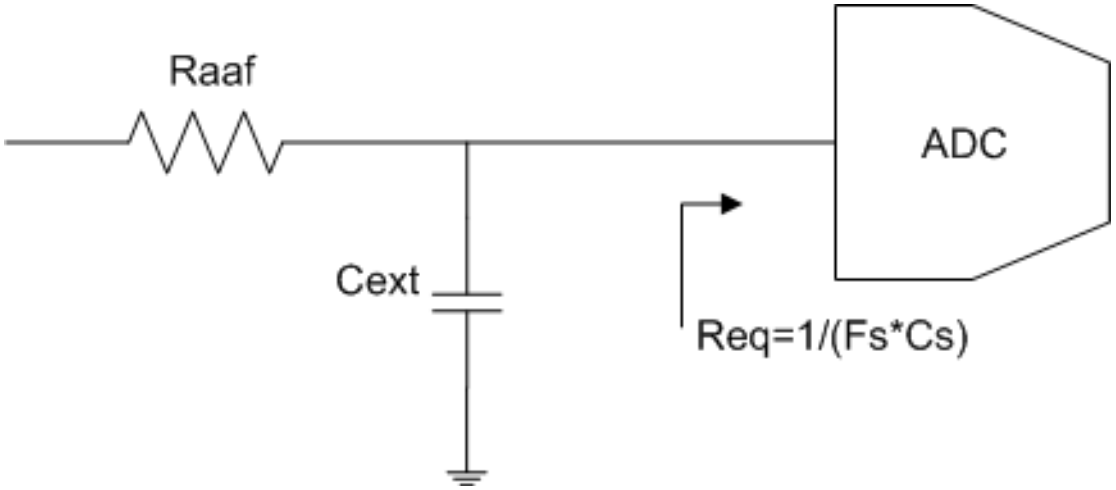
- Large ADC Over Sampling Ratio
  - ➔ One single pole Filter is enough to reduce the folding noise issue
- The Reading Block Noise budget is mainly used by the Charge Amplifier (High Complexity).
- If active solution is implemented the AAF Op-Amp needs Chopper Stabilization technique in order to remove the flicker Noise



- Passive Filter with external capacitor solution is widely used in very high performance standalone ADC.

Anti-Alias Filter (2)

- The value of the AAF resistor is designed in order to have an attenuation of 0.4dB between the Dem. output and the ADC Input



F_s=6MHz, C_s=10pF ➔ R_{eq}=17MΩ

R_{aaf}=800Ω

Anti-Alias Filter (3)

- The AAF noise voltage:

$$v_{n_{R_{aaf}}} = \sqrt{4 \cdot k_b \cdot T \cdot R_{aaf} \cdot BW} = 65nV$$

Negligible

C_{ext}=20nF >> C_s

Cut-Off frequency: 10kHz < Modulation frequency

Attenuation at the ADC sampling frequency: -56dB

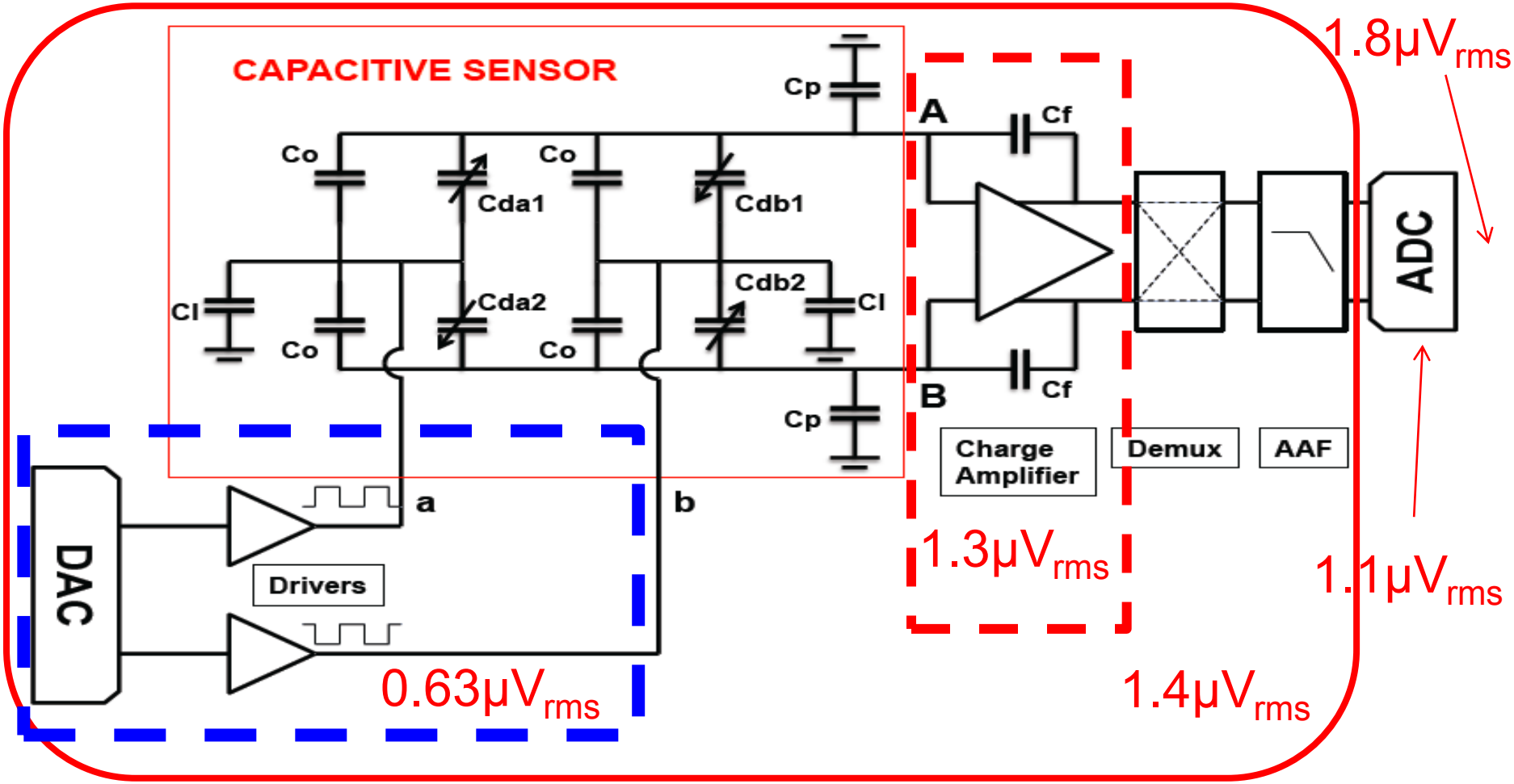
Anti-Alias Filter (4)

Passive Anti-Alias Filter solution

- ☺ Simple
- ☺ Less Risk compared with Active solution
- ☺ Noiseless
- ☺ No power consumption
- ☹ Requires external capacitors
- ☹ Gain Error

Bias Circuit

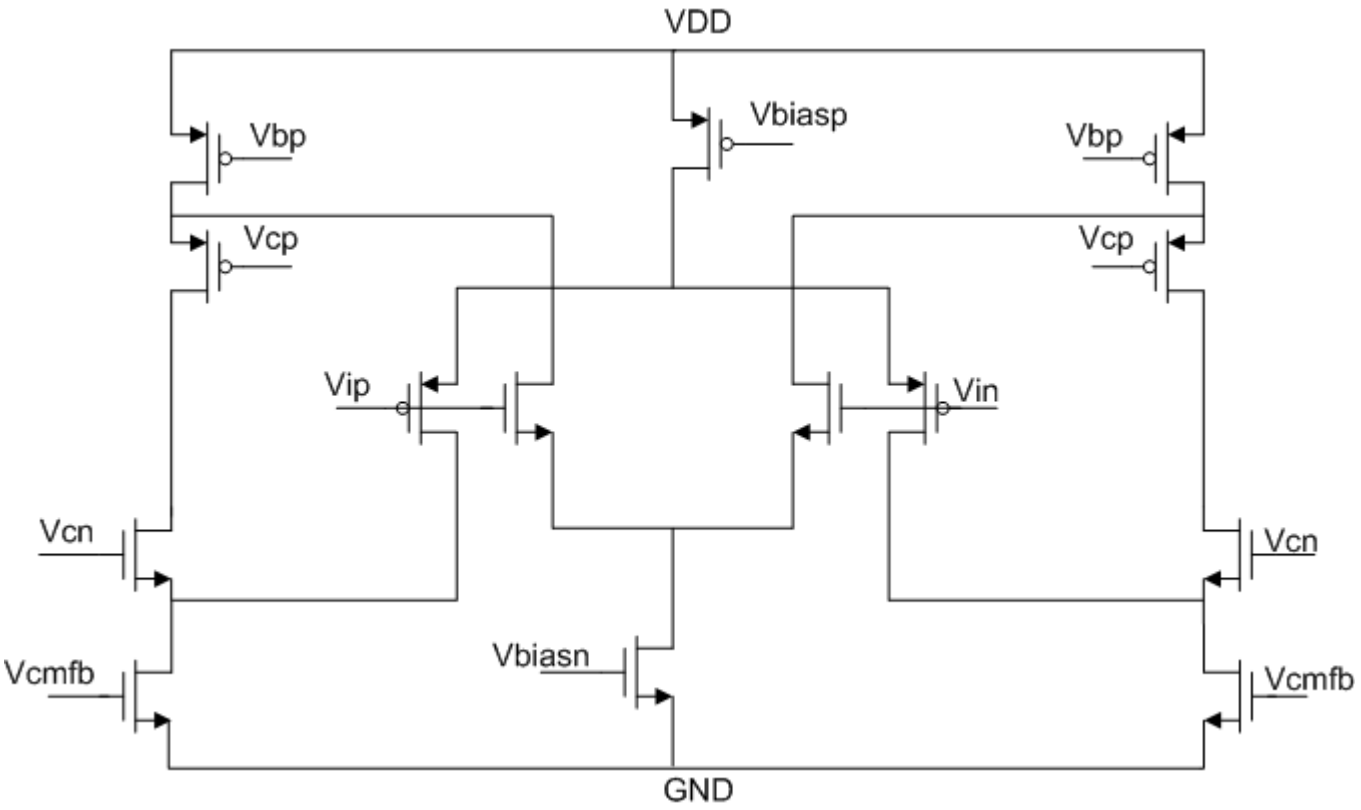
- Assuming no-noise sensor



Bias Circuits

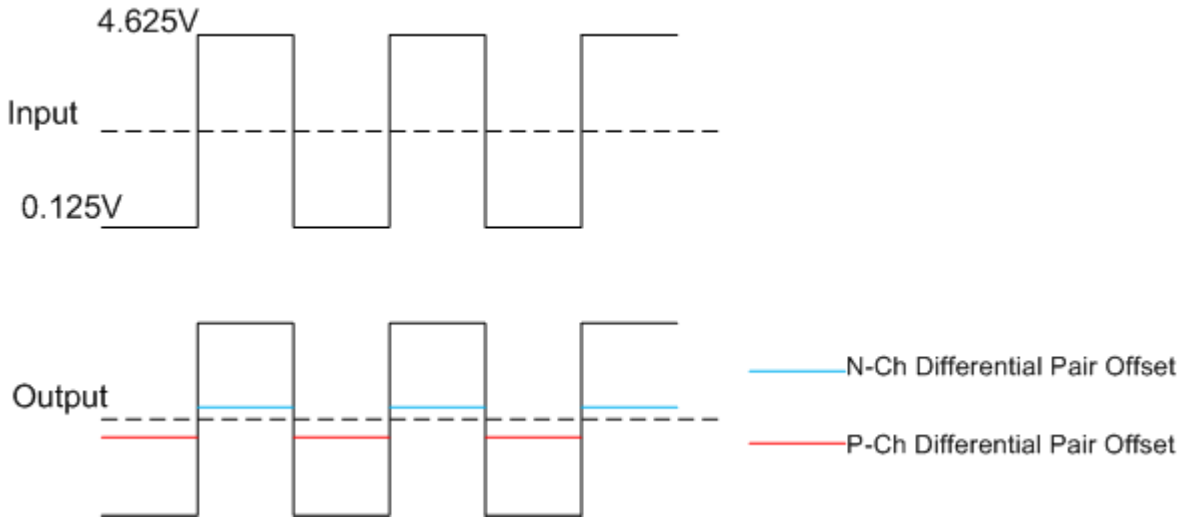
- Low Power/Low Noise Application ➔ Reduce no. of circuits
- The Biasing circuit is divided in two blocks
  - DAC that is used to set the amplitude of the Carrier
  - Driver feeds the Sensor and Buffer the DAC output
    - High Impedance input Driver
- Two possible Implementations:
  - DAC dynamic Range 4.5V
    - Driver ➔ Buffer
      - ☹ Rail-to-Rail Input Stage Op-Amp
  - DAC dynamic Range 2.5V (as ADC)
    - Driver ➔ Non-Inverter gain configuration
      - ☹ The DAC and Driver Input Noises are amplified

Bias circuit / Rail-to-Rail Input Stage (1)



Bias circuit / Rail-to-Rail Input Stage (2)

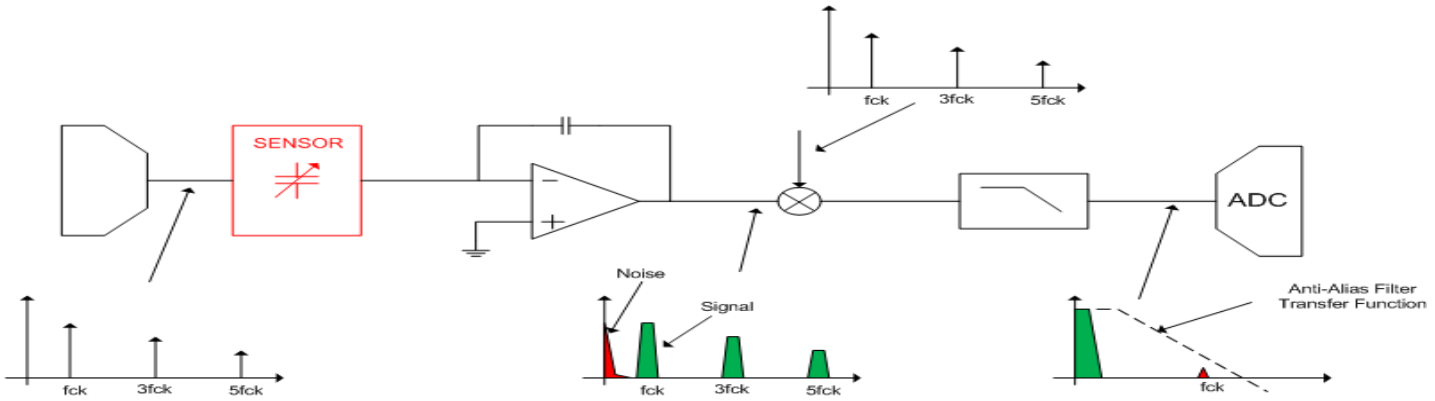
- Rail-to-Rail Input stage critical point ➔ distortion due to different offset of the P-ch and N-ch diff-pairs



- A squared wave is added to the carrier, its amplitude is equal to the difference between the N-ch and P-Ch differential pairs Offset.
- The carrier amplitude is effected by Offset Issue and it depends on DAC setting ➔ equivalent to an INL issue

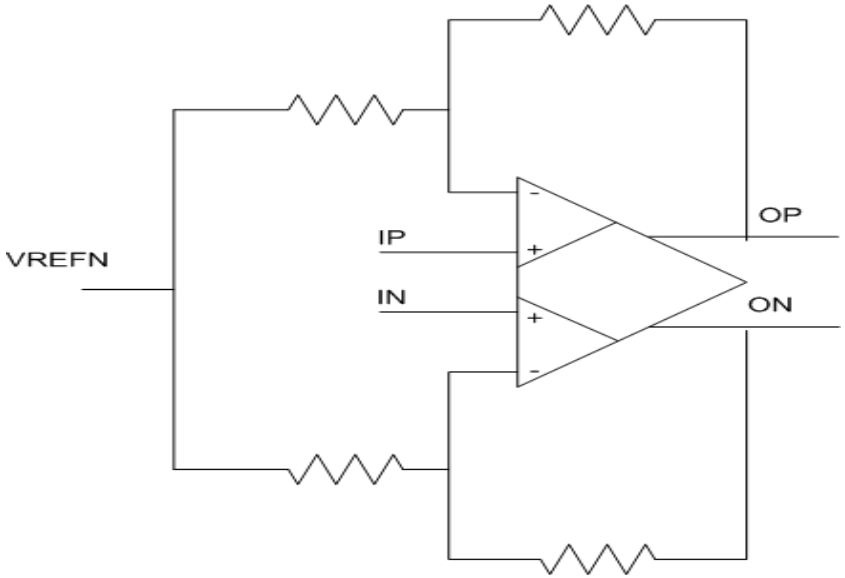
Bias circuit / Rail-to-Rail Input Stage (3)

- INL problem reduced increasing the MOS sizes to be < DAC INL
- Additional problem ➔ the diff-pair differential Flicker Noise is modulated
  - The power of the modulated Flicker Noise is equal to the sum of P-Ch and N-Ch differential pairs Flicker Noise power
  - The Driver Modulated Flicker Noise is demodulated in base band by the Demodulator and so it appears at ADC output



Bias circuit / Non Inverting Amplifier (1)

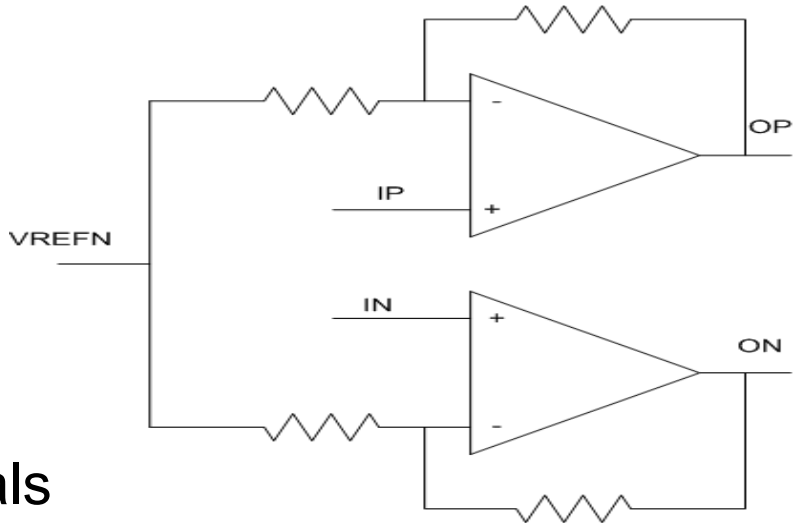
Fully Differential Difference Amplifier



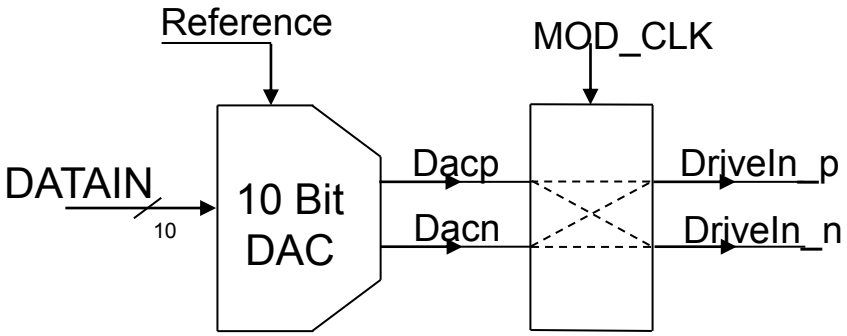
- ☺ No extra Pole due to current generator
- ☺ Good CMRR
- ☹ More design Complexity
- ☹ Needs Common Mode Feedback Circuit

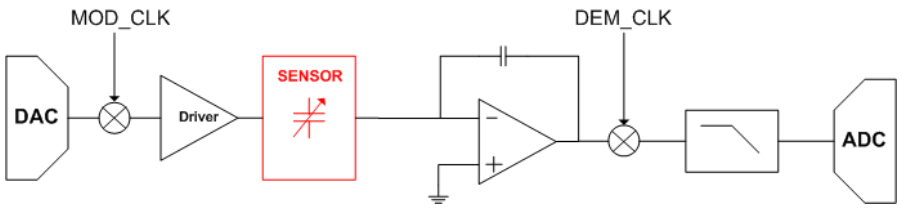
Bias circuit / Non-Inverting Amplifier (2)

- Single Ended opamp
  - ☺ Simple Architecture
  - ☺ Less power (No CMFB)
  - ☹ Extra pole due to differential to Single-Ended MOS diode
  - ☹ No Common Mode Rejection (the Common Mode and Differential signals are Amplified)

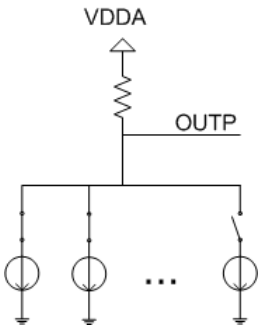


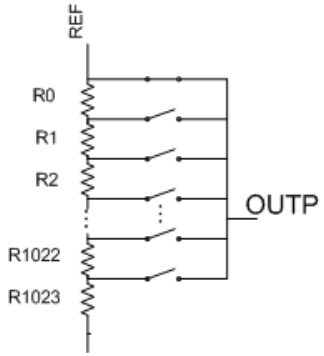
Bias circuit / DAC Architecture





- Differential DAC inserted before the Modulator
  - ☺ Static DAC.
  - ☹ DAC noise is not Choppered (Inserted before Modulator).
- Two possible topologies:
  - Current Steering
  - Resistive DAC Array (Poly Resistor)





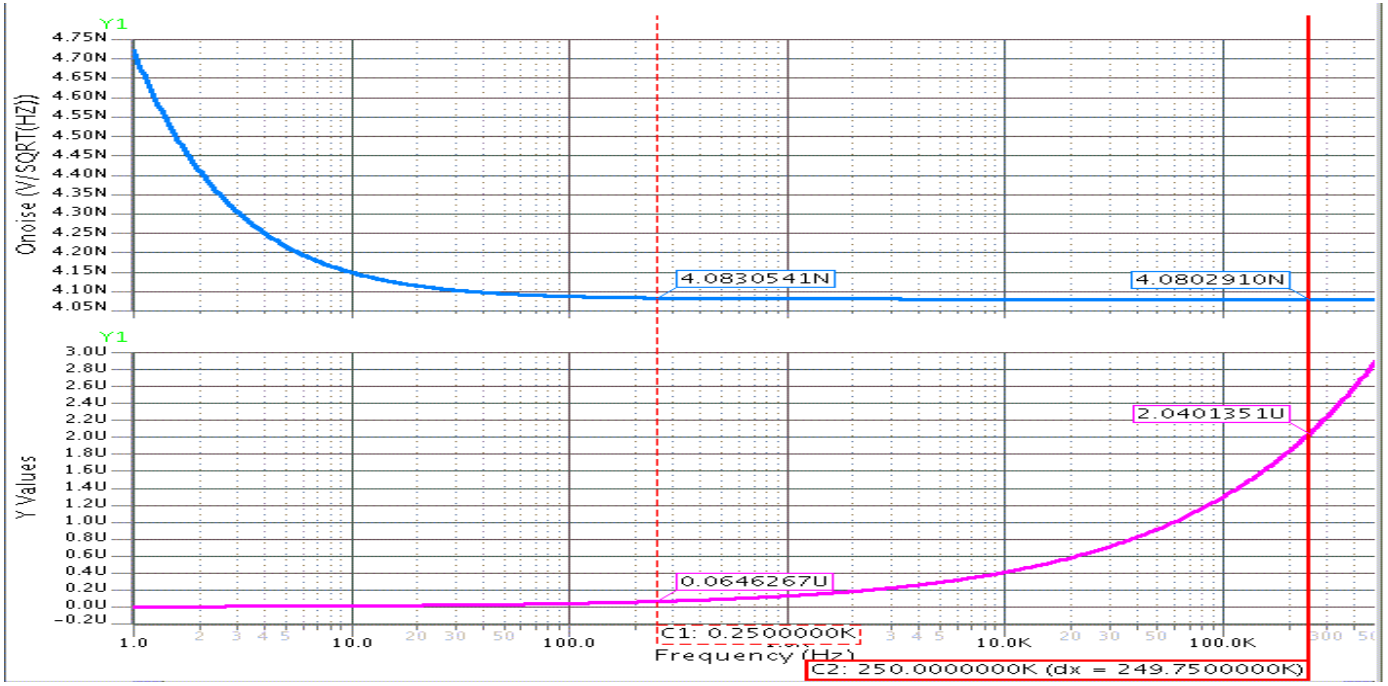
- Poly Resistor Flicker Noise is lower than MOS flicker Noise

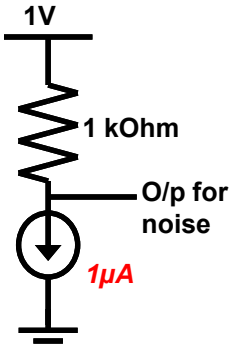
Rp1pp (p+poly res) Flicker/Thermal Noise evaluation (1)

- Flicker noise (pink noise) is present in polysilicon resistor with thermal noise.
  - It depends on ***bias voltage***, ***area*** and ***frequency*** as shown below:

  $Vn^2 \propto V_{bias}^2 / (W.L.f)$ ➔ flicker noise increases as bias voltage increases
- Ideal thermal noise for 1kΩ ➔ $\sqrt{[4*1.38e\text{-}23 \cdot 300 \cdot 10^3]} = 4.07nV/\sqrt{Hz}$

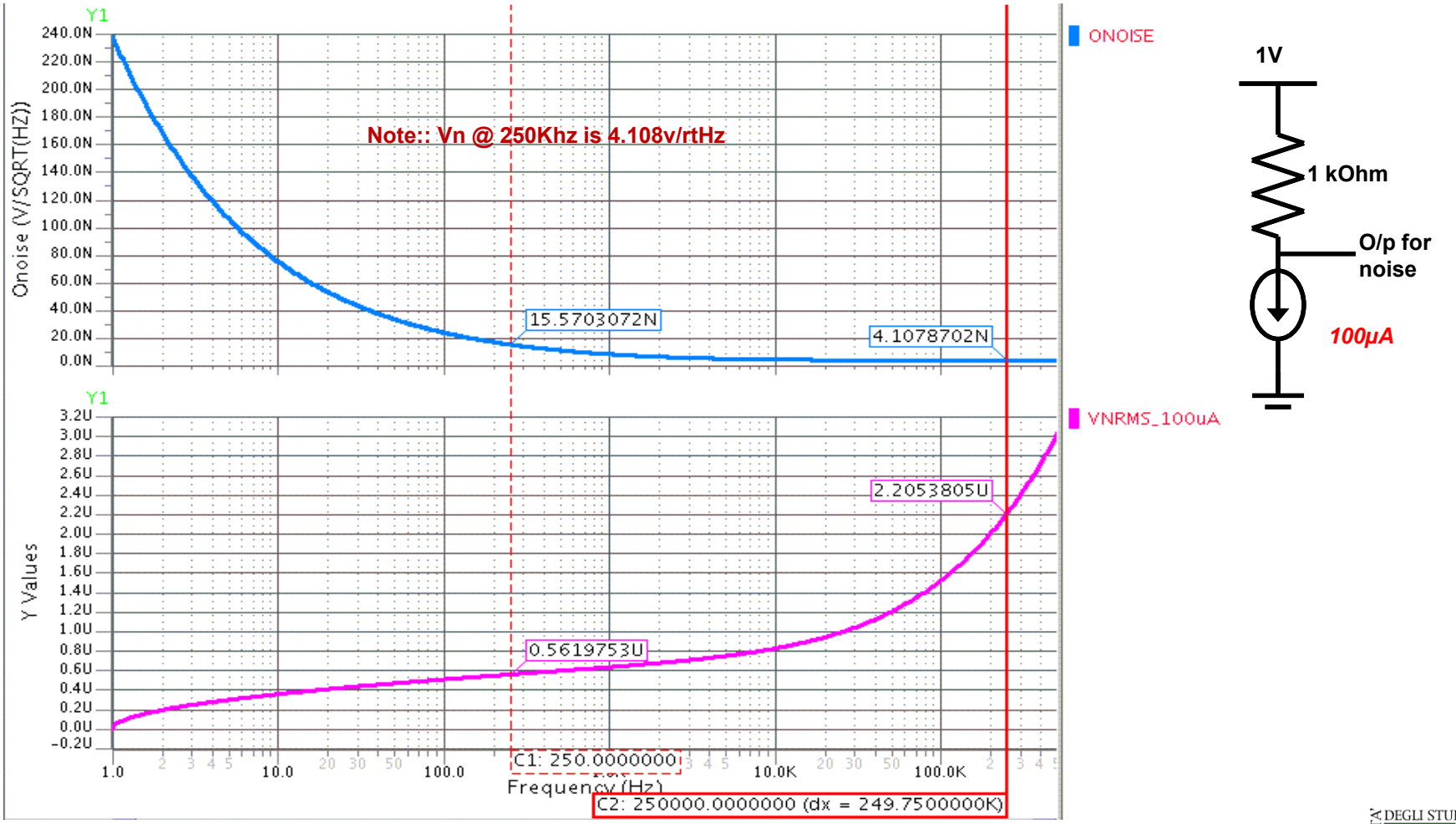
- Total noise simulation graph of 1kΩ, Rp1pp resistor with 1uA (➔ ΔV = 1mv)





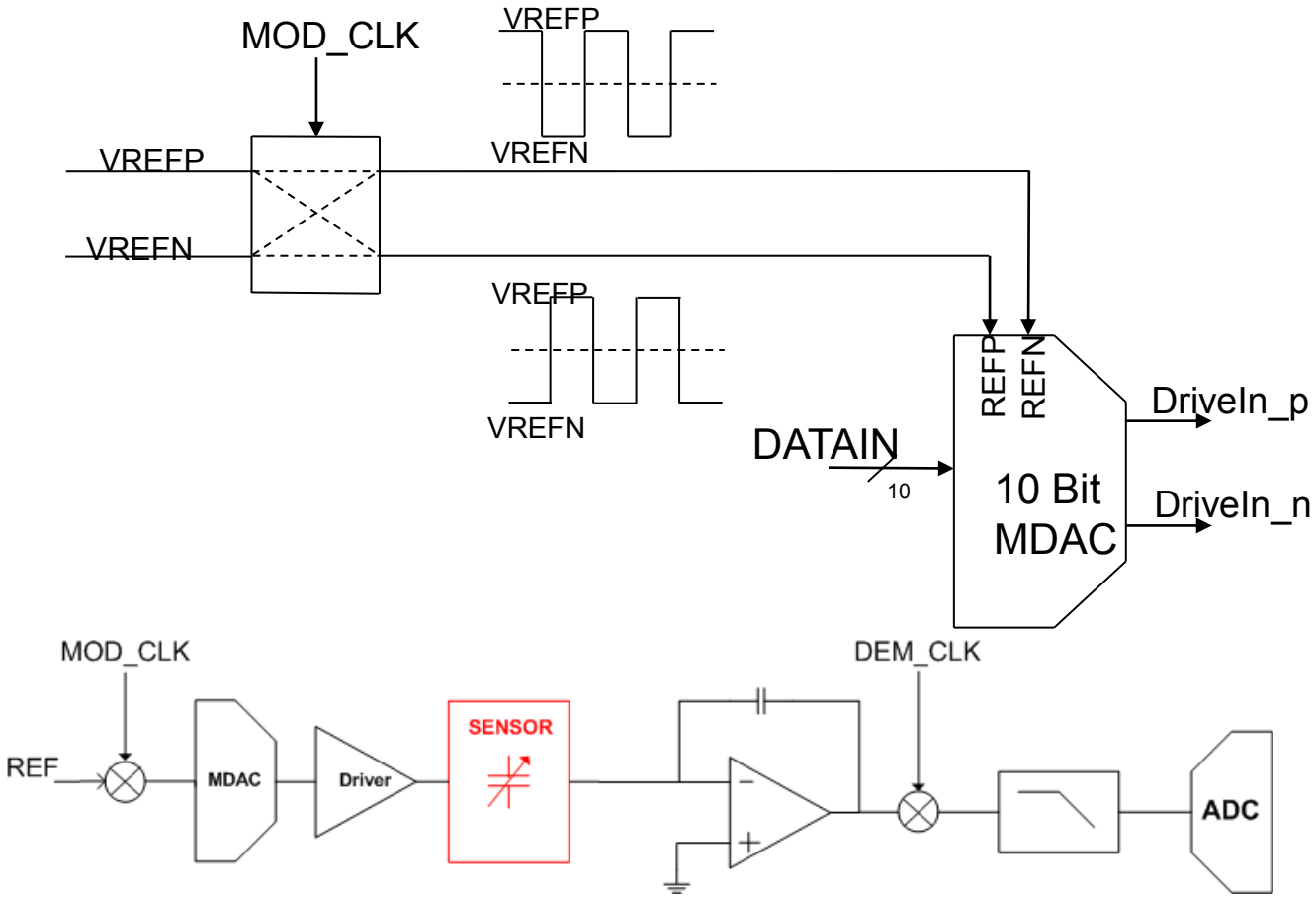
Rp1pp (p+poly res) Flicker/Thermal Noise evaluation (2)

- Total noise simulation of 1kΩ, Rp1pp resistor with 100uA (➔ ΔV=0.1V)



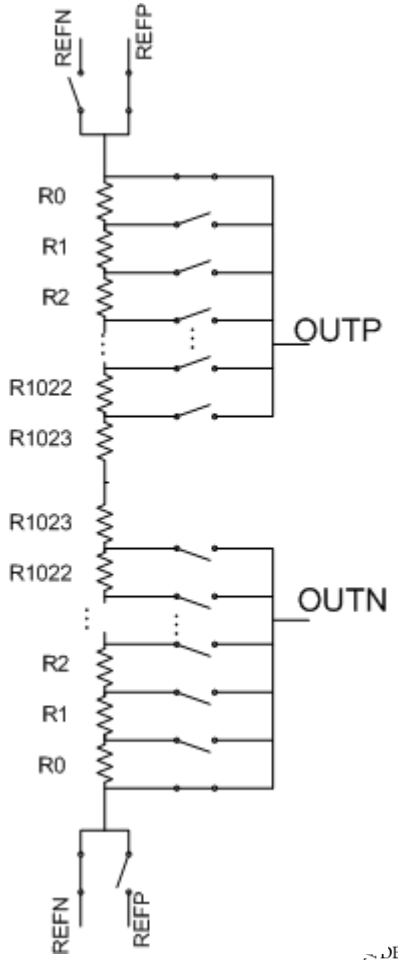
MDAC Architecture

- DAC Flicker Noise Reduction
  - ☹ Increase the dimension of the Resistor (Huge Impact on device area)
  - ☺ Move the Modulation before the DAC ➔ MDAC Architecture



MDAC topology (1)

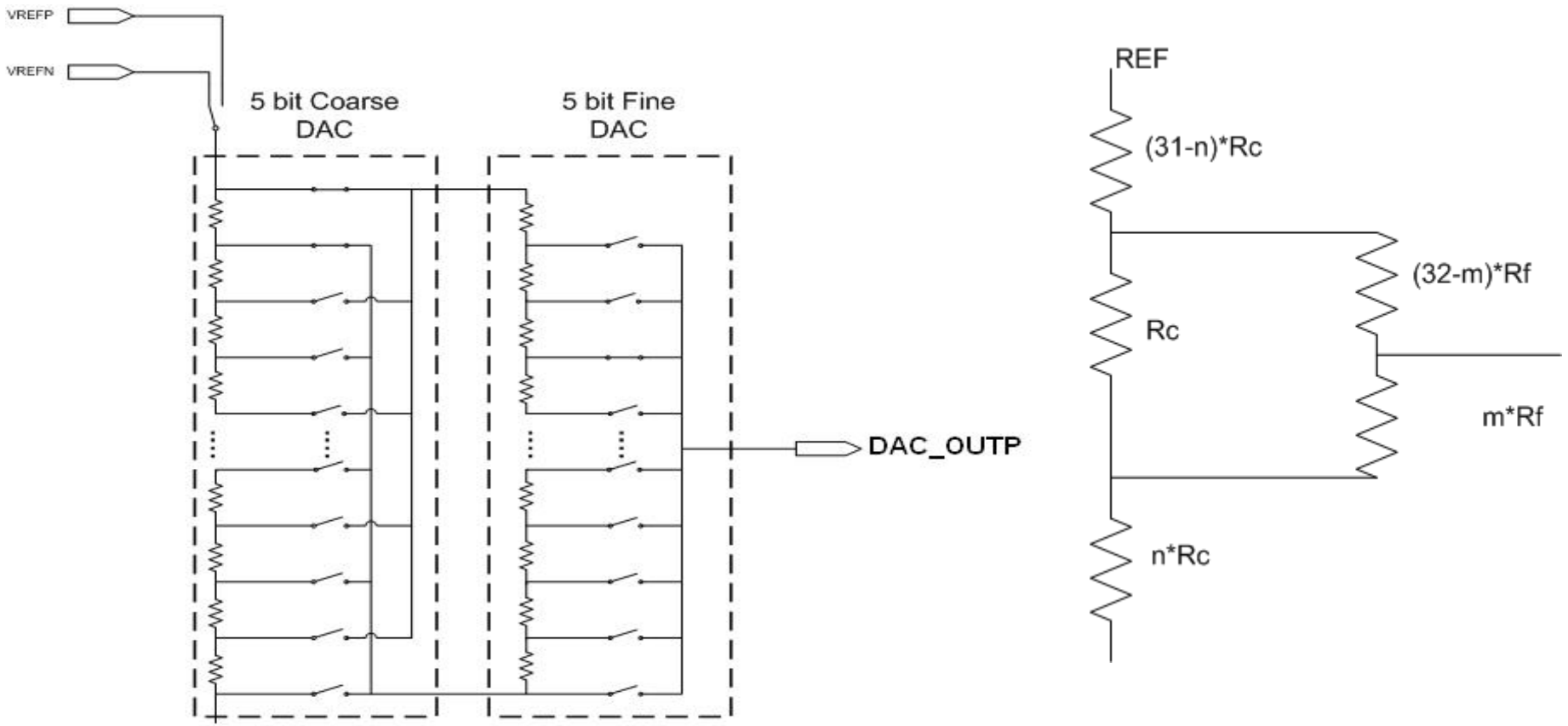
- 10 Bit Differential MDAC Single Resistor String solution:
  - 2*1024 resistors
  - 2*1024 switches



- ☺ Good linearity
- ☹ Too Small value of the Resistor Module
- ☹ Huge Number of switches
  - Area
  - Parasitic Capacitor

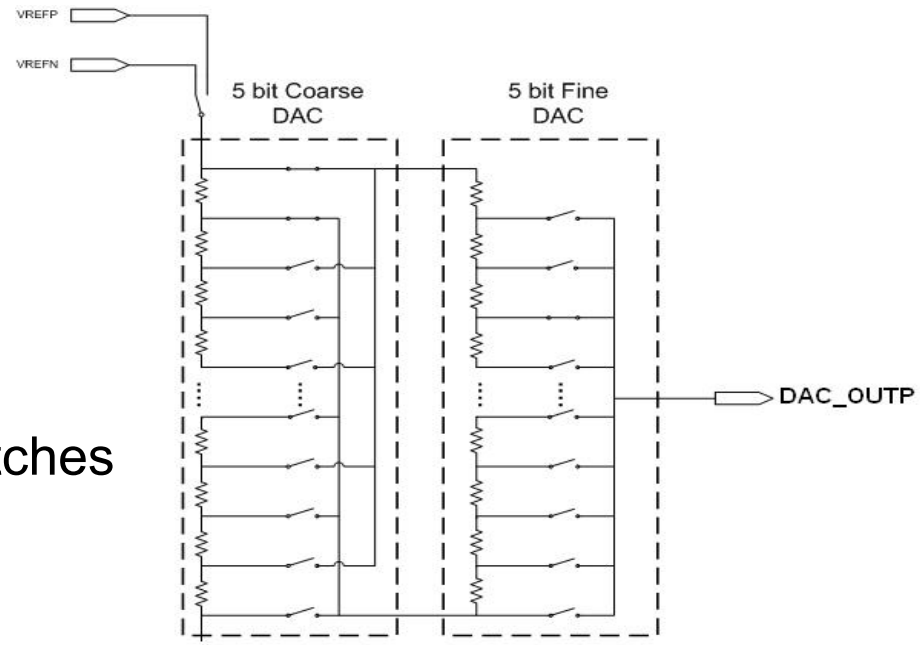
MDAC topology (2)

10 Bit Differential MDAC Double resistors (Segmented)String Array



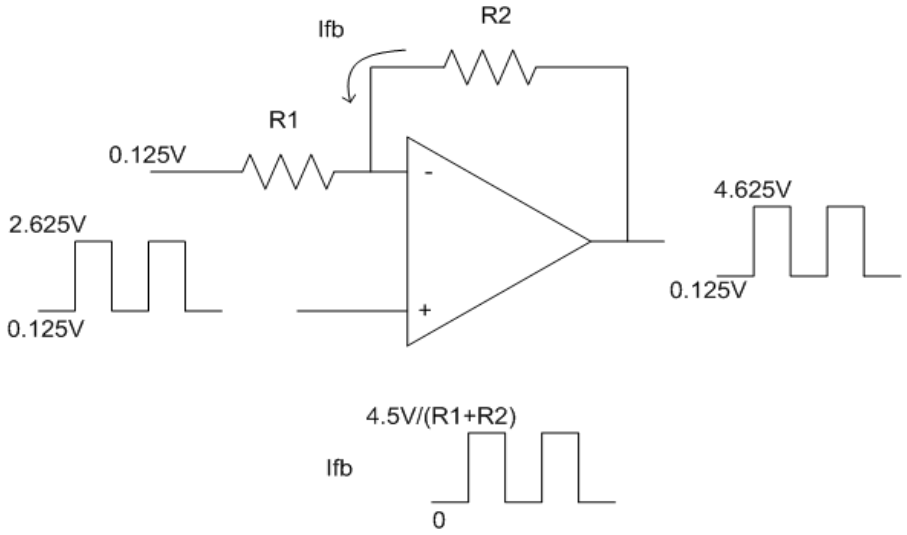
MDAC topology (3)

- 10 Bit Differential MDAC Double Resistor String Array solution:
  - 2*64 resistor
  - 2*64 switches

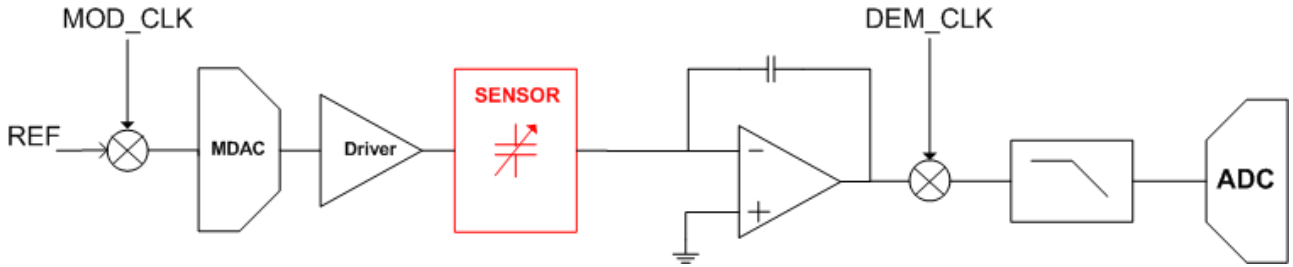


- ☹ Worse linearity
- ☺ Bigger Resistor Module
- ☺ Reduced Number of switches

Driver Feedback resistor (1)



- The squared wave current flowing in the feedback resistor modulates the flicker Noise of the P-Poly resistance
- The resistor flicker noise is folded in base band by the demodulator

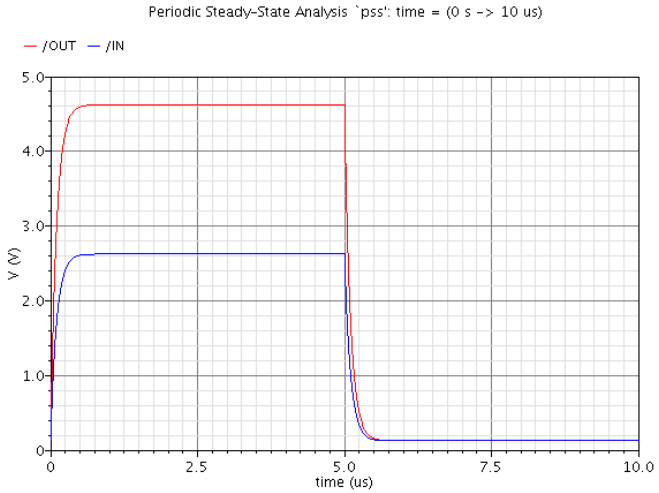


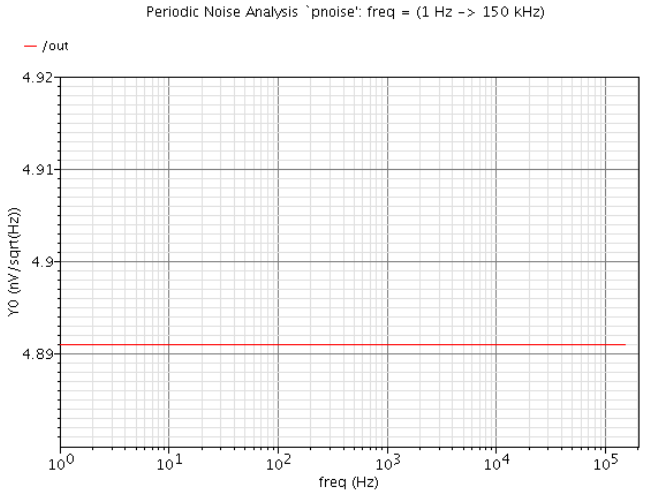
Driver Feedback resistor (2)

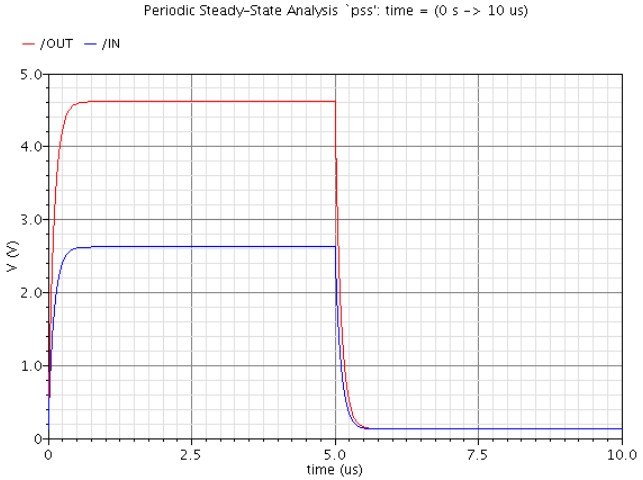
Ideal Op-Amp
Ideal FeedBack resistor

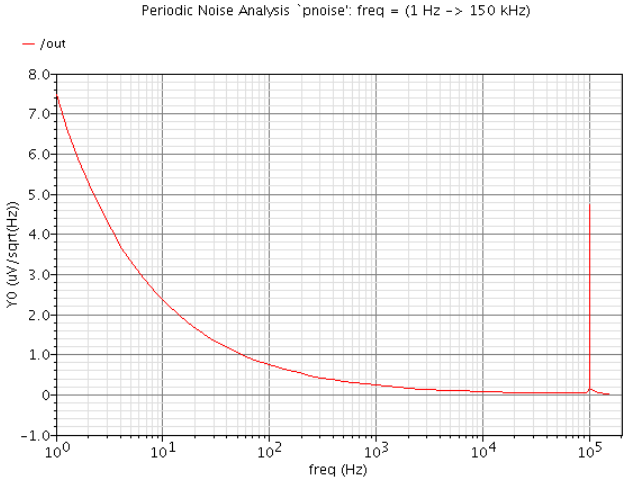
Steady state Noise Analysis

Ideal Op-Amp
Poly Resistor









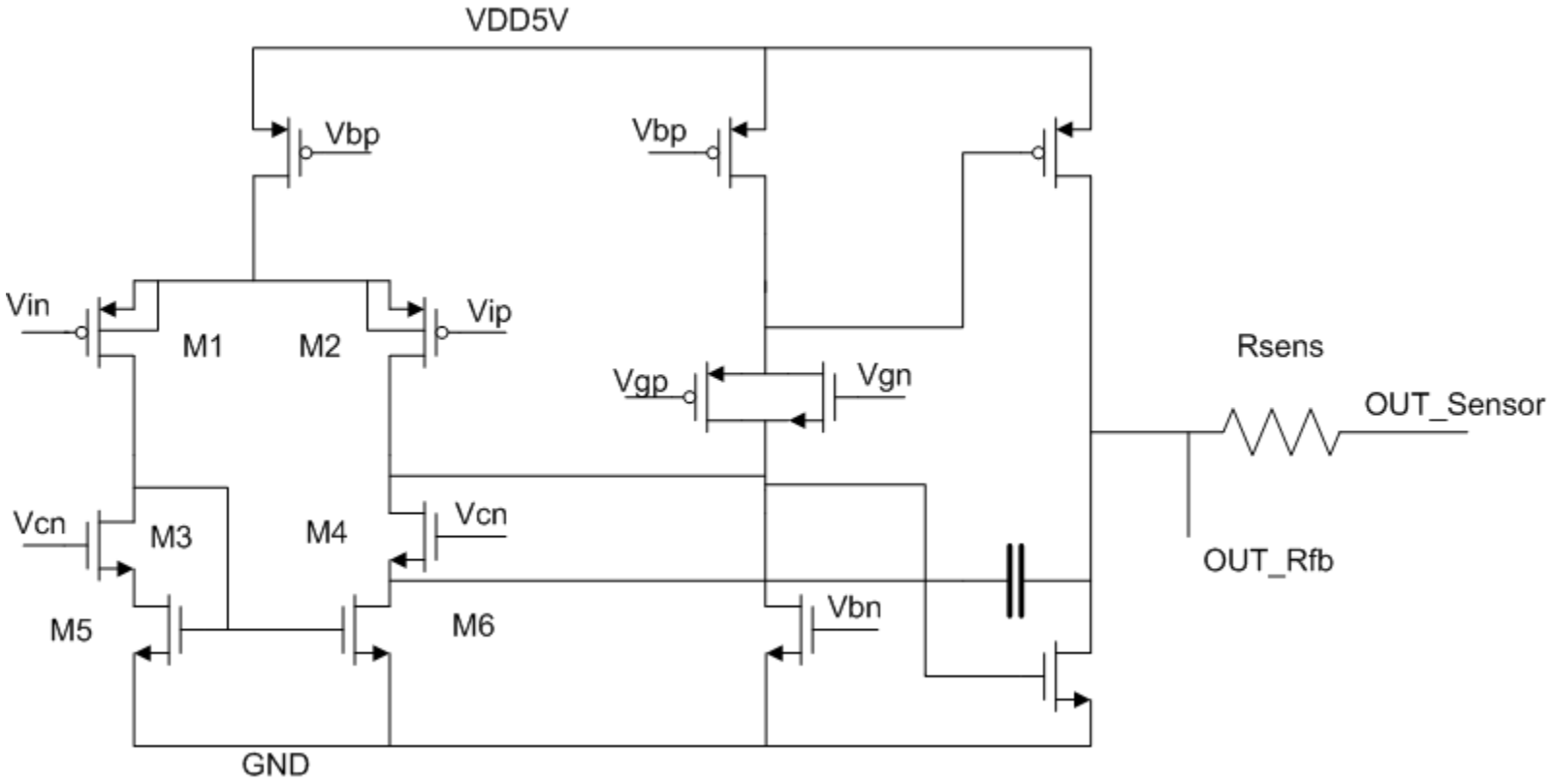
Driver Feedback resistor (3)

- Solutions
  - Increase the value of the feedback resistor
    - ➔ maximum current reduction
    - ➔ thermal noise increase
  - Increase the feedback resistor area
    - ➔ flicker noise reduction
    - ➔ parasitic capacitor increase
    - ➔ stability issue and/or reduced closed loop bandwidth
  - Use Diffused resistor, with negligible flicker noise
    - ➔ Linearity Issue

Driver Operational Amplifier (1)

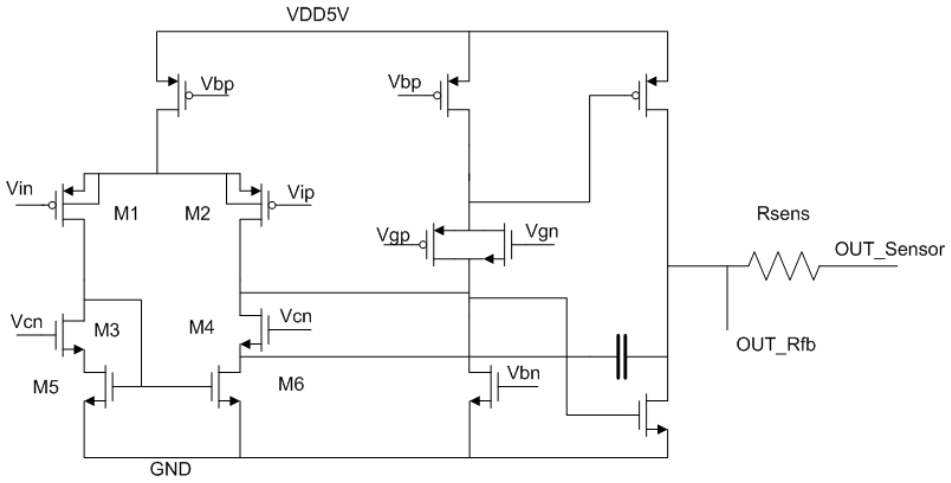
- Output Dynamic range and Resistive feedback
  - ➔ Two stage operational Amplifier
- Low power
  - ➔ Class AB Output Stage
- Input Voltage Range [125mV-to-2.625V]
  - ➔ P-Ch Input stage and supplied under 5V domain
- Output Voltage Range [125mV-to-4.625V]

Driver Operational Amplifier (2)



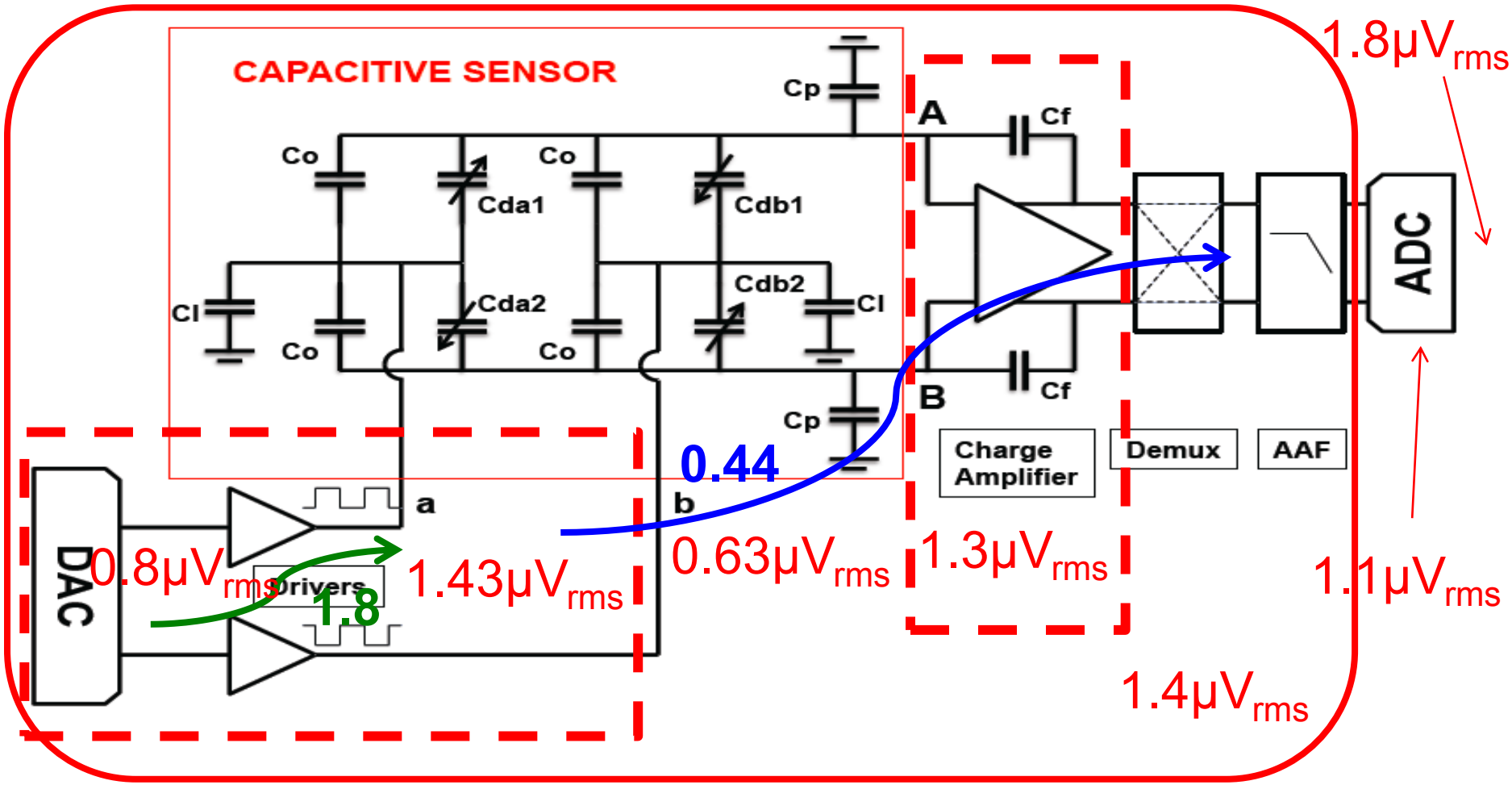
Driver Operational Amplifier (3)

- The Input Voltage Range is compatible with 3.3V MOS
  - 3VMOS better noise performance than 5VMOS
  - ➔ (M1, M2, M3, M4, M5 and M6 are 3.3V MOS)
- Ahuja compensation
  - ➔ move the output pole at higher frequency
- Output series resistor to Sensor Capacitive load adds a zero that help stability



Noise Budget Partitioning

- Assuming no-noise sensor



Biasing Circuit Design (1)

- Driver Gain G_{Driver}=4.5V/2.5V=1.8

$$V_{nBias@DriverOutput} = \frac{0.63\mu V}{0.44} = 1.43\ \mu V_{rms}$$

$$V_{nBias@DriverInput} = \frac{V_{nBias@DriverOutput}}{G_{Driver}} = \frac{1.43\ \mu V_{rms}}{1.8} = 0.79\ \mu V_{rms}$$

- The noise budget is equally divided between **MDAC** & **Drivers**

$$V_{nMDAC} = V_{nDrivers} = \frac{V_{nBias@DriverInput}}{\sqrt{2}} = 0.56\ \mu V_{rms}$$

- Two equal single-ended drivers are used

$$V_{nDriver} = \frac{V_{nDrivers}}{\sqrt{2}} = 0.4\ \mu V_{rms}$$

Biasing Circuit Design (2)

- Driver Noise Contributors
  - Opamp
  - Feedback resistor
- The Driver Noise budget is equally divided between opamp and Feedback resistor contributors (No optimization)

$$Vn_{D\_OP} = Vn_{D\_RFB} = \frac{Vn_{Driver}}{\sqrt{2}} = \frac{0.4\ \mu V}{\sqrt{2}} = 0.28\ \mu V$$

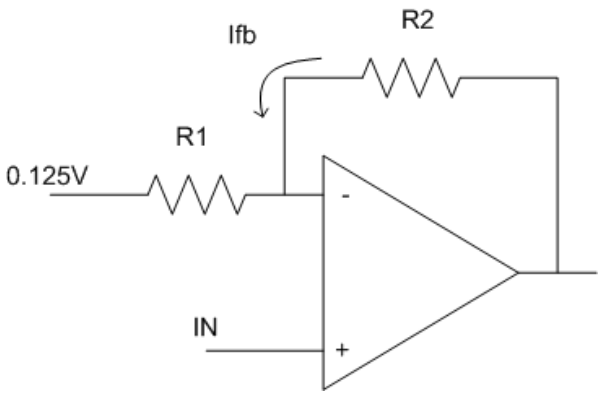
Only thermal noise

$$\frac{Vn_{D\_OP}}{\sqrt{BW}} = \frac{Vn_{D\_RFB}}{\sqrt{BW}} = \frac{0.28\mu V}{\sqrt{300}} = 16nV\ /\sqrt{Hz}$$

$$\left(\frac{Vn_{D\_RFB}}{\sqrt{BW}}\right)^2 = \frac{4\,k_b\,T\,R_2}{\left(1+\frac{R_2}{R_1}\right)}$$

$$R_2 = 28k\Omega \quad R_1 = 35k\Omega$$

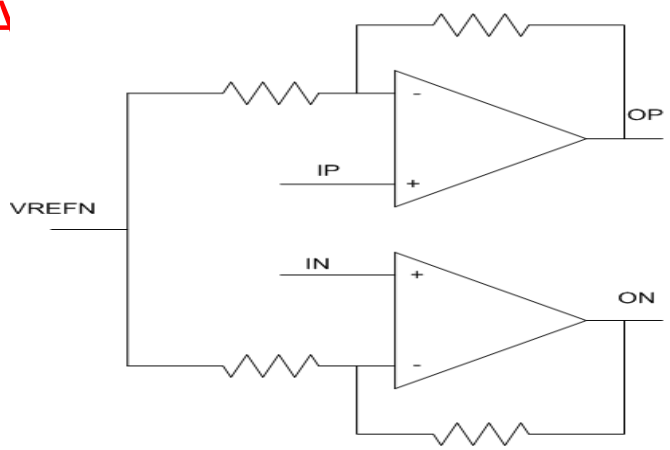
$$Ifb|_{max} = 70\ \mu A$$



Biasing Circuit Design (3)

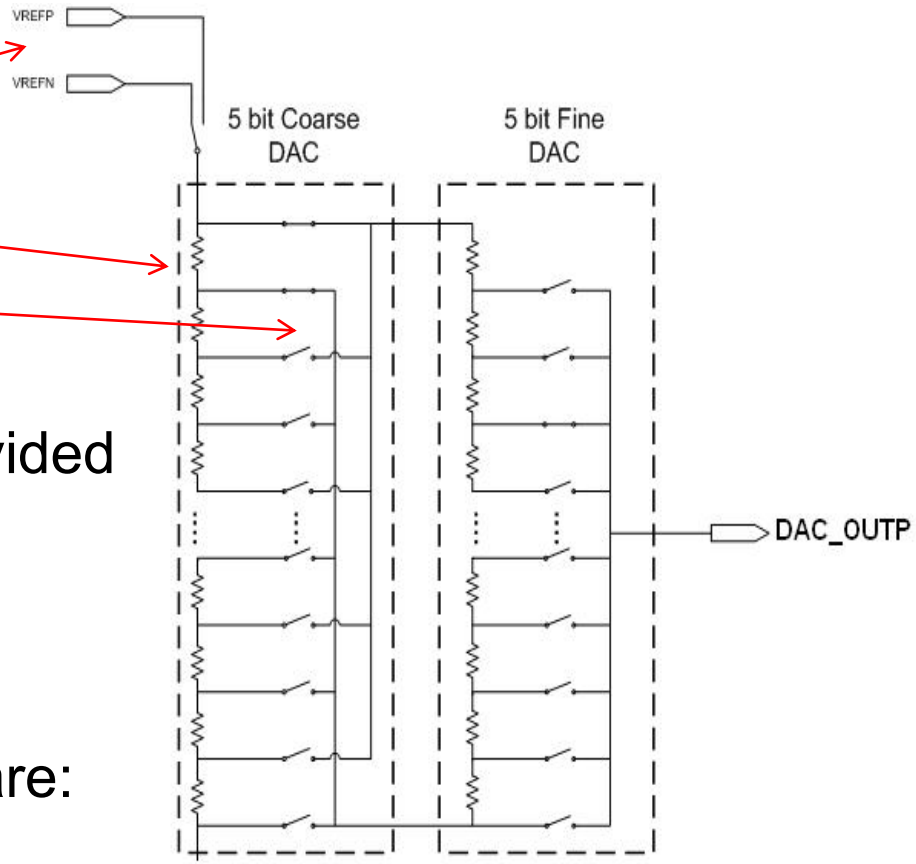
- Opamp design is mainly driven by gain bandwidth requirement
  - GBW=4MHz
  - Input referred Noise density= 28nV/√Hz
  - Driver Current Consumption =300uA

- Total Driver Current consumption
  - I_{tot}=300μA+300μA+72μA=672μA
  - P_{tot}=3.4mW



Biasing Circuit Design (4)

- DAC Noise three contributors:
  - Reference Voltage
  - Resistor Array
  - Switches

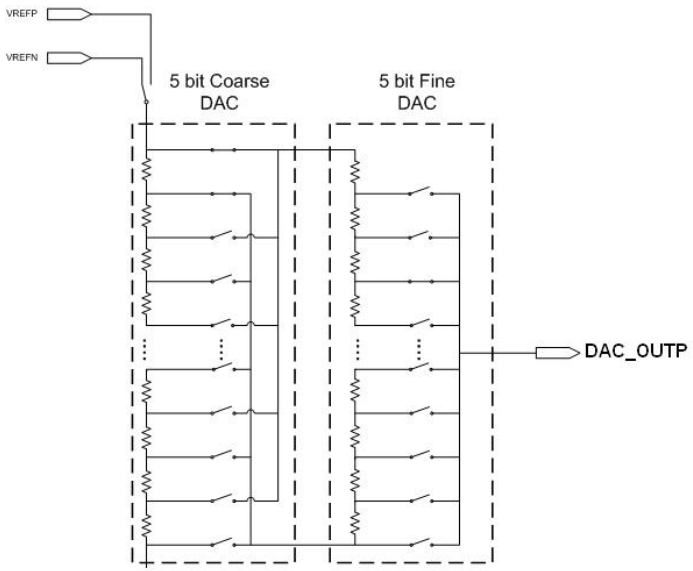


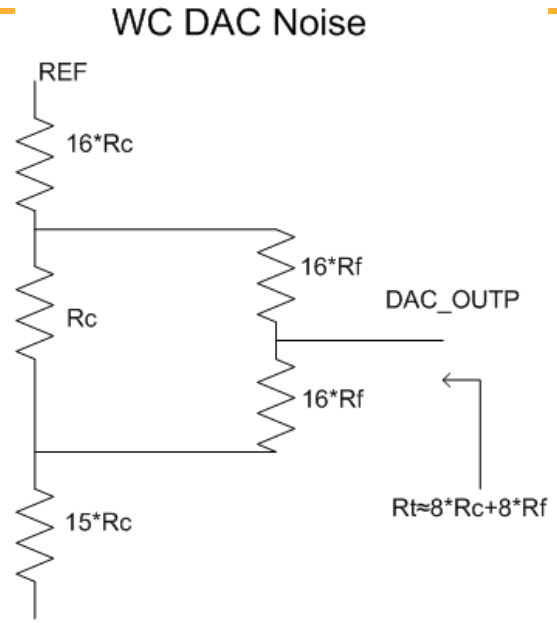
- The Noise Budget is equally divided between the three contributors
  - No optimization

- The single ended contributors are:

$$\frac{Vn_{MDAC}}{\sqrt{6}} = \frac{0.56\ \mu V}{\sqrt{6}} = 0.22\ \mu V \ \square\ 13nV/\sqrt{Hz}$$

Biasing Circuit Design (5)





- The relationship between Coarse and Fine resistor depends on DAC Linearity requirements
  - Ex.: $R_f = 4 \cdot R_c$

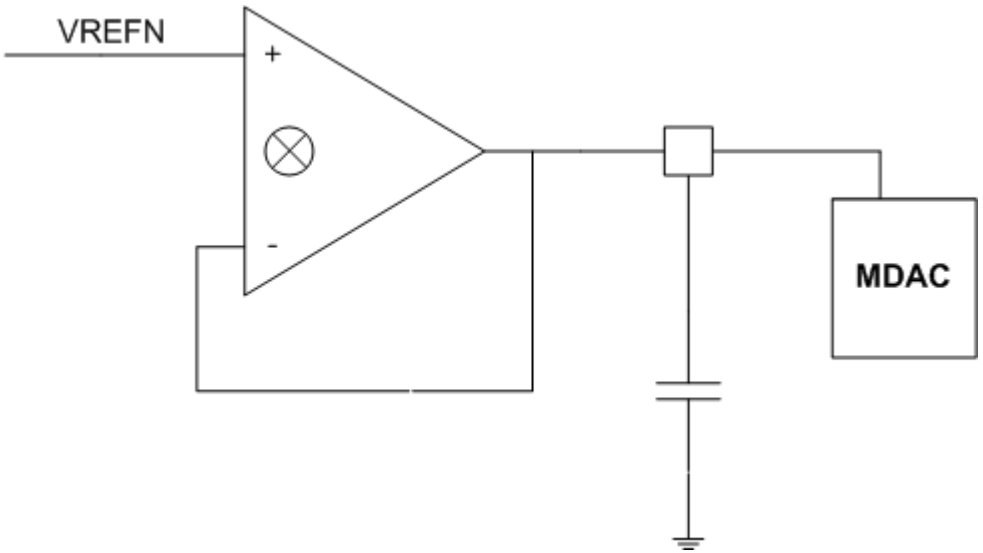
$$\left(13nV/\sqrt{Hz}\right)^2 = 4 \times K_b \times T \times 8 \times (R_c + R_f)$$

$$R_c = 255\Omega \qquad R_f = 1020\Omega$$

$$I_{DAC} = \frac{V_{ref}}{32 \times R_c \times 2} = 153\mu A$$

Biasing Circuit Design (6)

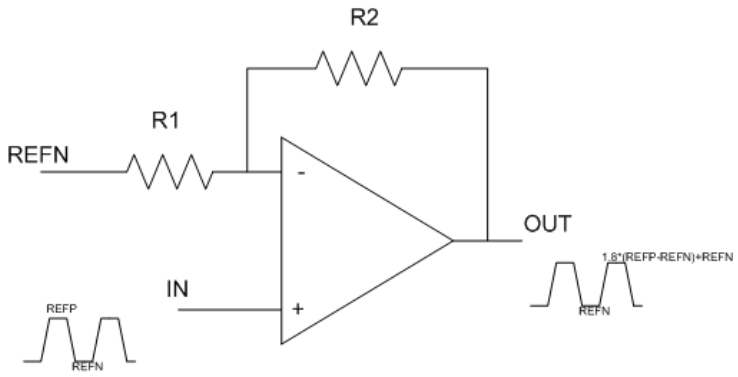
- Power consumption reduction
  - ➔ two external caps filter the noise coming from V_{REF}
  - The DAC reference opamp is choppered
  - Static opamp
    - ➔ Low power consumption (<100µA per-buffers)



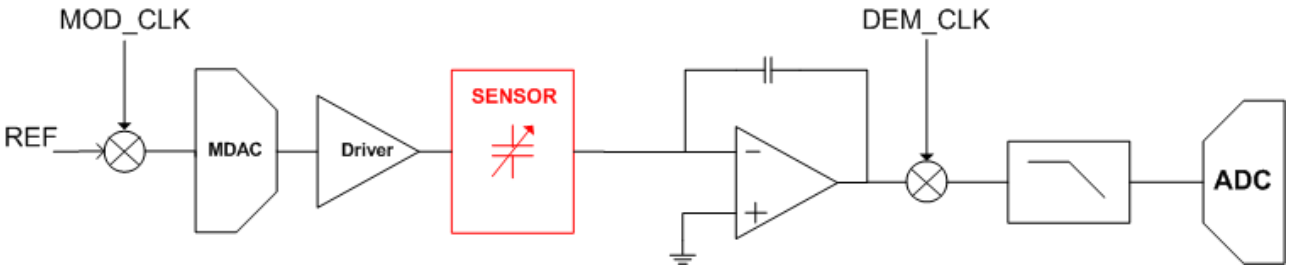
Power Consumption

	Current Consumption [µA]	Supply Voltage [V]	Power Consumption [mW]
Charge Amplifier	2200	3.3	7.3
Anti-Alias Filter	0	3.3	0
Drivers	672	5.0	3.4
Differential MDAC	353	3.3	1.16

Driver Noise vs. DAC Output Slope (1)

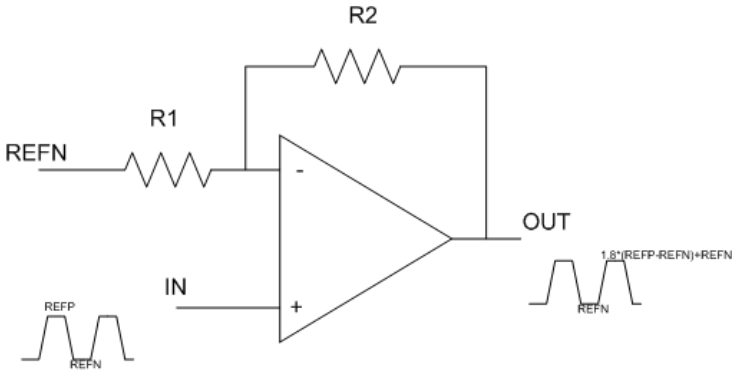


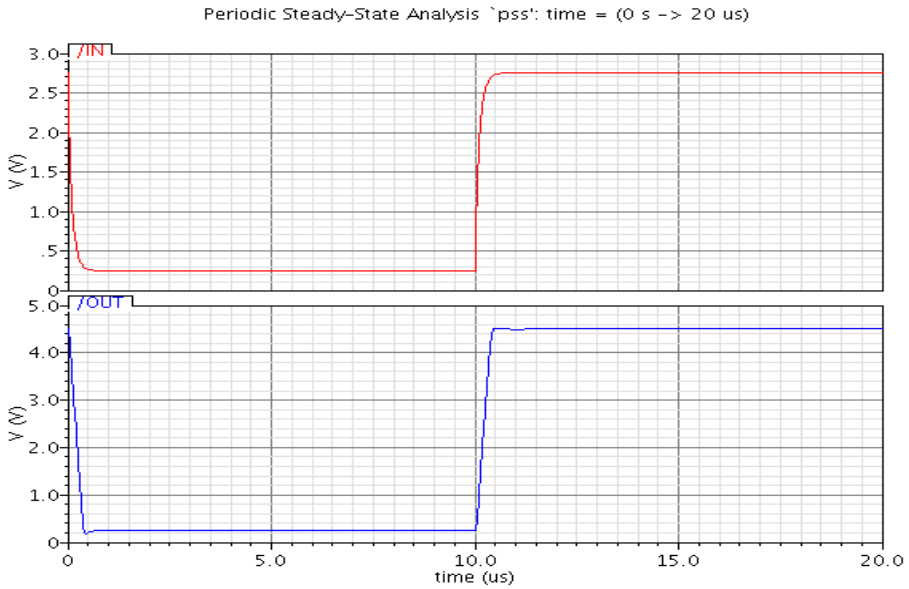
- Output steps would have to be as more ideal as possible

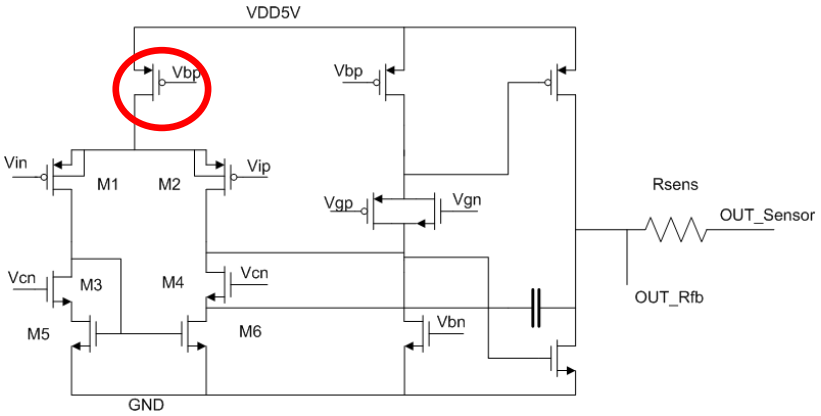


Driver Noise vs. DAC Output Slope (2)

- Tal current generator noise is modulated by the diff-pair un-balancement in slew-rate conditions
  - ➔ Additional noise







Driver Noise vs. DAC Output Slope (3)

- Tail current generator modulated noise reduction
  - Sol1 ➔ Increase Op-Amp Gain Bandwidth
    - ➔ Increase power consumption
  - Sol2➔ Decrease DAC Output Signal Slope
    - ➔ Increase Gain error (The effect is equivalent to reduce the Carrier Amplitude)
    - ➔ To match the maximum ADC dynamic range the Charge Amplifier gain has to be increased
- Trade off GBW vs. Slope ➔ Power vs. Noise

ADC Architecture

- Introduction
- Design Objectives
- Noise Budget Partitioning
- Architecture
- ADC Architecture

20b 250Hz ADC

- Sigma-Delta is the only possible 20b ADC solution
  - No matching requirement
  - Oversampling requirement (easy to be performed at small signal bandwidth)

20b 250Hz Sigma-Delta ADC

- Overall Specs

ADC Resolution:	> 20 bit (SNR >123 dB)
THD	< -90 dB
Bandwidth	1Hz-250Hz
Output rate	500 Sps
Anti Aliasing Filter	External
Supply Voltage	3.3V
Area	< 3.5 mm^2

20b 250Hz Sigma-Delta ADC

- Noise Budget calculation
  - Reference Voltage: 2.5V
  - Input Amplitude: $4V_{pp}$ ($1.4V_{rms}$)
  - For 125dB-SNR ➔ Total Noise ≈ 700 fV^2

20b 250Hz Sigma-Delta ADC

- Noise Budget calculation
  - For 125dB-SNR ➔ Total Noise ≈ 700 fV^2
  - Noise Budget
    - Opamp Noise after chopper 150 fV^2
    - kT/C Noise 250 fV^2
      - 250 fV^2 < kT/(Cs·OSR)
    - Reference Noise 200 fV^2
    - Q_{noise} + Other noise < 50fV^2
  - ➔ Equivalent SNR (considering only Q_{noise}) = 136 dB
    - ➔ MATLAB SNR requirement > 136 dB

20b 250Hz Sigma-Delta ADC

- Sampling frequency choice
  - Low sampling frequency
    - Quantization noise
      - Low OSR ➔ low resolution
        - ➔ high order
          - Q_N is not the key limitation !!!
    - Thermal noise
      - Low OSR ➔ large in-band noise
        - For a given DR ➔ Larger C_S ➔ higher Power

$$N_{inband} = \frac{\frac{kT}{C_s}}{OSR} = \frac{2 \cdot F_b}{F_s} \cdot \frac{kT}{C_s}$$

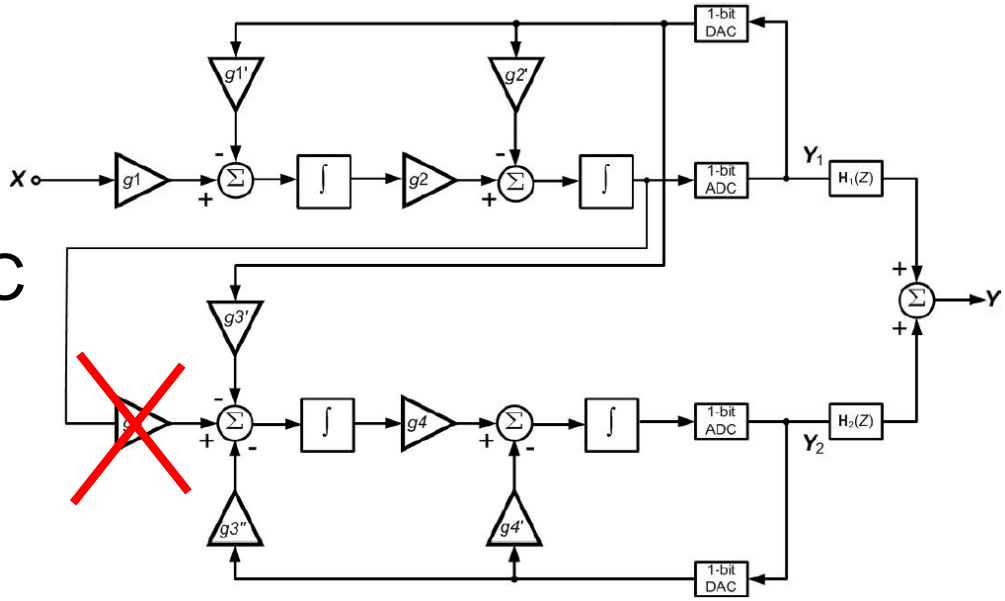
  - High sampling frequency
    - Smaller sampling period
      - Larger opamp bandwidth spec ➔ higher power
      - Larger slew-rate ➔ higher power

20b 250Hz Sigma-Delta ADC

- Sampling frequency choice
  - Trade-off choice
    - ➔ OSR= 8.192
    - ➔ Fs = 250 x 2 x 8.192 = 4.096 MHz
    - ➔ $N_{inband}^2=(kT/C_S)/OSR$
      - ➔ $C_S = kT / (N_{inband}^2 \cdot OSR) = 10pF$

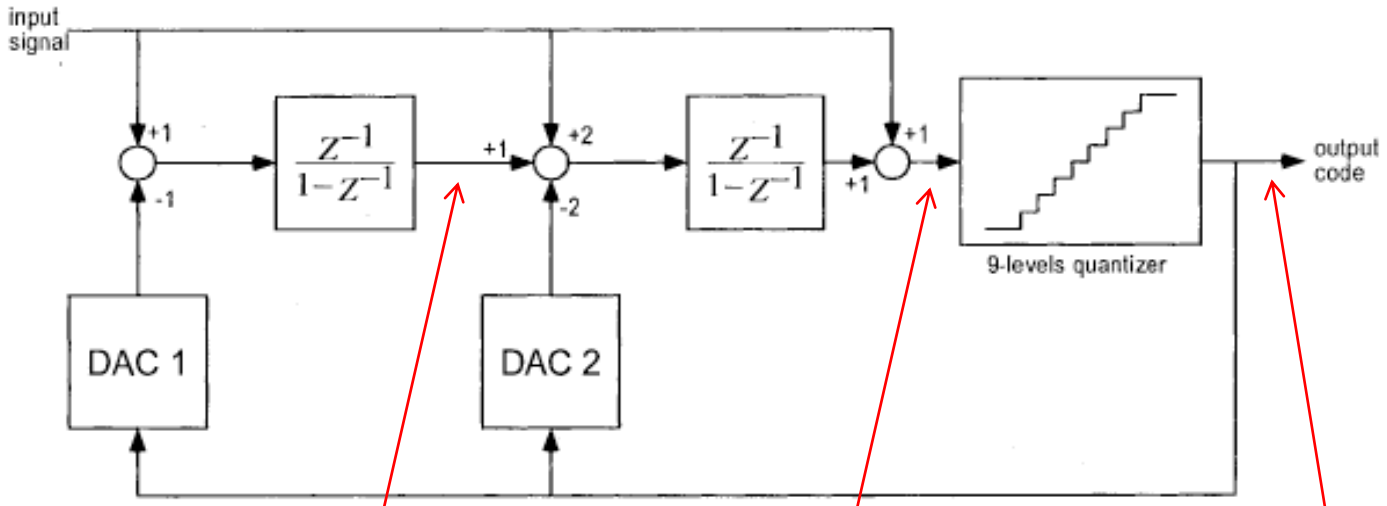
20b 250Hz Sigma-Delta ADC – Topology Choice

- Single-bit 2+2-MASH
  - ☺ No DAC cap mismatch sensitivity
  - ☹ Cap mismatch sensitivity in the noise canceling network
  - ☹ Large Slew-rate requirements
  - ☺ Simple feedback DAC network
  - Stability !!!



20b 250Hz Sigma-Delta ADC – Topology Choice

- 2nd-order FeedForward single-loop

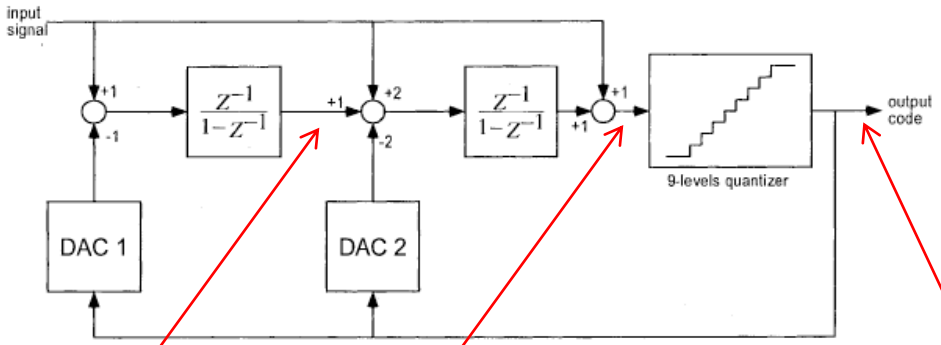


$$P = Q \cdot \left(-1 + z^{-1}\right) \cdot z^{-1} \qquad R = Q \cdot \left(-2 + z^{-1}\right) \cdot z^{-1} \qquad Y = X + Q \cdot \left(1 - z^{-1}\right)^2$$

- No signal in P & R
  - Maximum opamp output swing ➔ Quantizer LSB
  - Useful for multi-bit quantizer
    - ➔ Small integrator output swing

20b 250Hz Sigma-Delta ADC – Topology Choice

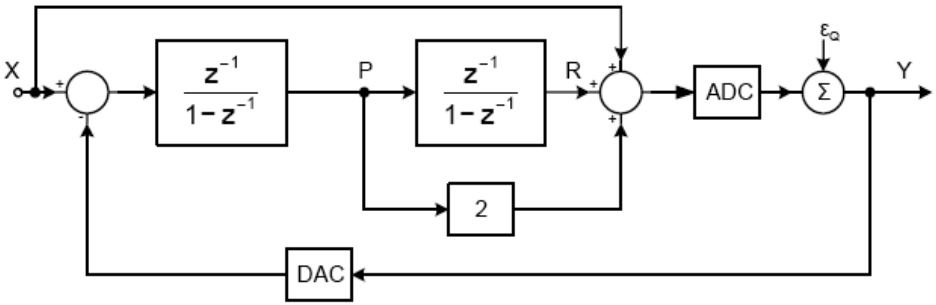
- 3-bit 2nd-order FeedForward single-loop
  - ☹ DAC cap mismatch sensitivity
  - ☺ No Cap mismatch sensitivity in the noise canceling network
  - ☺ No Finite opamp sensitivity in the noise canceling network
  - ☺ Reduced Slew-rate requirements
  - ☹ Feedback DAC network with DEM



$$P = Q \cdot \left(-1 + z^{-1}\right) \cdot z^{-1} \qquad R = Q \cdot \left(-2 + z^{-1}\right) \cdot z^{-1} \qquad Y = X + Q \cdot \left(1 - z^{-1}\right)^2$$

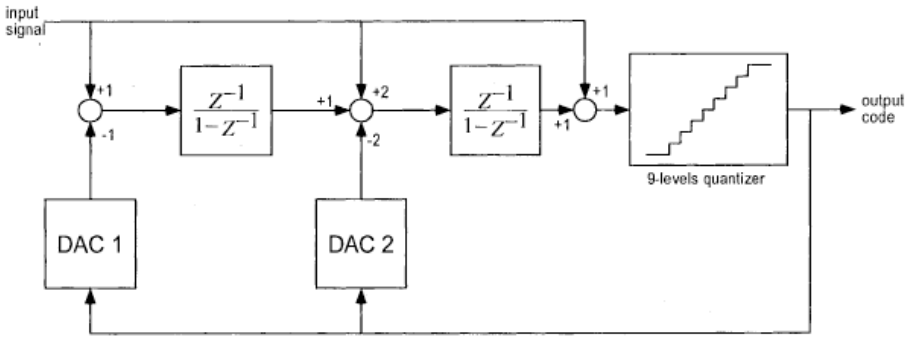
20b 250Hz Sigma-Delta ADC – Topology Choice

- Silva's Topology ←←
  - ☺ Two input branches
    - Lower load for the previous stage
  - ☺ Single DAC



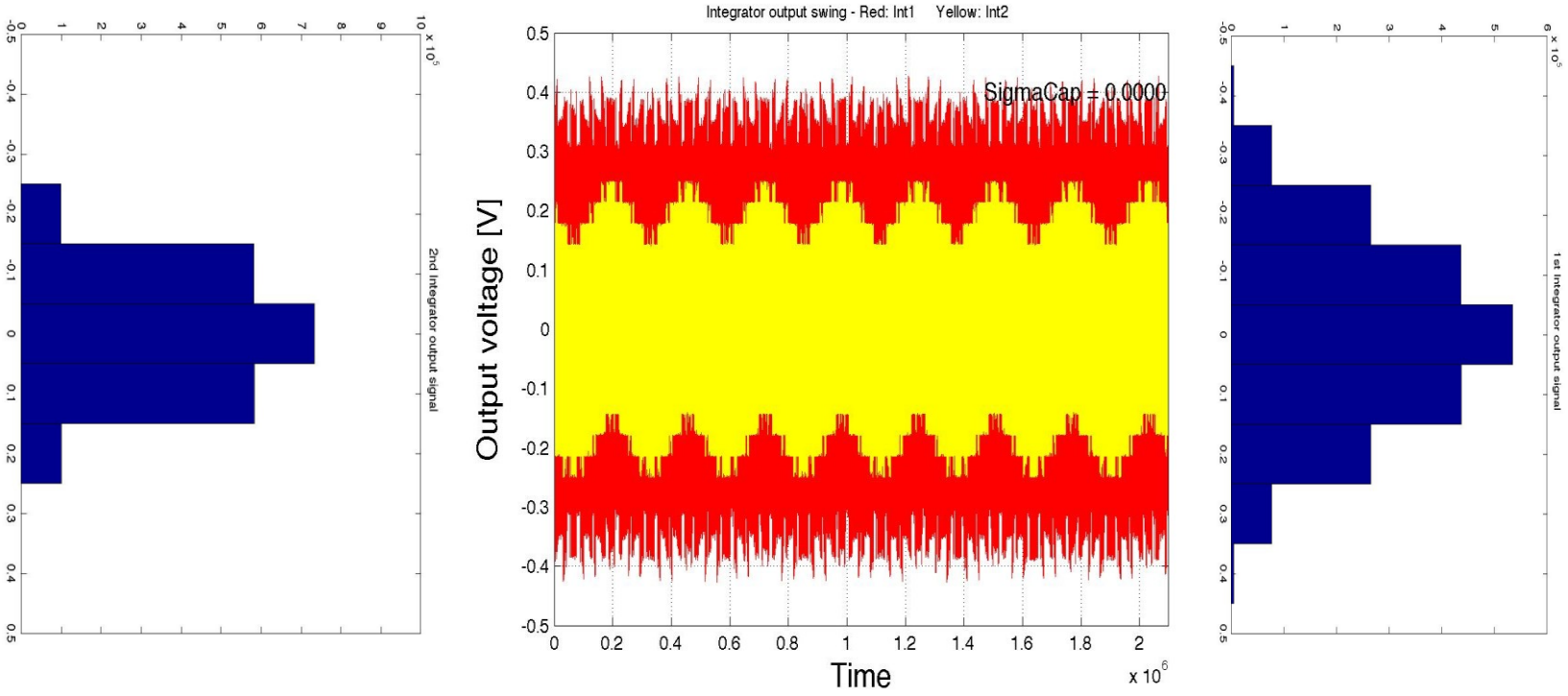
$$P = Q \cdot \left(-1 + z^{-1}\right) \cdot z^{-1} \qquad R = Q \cdot \left(-2 + z^{-1}\right) \cdot z^{-1} \qquad Y = X + Q \cdot \left(1 - z^{-1}\right)^2$$

- Nys's Topology
  - ☹ Three input branches
    - Higher load for the previous stage
  - ☹ Two DACs



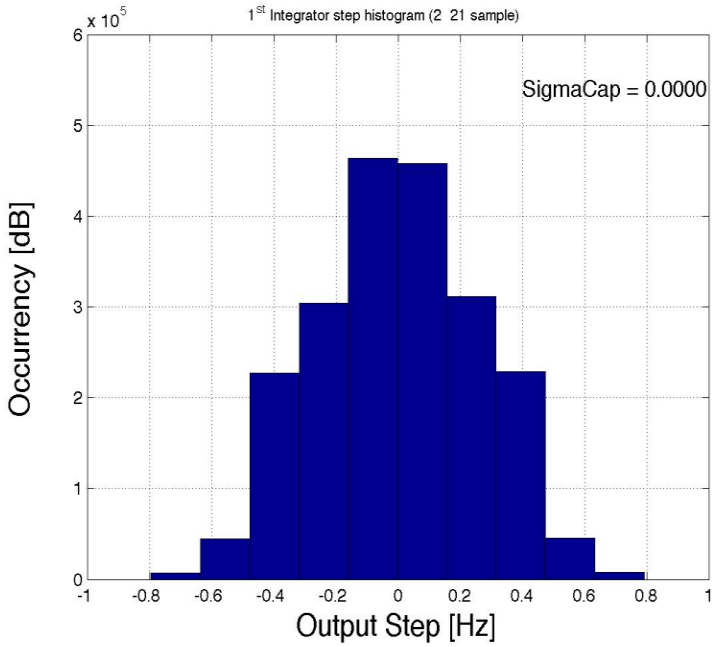
20b 250Hz Sigma-Delta ADC – Topology Choice

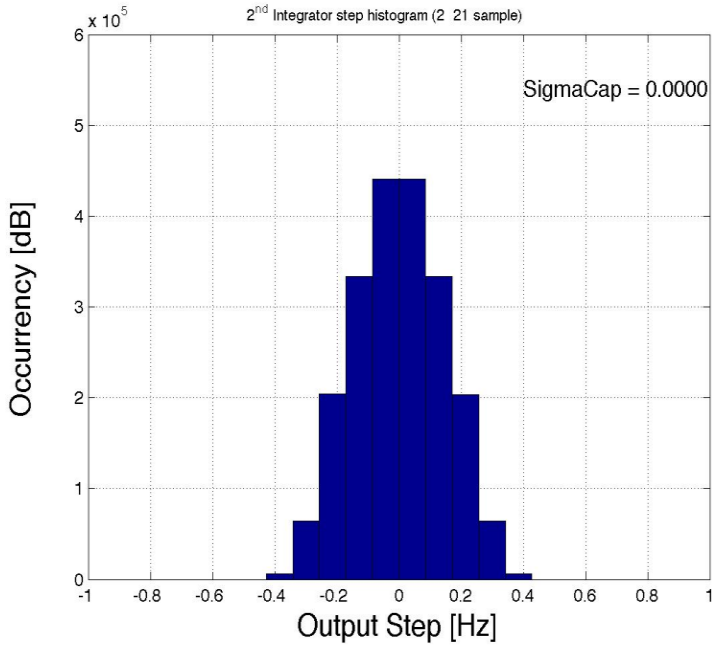
- FF Topology
- Amplitude swing @ Integrator outputs
  - Output swing < $V_{FS}/2$ ➔ relaxed opamp output swing
    - ➔ Low Power Consumption



20b 250Hz Sigma-Delta ADC – Topology Choice

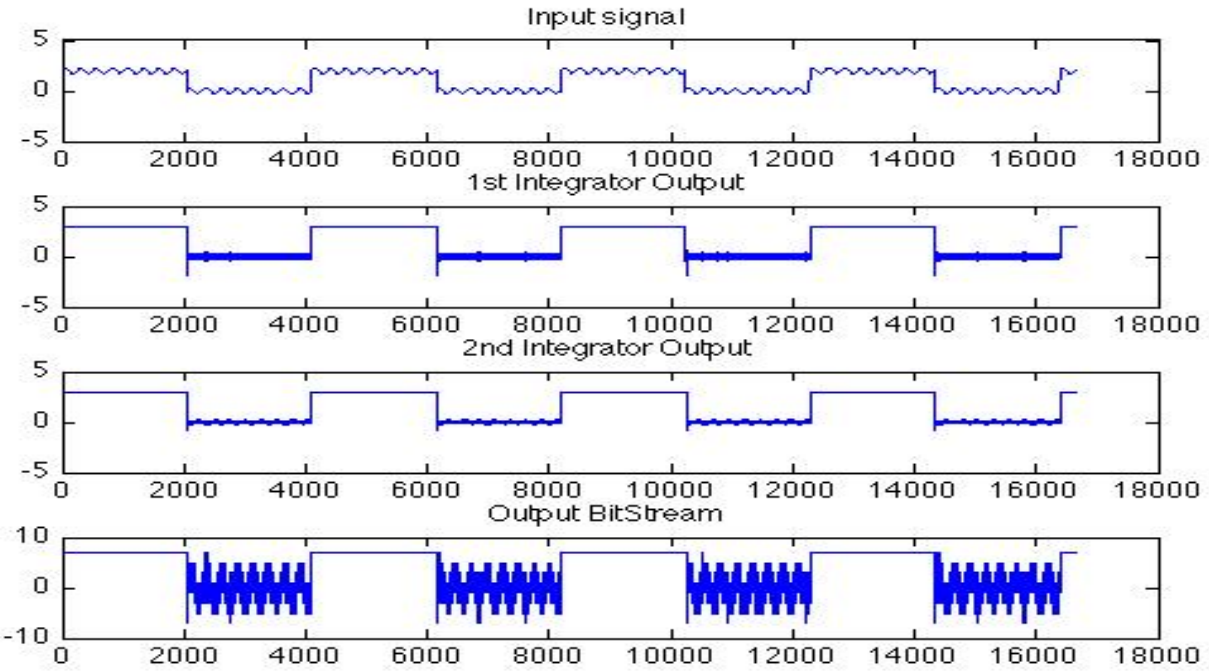
- FF Topology
- Integrator output step histogram
  - SR is still important





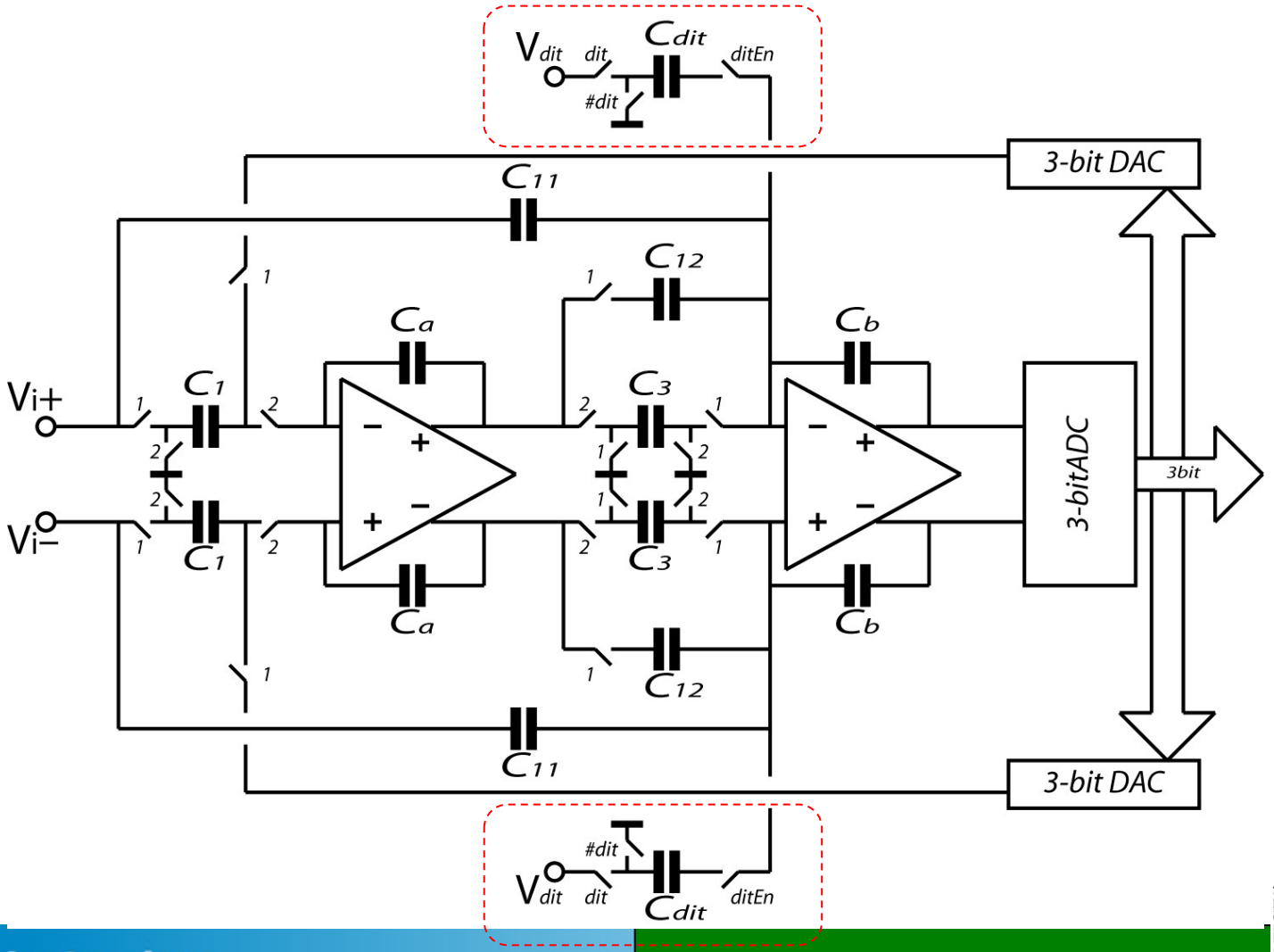
20b 250Hz Sigma-Delta ADC – Topology Choice

- FFSDM ➔ Stability & Recovery Test
  - Input overload signal
  - The structure recovers from overload
    - No reset circuit is need



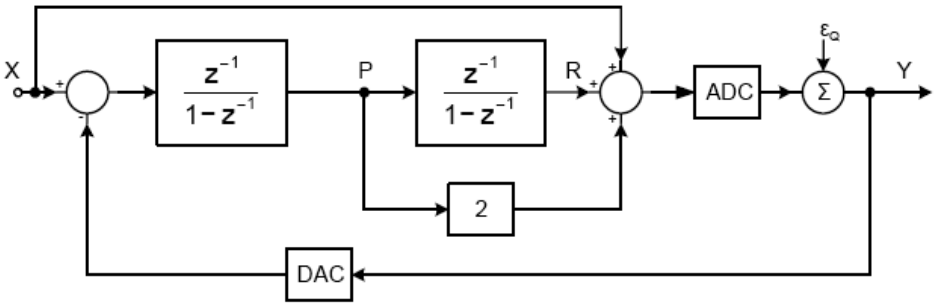
20b 250Hz Sigma-Delta ADC – Topology Choice

- FFSDM – SC Implementation



20b 250Hz Sigma-Delta ADC – Topology Choice

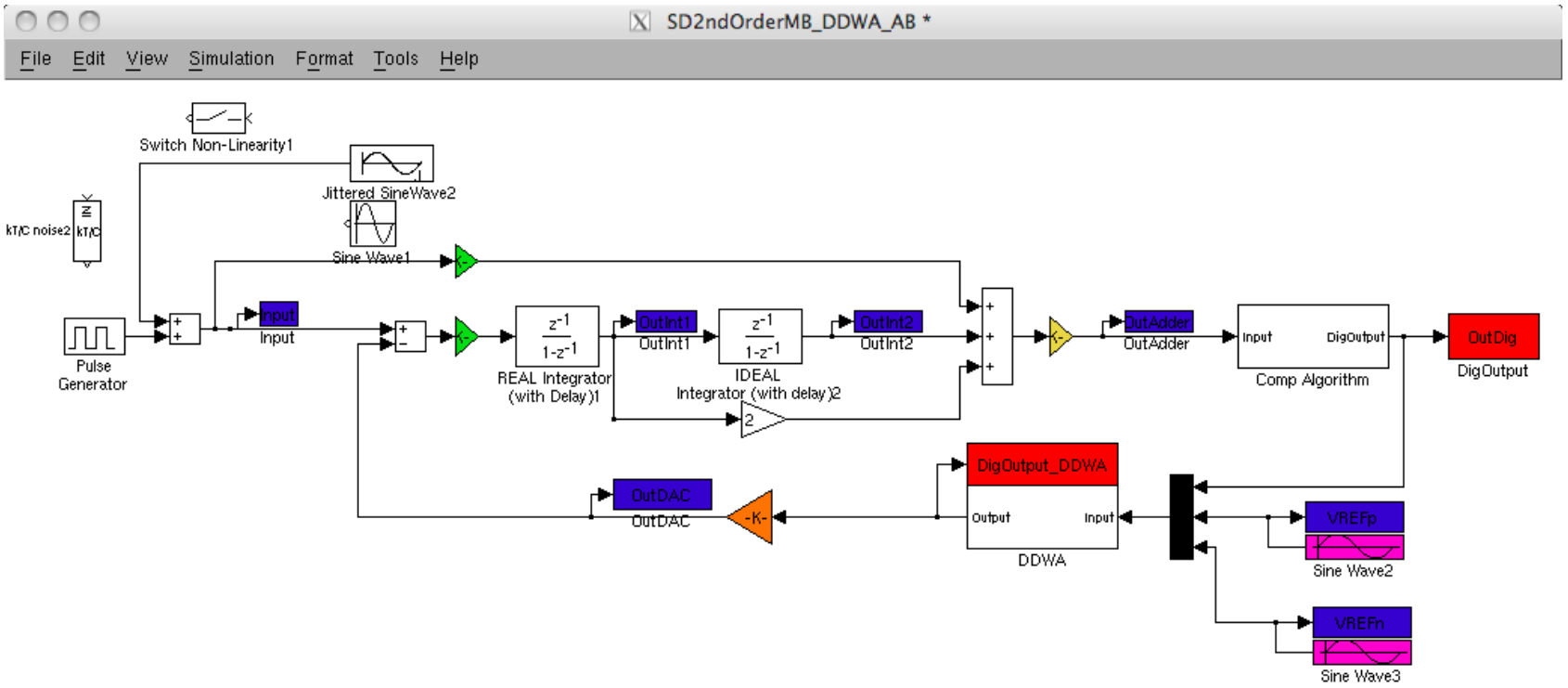
- FFSDM ➔ Architecture development
  - Q_{noise}
  - DAC non-linearity (Cap mismatch)
  - Instability / Recovery time
  - Idle tones
  - Quantizer V_{TH} Error
  - FF Adder Gain Error



- Circuit design development
  - Opamp performance effects
    - Gain, Bandwidth, Slew-Rate
  - Sampling Jitter
  - Thermal noise

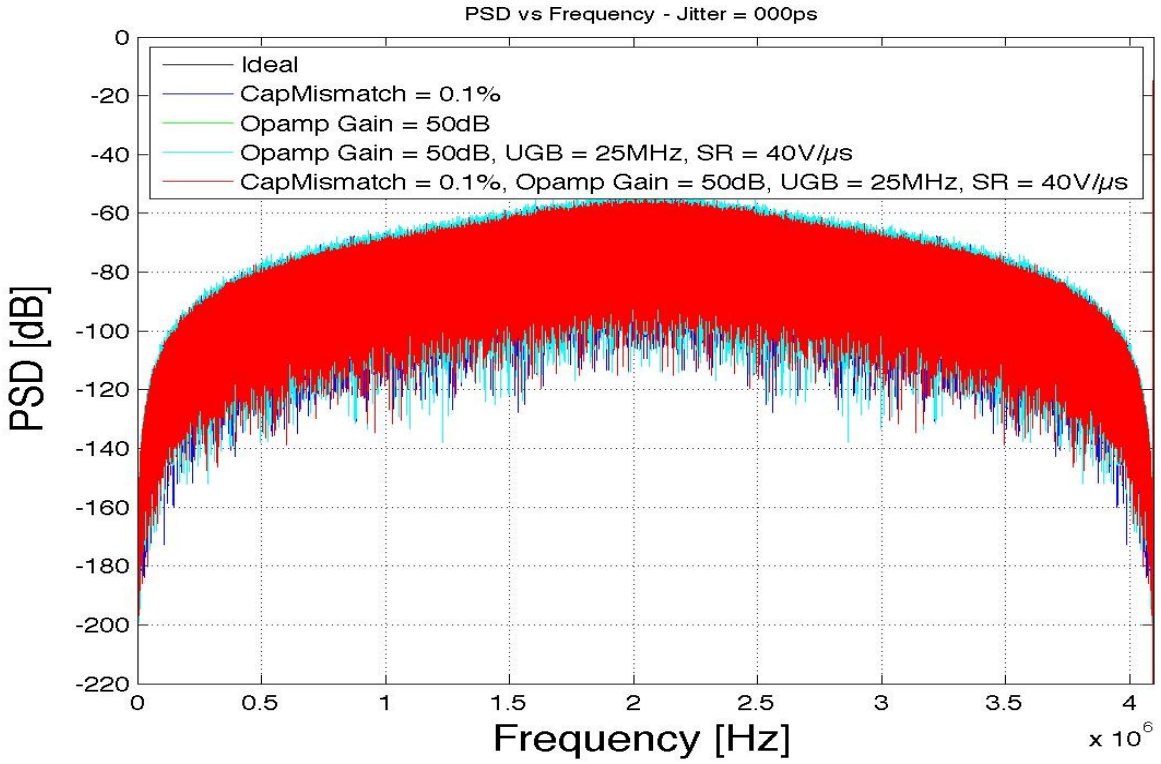
20b 250Hz Sigma-Delta ADC – Topology Choice

- Simulink model
  - Transient effects (SR, QN, Jitter, mismatch)
  - Small signal effects (Thermal&1/f, Gain&Bandwidth)



20b 250Hz Sigma-Delta ADC – Topology Choice

- FFSDM - Real opamp performance
  - Gain = 50dB, UGB = 25MHz, SR = 40V/µs
    - Poor opamp gain requirement ➔ **LowPowerCons**

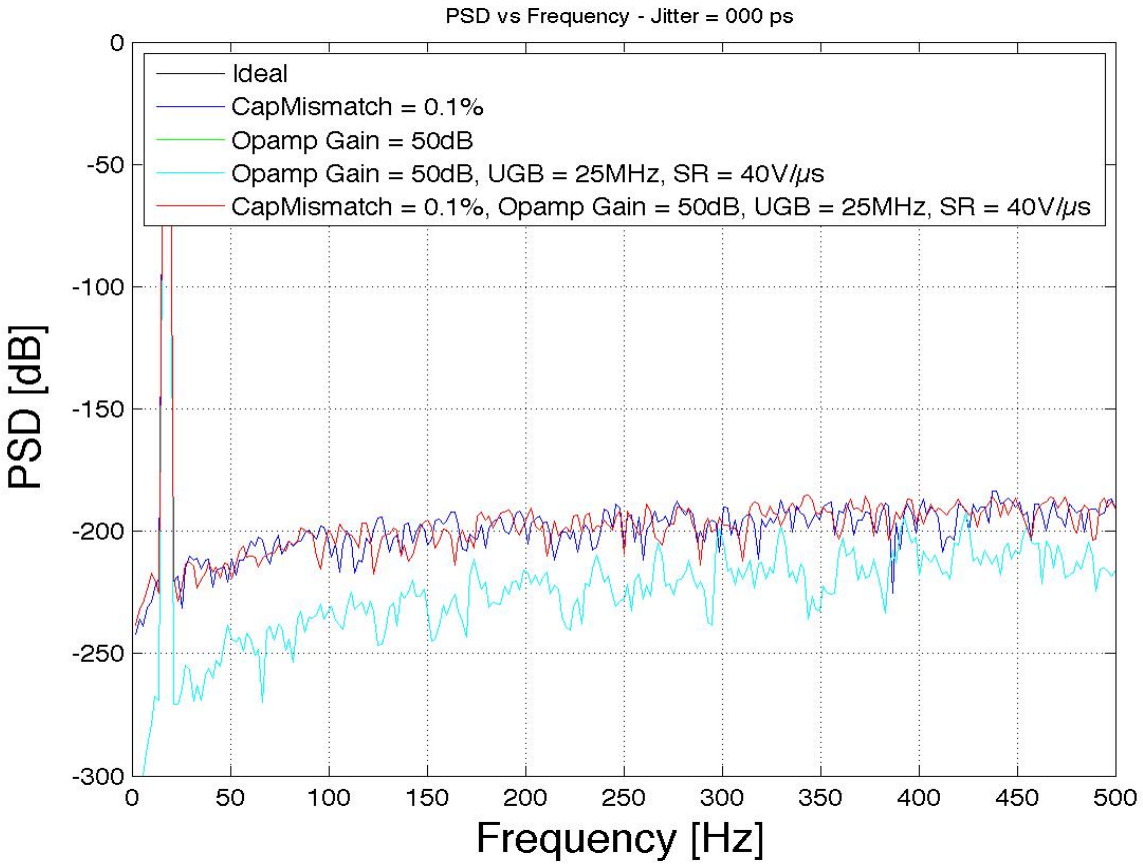


20b 250Hz Sigma-Delta ADC – Topology Choice

- FFSDM - Real opamp performance

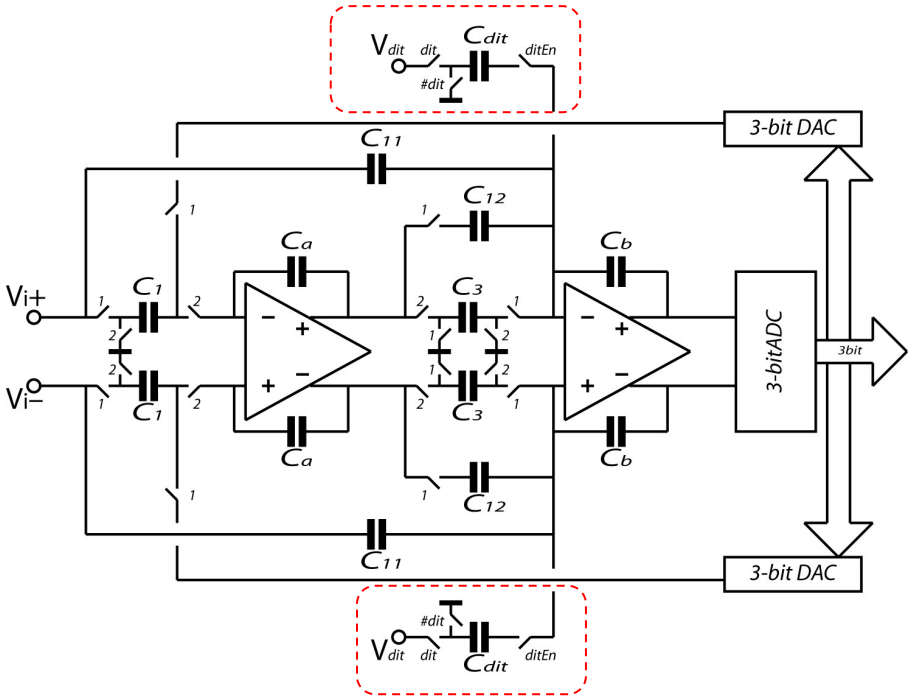
- $SNR_{NoJitter}$

- 192.71dB
- 168.08 dB
- 192.71 dB
- 192.71 dB
- 168.078dB



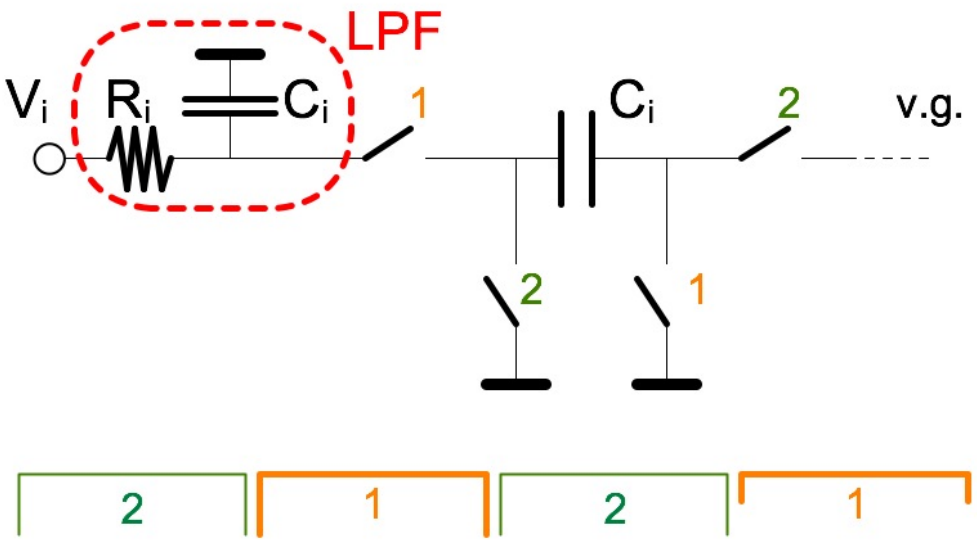
20b 250Hz Sigma-Delta ADC – Topology Choice

- Dither Avoids Spurious_Tone generation at low signal-level
  - @ Low-Level Multibit ADC behaves like a single-bit ADC
- Dither is implemented with an SC branch
  - C_{dit} = 1/10 Cb
  - connected at the 2nd-opamp input
  - *dith* frequency = Fs/4
  - ➔ input tones at Fs/4, i.e. far from the signal band
- can be disabled (dithEn signal)



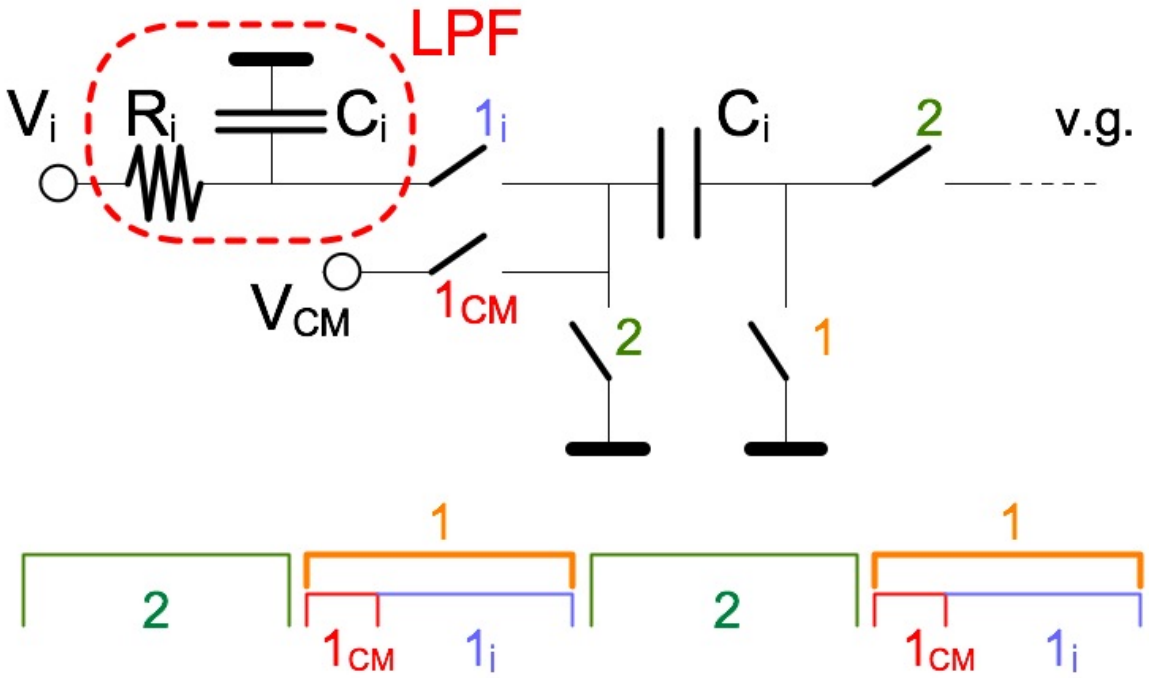
20b 250Hz Sigma-Delta ADC – Implementation

- Input noise reduction
  - The aggressive AAF reduces input noise bandwidth
    - It reduces settling time of the sampling operation
  - The final sampled value depends on charging starting point
    - ➔ Sampling error depends on signal amplitude
      - THD



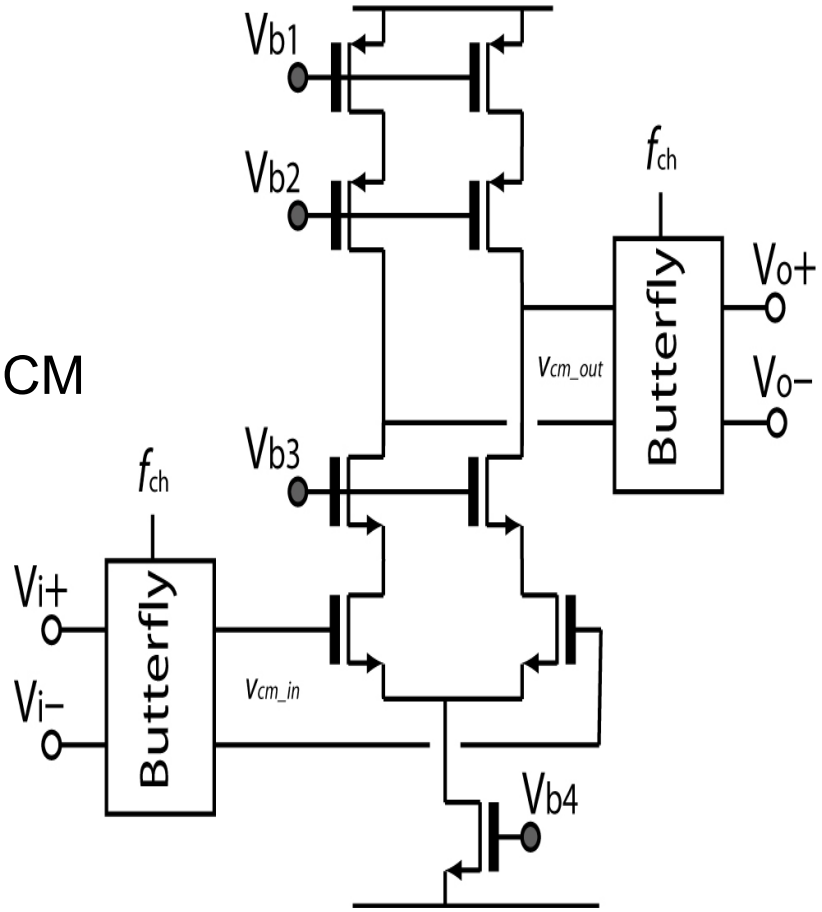
20b 250Hz Sigma-Delta ADC – Implementation

- Input noise reduction - Solution
  - The sampling capacitor is reset at the beginning of the sampling phase
    - ➔ The signal-dependent error is canceled



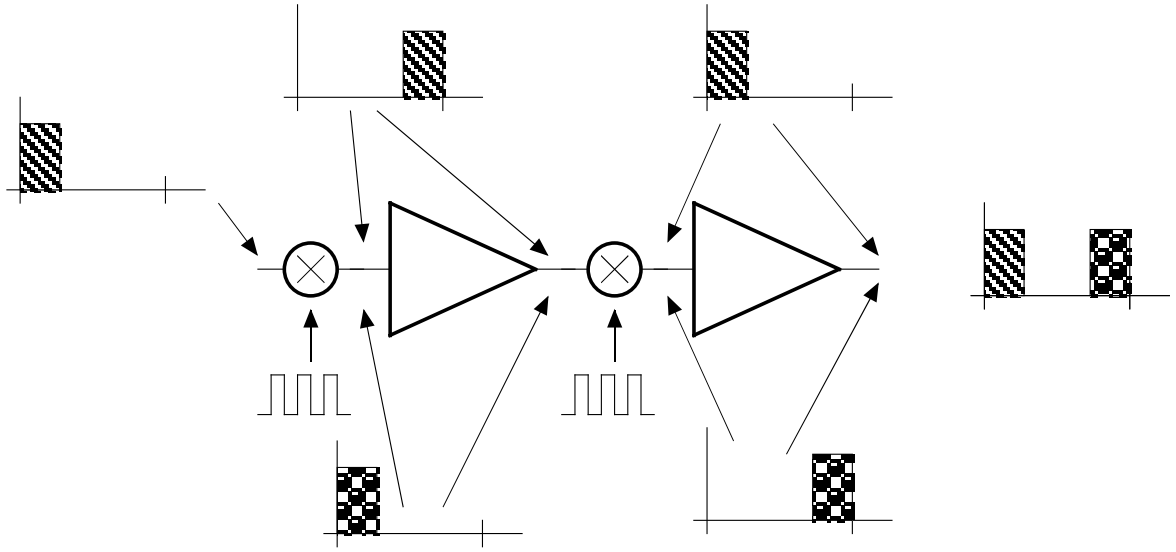
20b 250Hz Sigma-Delta ADC – Implementation

- 1st-opamp design
  - 1/f Noise ➔ Chopper
  - FFSDM
    - ➔ Reduce swing
    - ➔Telescopic cascode
      - Different input.vs.output CM compensated in the SC structure



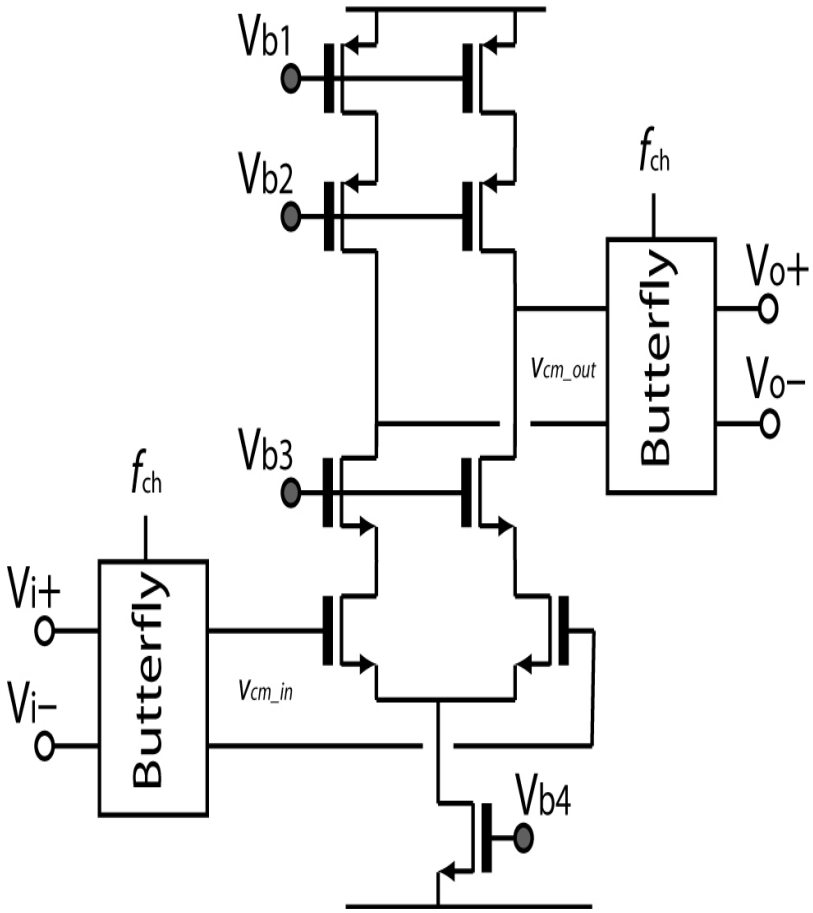
20b 250Hz Sigma-Delta ADC – Implementation

- Chopper concept
  - Chopper frequency choice: Trade-off motivation
    - Low chopping frequency ➔ Larger in-band noise folding
    - High chopping frequency ➔ Large-&-frequent opamp output steps
- Chopper frequency choice ➔ $F_s/8$



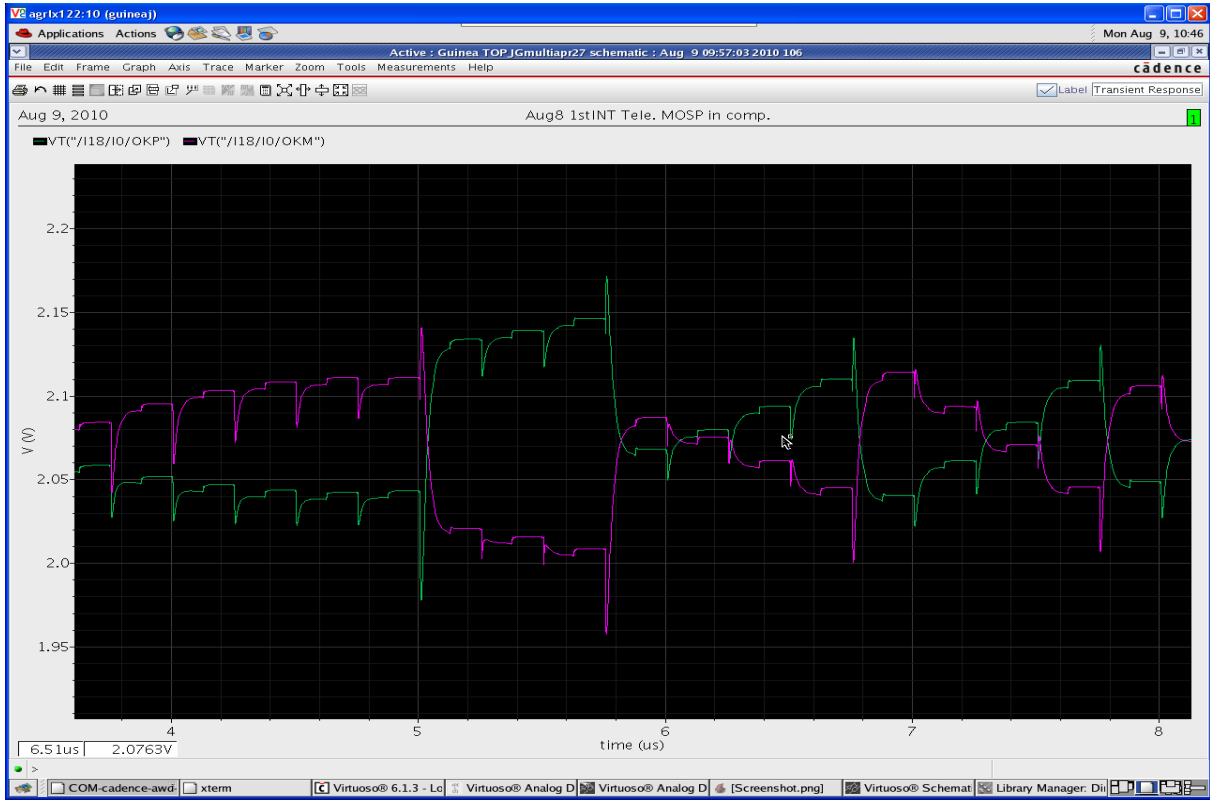
20b 250Hz Sigma-Delta ADC – Implementation

- Chopper concept
  - In a two-stage opamp only the 1st-stage in chopped
    - Negligible 2nd-stage 1/f noise
    - Smaller 1st-stage output swing
  - In a single-stage opamp
    - ➔ The full opamp is chopped
    - ➔ Significant output swing
    - !!! BUT in FF-SDM
      - ➔ small 1st-opamp output swing
      - ➔ Chopper is not critical



20b 250Hz Sigma-Delta ADC – Implementation

- Chopper Transient evolution
  - Output1➔ pink line
  - Output2➔ Green line

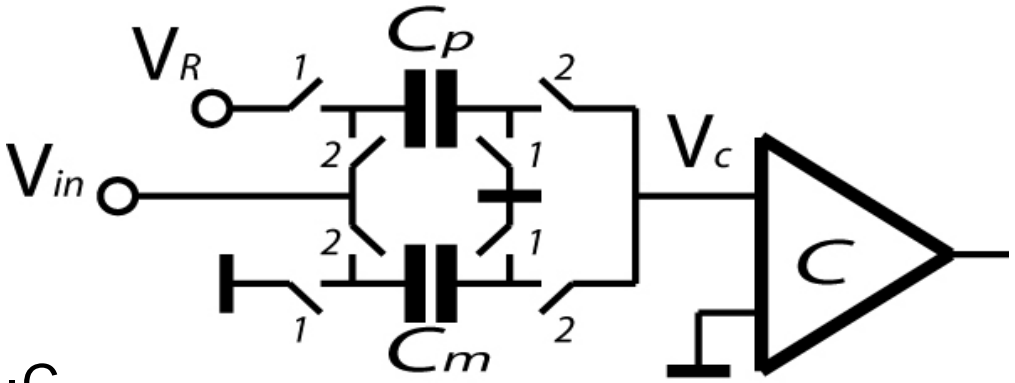


DC-gain	93dB
UGB	35MHz
Settling time (closed loop configuration)	< 120ns
Chopper frequency	Fs/8
Current consumption	390μA

20b 250Hz Sigma-Delta ADC – Implementation

- Multibit ADC
- ADC Threshold voltage generation
  - Passive SC solution in the comparator (single-ended version)
- Charge balance

$$V_c(2) = V_{in} - \frac{C_p}{C_p + C_m} \cdot V_R$$

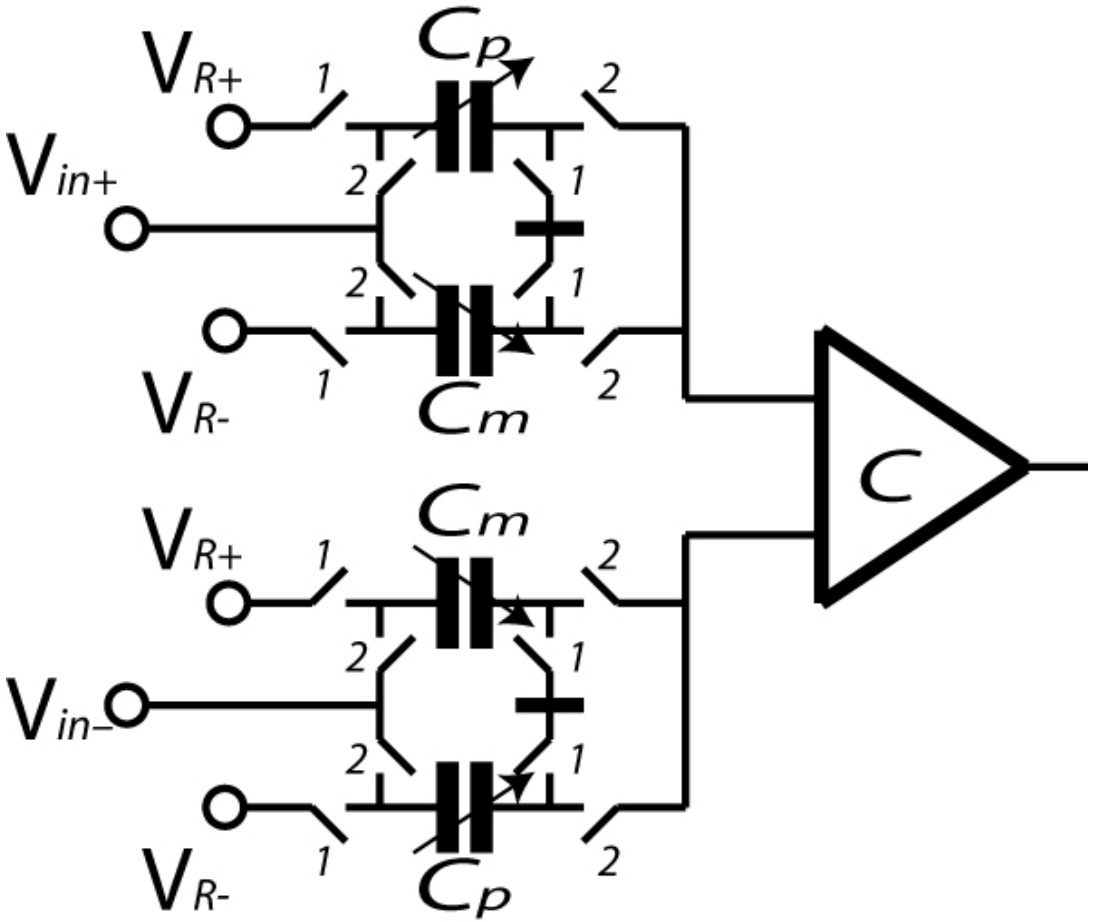


- V_{TH}=7 ➔ C_p = 7·C & C_m = 1·C
- V_{TH} =5 ➔ C_p = 5·C & C_m = 3·C
- V_{TH} =3 ➔ C_p = 3·C & C_m = 7·C

$$V_c(2) = V_{in} - \frac{C_p \cdot V_{R+} + C_m \cdot V_{R-}}{C_p + C_m} = V_{in} - \frac{C_p - C_m}{C_p + C_m} \cdot V_{R+}$$

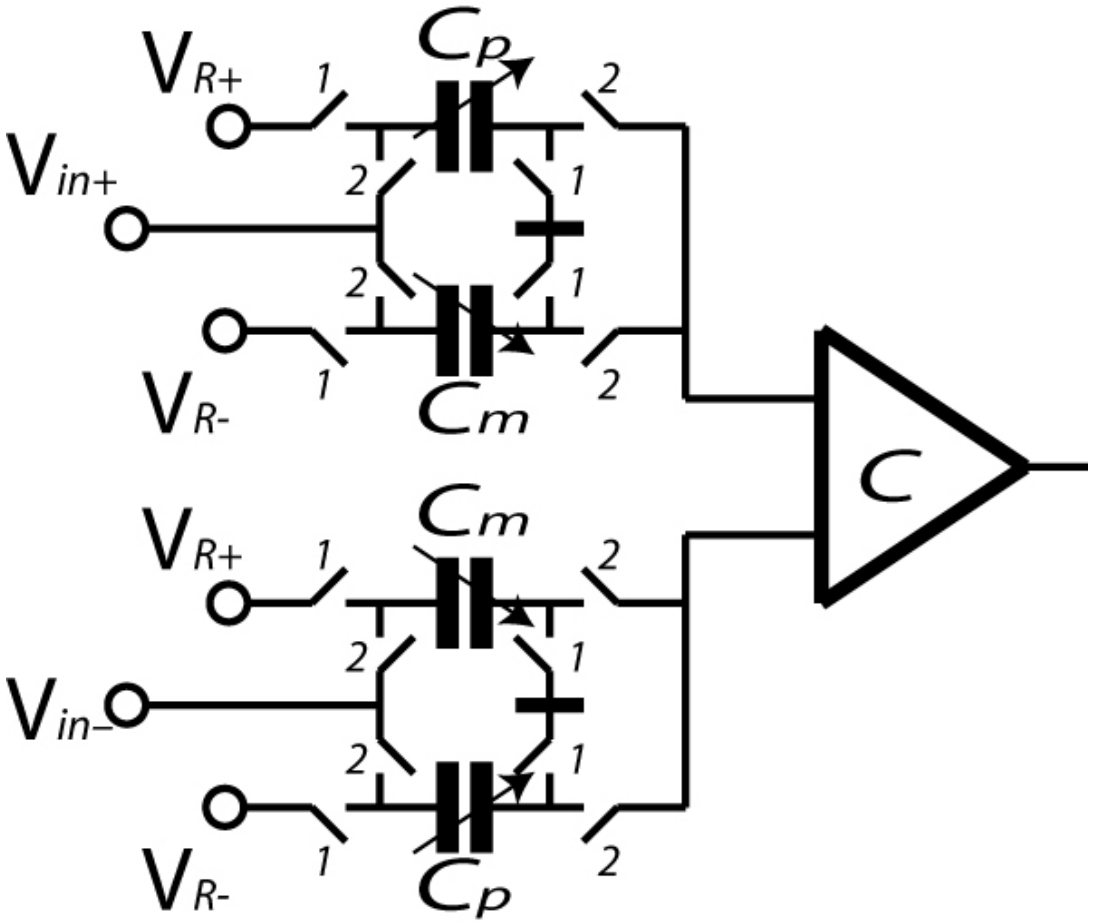
20b 250Hz Sigma-Delta ADC – Implementation

- Multibit ADC
- Fully-differential scheme



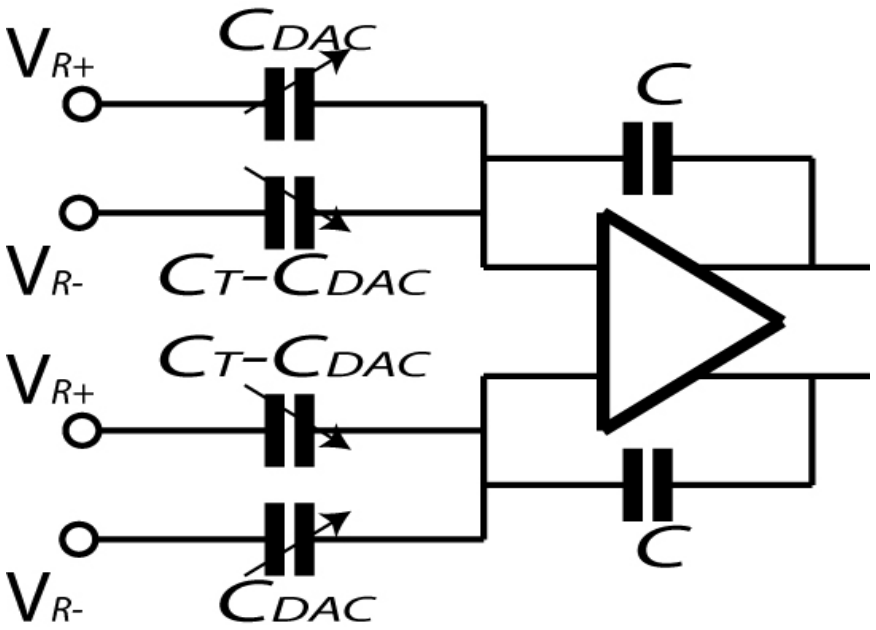
20b 250Hz Sigma-Delta ADC – Implementation

- Multibit ADC
- Fully-differential scheme



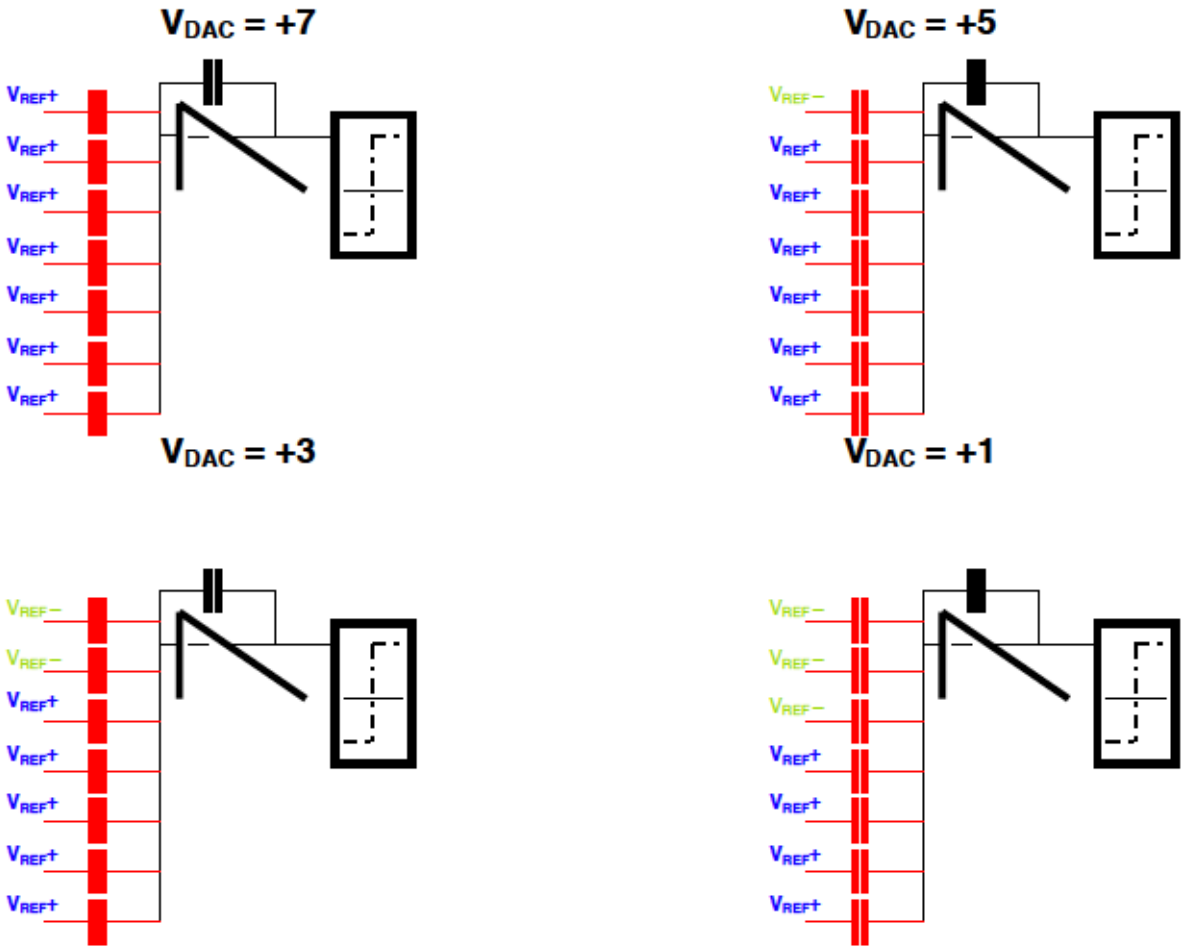
20b 250Hz Sigma-Delta ADC – Implementation

- Multibit DAC
- Fixed total opamp input capacitance
  - Independent on the input data
- Fixed total load for V_{R+} & V_{R-}
  - Independent on the input data



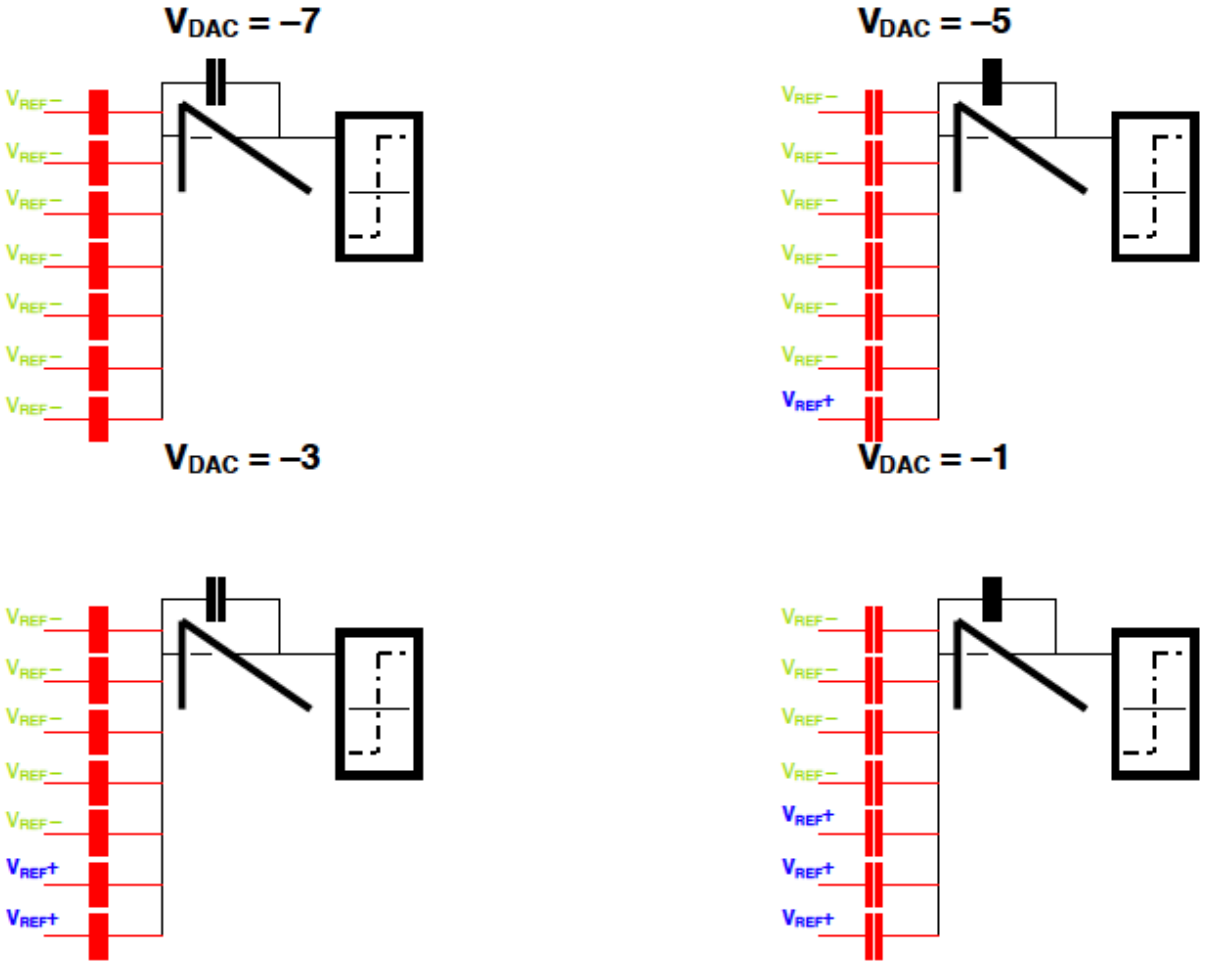
20b 250Hz Sigma-Delta ADC – Implementation

- Multibit DAC: 3bit operation example



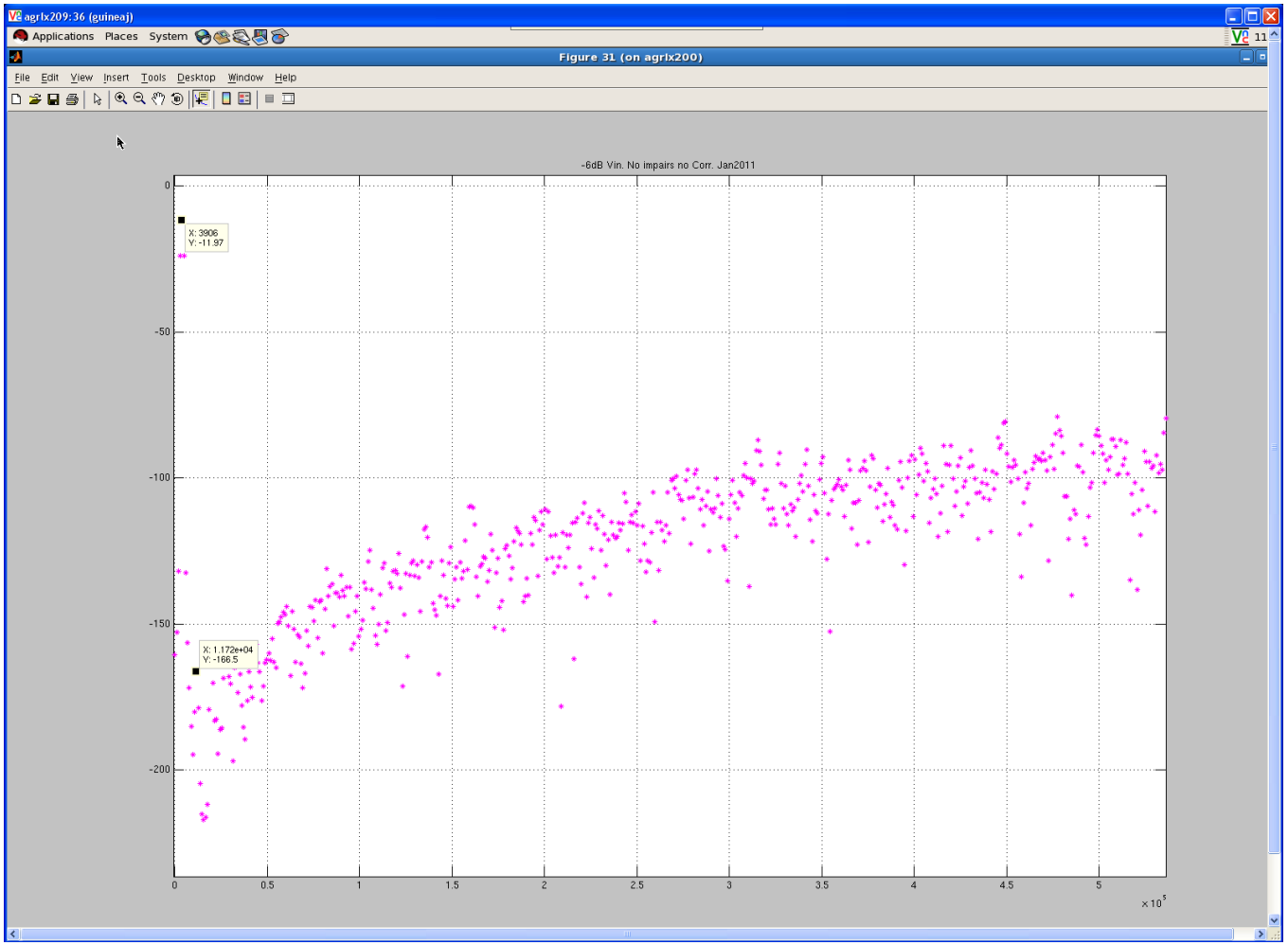
20b 250Hz Sigma-Delta ADC – Implementation

- Multibit DAC: 3bit operation example



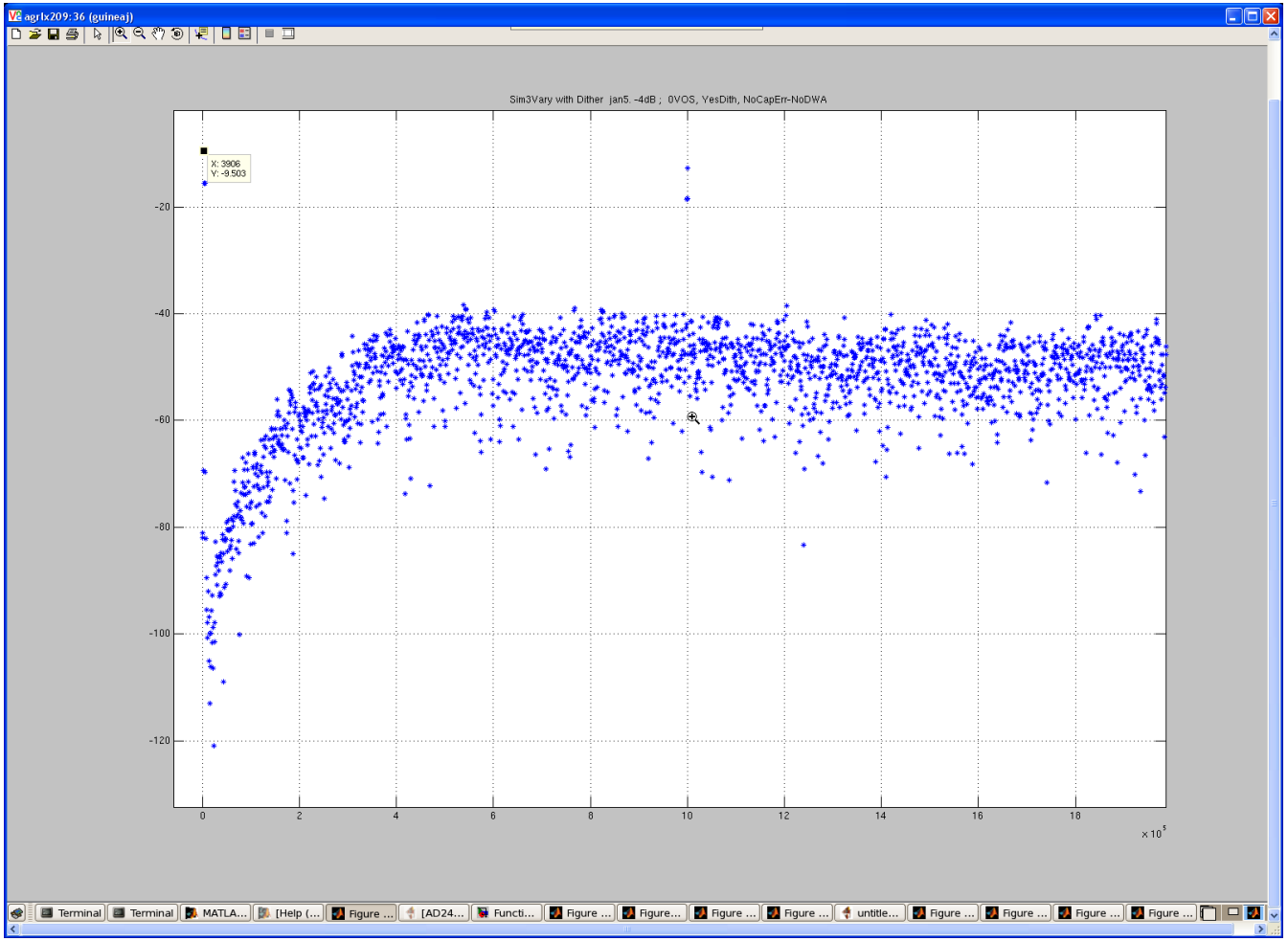
20b 250Hz Sigma-Delta ADC – Simulation

- A_{in}=-4dB$_{FS}$, Dither=NO



20b 250Hz Sigma-Delta ADC – Simulation

- A_{in}=-4dB$_{FS}$, Dither=**YES**



Overall System Power Consumption

	Current Consumption [µA]	Supply Voltage [V]	Power Consumption [mW]
Charge Amplifier	2200	3.3	7.3
Anti-Alias Filter	0	3.3	0
Drivers	672	5.0	3.4
Differential MDAC	353	3.3	1.16
ADC	890	3.3	3