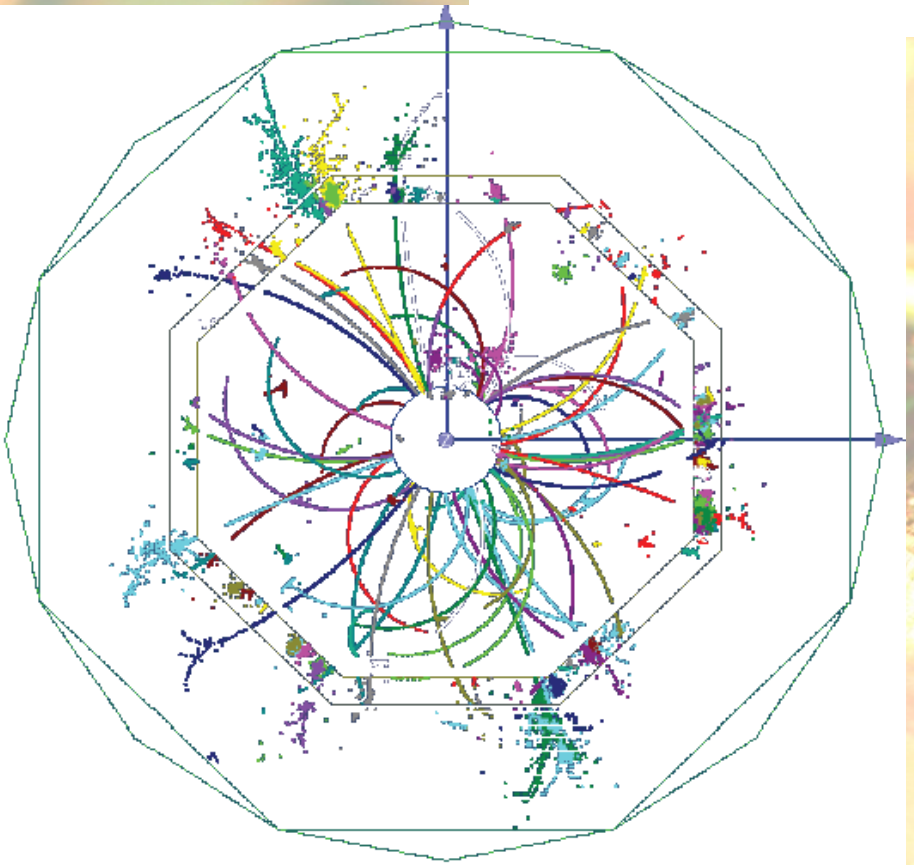
IN2P3

Omega



Design in 0.35µm

MUX meeting CERN 2011

C. de LA TAILLE

IN2P3

Taille@in2p3.fr

CNRS CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

IN2P3 INSTITUT NATIONAL DE PHYSIQUE NUCLÉAIRE ET DE PHYSIQUE DES PARTICULES

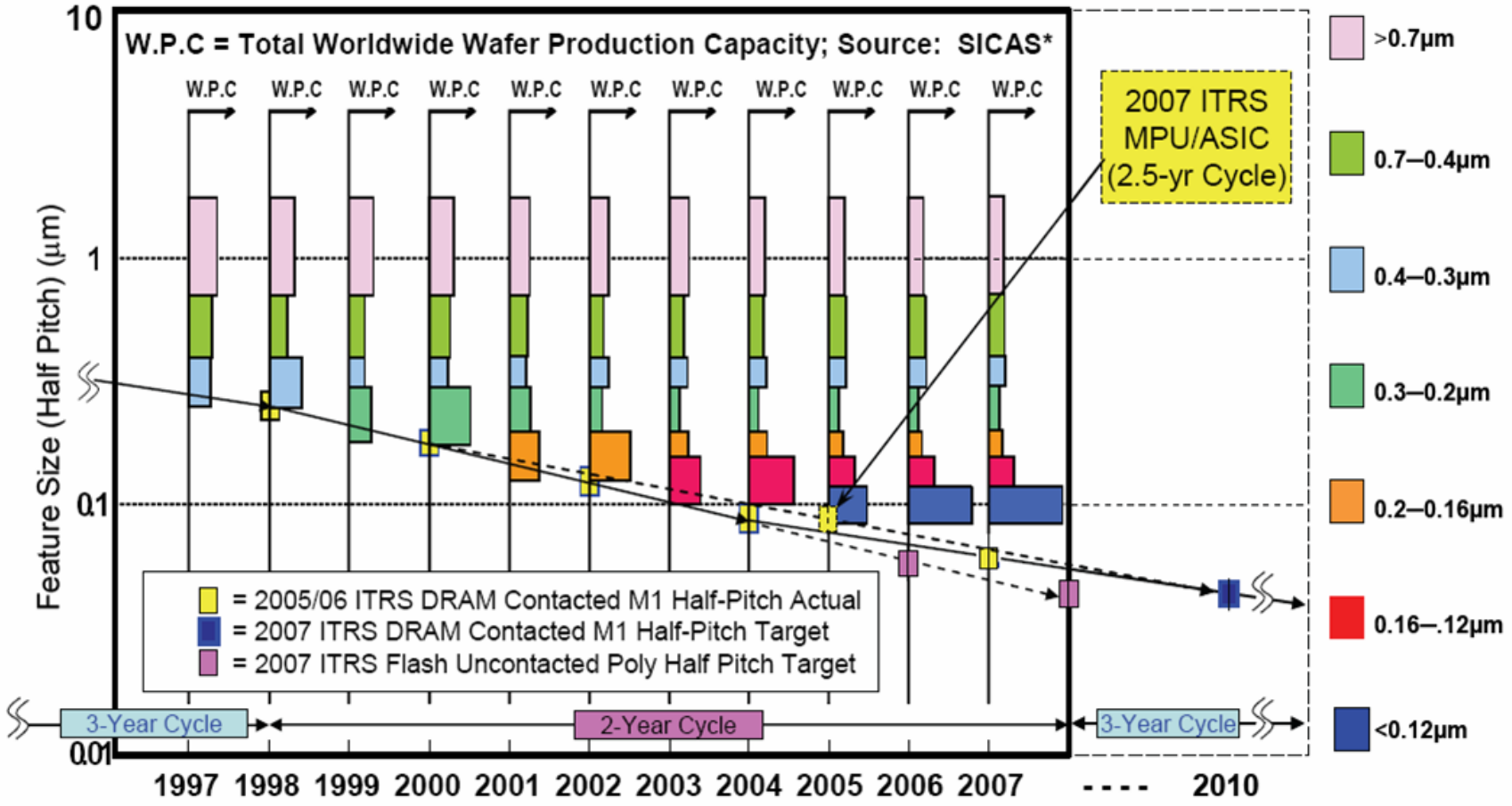
Orsay MicroElectronic Group Associated

Welcome to Jurassic 0.35µm park

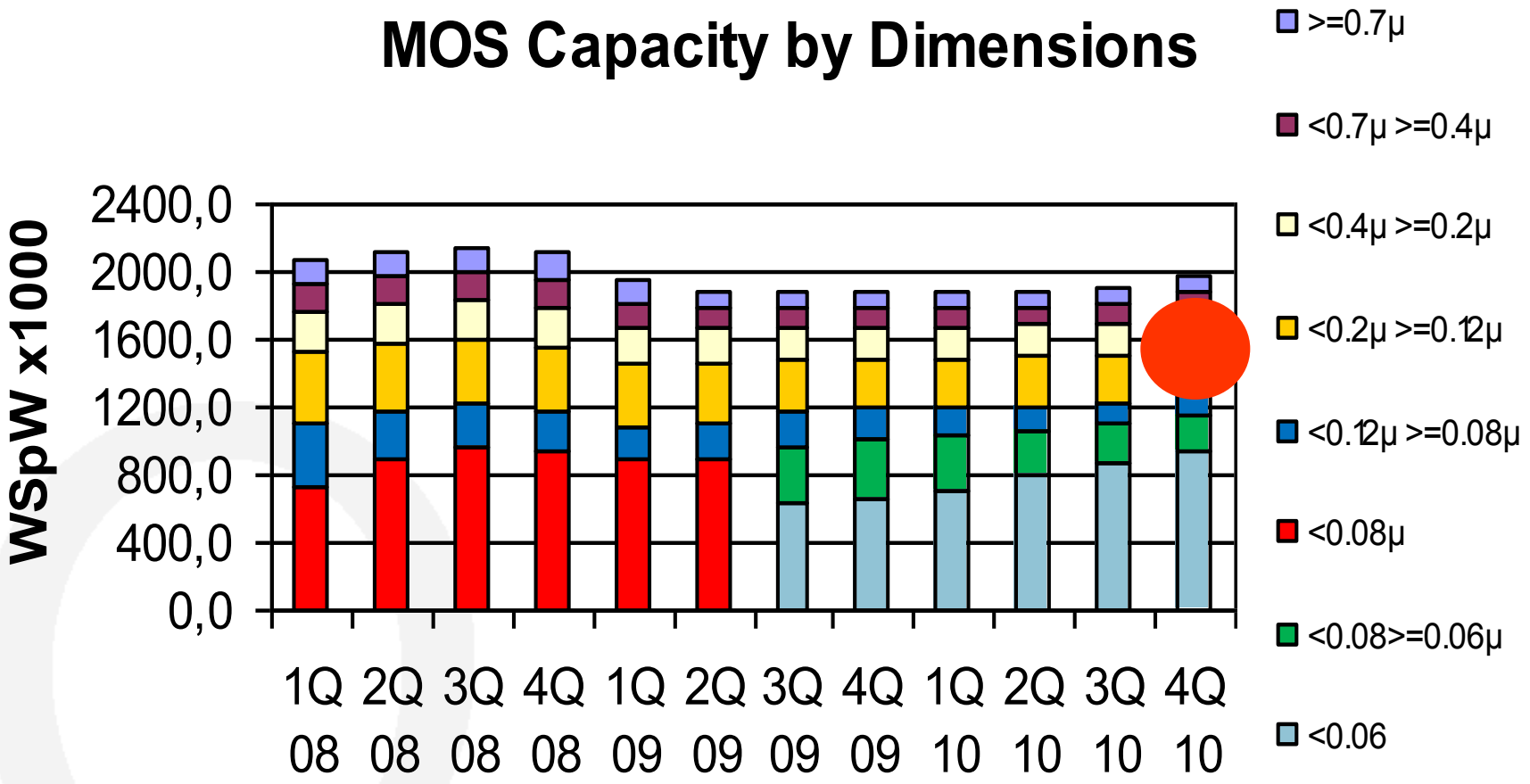
Still, many visitors !

Science & Technology
Facilities Council

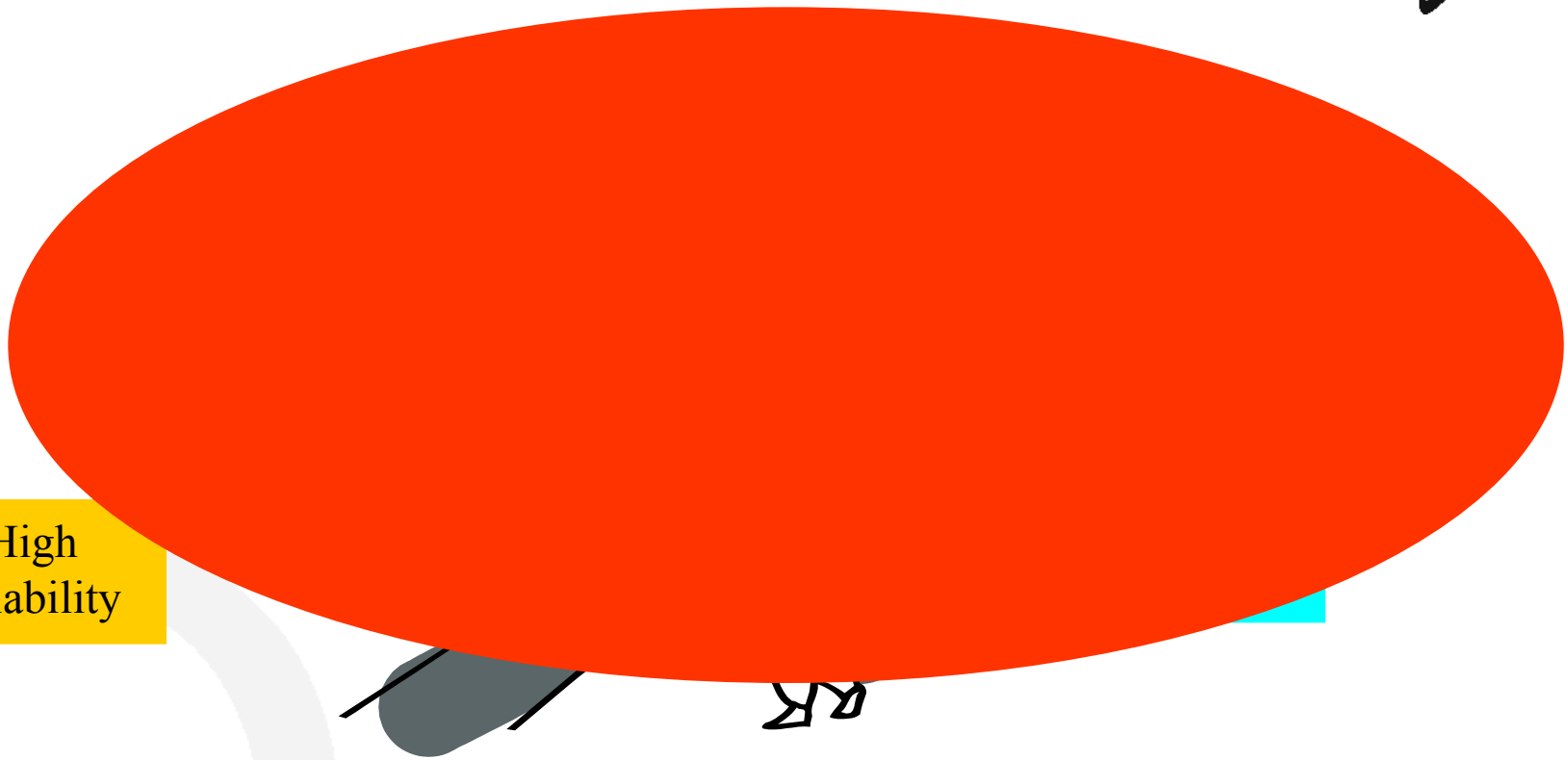
Semiconductor roadmap (SIA)



Semiconductor roadmap (detail 2008-10)



Readout electronics : requirements



High reliability

Radiation hardness

Low cost !
(and even less)

Low material

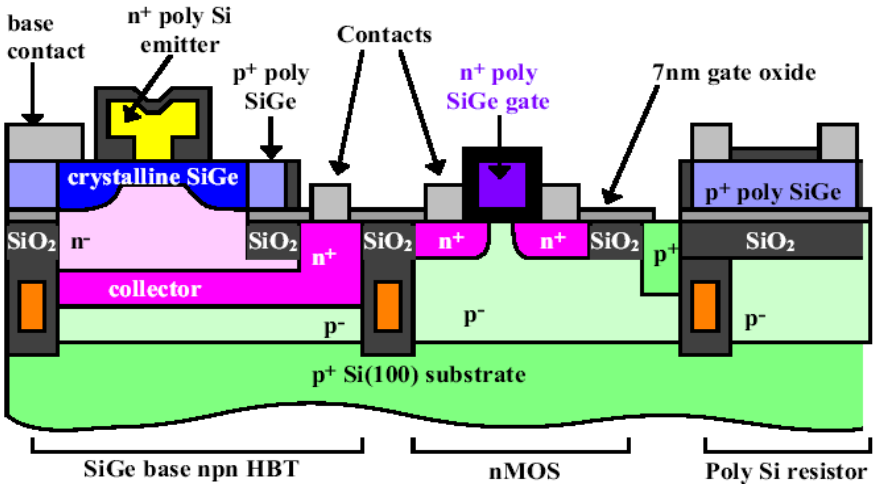
Motivations for design in 0.35 µm

- Solid state !

- Analog friendly
- Large dynamic range
- Low cost
- High speed with SiGe
- Low noise

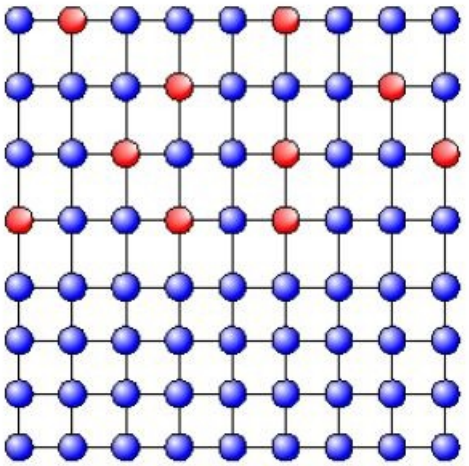
- Radiation tolerant (~Mrad)

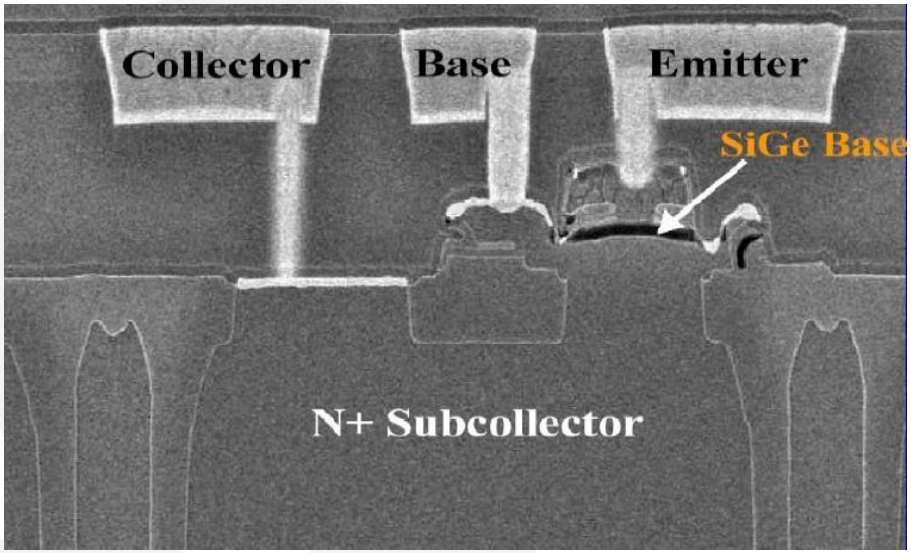
SiGe Bipolar in 0.35µm monolithic process

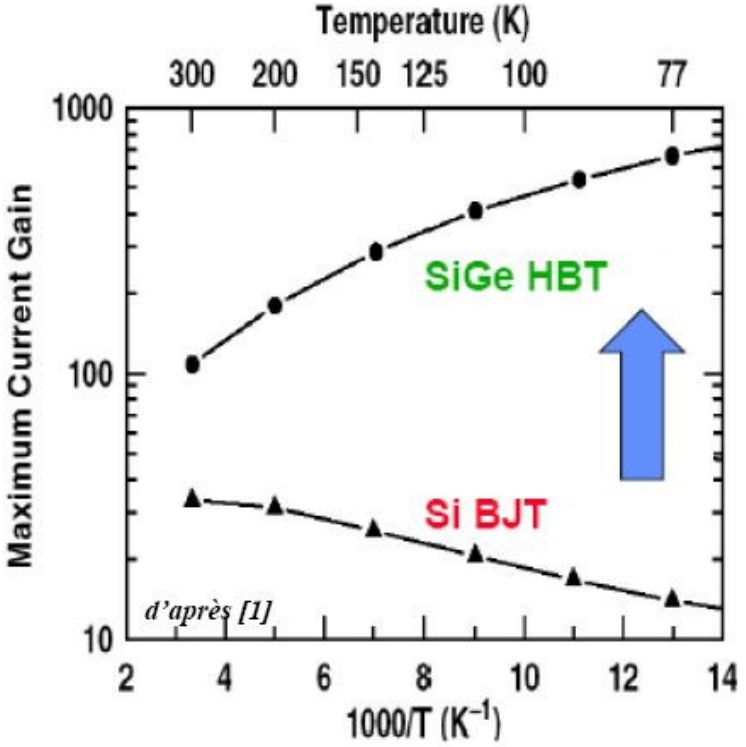


SiGe technology

- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-signal design

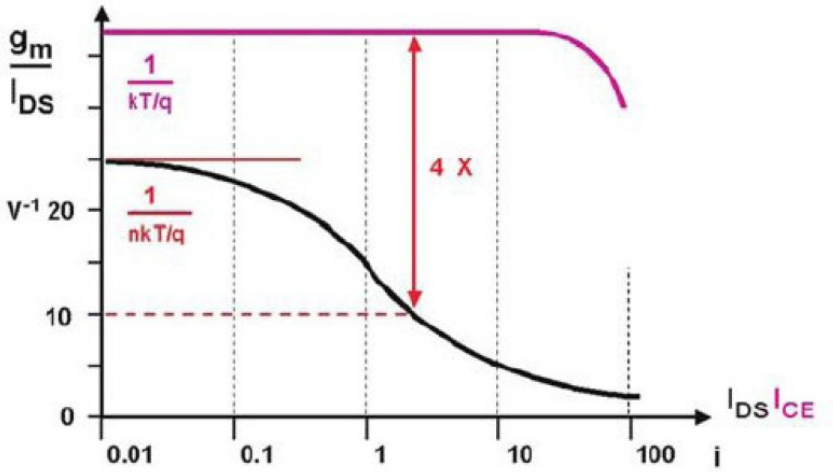


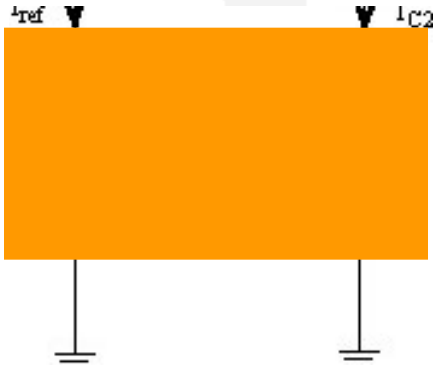


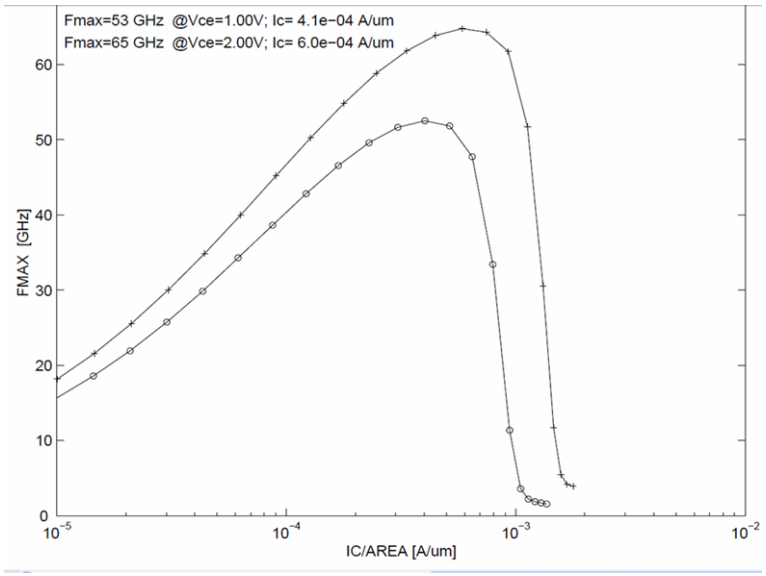


Power and speed with SiGe

- BJT : best g_m /I ratio $(1/U_T)$
  - Large transconductance with small devices
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and matching performance
- Large swing : V_{CEsat} ~3 U_T





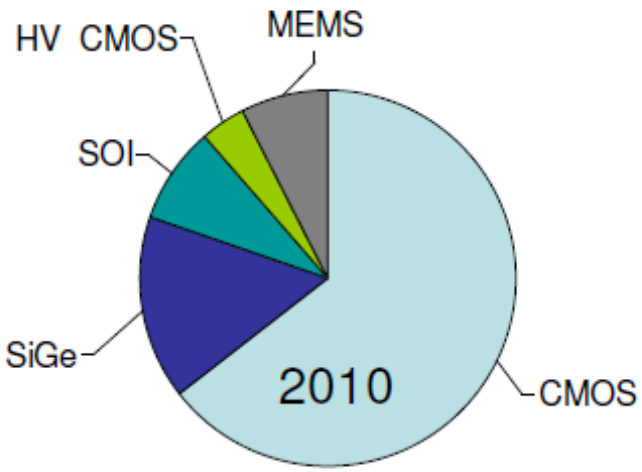


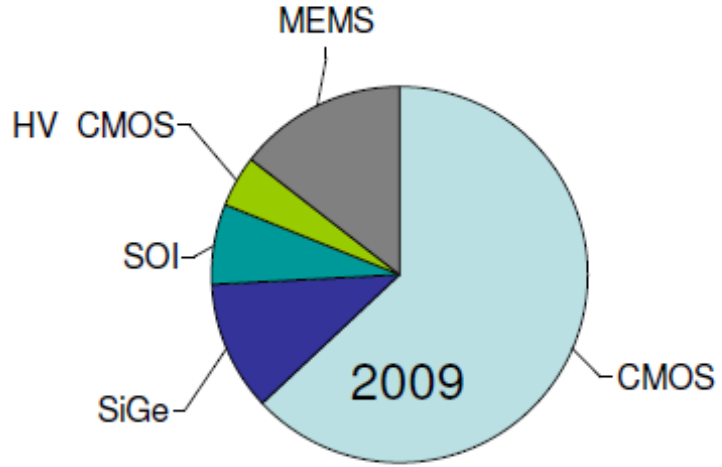
Example of prices, prototyping

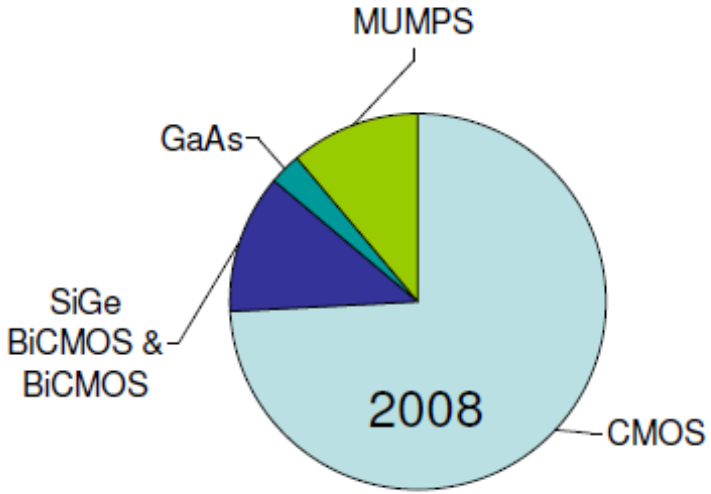
CMOS	.35 µ	AMS	650 €/mm²
CMOS opto	.35 µ	AMS	810 €/mm²
CMOS HV	.35 µ	AMS	1000 €/mm²
CMOS	130nm	ST	2200 €/mm²
CMOS	65 nm	ST	7500 €/mm²
CMOS	40 nm	ST	15000 €/mm²
SiGe BiCMOS	.35 µ	AMS	890 €/mm²
SiGe:C BiCMOS	130nm	ST	3500 €/mm²
SOI	130nm	ST	4000 €/mm²
SOI	65nm	ST	9500 €/mm²
Poly-SOI-Metal	MUMPS	MEMSCAP	3700 €/cm²

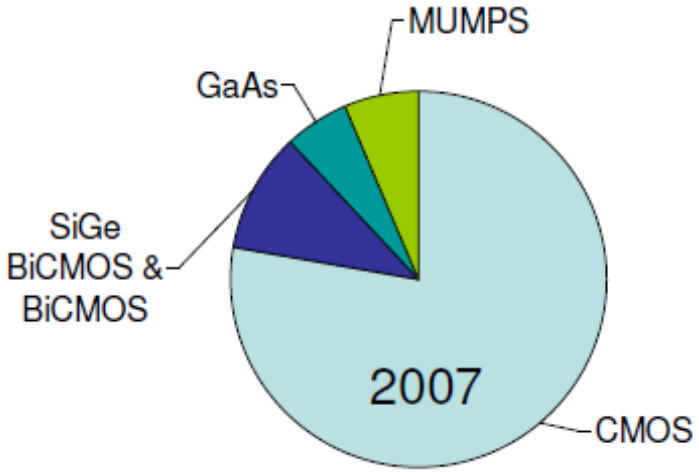
http://cmp.imag.fr/aboutus/slides/Slides2011/02_Runs_2011.pdf

Circuits per technology, evolution







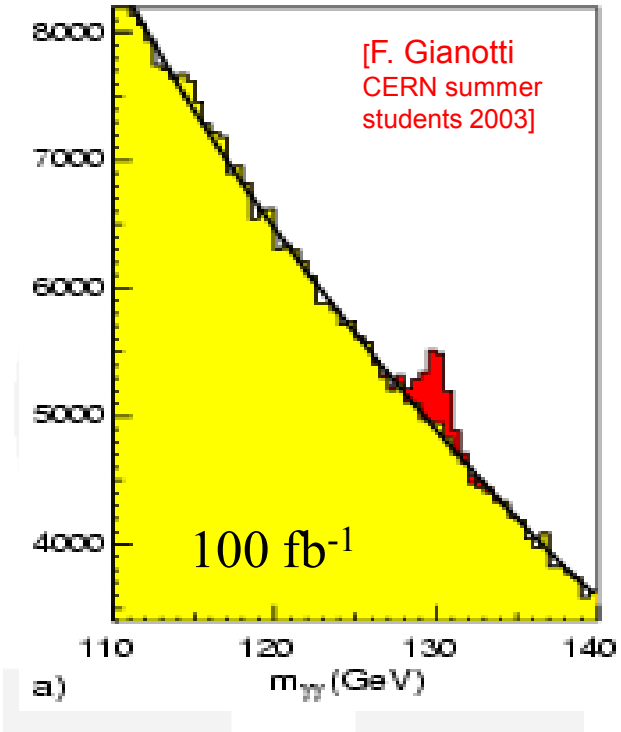


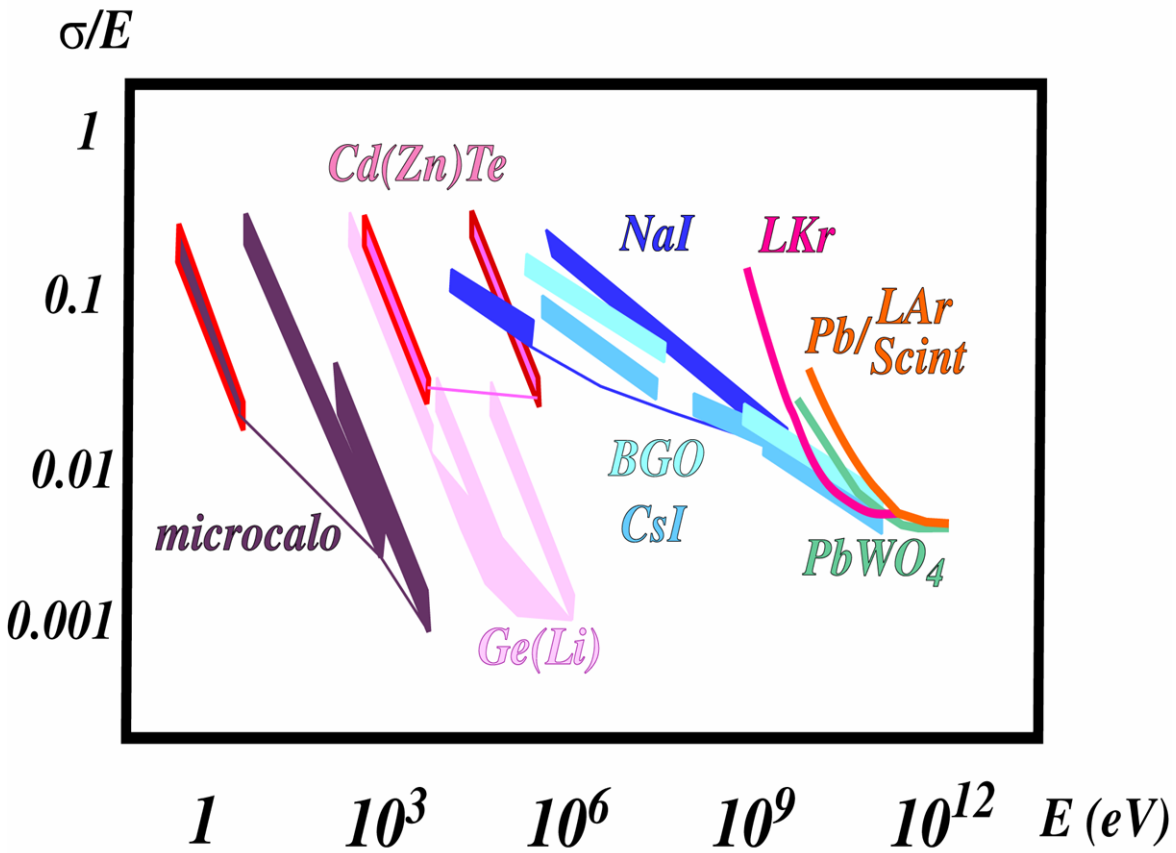
AMS 0.35 µm SiGe process

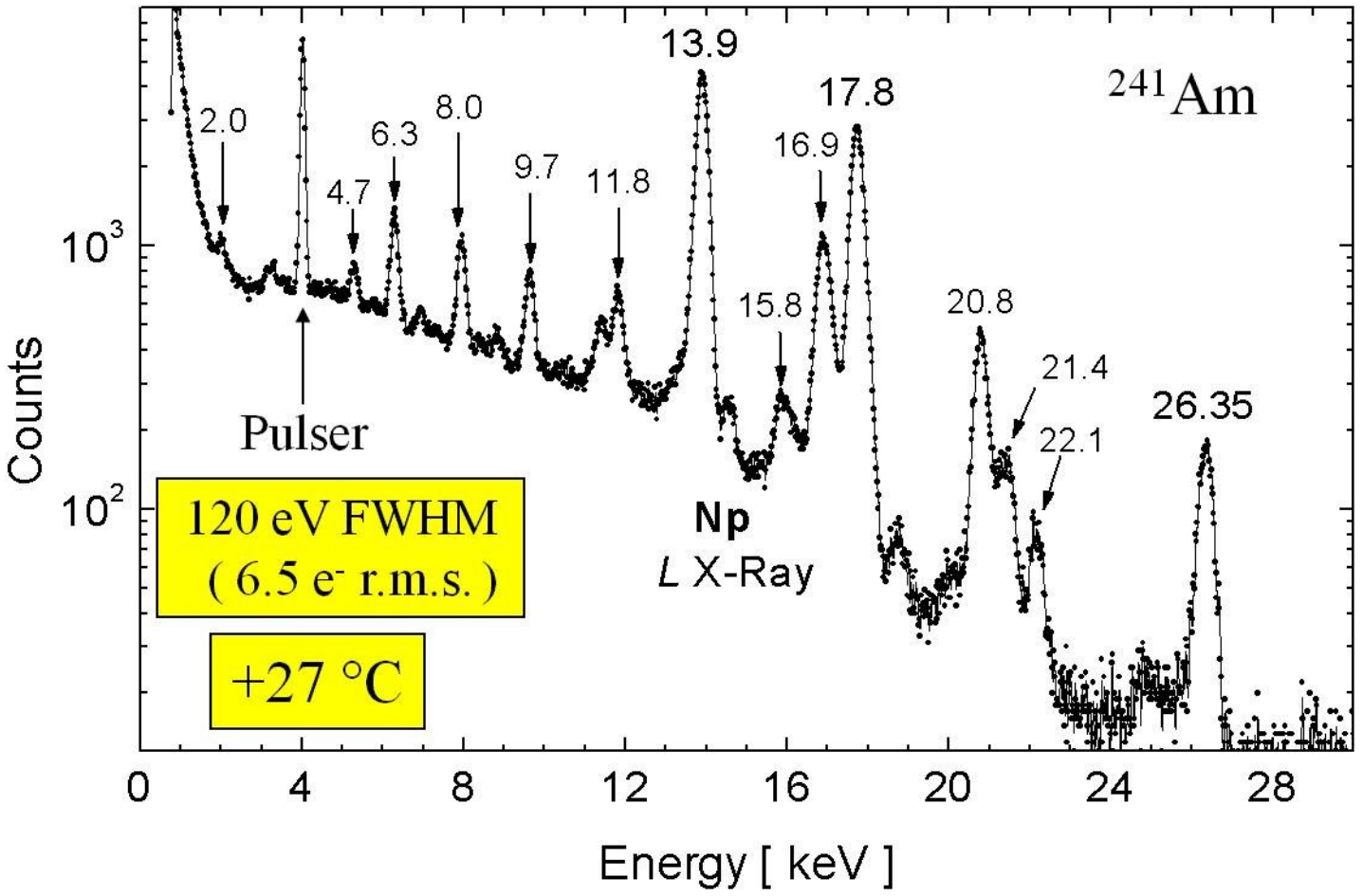
Process technology specifications	units	S35D4M5
Drawn MOS Channel Length	µm	0.35
Drawn Emitter Width	µm	0.4
Operating Voltage CMOS	V	3.3 and 5V
Number of Metal Layers	#	4
Number of Poly Layers	#	4
Substrate Type		p
Diffusion Pitch	µm	0.9
Metal1/2/3 Pitch	µm	0.95/1.1/1.2
Poly1 Pitch	µm	0.8
Thick Metal 4 pitch	µm	-
High Resistive Poly	kOhm/#	-
Poly1 / Poly2 Precision Caps	fF/µm²	0.9
Metal 2 / Metal 3 Precision Caps	fF/µm²	1.25
N/PMOS Active Channel Length	µm	0.30/0.30
N/PMOS Saturation Current	µA/µm	540/240
Gain	-	160
Early Voltage VAF	V	100
HS-HBT: BVceo	V	2.7
ft / fmax	GHz	60 / 70

Precision and dynamic range

- Dynamic range : maximum signal/minimum signal (or noise)
  - Typically : 10^3 – 10^5 for calorimetry or spectroscopy (10-16 bits)
- Precision/resolution : % level
- Precision and large dynamic range are key parameters for calorimeter electronics

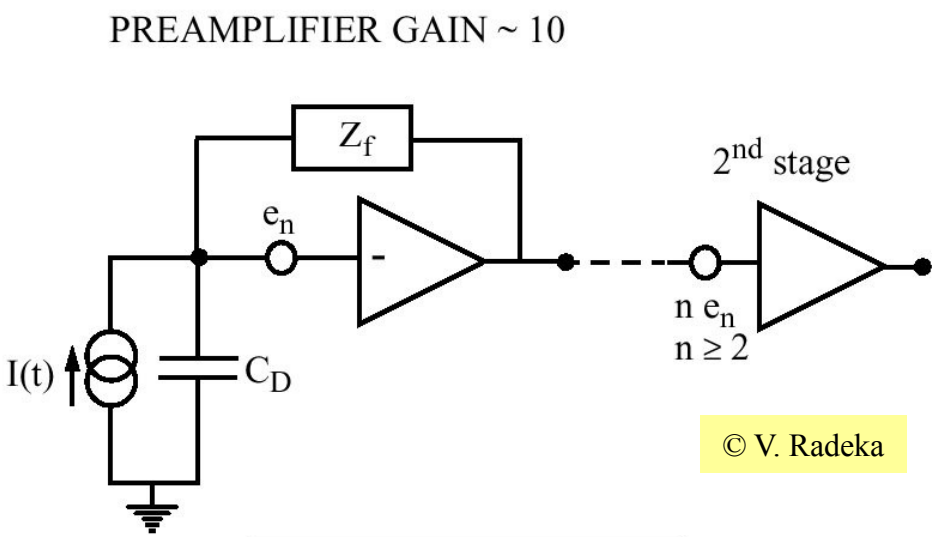


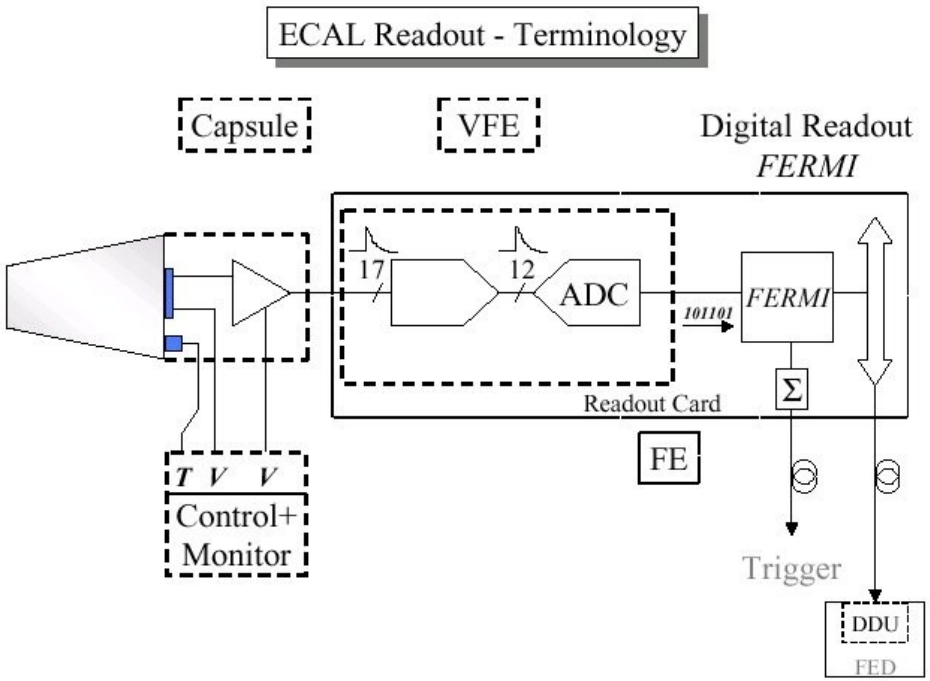




Dynamic range handling

- Maximum linear dynamic range : 16bits
  - Noise : v_n = 10 * 0.5 nV/√Hz * √10MHz = 30 µV
  - Max Signal : 2-3 V
  - Linear dynamic range : 10^5
- Classical handling of large dynamic range
  - Multi-linear
  - Well adapted to energy resolution
- Dynamic compression
  - Difficult with fast signals
  - Pulse shape variations
  - Bandwidth control





Examples of designs in 0.35 µm

http://dinamico2.unibg.it/feewk2011/Home.html

- 9 talks (/~40) involving 035µ
  - DC/DC converter (CERN)
  - MAPS : Mimosa 2* (Strasbourg), 4TMAPS (Heidelberg)
  - Spectroscopy (RAL)
  - Photon science : STARX32 (Milano) ASTEROID/VERITAS (MPI)
  - SiPM readout : SPIROC (Omega) BASIC32 (Bari) Rapsodi (Krakow)

http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=122027

DC/DC converters

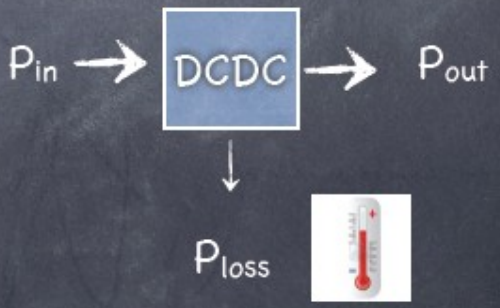
DC/DC ASIC design

Radiation tolerance:
- Technology choice
  - HV transistors (10V)
  - LV transistors (control circuit)
- Layout and design technique (ELT, triplications)

2007-2009	pre-selection of CMOS technologies with HV extension
2008-2010	design of prototypes in the two pre-selected technologies (0.25 and 0.35um)
2010	SEE tests on the two technologies led to selection of 0.35um

Design for high efficiency:

$$\text{efficiency} = \frac{P_{out}}{P_{in}}$$

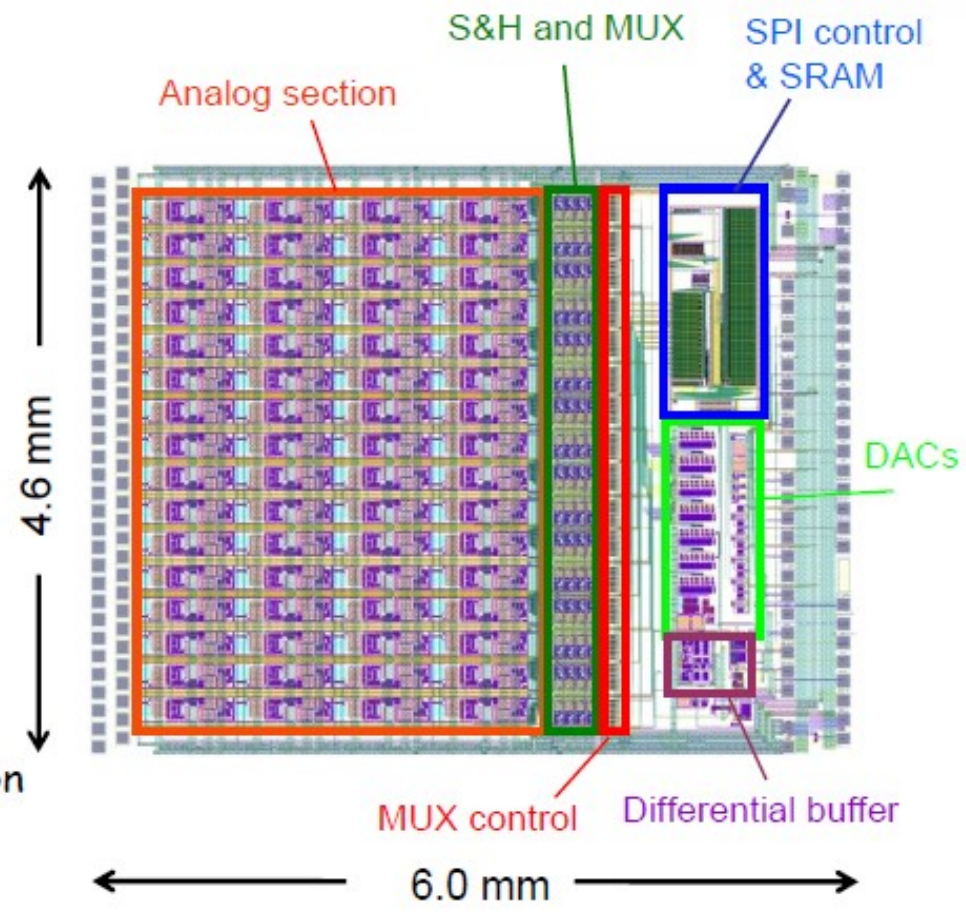


S. Michelis, PH-ESE-ME, CERN, FEE Workshop, Bergamo 2011

DEPFET Readout ASIC

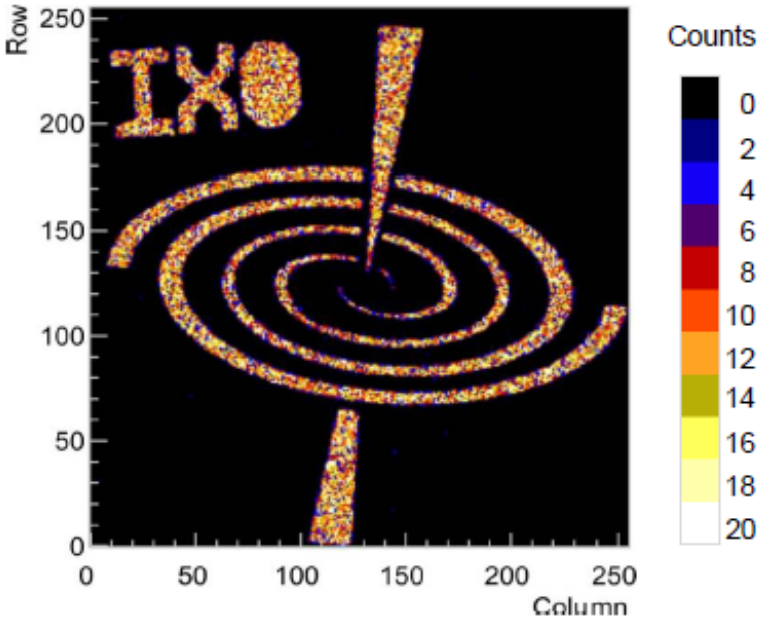
ASTEROID1.5

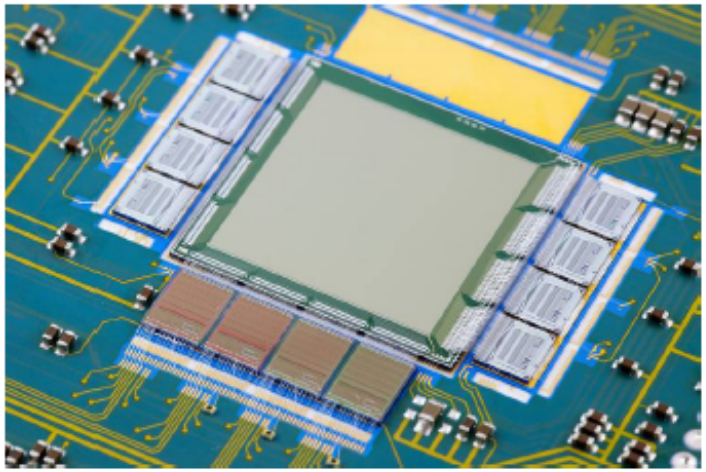
- AMS CMOS 0.35µm 3.3 V
- readout ASICs for DEPFET Pixel
- source follower readout
- 64 readout channels
- trapezoidal filter
- readout speed 4-6 µs
- selectable gain settings
- electronic noise < 2e
- dynamic input range: ca. 25keV
- MUX 64:1 @16 MHz with window-mode operation and power switching
- bias DACs
- DICE SRAM (radhard) for internal sequencing and configuration
- system-friendly single test feature
- system-friendly SPI slow control interface
- P/ch= ca. 8mW



in cooperation with
Politecnico di Milano
Milano, Italy

DEPFET XL Measurements





DEPFET PIXEL

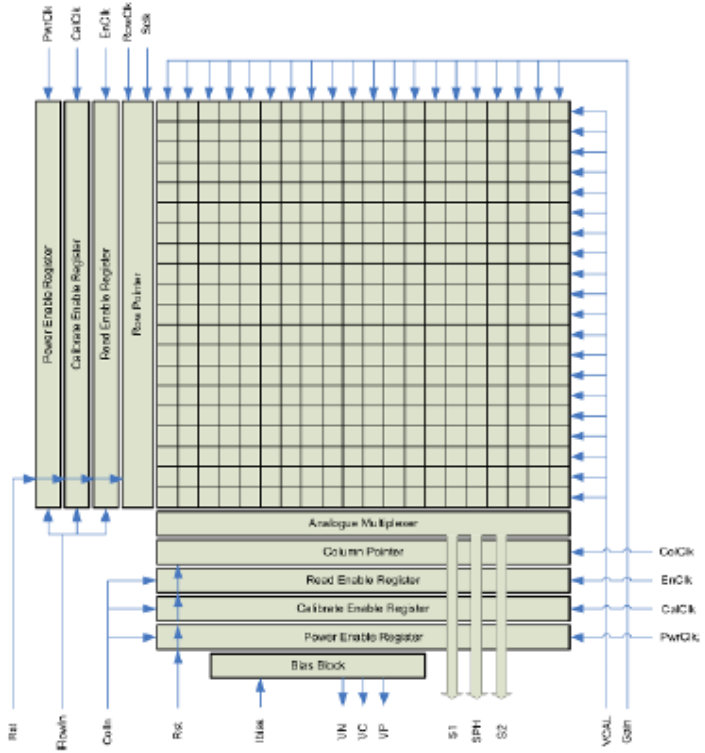
- 256 x256 pixels of 75μm x 75μm
- 450μm fully depleted silicon
- backside illuminated
- readout speed:

  6.4μs per row (1.6ms per frame)
- 4 Asteroid / 8 SWITCHER ASICs

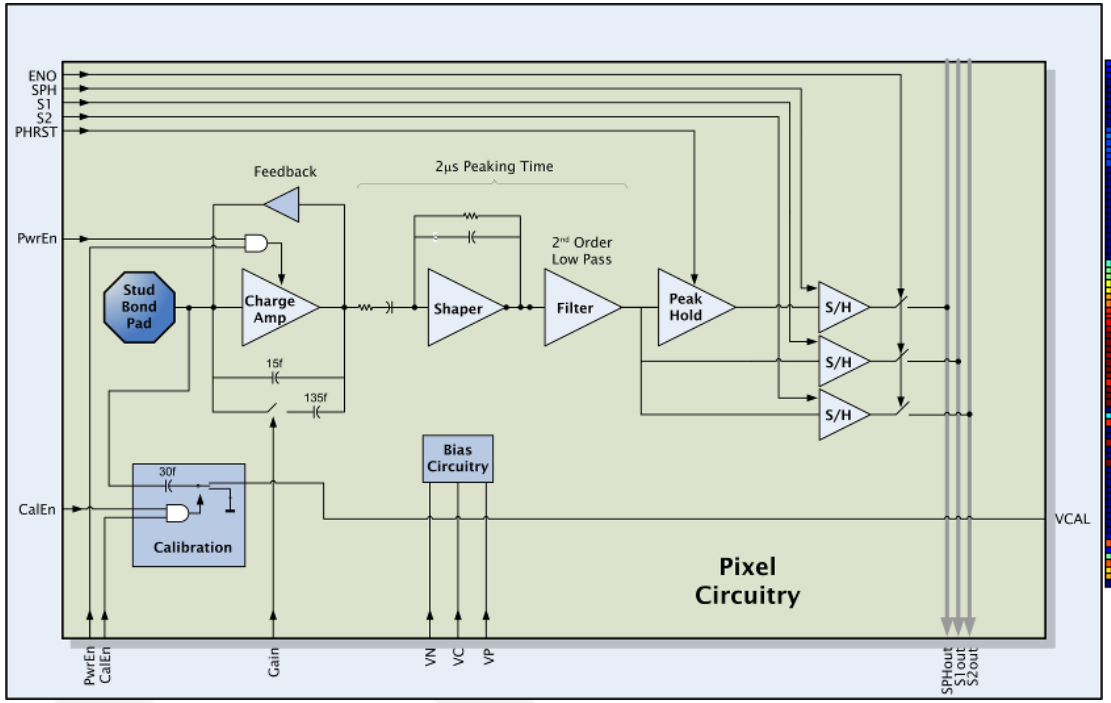
Science & Technology Facilities Council
Technology

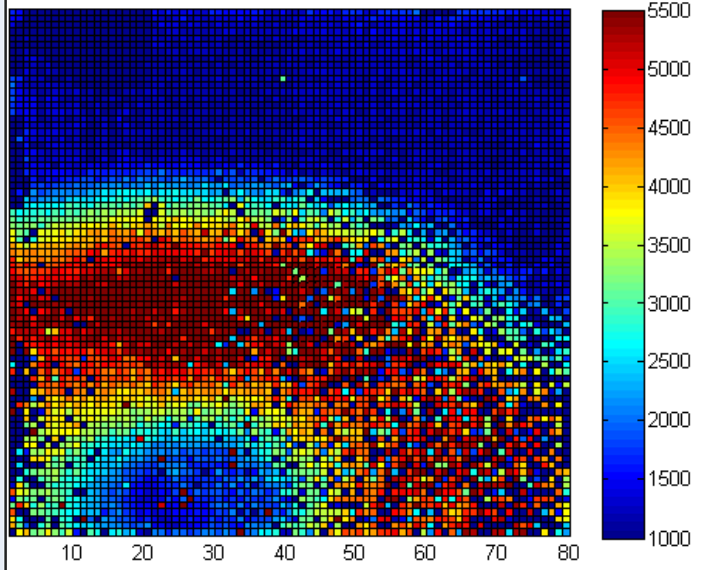
3D-ASIC development

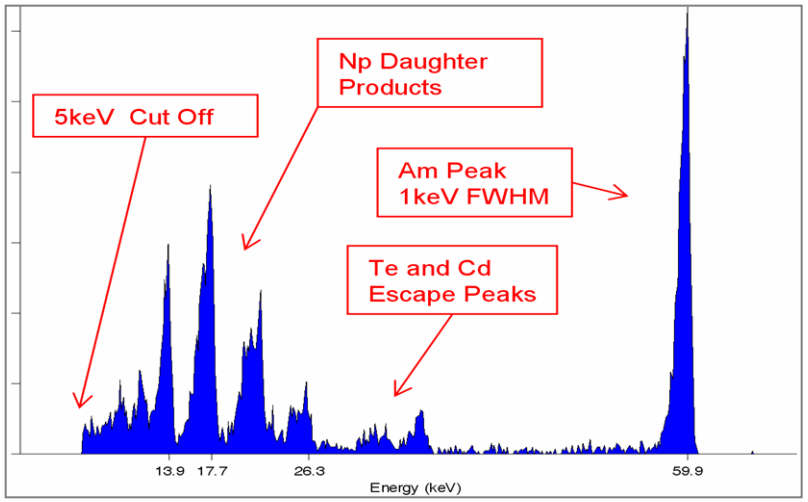
Cd(Zn)Te Spectroscopy ASIC



- Rolling shutter type readout
- Four 80x20 pixel arrays on one ASIC
- 250mm x 250mm pixels
- Gold stud bonded to CZT
- Programmable regions of interest
- 12 Analogue outputs
- Selectable range 150keV - 1500keV
- Noise <1keV FWHM with CZT detector
- AMS 0.35um CMOS


ENO
SPH
S1
S2
PHRST
PwrEn
CalEn
Feedback
2µs Peaking Time
2nd Order Low Pass
Stud Bond Pad
Charge Amp
Shaper
Filter
Peak Hold
S/H
S/H
S/H
15f
135f
30f
Calibration
Bias Circuitry
VCAL
Pixel Circuitry
PwrEn
CalEn
Gain
VN
VC
VP
SPHout
S1out
S2out


5500
5000
4500
4000
3500
3000
2500
2000
1500
1000
10
20
30
40
50
60
70
80


5keV Cut Off
Np Daughter Products
Am Peak 1keV FWHM
Te and Cd Escape Peaks
13.9
17.7
26.3
59.9
Energy (keV)

STARX-32: a 3 cm^2 Mixed Signal ASIC with Spectroscopic-Grade Front-End and on-chip Parallel A/D Conversion for High Speed X-Ray Imaging with Semiconductor Pixel Detectors

Giuseppe Bertuccio
on behalf of LFDR team

Politecnico di Milano - Como Campus
Department of Electronics Engineering and Information Science
and National Institute of Nuclear Physics (INFN)
Milan, Italy

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 56, NO. 3, JUNE 2009 1511

Noise Minimization of MOSFET Input Charge Amplifiers Based on $\Delta\mu$ and ΔN $1/f$ Models

Giuseppe Bertuccio and Stefano Caccia

***Abstract*—The optimization of the noise performance of integrated complementary metal–oxide semiconductor (CMOS) charge amplifiers is studied in detail considering accurate $1/f$ noise modeling for the input metal–oxide semiconductor field-effect transistor (MOSFET) biased in a strong inversion-saturation region. This paper aims to generalize and correct previously published analyses which have been based on two limiting and sometimes not applicable assumptions: a fixed MOSFETs bias current and the general validity of the McWhorter $1/f$ noise model. This study considers the two main $1/f$ noise models: 1) the mobility fluctuation, known as $\Delta\mu$ or Hooge model, which is followed by p-channel MOSFETs and 2) the carriers number fluctuation, also known as ΔN or McWhorter model, which is applicable only for n-channel MOSFETs. The front-end noise optimization is made with the $1/f$ component alone, thus determining the ultimate performance, and also considering the presence of series and parallel white noise sources. It is shown that different design criteria are valid of p- or n-channel MOSFETs: the $\Delta\mu$ model results in an optimum bias current and a different optimum gate width with respect to ΔN model. Two-dimensions suboptimum noise minimization criteria are derived when power or area constraints are imposed to the circuit design. Starting from experimental data on CMOS 1/f noise, examples of application of the presented analysis are shown to predict the lower limits of the $1/f$ noise contribution for the currently available CMOS technologies.**

***Index Terms*—Charge amplifier, complementary metal–oxide semiconductor (CMOS) integrated circuit (IC), integrated circuits (ICs), low-noise circuit, 1/f noise.**

amplifier concept for radiation detector readout [3], a large variety of implementations have been studied and developed involving all types of front-end devices and technologies (junction field-effect transistor (JFET), metal semiconducor field-effect transistor (MESFET), high-electron mobility transistor (HEMT) , bipolar junction transistor (BJT), metal-oxide semiconductor field-effect transistor (MOSFET)) in order to maximize performance in terms of speed, noise, power consumption, or chip area. In the last five years, intense attention has been given to the design of charge amplifiers implemented in CMOS technologies because of their advantages in terms of high integration density, low power consumption, wide bandwidth and digital logic integration, as required in many applications.

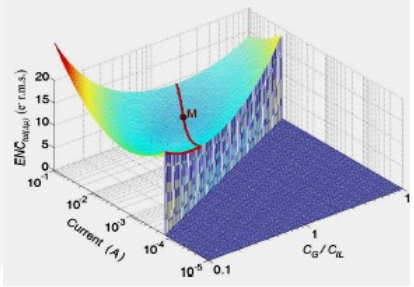
The most common objective in CSA design is the minimiz tion of the equivalent noise charge (ENC), which requires careful design of the input stage. In particular, the $1/f$ noi associated with the drain current of the input device plays major role in ultra low-noise design, as recently demonstrat with CSA with noise levels of a few electrons root mean squa (rms) [4].

Previous works have studied the noise optimization of CMC CSA but with two restrictive and sometimes not applicable a sumptions: 1) a fixed bias current of the input MOSFET, main determined by power consumption or bandwidth constraints a 2) the general validity of the McWhorter $1/f$ model (see ne section) [5]–[10]. In our analysis, we remove both of these a

$$ENC^2_{1/f(\Delta\mu)} = 2\pi A_2\left(\frac{n\alpha_H L}{q\sqrt{2\mu}}\right)\left[\frac{(C_{IL}+C_G)^2}{\sqrt{C_G^3}}\right]\sqrt{I}$$

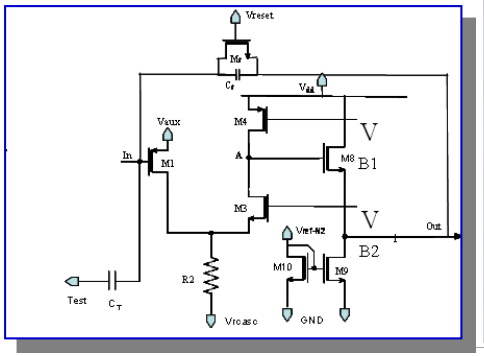
$$ENC^2_{1/f(\Delta N)} = 2\pi A_2\left(\frac{nkTN_T}{2\gamma C_{ox}^2}\right)\left[\frac{(C_{IL}+C_G)^2}{C_G}\right]$$

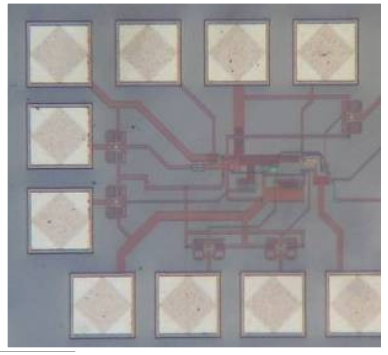
$$I \geq I_{\min} = R_{\min} I_S,$$

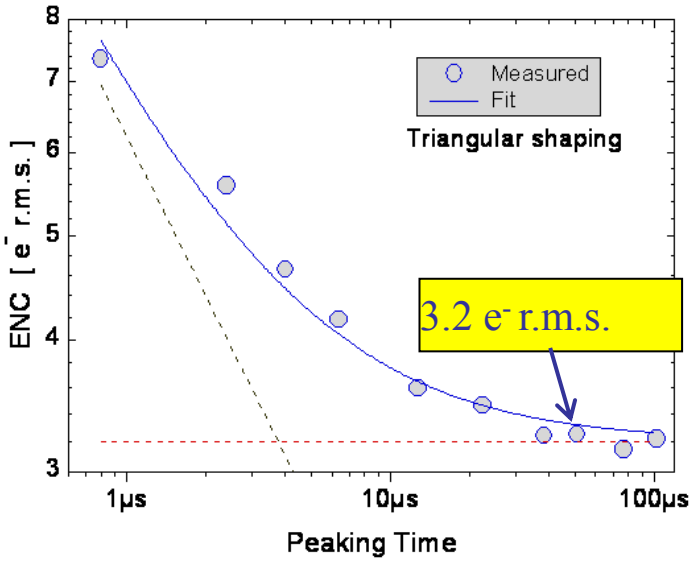


$$\begin{cases} ENC^2_{tot(\Delta\mu)} = k_{ws}\frac{(C_{IL}+C_G)^2}{\sqrt{C_G}}\frac{1}{\sqrt{I}}\frac{1}{\tau} \\ \quad + k_{\Delta\mu}\frac{(C_{IL}+C_G)^2}{\sqrt{C_G^3}}\sqrt{I} + k_{up}\tau \\ I \geq R_{\min} I_S \end{cases}$$

G. Bertuccio , S. Caccia
IEEE Trans. Nucl Sci. 56, 2009, pp. 1511

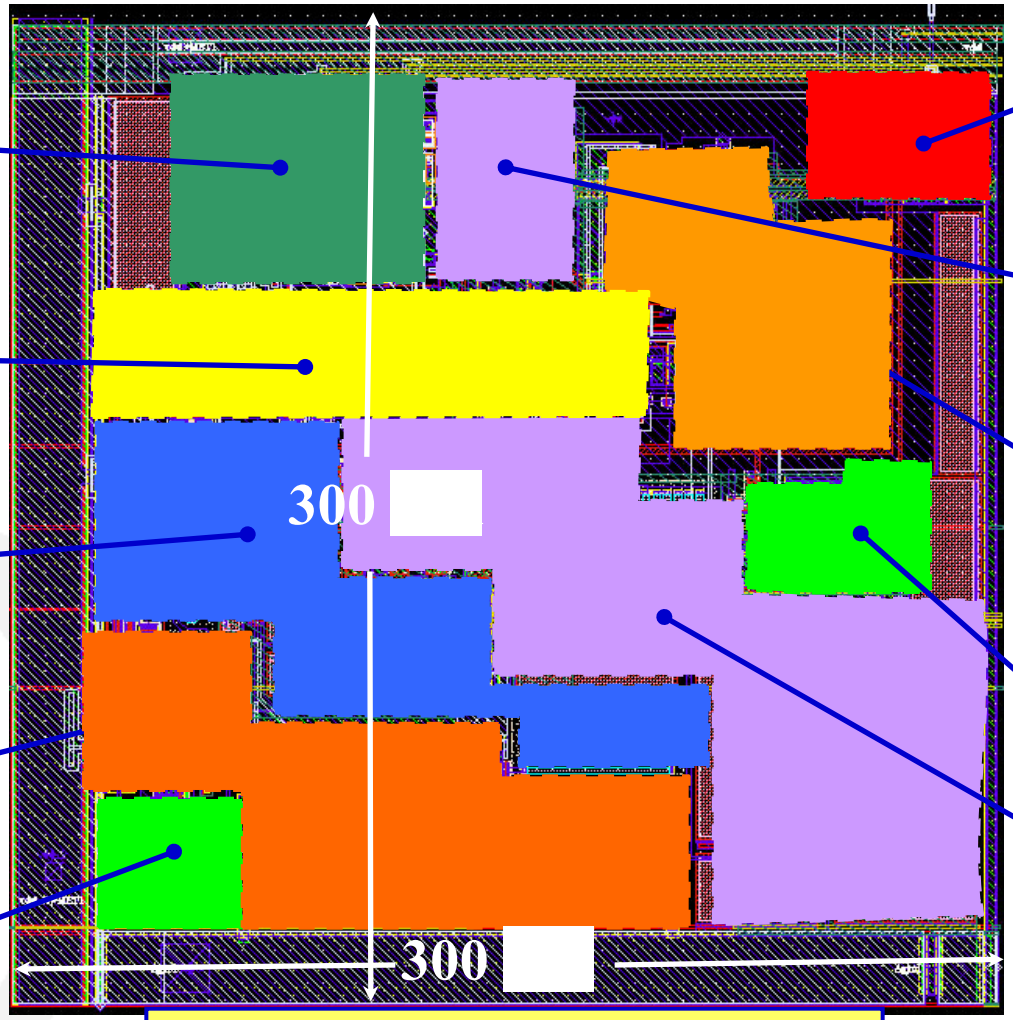






G. Bertuccio et al., NIM, A 579, 2007, pp. 243

Readout Pixel Cell Layout



Reset/PUR Logic
+Trigger Trasm.
<< 1 µW

Amplitude
Discriminator
37 µW

Shaper 1st
98 µW

Charge
Preamplifier
115 µW

Input Pad
Ø=35 □m

Output Buffer
49 µW

Peak
Discriminator
21 µW

Peak Stretcher
35 µW

DC stabilizer

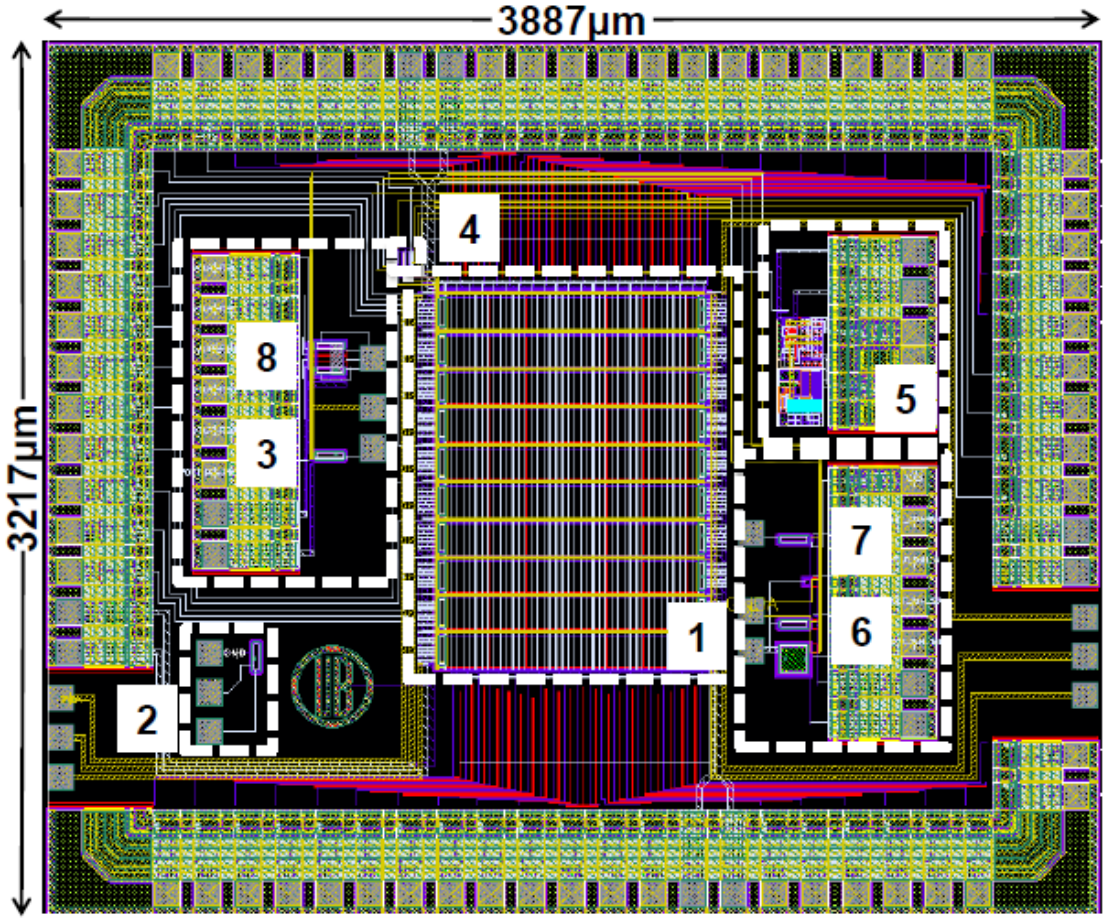
Shaper 2nd
71 µW

Total Power Consumption: 483 □W

GAPDs in AMS 0.35 HV

UNIVERSITAT DE BARCELONA

Short term plans towards the use of APDs in a tracker for ILC
FLC_APD_v1 - AMS R3



1. 10 x 43 GAPD array
2. Test photodiode
3. Test pixel
4. Control signal generation circuit
5. Pad LVDS
6. Active inhibit pixel
7. Current mode pixel
8. 1 x 5 GAPD array with PAD layer

8th Int. Meet. on Front-End Electronics – Bergamo 24-27 May 2011
Angel Diéguez – University of Barcelona

ICCUB

Department of Electronics
Universitat de Barcelona

SiPM readout chips

Chip name	group	year	Technology	channels	Application
FLC_SiPM	Orsay	2004	BiCMOS 0.8µm	18	ILC HCAL
NINO	CERN	2004	CMOS 0.18µm	8	ALICE TOF
MAROC2	Orsay	2006	SiGe 0.35µm	64	ATLAS lumi
SPIROC	Orsay	2007	SiGe 0.35µm	36	ILC HCAL
PETA	Heidelberg	2008	CMOS 0.18µm	40	PET
RAPSODI	Krakow	2008	CMOS 0.35µm	2	Snooper
BASIC	Bari	2009	CMOS 0.35µm	32	PET
SPIDER	Ideas	2009		64	Spider rcih

Club building blocks 0.35µm

- Mission :

  Design of basic building blocks usable by all in2p3 labs for physics experiments

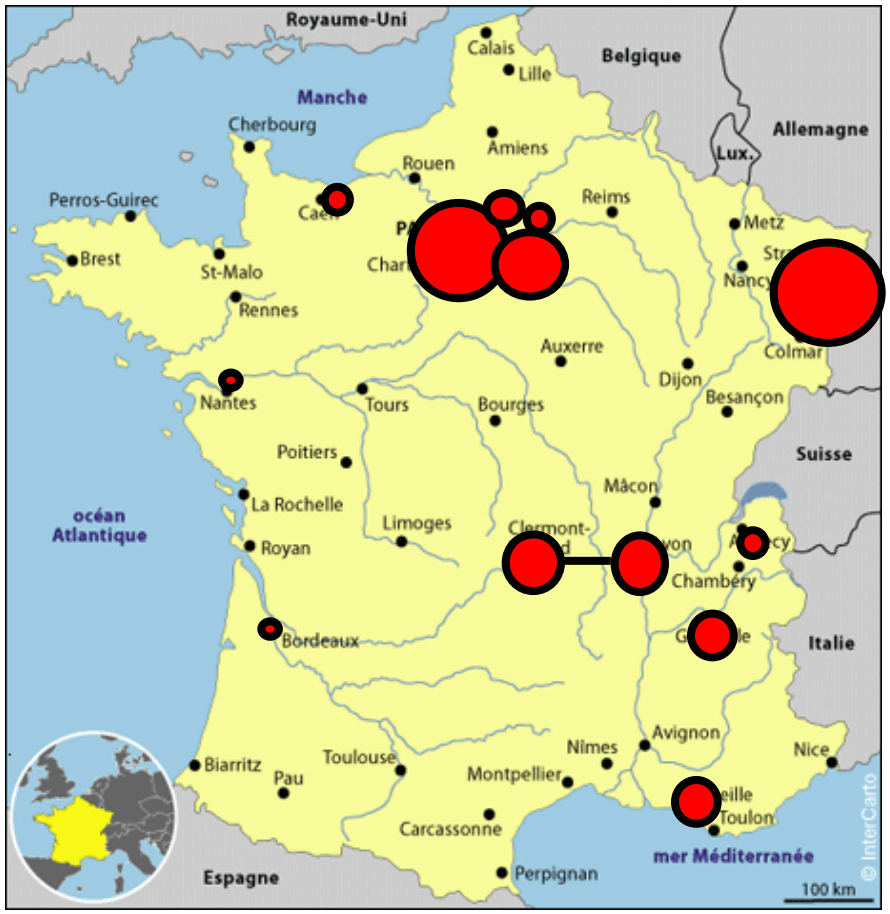
- Motivations
  - Target analog technology (0.35µm SiGe AMS)
  - Optimize ressources and competences within in2p3
  - reduce developpement times
  - Increase visibility of in2p3 in microelectronics

- First results
  - 2-3 runs /yr financed by in2p3
  - Porquerolles workshop
  - Fruitful exchanges
  - Now extended to IBM 130 nm

Microelectronics at IN2P3

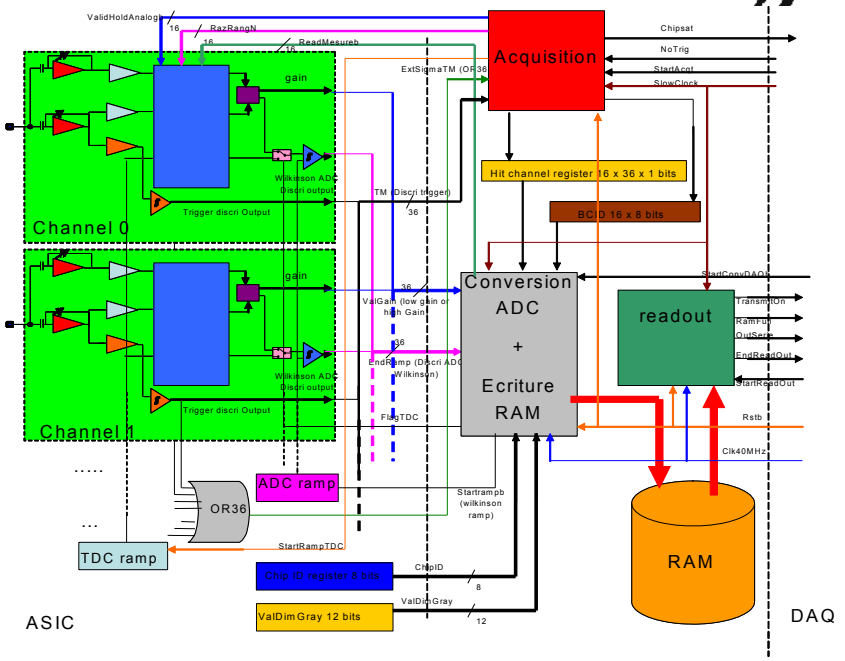
- Large force of micro-electronics engineers (~50)
  - Experience in designing and building large detectors
  - Common Cadence tools
  - But scattered in ~15 labs

- National organization :
  - Building blocks : « club »0.35µm SiGe
  - Networking 0.35 and 130 nm
  - Creation of poles with critical mass (~10 persons)
    - Orsay (OMEGA)
    - Clermont-Lyon (MICHRAU)
    - Strasbourg (IPHC)



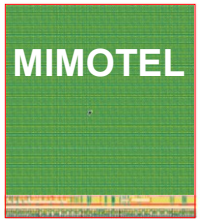
Motivation for poles

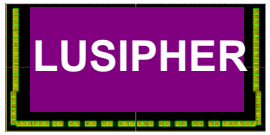
- Continuous increase of chip complexity (SoC, 3D…)
  - Minimize interface problems
- Importance of critical mass
  - Daily contacts and discussions between designers
  - Sharing of well proven blocks
  - Cross fertilization of different projects
- Large R&D activity
  - ILC detectors
  - sLHC (+3D electronics)
  - Medical imaging
  - space

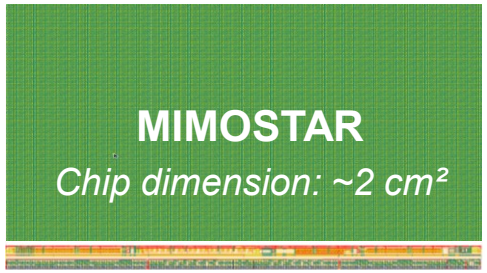


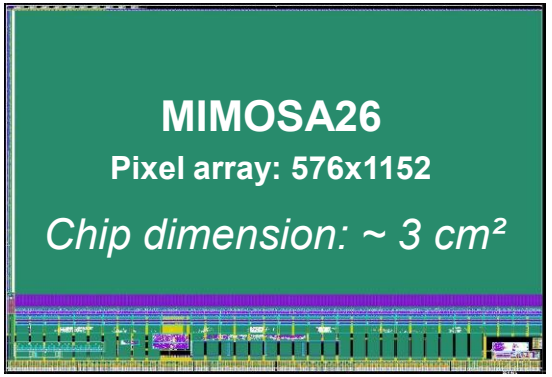
Examples of chips at IN2P3

- MAPS sensors at IPHC (Strasbourg)

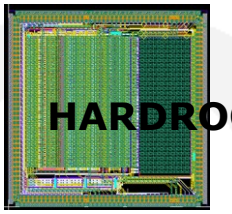


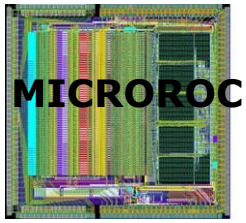


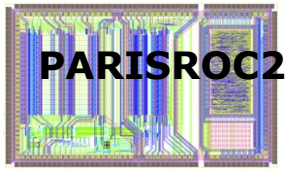


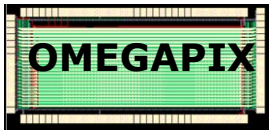


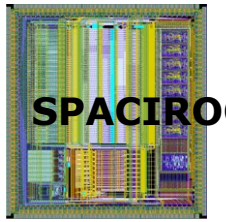
- ROC chips at OMEGA (Orsay)

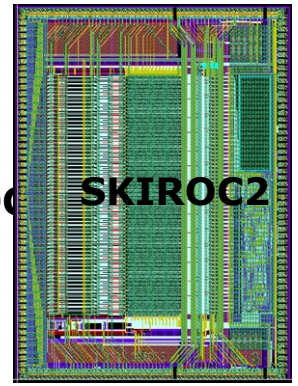




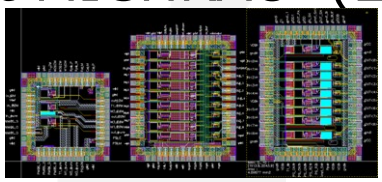


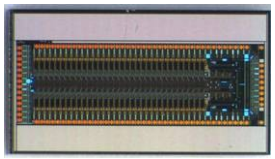


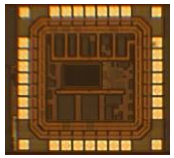


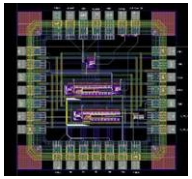


- Chips at MICHRAU (Lyon-Clermont)



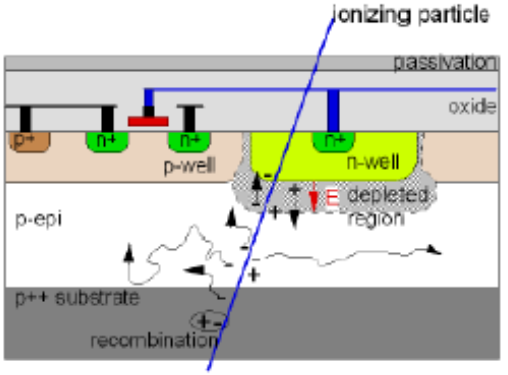






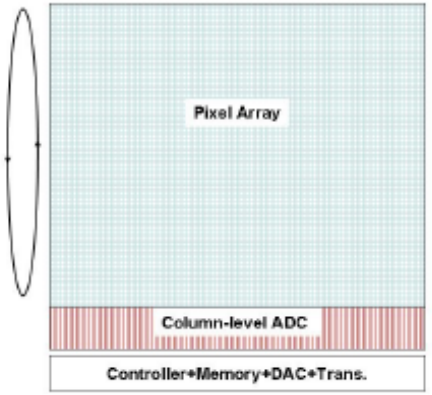
CMOS Pixel Sensors: State of the Art

- **Prominent features of CMOS pixel sensors:**
  - high granularity ⇒ excellent (micronic) spatial resolution
  - very thin (signal generated in 10-20 μm thin epitaxial layer)
  - signal processing μ-circuits integrated on sensor substrate
    - ⇒ impact on downstream electronics (⇒ cost)



- **Organisation of MIMOSA sensors:**
  - manufactured in 0.35 μm OPTO process
  - signal sensing and analog processing in pixel array
  - mixed and digital circuitry integrated in chip periphery
  - read-out in rolling shutter mode

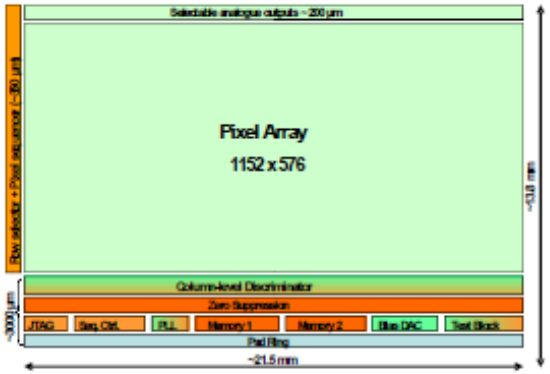
    (pixels grouped in columns read out in //)
    - ⇒ impact on power consumption

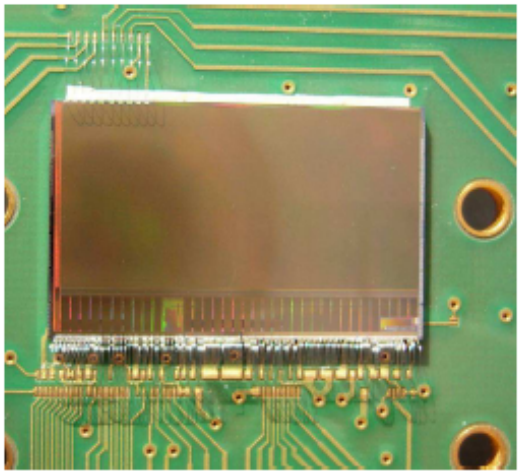


MOSA26 : EUDET Beam telescope

CMOS Pixel Sensors: State of the Art

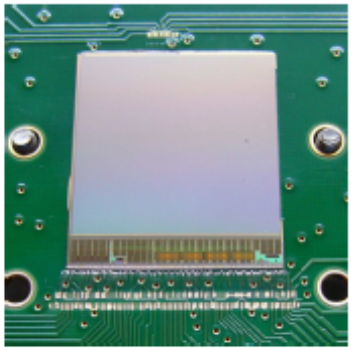
- **Main characteristics of MIMOSA sensor equipping EUDET BT:**
  - ✳ 0.35 μm process with high-resistivity epitaxial layer (coll. with IRFU/Saclay)
  - ✳ column // architecture with in-pixel amplification (CDS) and end-of-column discrimination, followed by $\emptyset$
  - ✳ active area: 1152 columns of 576 pixels (21.2×10.6 mm^2)
  - ✳ pitch: 18.4 $\mu m \longmapsto \sim$ 0.7 million pixels
    charge sharing $\Rightarrow$ $\sigma_{sp} \lesssim 4\ \mu m$
  - ✳ $t_{r.o.} \lesssim 100\ \mu s$ ($\sim 10^4$ frames/s)
    $\Rightarrow$ suited to $>10^6$ part./cm^2/s
  - ✳ $\sim$ 250 mW/cm^2 power consumption (fct of N_{col})

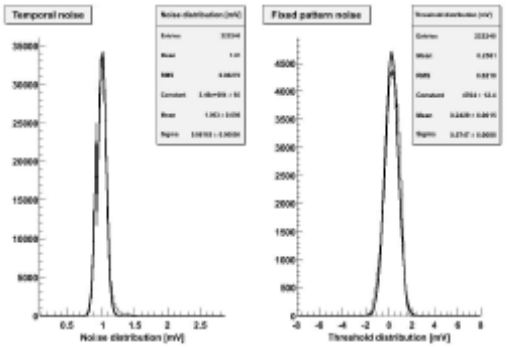




STAR-PXL Detector : MIMOSA-28

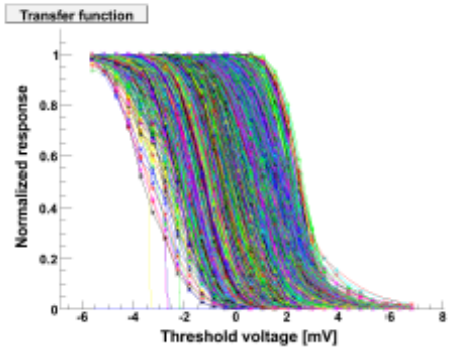
- **Use ULTIMATE sensor (alias MIMOSA-28) equipping STAR-PXL detector**
  - ▷ derived from MIMOSA-26 equipping EUDET BT
- **Main characteristics of ULTIMATE:**
  - ⁕ 0.35 μm process with high-resistivity epitaxial layer
  - ⁕ column // architecture with in-pixel cDS & amplification
  - ⁕ end-of-column discrimination and binary charge encoding, followed by Ø
  - ⁕ active area: 960 columns of 928 pixels (19.9×19.2 mm^2)
  - ⁕ pitch: 20.7 $\mu m \rightarrowtail \sim$ 0.9 million pixels
    - ↪ charge sharing ⇛ $\sigma_{sp} \sim$ 3.5 μm expected
  - ⁕ $t_{r.o.} \lesssim 200\ \mu s$ ($\sim 5 \times 10^3$ frames/s)
    - ⇛ suited to $> 10^6$ part./cm^2/s
  - ⁕ 2 outputs at 160 MHz
  - ⁕ $\lesssim$ 150 mW/cm^2 power consumption





▷▷▷ **Chip back from foundry ⇛ lab tests under way since early April :**

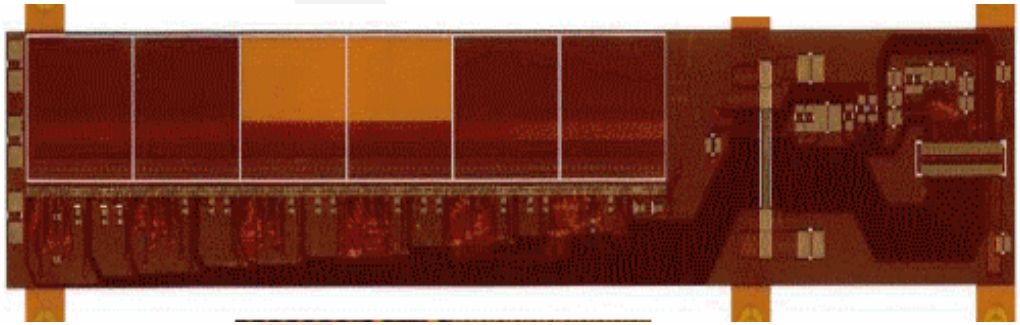
- ⁕ N $\lesssim$ 15 e$^-$ ENC at 30-35°C (as MIMOSA-22AHR)
- ⁕ CCE (^{55}Fe) similar to MIMOSA-22AHR
- —○ **m.i.p. detection assessment at CERN-SPS in June-July '11**

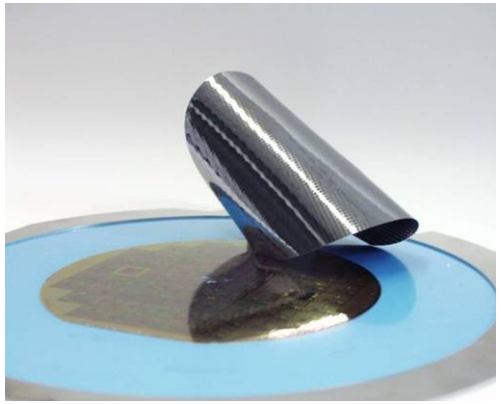


Monolithic Active Pixel Sensors (MAPS) : imagers

Binary sparsified readout sensor for EUDET beam telescope:
> 2 cm^2 active area, 0.7 Mpixel tracker

- Medium speed readout (100 µm integration 10 kFrame/s)
- Spatial resolution < 4 µm for a pitch of 18.4 µm
- Efficiency for MIP > 99.5 %
- Fake hit rate < 10^{-6}
- Radiation hardness > 10^{13} n/cm^2 (high resistivity epi substrate)
- Easy to use, "off-shell" product: used already in several application





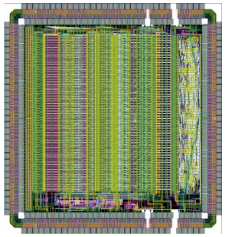
OMEGA/Orsay « ROC chips »

- Move to Silicon Germanium 0.35 µm BiCMOS technology in 2004
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

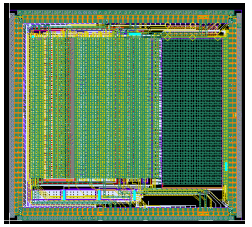
http://omega.in2p3.fr

Chip	detector	ch	DR (C)
MAROC	PMT	64	2f-50p
SPIROC	SiPM	36	10f-200p
SKIROC	Si	64	0.3f-10p
HARDROC	RPC	64	2f-10p
PARISROC	PM	16	5f-50p
SPACIROC	PMT	64	5f-15p
MICROROC	µMegas	64	0.2f-0.5p

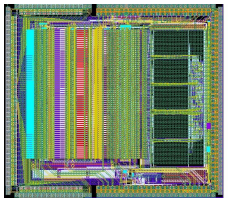
MAROC3



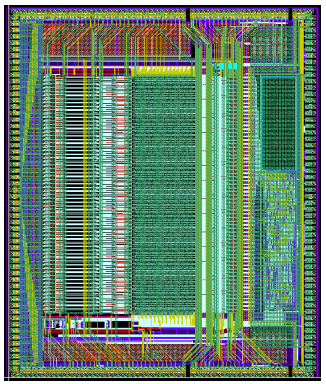
HARDROC2



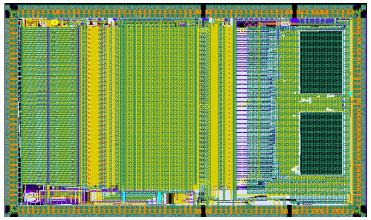
MICROROC1



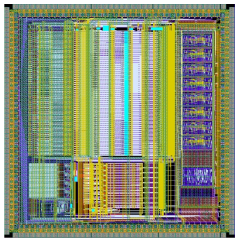
SKIROC2



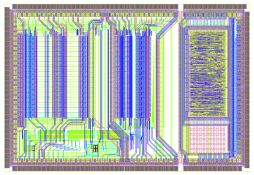
SPIROC2



SPACIROC

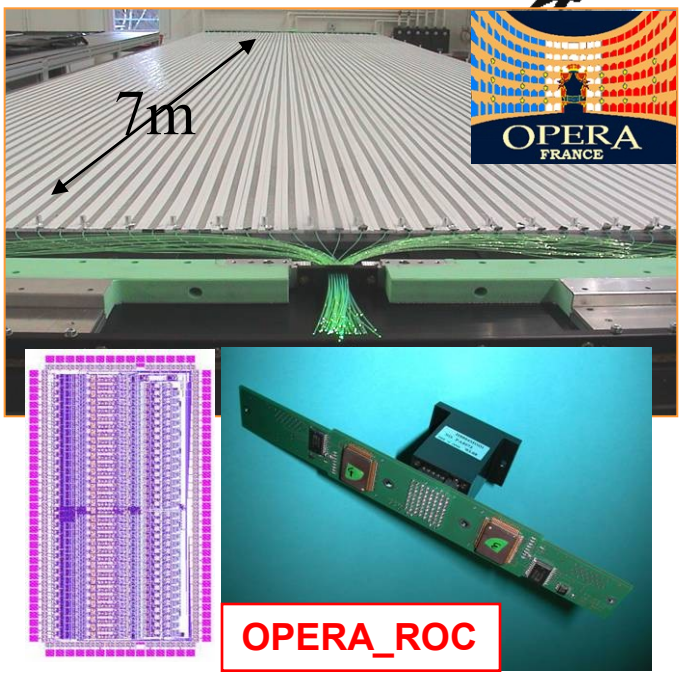


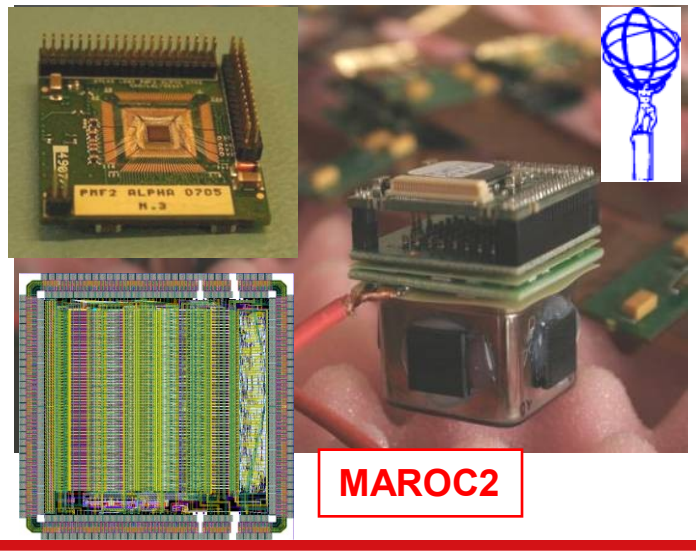
PARISROC2



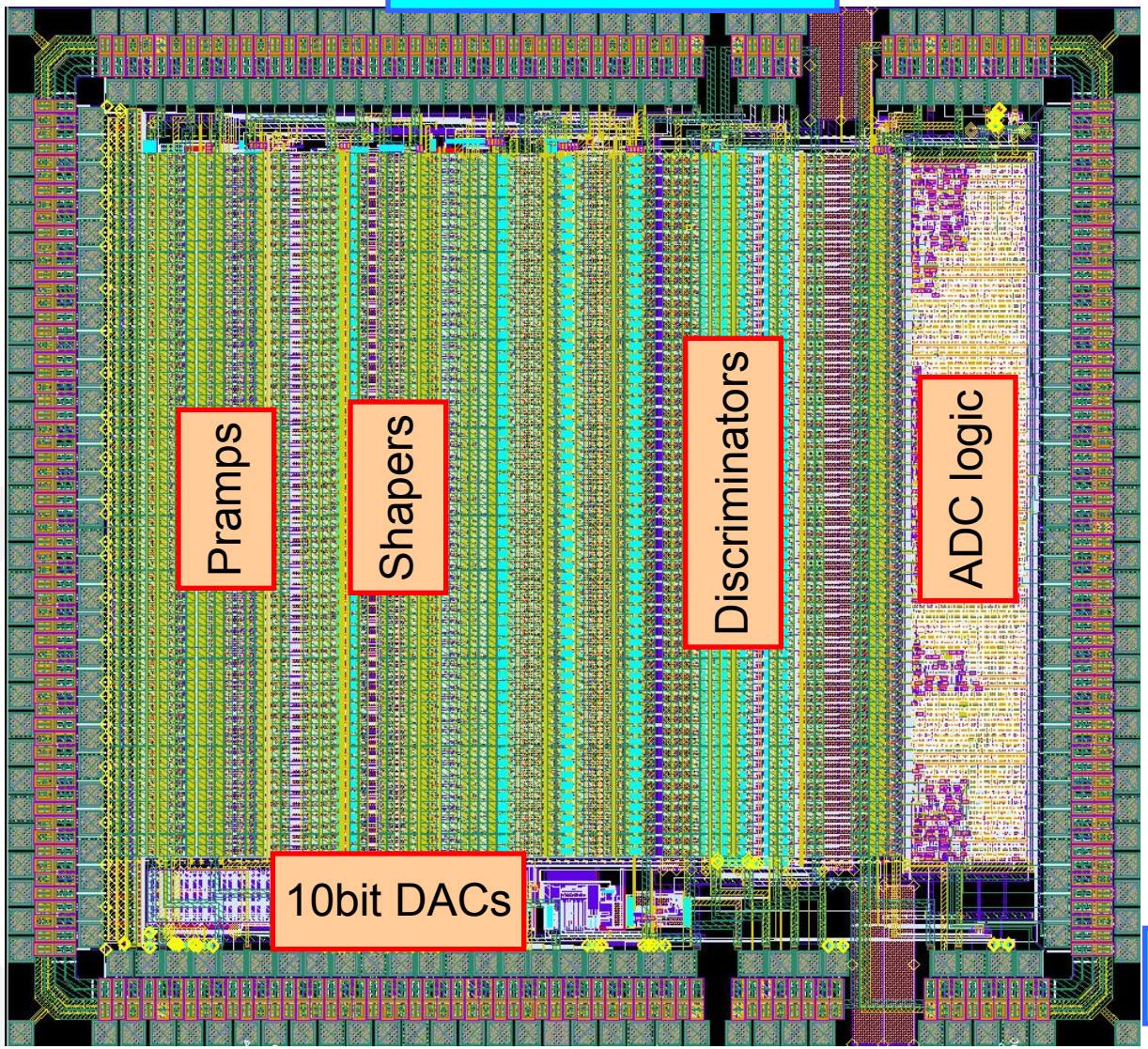
MAROC history

- Started with OPERA_ROC (2001)
  - 32 Ch BiCMOS 0.8 µm for H7500
  - 3000 chips produced in 2002
- MAROC1 (2004)
  - 64 Channels
  - SiGe 0.35 µm
  - OK except pb of Substrate coupling
- MAROC2 (2006)
  - produced to equip the ATLAS luminometer and Double Chooz scintillating fibers
  - Fixed substrate coupling
  - 1000 chips produced
- MAROC3 (2009)
  - Lower power dissipation
  - 1000 chips produced





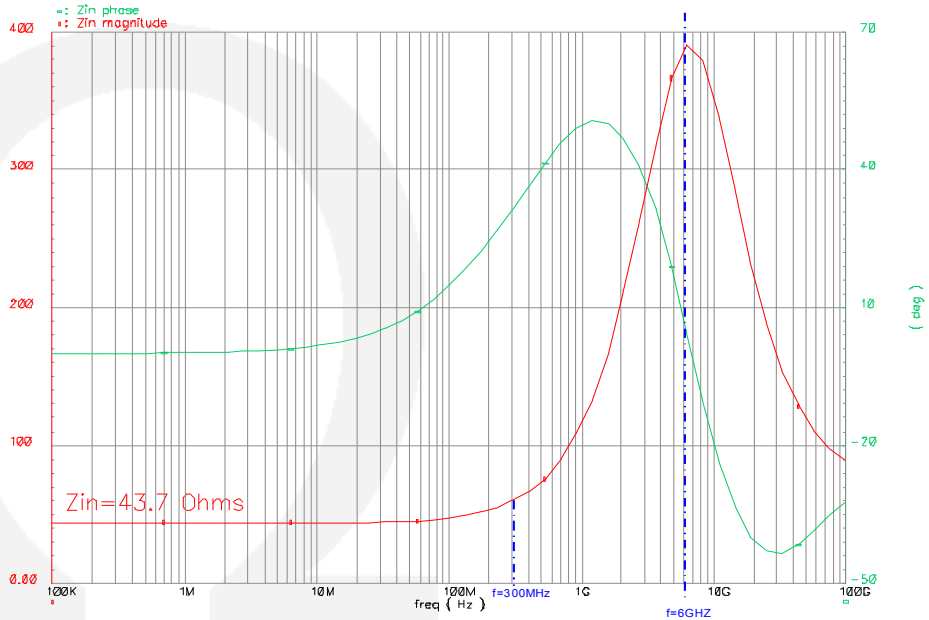
MAROC3 overview

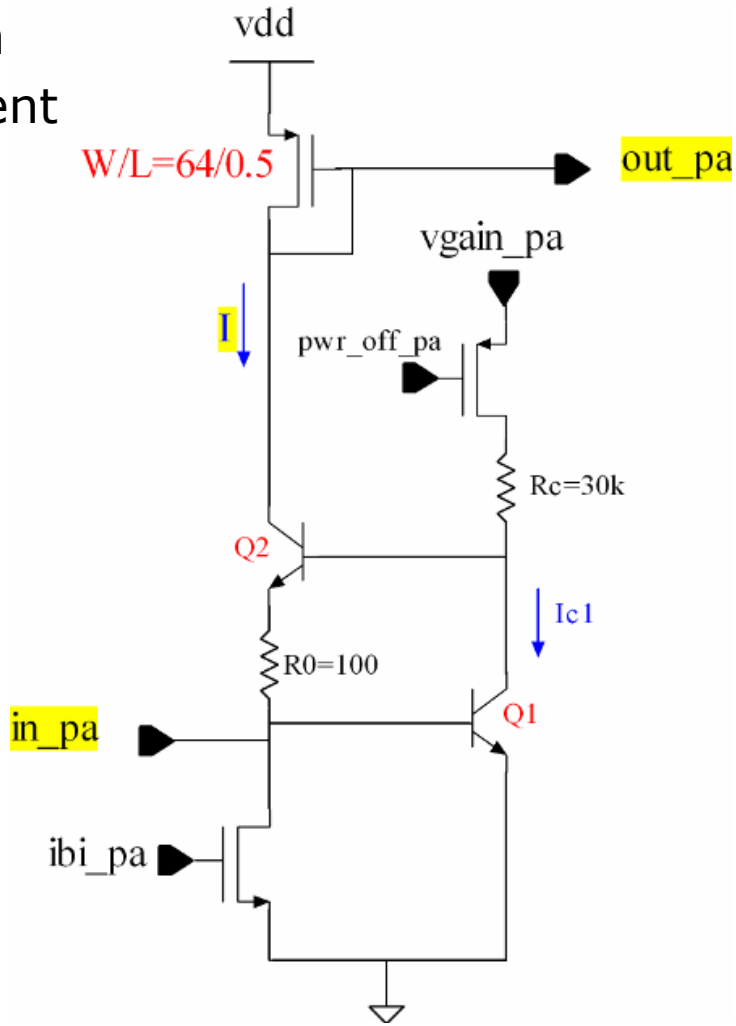


AMS SiGe 0.35µm
Package: CQFP240
Area: 16 mm2

MAROC preamplifier

- **Current conveyor**
  - « Super common base » configuration
  - low input impedance, small « equivalent inductance » (<20 nH)
  - Zin = $1/g_{m1}g_{m2}R_c$ = 10-100Ω
  - good performance of SiGe
- **Variable output mirrors : 8 bits**
  - **Multiple outputs**

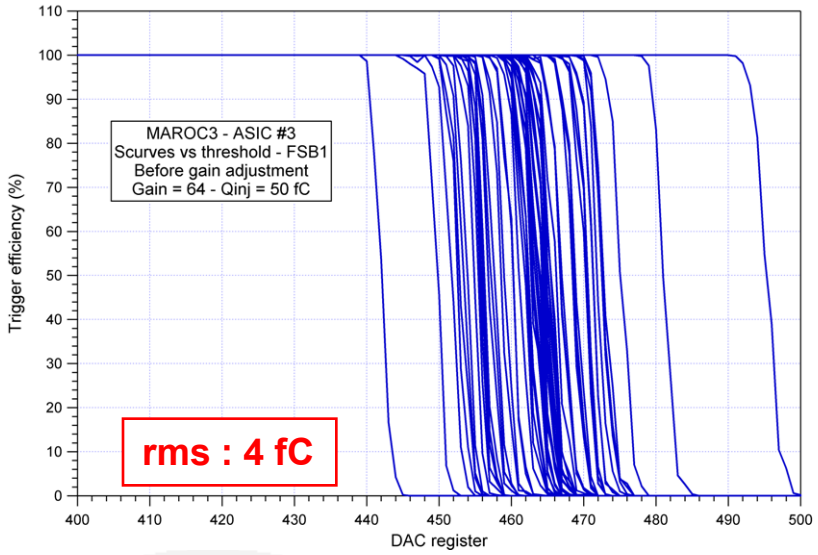


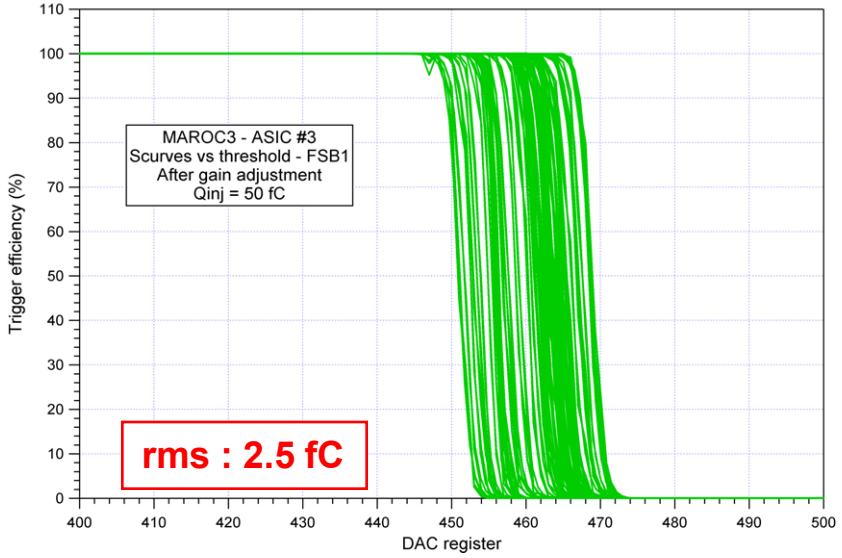


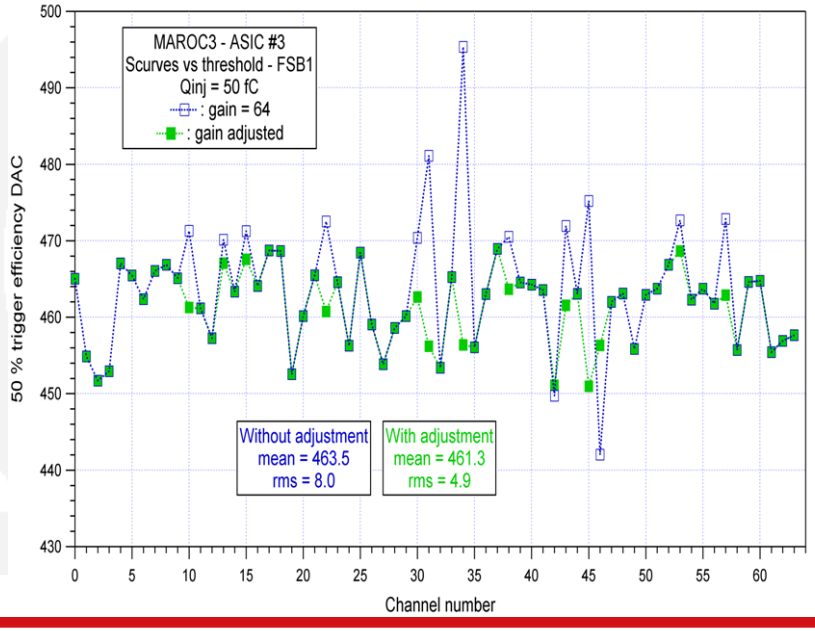
ATLAS note : ATL-LARG-95-010 (1995)

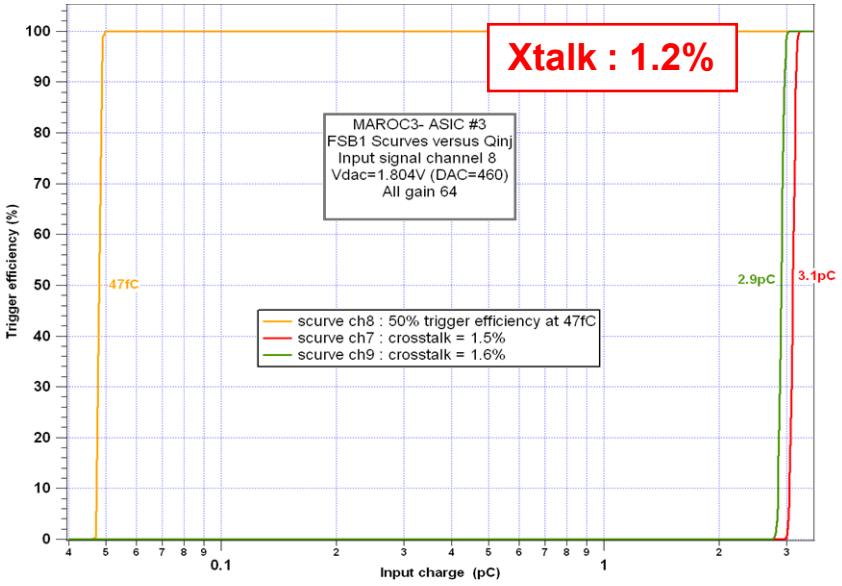
Nucl Instr and Meth **A521** (2004) 378-392

Gain correction : scurves with FSB



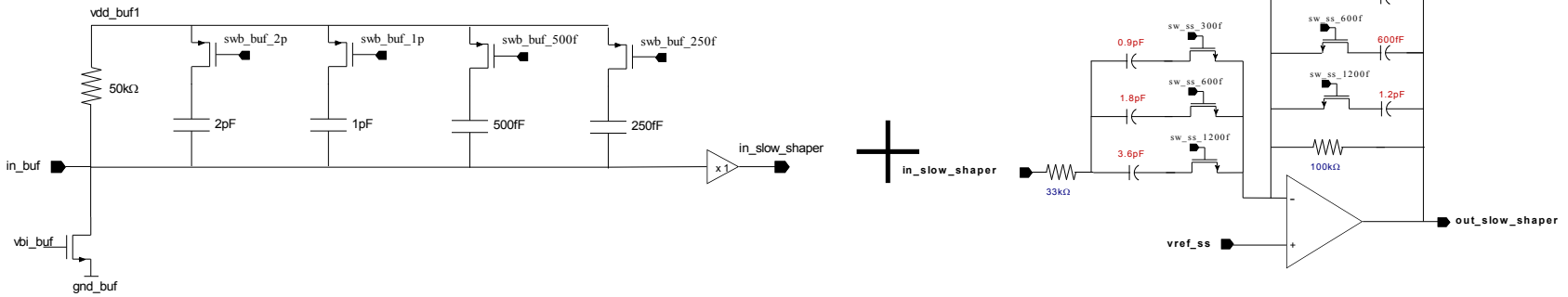


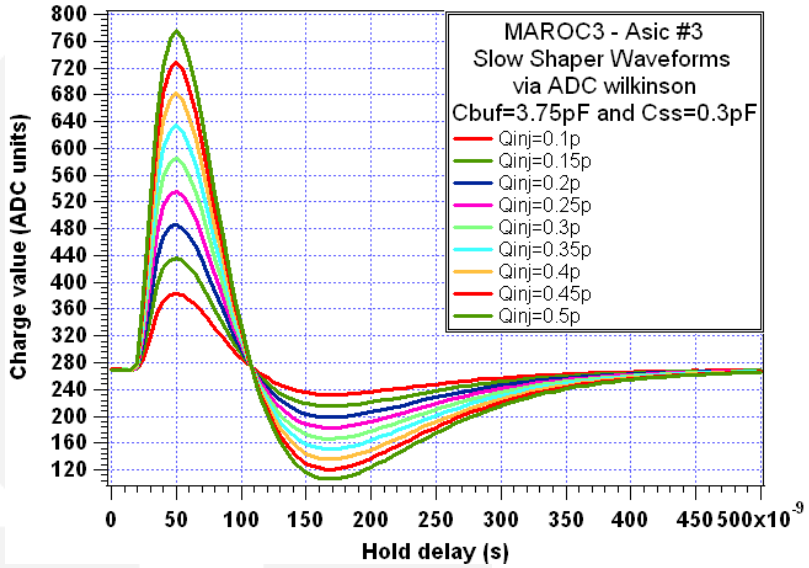


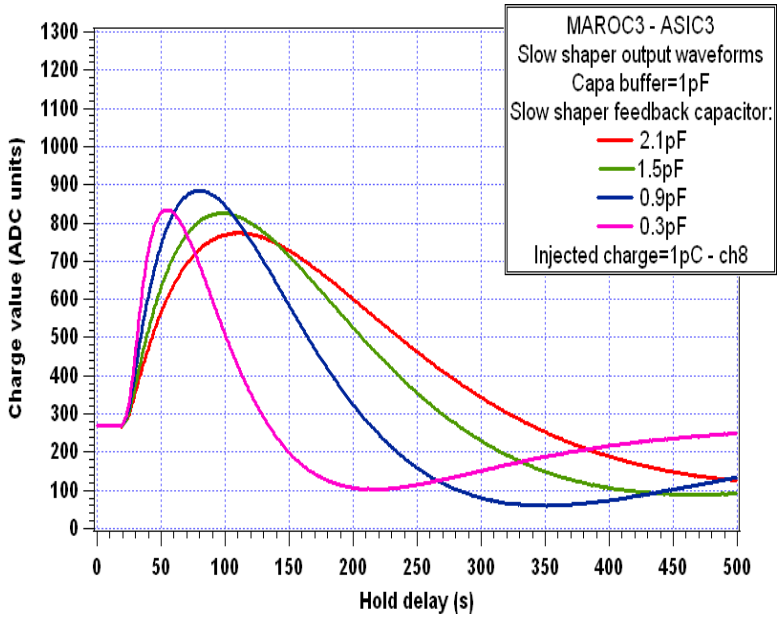


Charge measurements: Slow shaper

- Variable integrator + variable CRRC shaper (25-100 ns)
- 2 Track & Hold. Pedestal dispersion : 1.3 mV rms

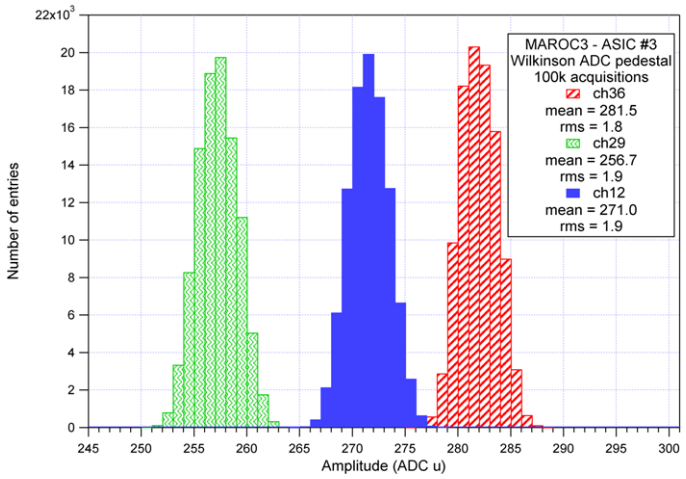


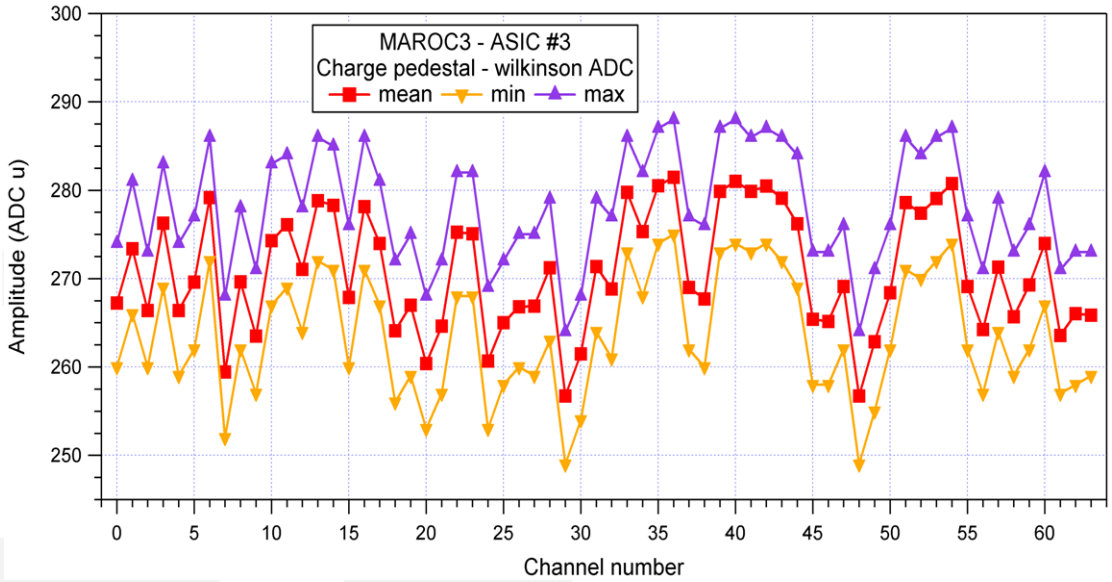


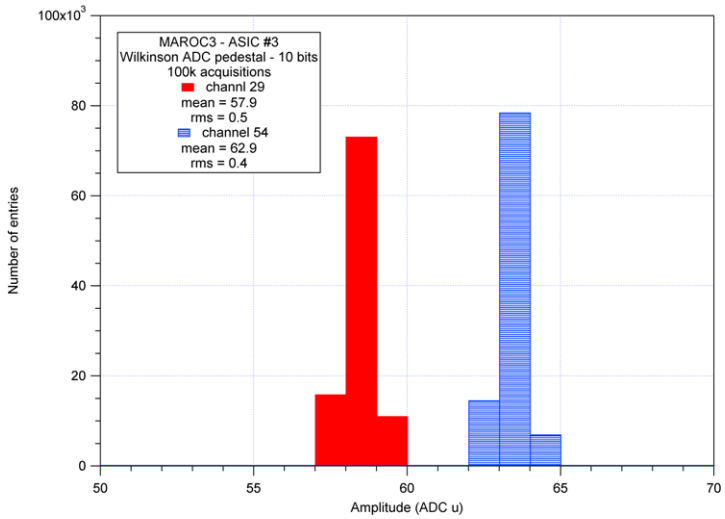


Wilkinson ADC

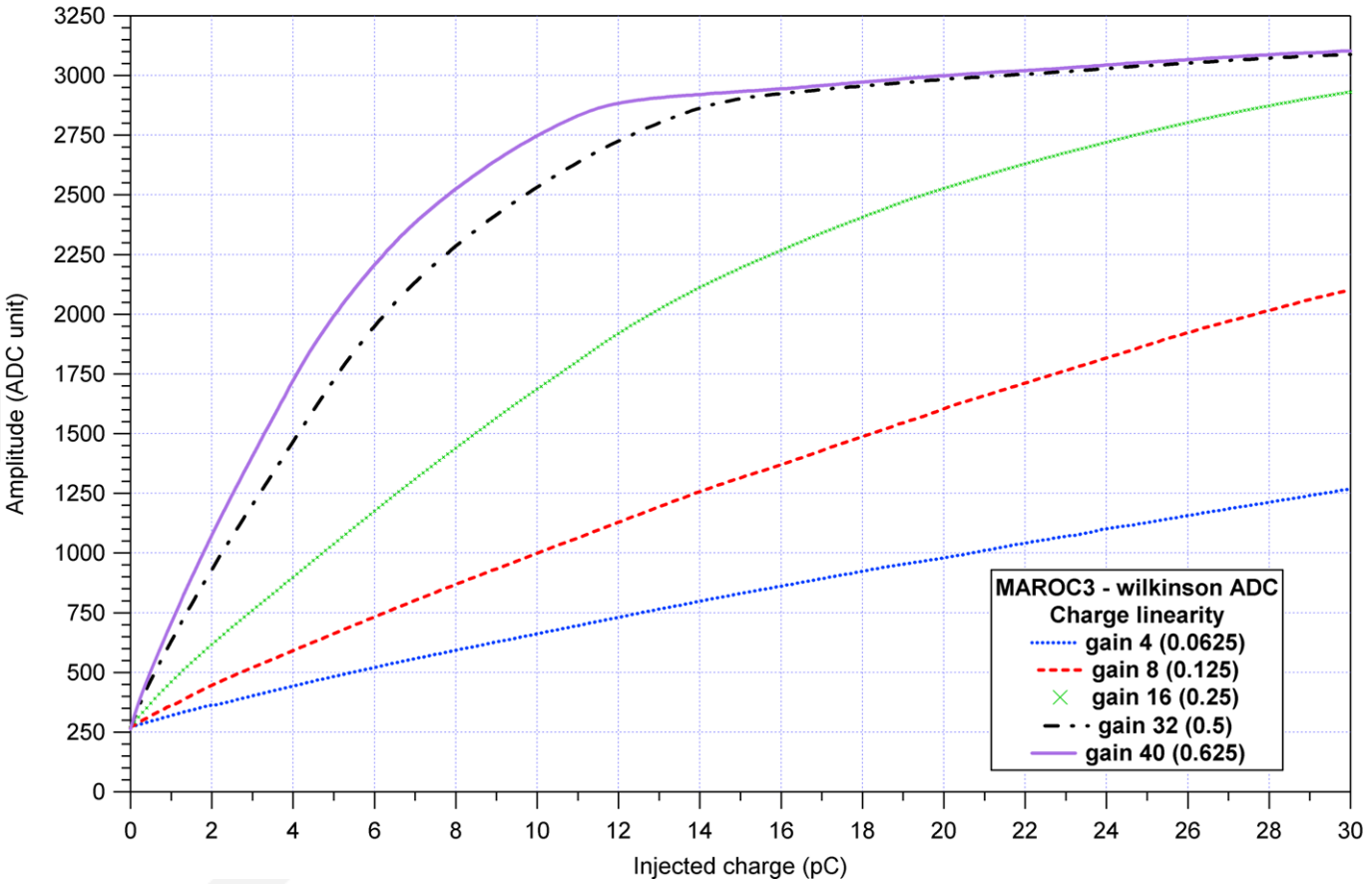
- Selectable 8/10/12 bits
- Conversion time : 6/25/100 µs
- Overall noise : 0.5/2 ADCU (600µV)
- Useful for gain calibration







Overall linearity at variable gain



Variant : SPACIROC for JEM/EUSO

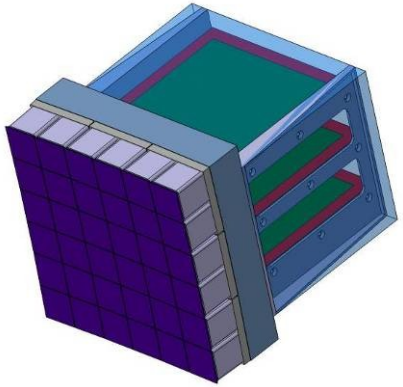
ASIC Functions:

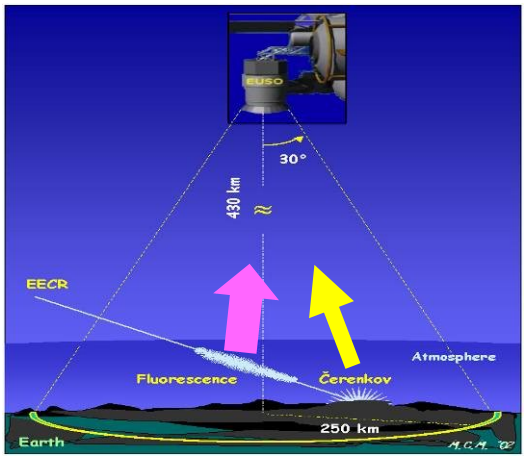
Analog part:

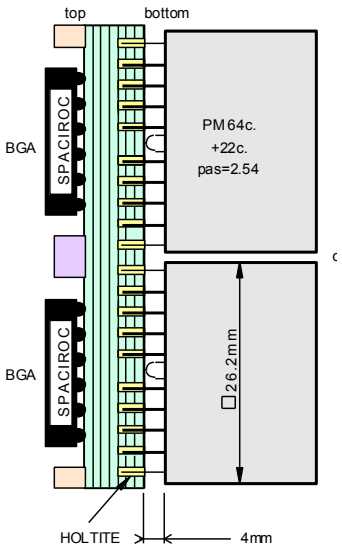
1. Photoelectron counting (20-100MHz)
2. Time Over Threshold (collab. JAXA/Riken)

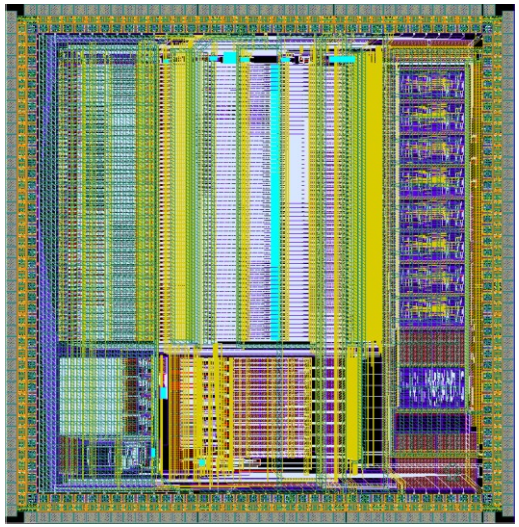
Digital part (LAL):

1. Digitization,
2. Memory,
3. Send data to FPGA for triggering







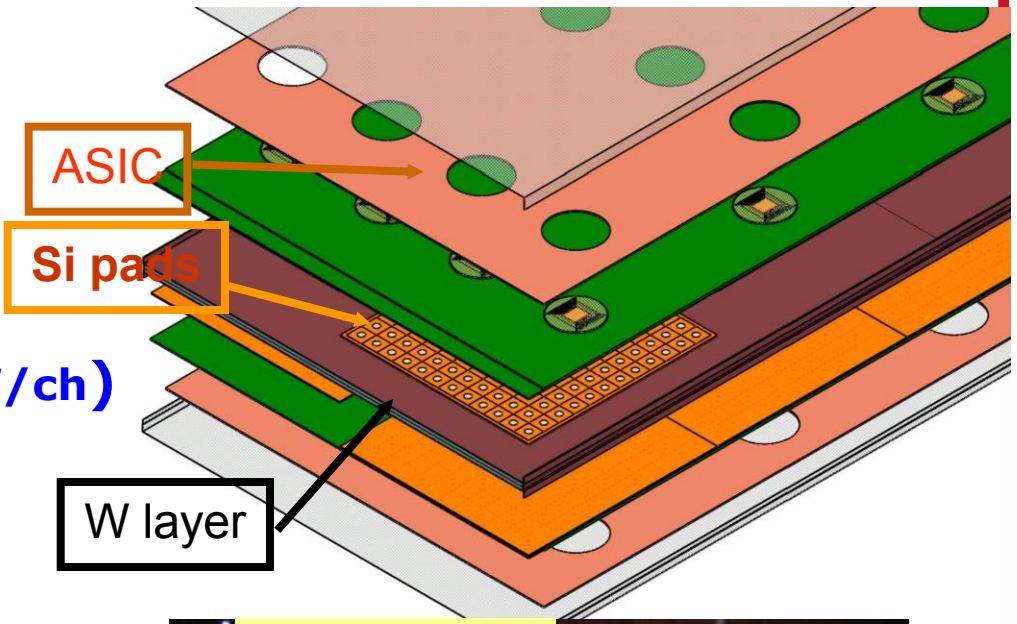


Crucial points

- Power consumption < 1 mW/ch
- data flow ~ 384 bits / 2.5 µs
- Radiation tolerance : triple voting

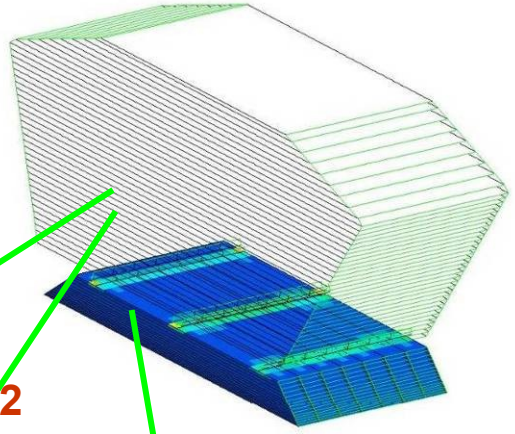
ILC Challenges for electronics

- Requirements for electronics
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - Front-end embedded in detector
  - 10^8 channels
  - **Ultra-low power : (25µW/ch)**
  - Compactness
- « Tracker electronics with calorimetric performance »



CALICE second generation ASICs

- auto-trigger, analog storage, digitization and token-ring readout !!!
- power pulsing : <1 % duty cycle
- integration issues

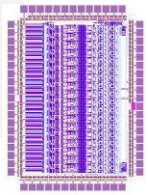


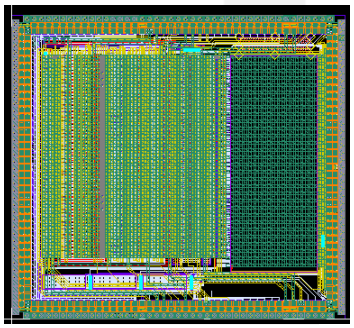
SKIROC2
ECAL Si
64 ch.

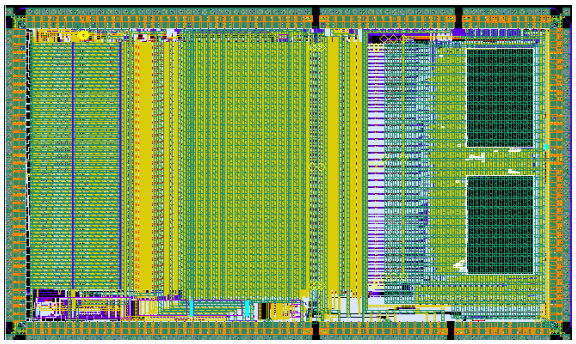
HARDROC2
SDHCAL RPC
64 ch 16 mm^2

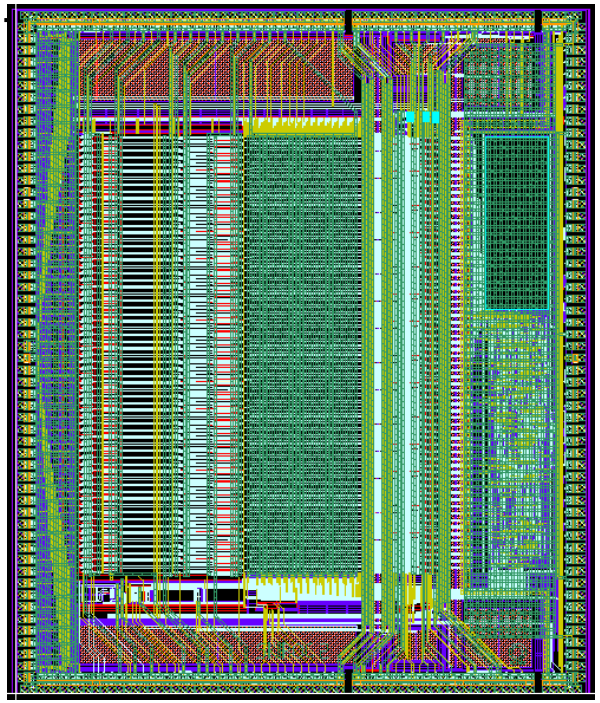
SPIROC2
AHCAL SiPM
36 ch 30 mm^2

FLC_PHY3 (2003)



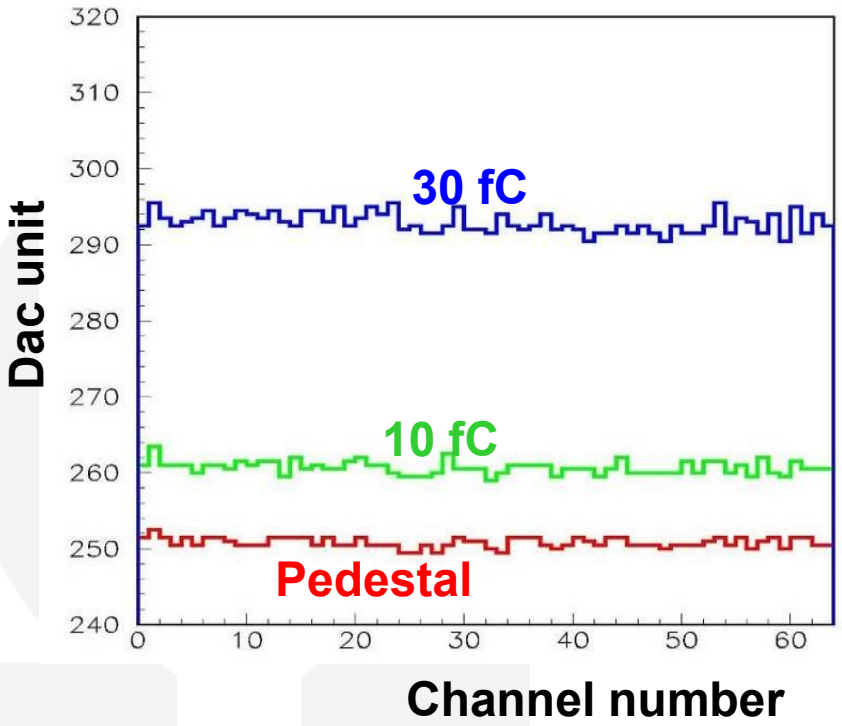


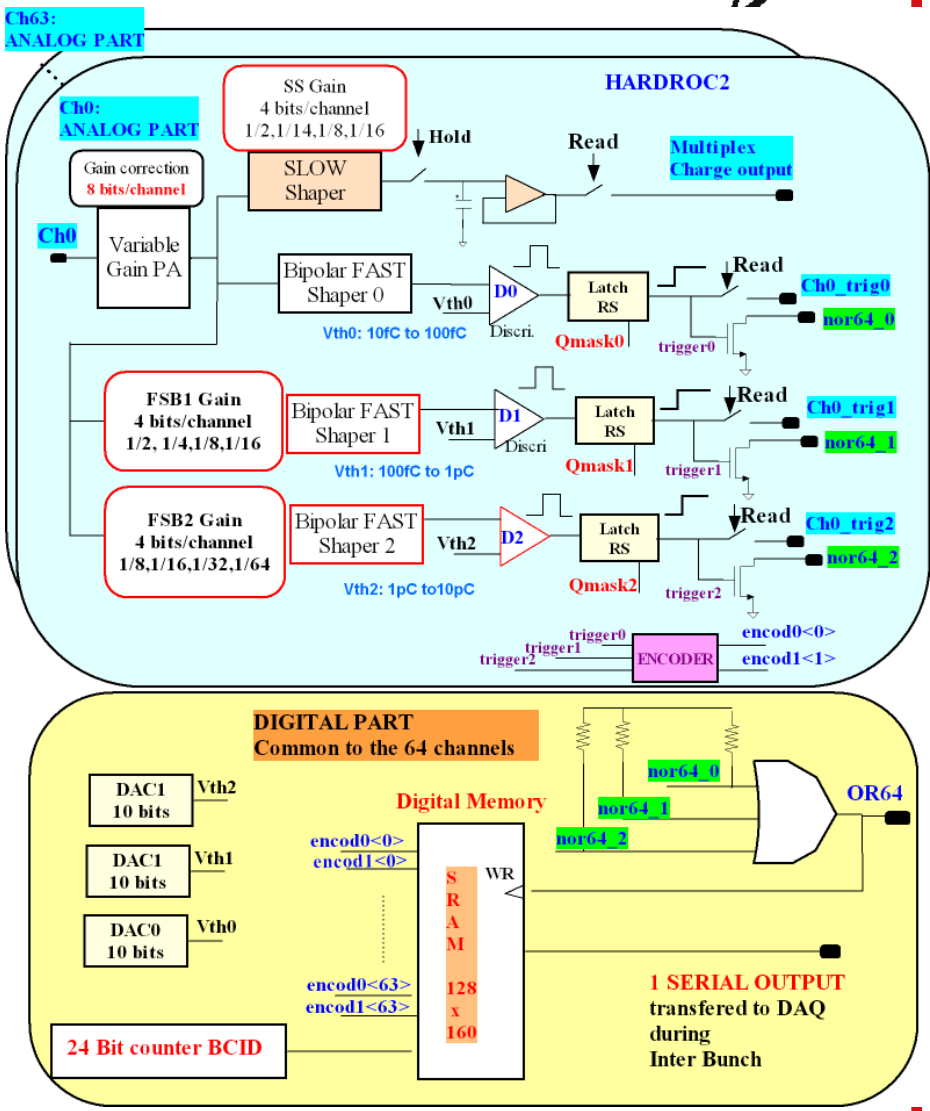




HaRDROC : ILC DHCAL readout

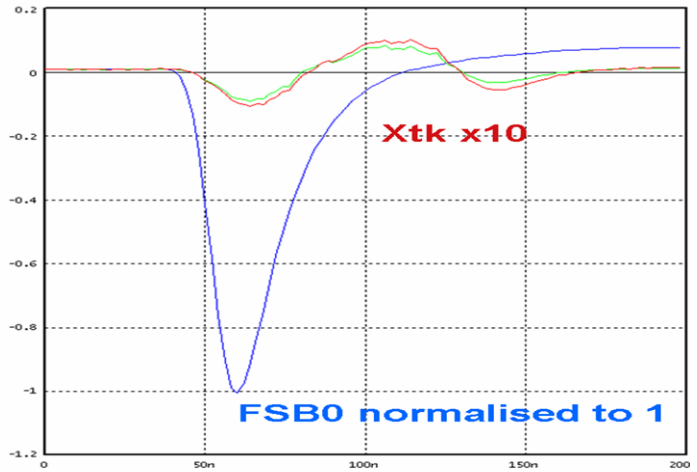
- Hadronic Rpc Detector Read Out Chip : 64 channels
  - Variable gain, low input impedance preamps + shaper + 3 discris
  - Full power pulsing => 7 µW/ch
  - Fully integrated ILC sequential readout

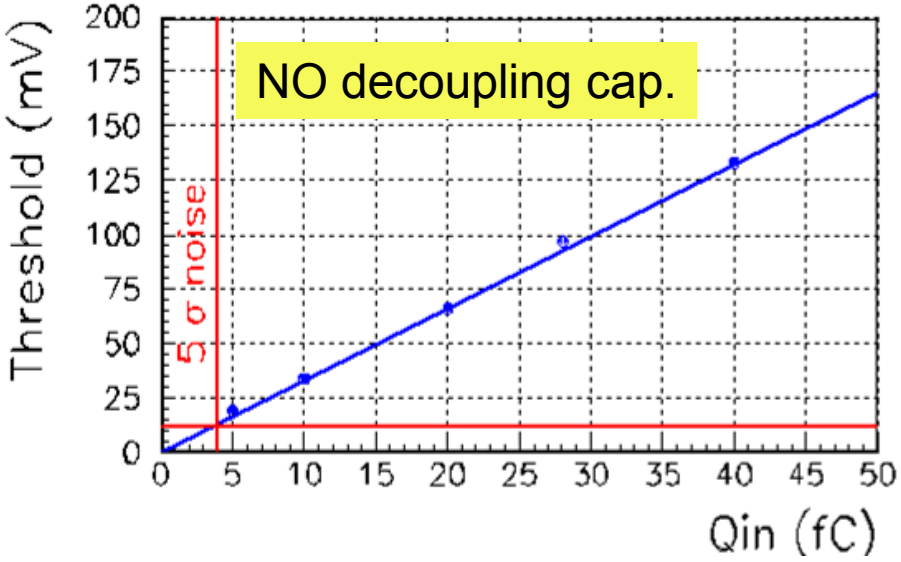


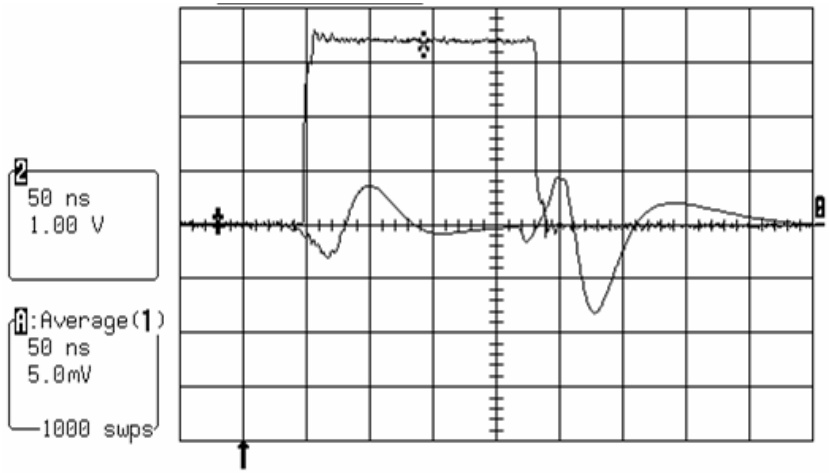


Analog and Digital crosstalk

- Analog Crosstalk ~1%
  - Well differentiated, capacitive like
  - Dominated by the input
  - No long distance crosstalk
- Digital crosstalk : 3 fC
  - Coupling of discriminator to inputs through ground or substrate
  - Trigger on CH1 and look at analog signal on CH2

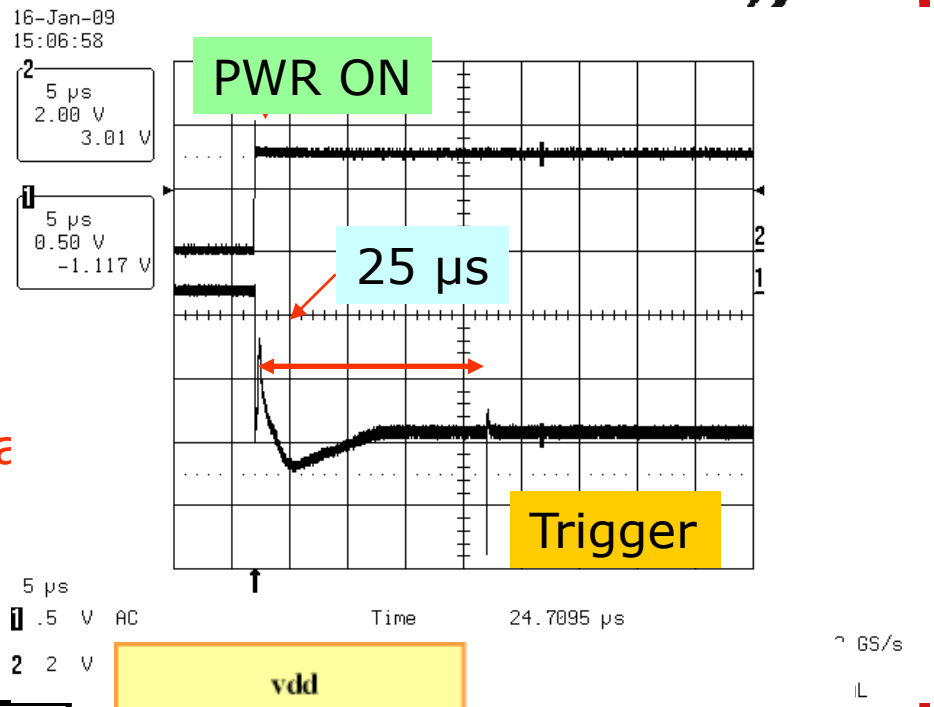




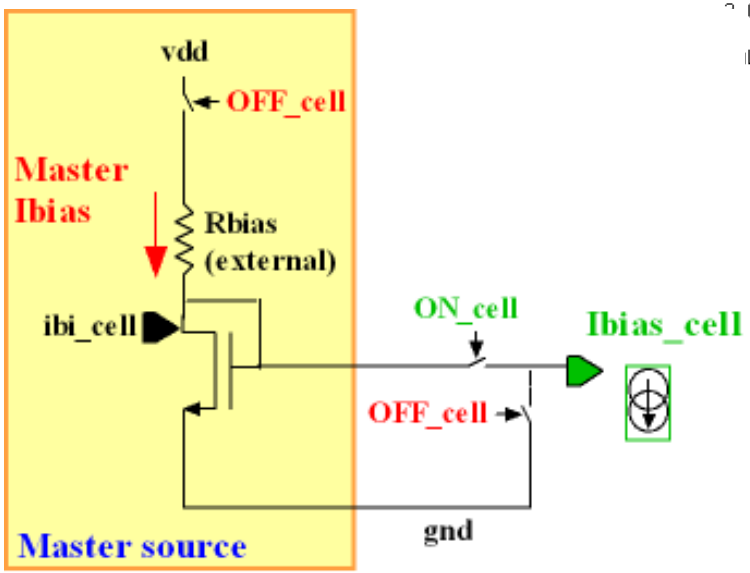


Power pulsing

- Total power on : 100 mW
- Total power off : 10 µW
- Power dissipation
  - 1.5 mW/ch continuous
  - 25 µs awake time
  - 7.5 µW/ch with 0.5% duty cycle
- 10 µW/ch = 24h operation of full sla with 2 AAA batteries !

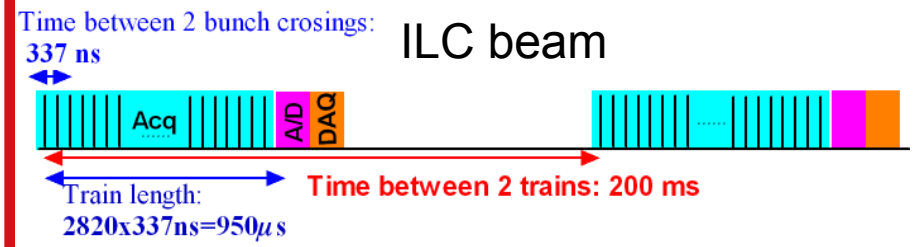


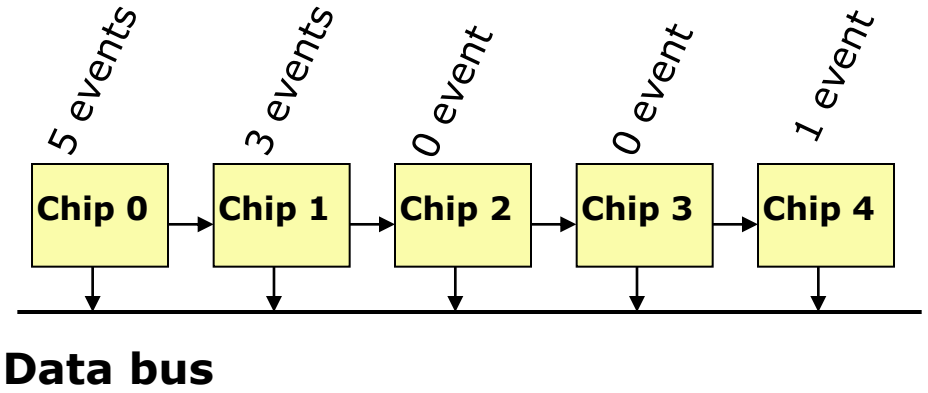
PA	5.46mA	DAC	0.84mA
3 FSB	12.3mA	BG	1.2mA
SS	*9.3mA*	vddd	0.67mA
3 Discris	7.3mA	vddd2	0.4mA (=0 if 40MHz OFF)
TOTAL	38mA		

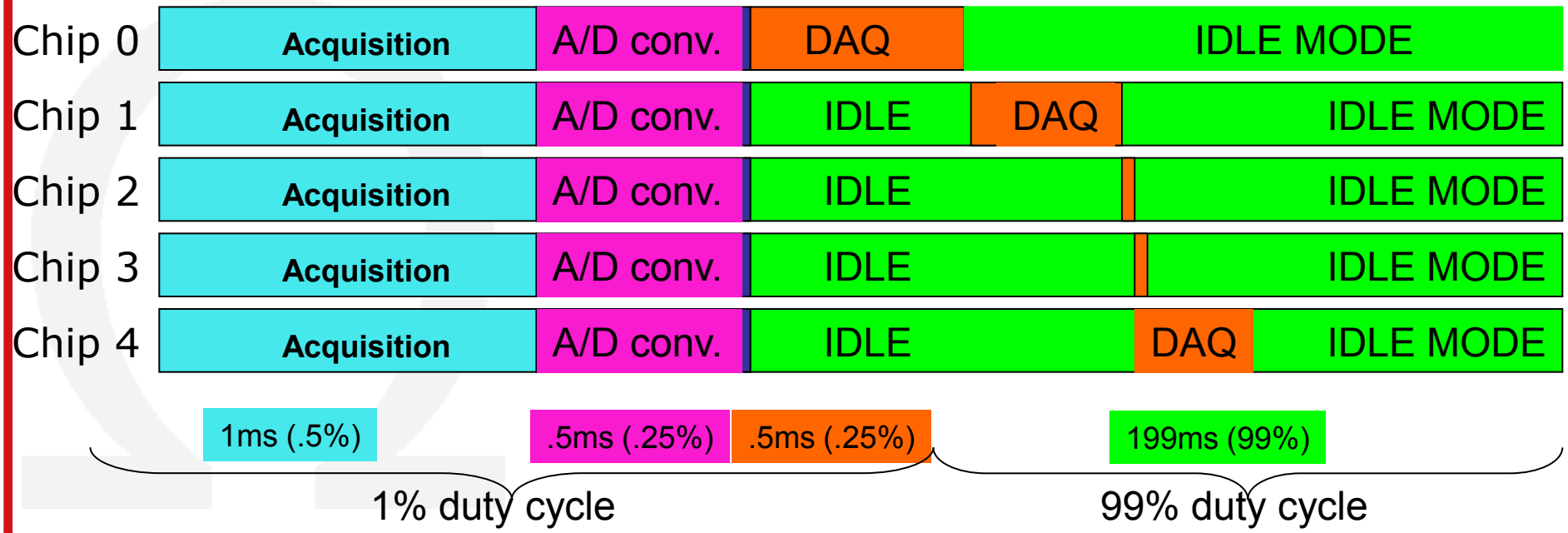


Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power

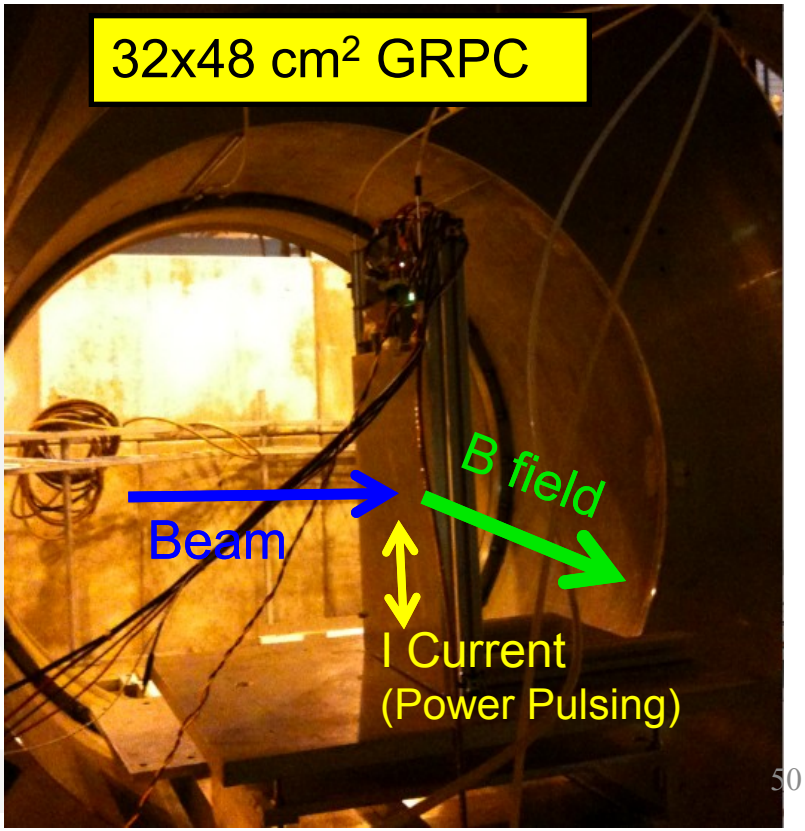


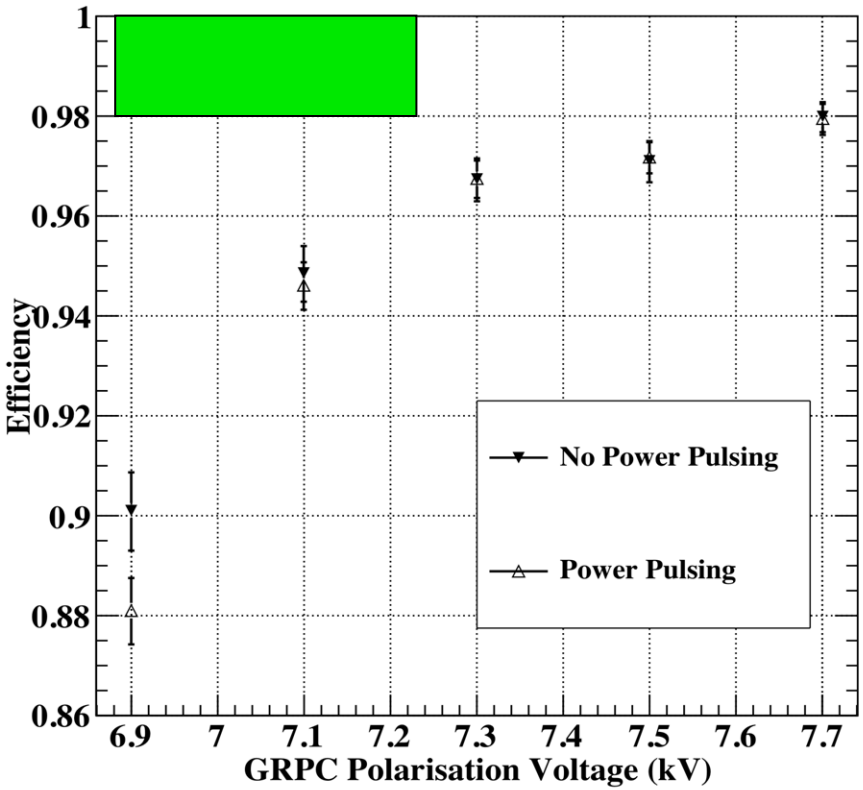




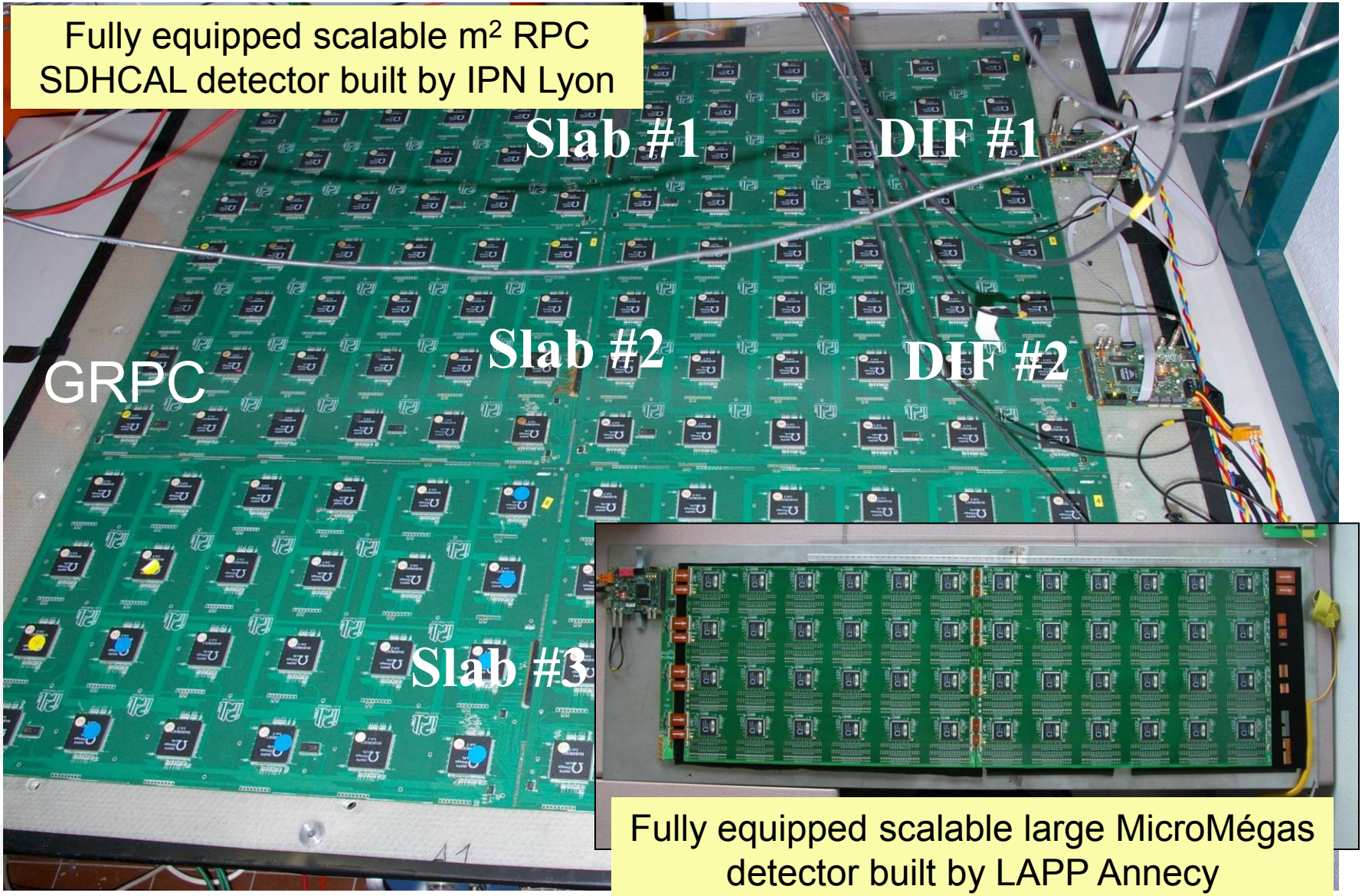
First power pulsing results

- Tests at system level, 50 Hz pulsing in 3T magnetic field
- No efficiency loss



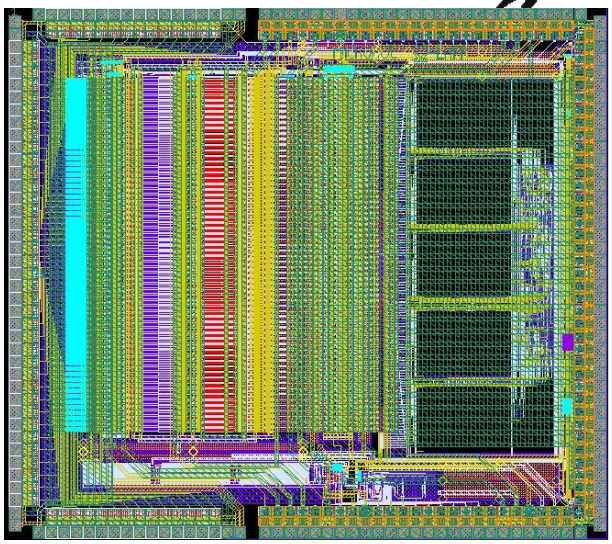


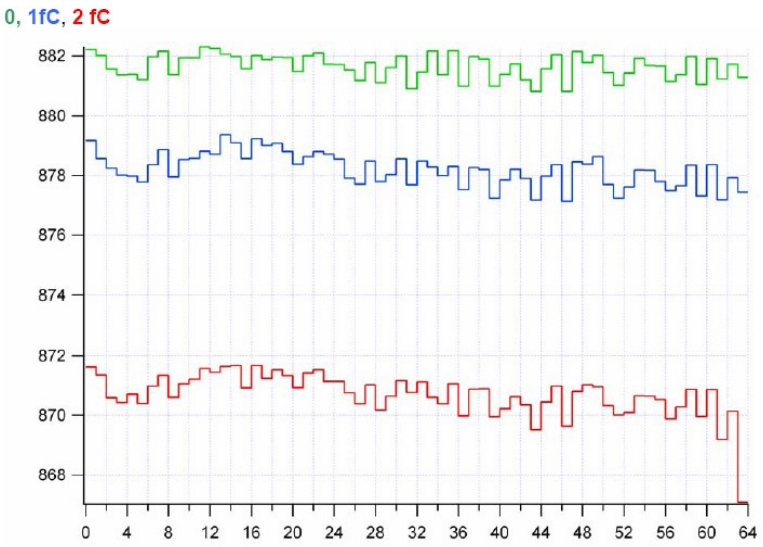
Square meter prototypes



Variant : MICROROC

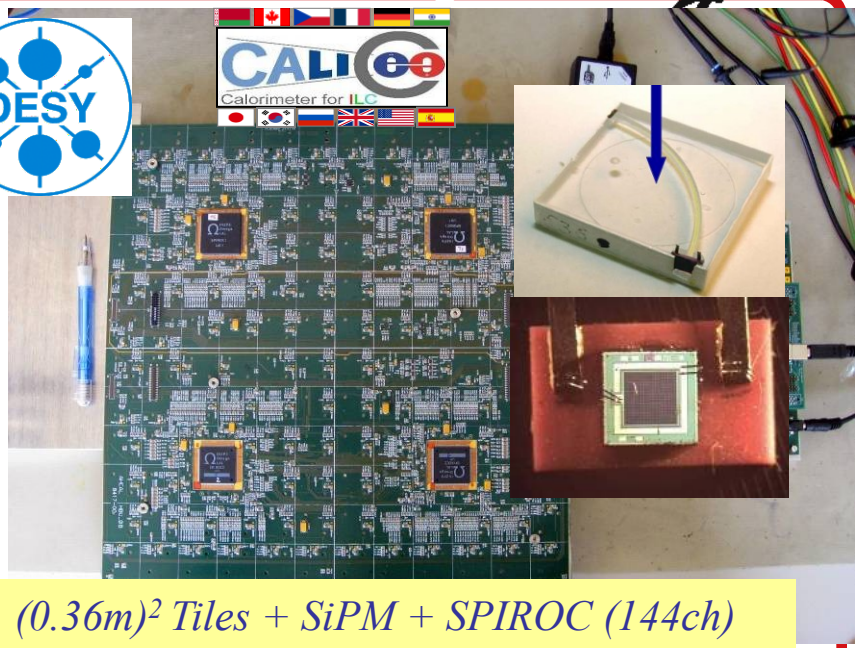
- MICROROC : MICROMEGAS Read Out Chip
  - Same as HARDROC but with charge preamp input stage + HV protection and slower shaping + 4bit DAC/channel
  - Preamp optimized for Cd=80 pF, noise = 0.2 fC. Cf=0.4pF Rf=5M
  - Maximum input charge : 500 fC
  - Bi-gain shaper (G1-G4), peaking tunable 50-200 ns (2 bits)
  - 3 thresholds
  - Lowest threshold ~2 fC
  - Pin to pin compatible with HR2
- Collaboration with LAPP Annecy



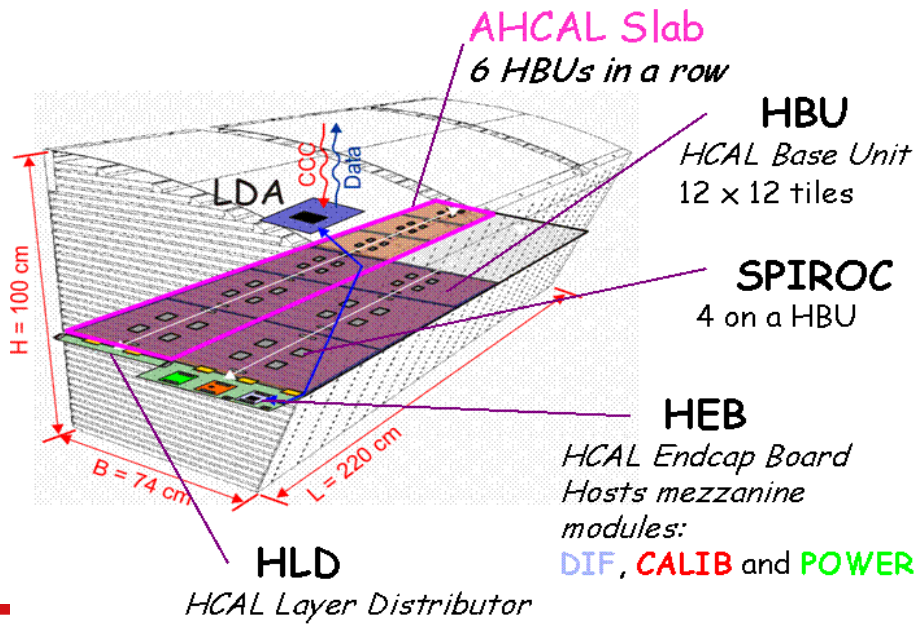


SPIROC for SiPM readout

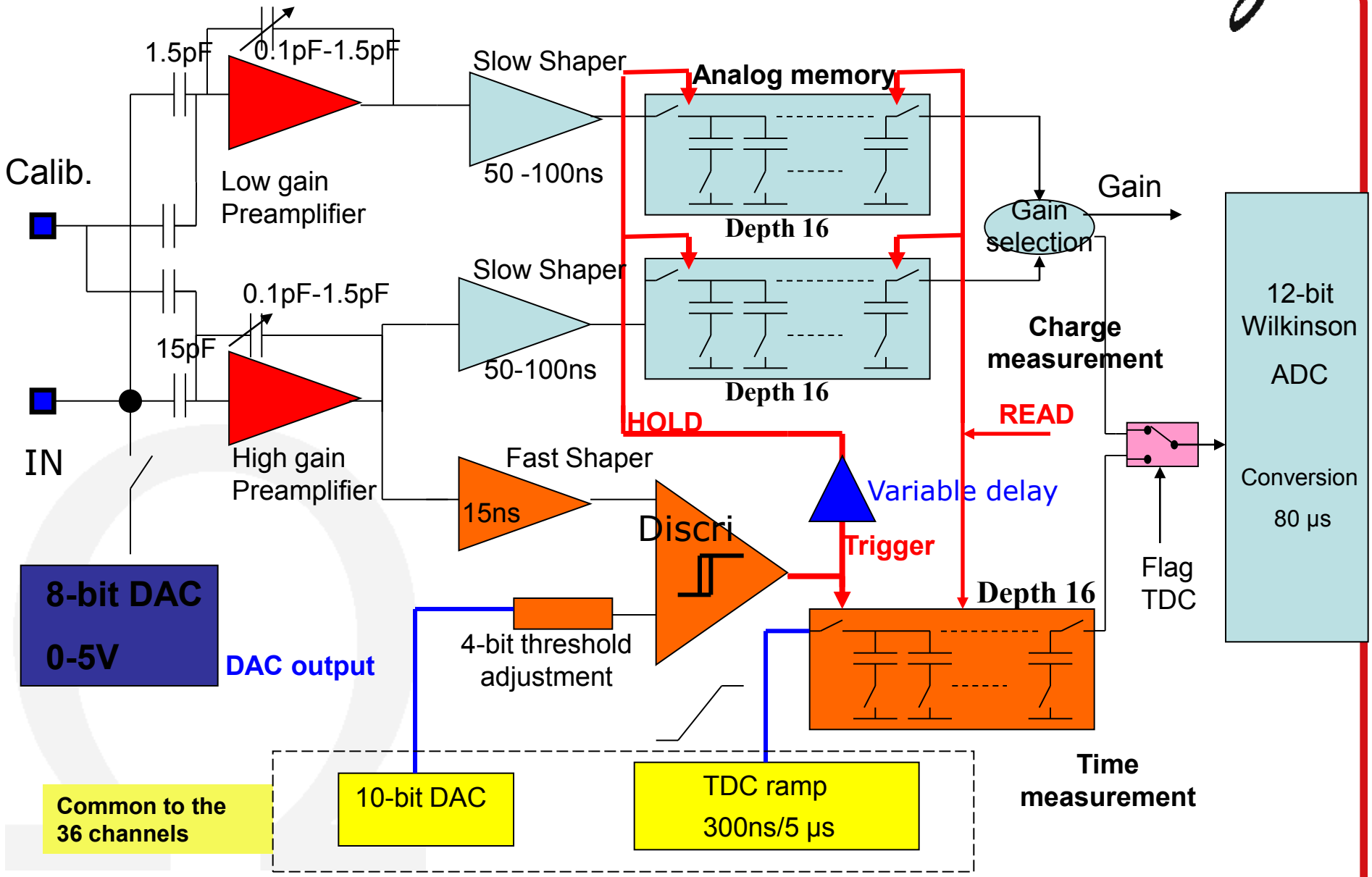
- SPIROC : Silicon Photomultiplier Integrated Readout Chip
- Developed to read out the analog hadronic calorimeter for CALICE (ILC)
- DESY collaboration (EUDET project)
- Chip embedded in detector :
  - ☐ Power consumption is an important issue
  - ☐ few external components
- Big detector with huge number of channels (8 millions)



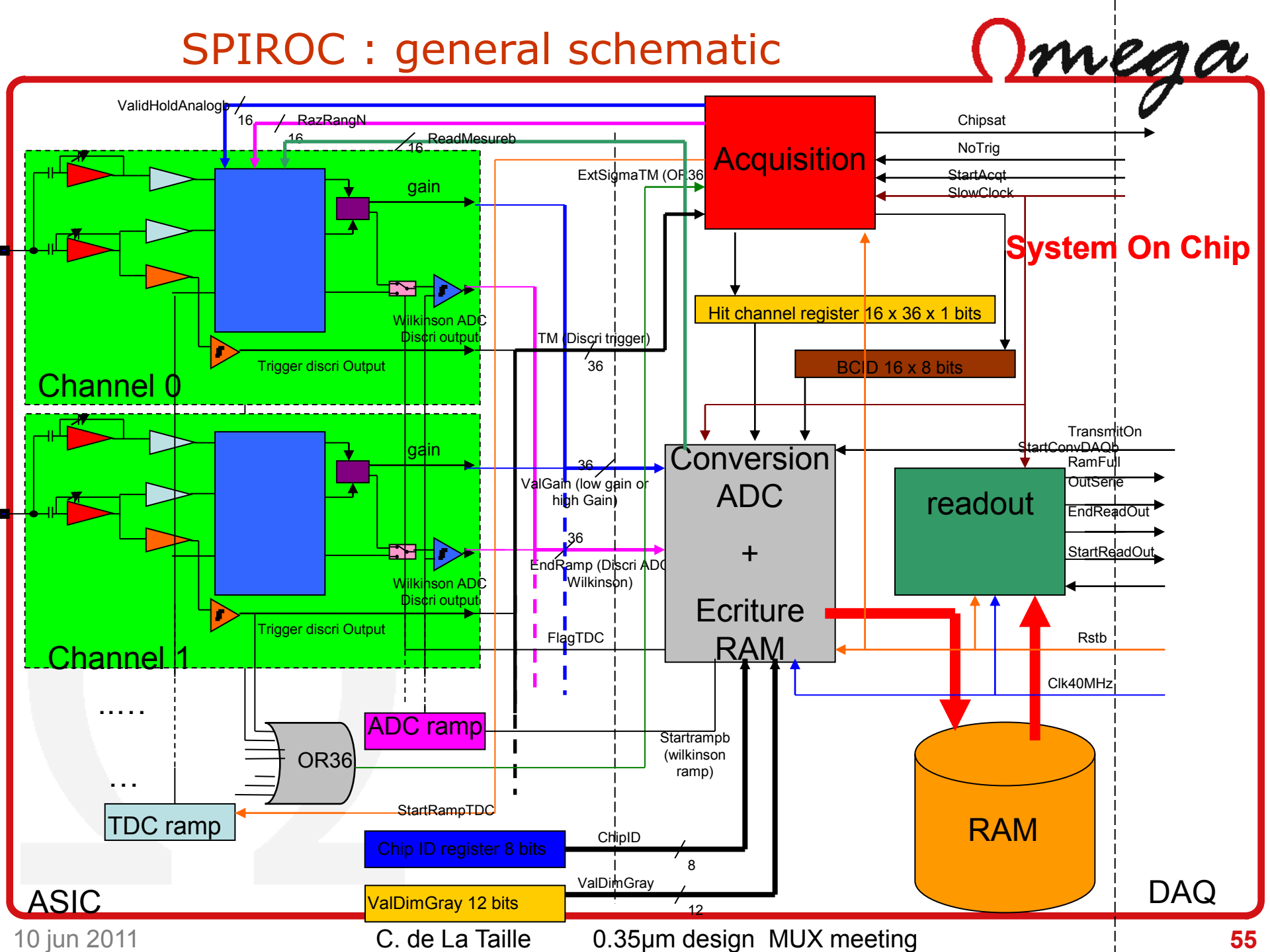
(0.36m)² Tiles + SiPM + SPIROC (144ch)



SPIROC : One channel schematic

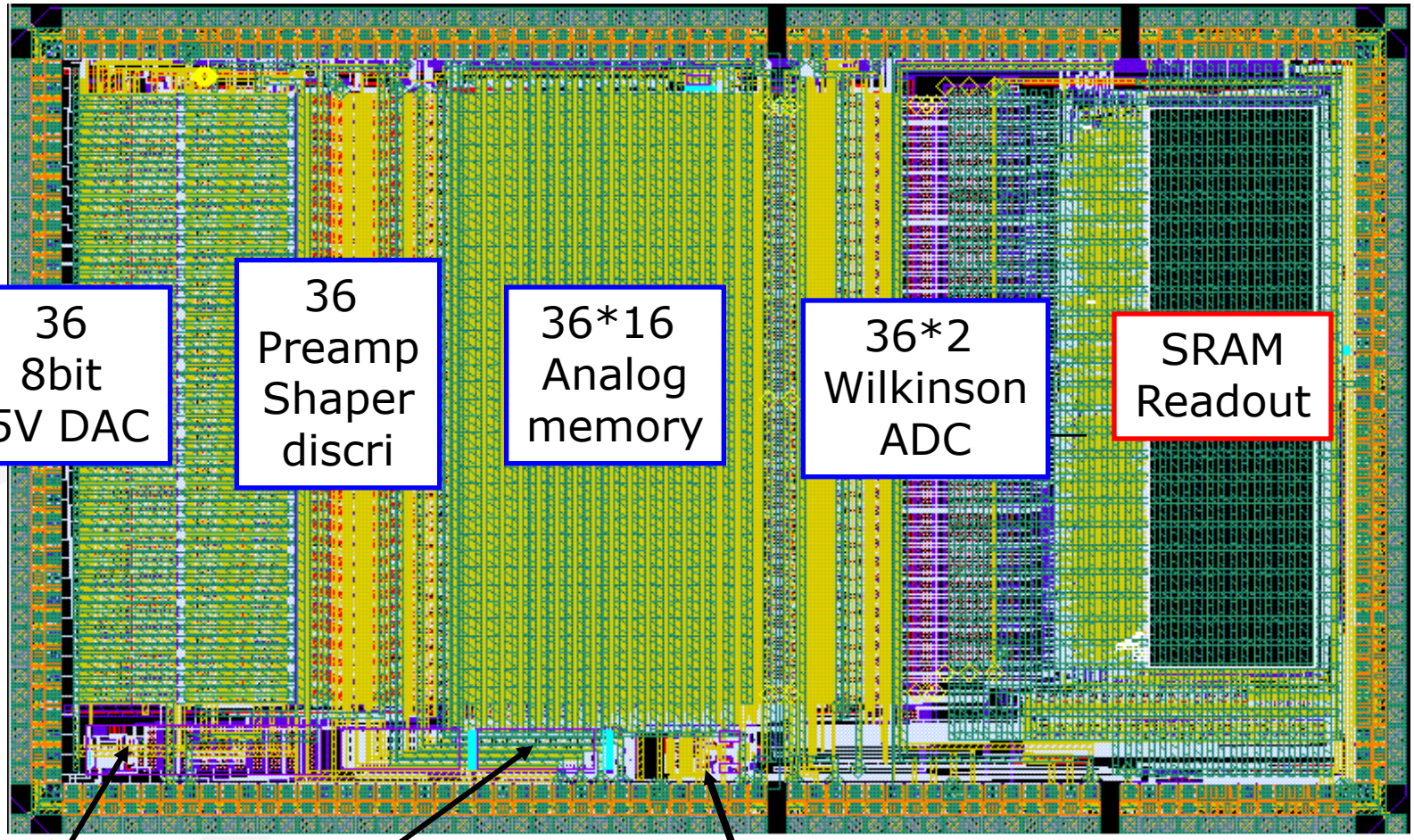


SPIROC : general schematic



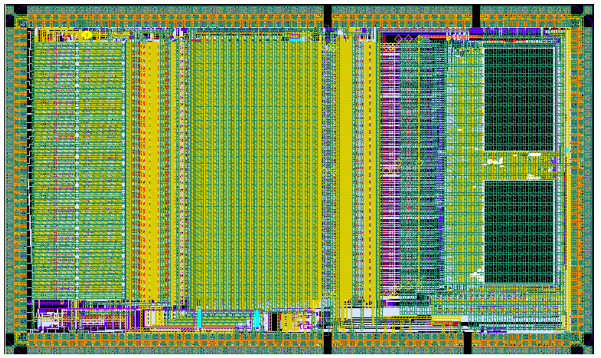
SPIROC layout

Techno : AMS SiGe 350nm - package : TQFP 208 - die size : 8x4= 32mm^2



SPIROC main features

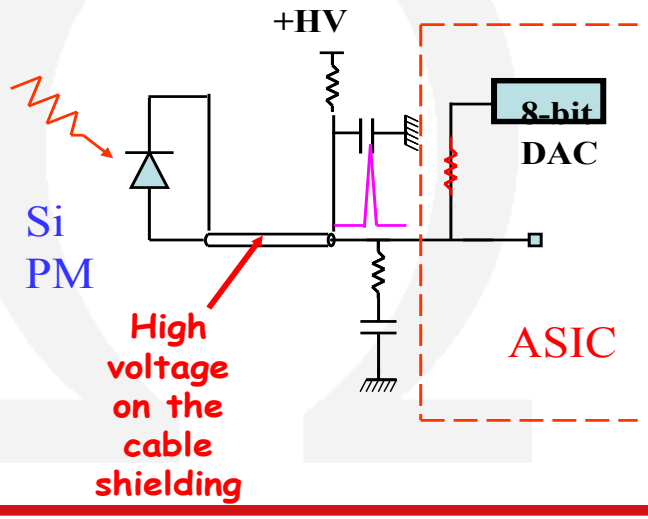
- 36 channels
- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC: **1 pe □ 2000 pe**
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
- Time measurement :
  - 12-bit Bunch Crossing counter (step=200ns)
  - 12 bit TDC step~100 ps

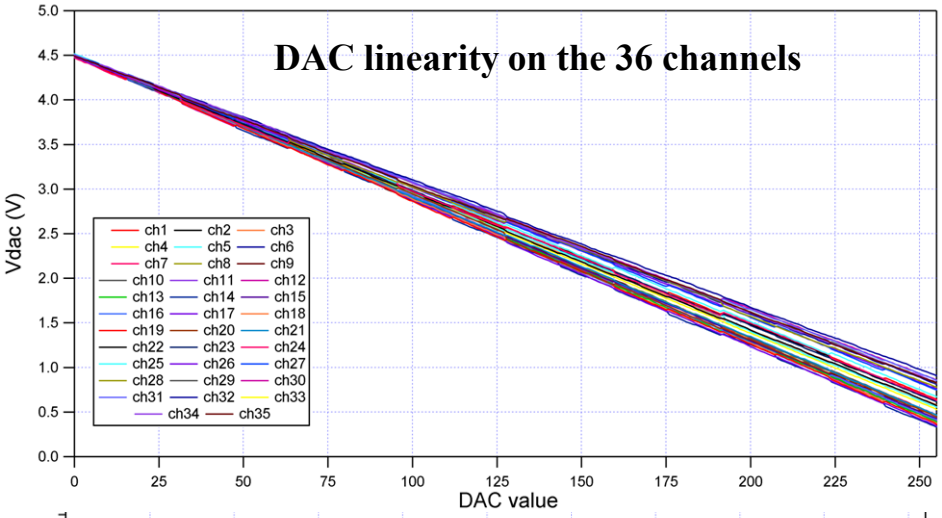


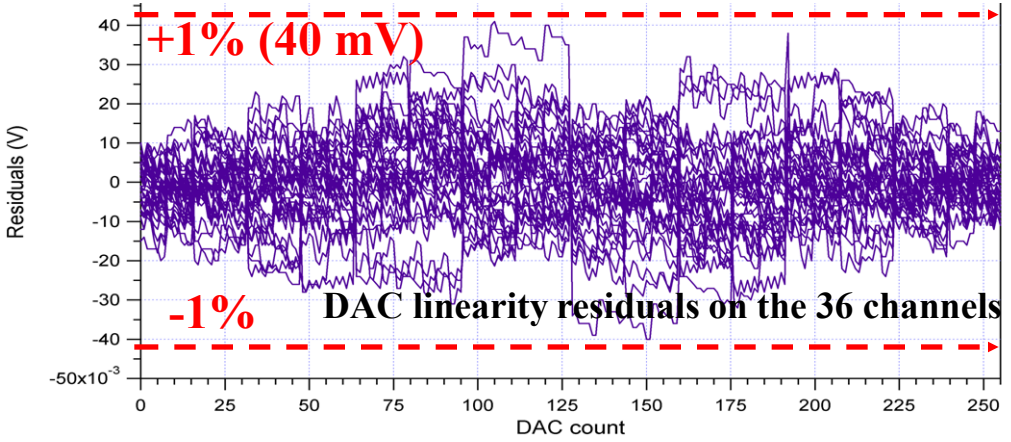
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout

SPIROC2 input DAC

- Input DAC to optimize SiPM bias voltage
- 8-bit DAC, 5V range, LSB=20mV
- 36 DAC (one per channel)
- Ultra low power (<1µW) : no power pulsing
- Can sink 10 µA leakage current
- Linearity : ± 1%
- DAC uniformity between the 36 channels : ~3%

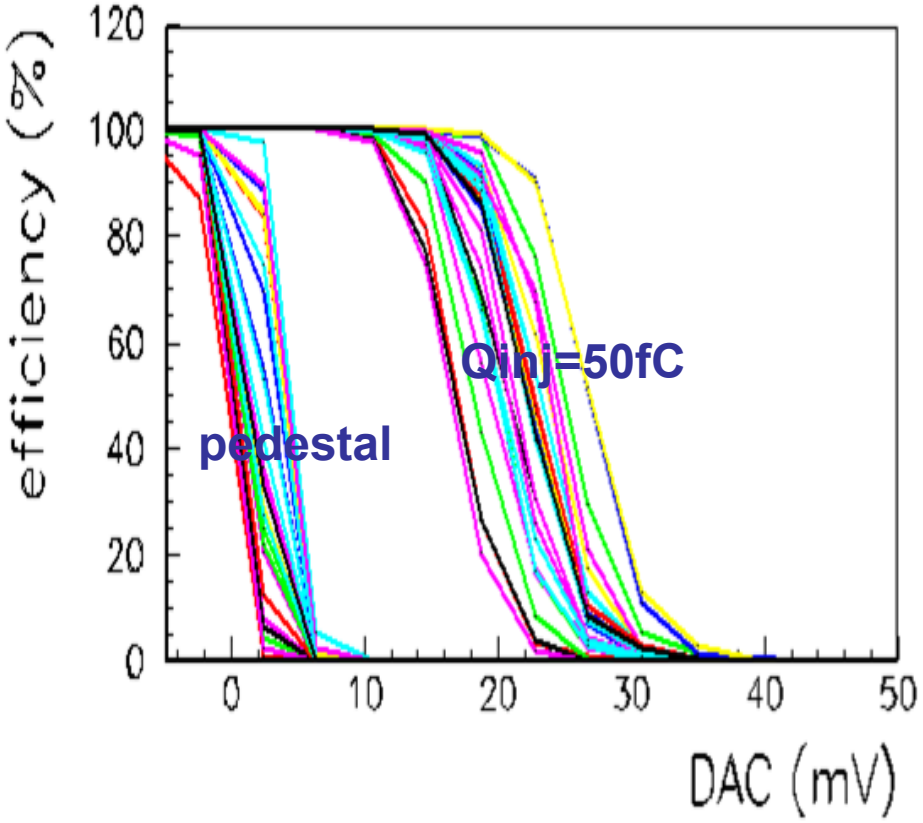


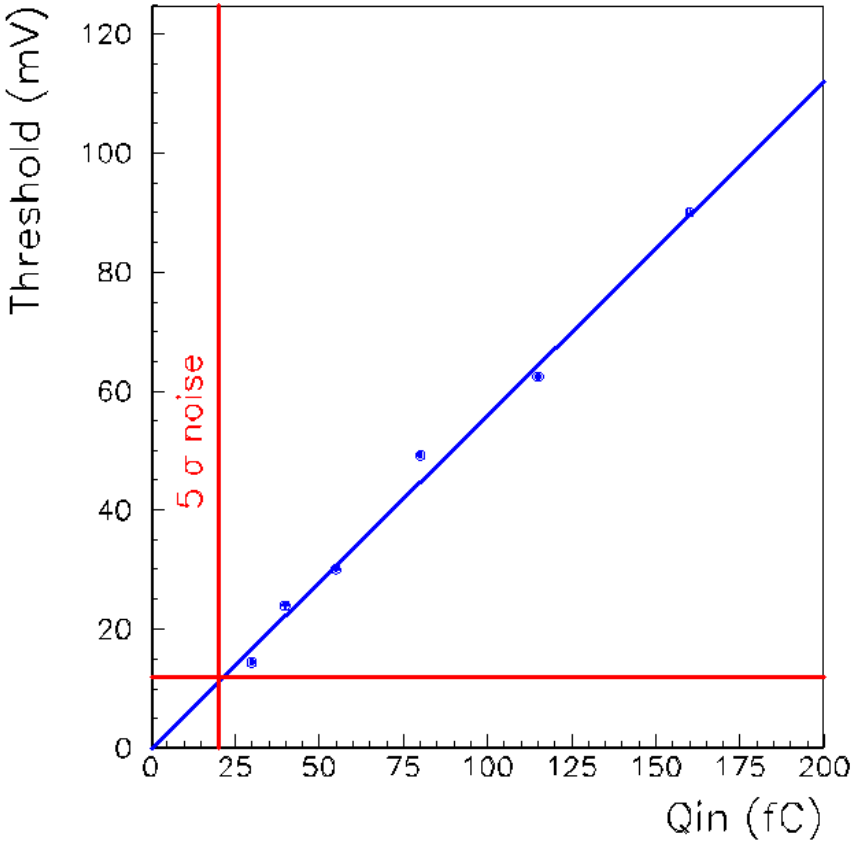




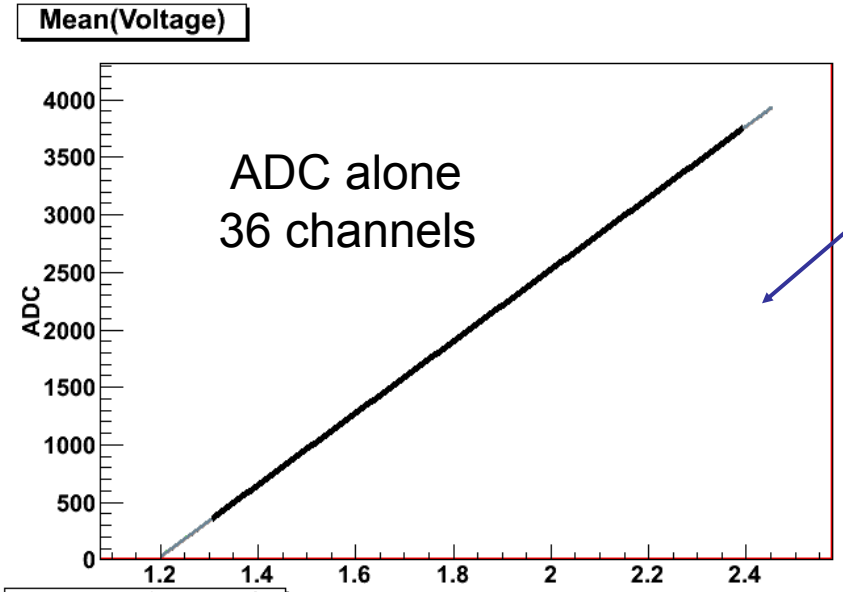
S-curves on fast shaper

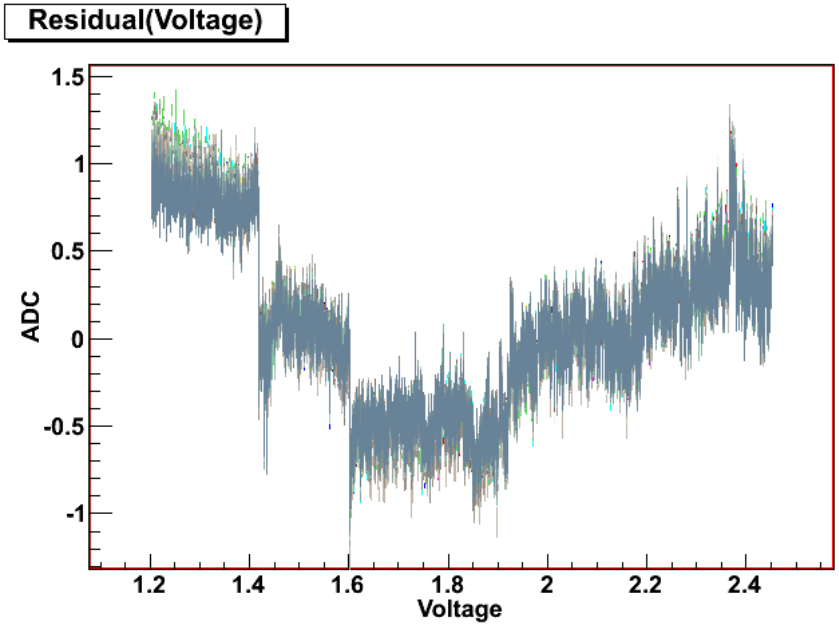
- Trigger efficiency versus Threshold (1UDAC=2mV)
- Qinj=50 fC (1/3 pe-)



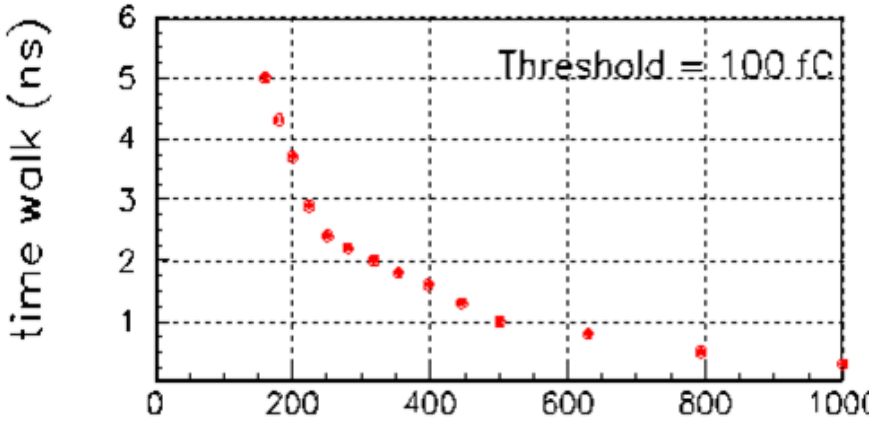


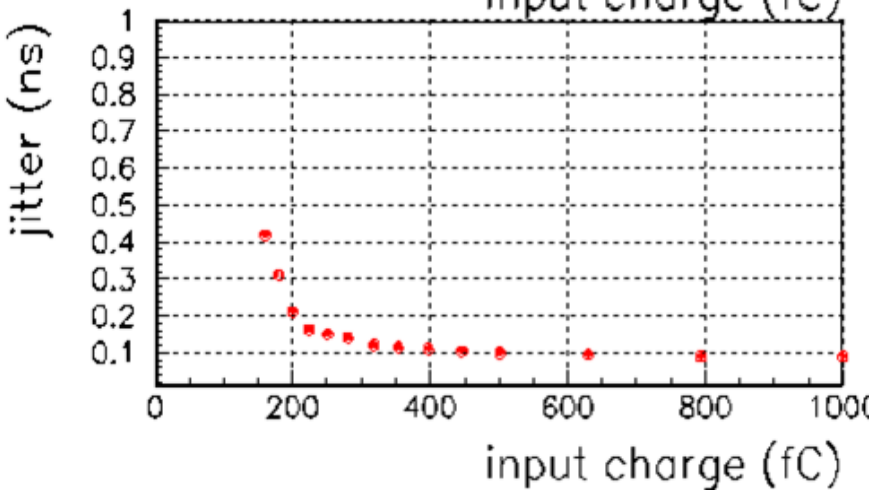
SPIROC2 performance



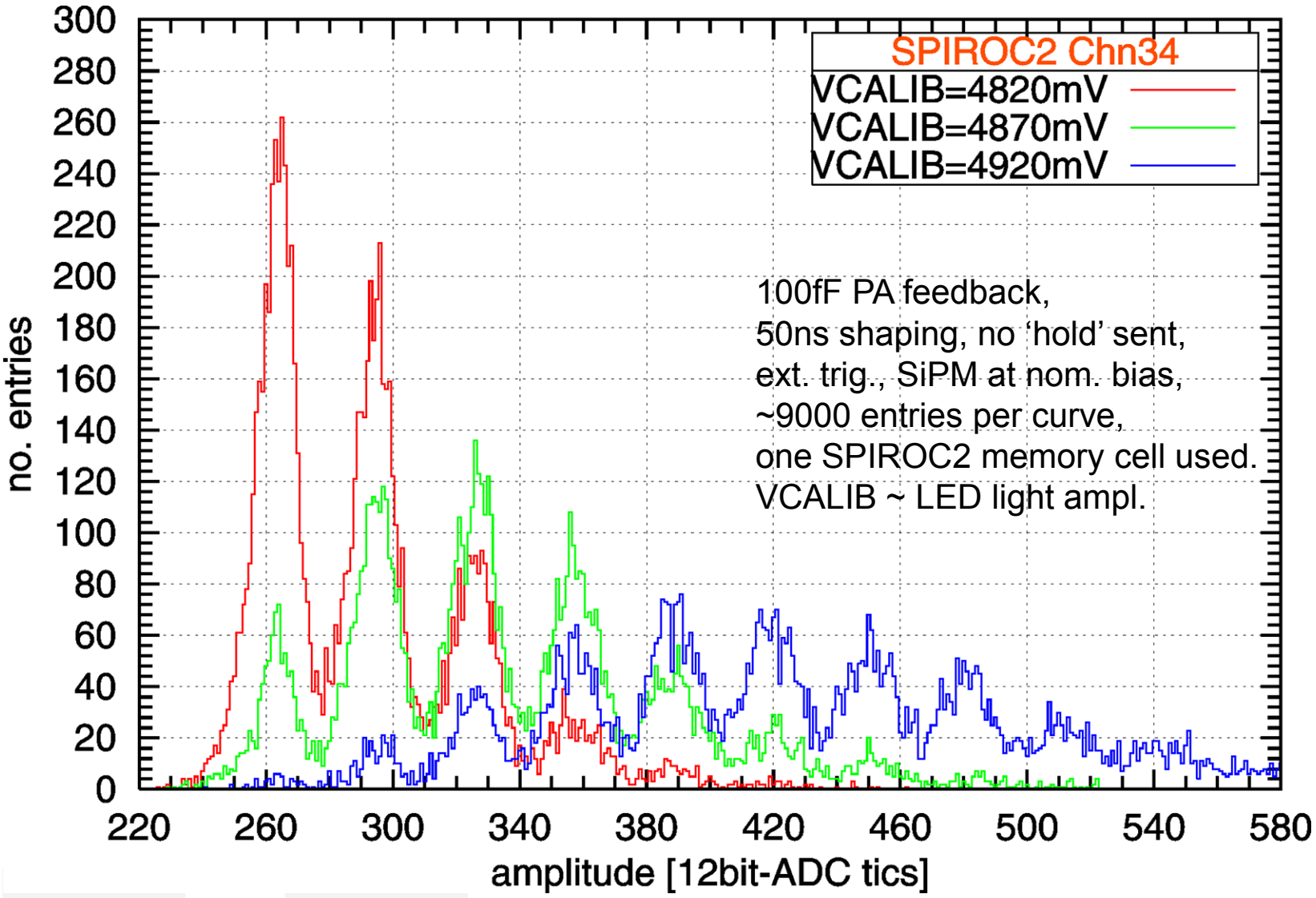


- Wilkinson ADC well suited to multichannel conversion
- Very good uniformity and linearity

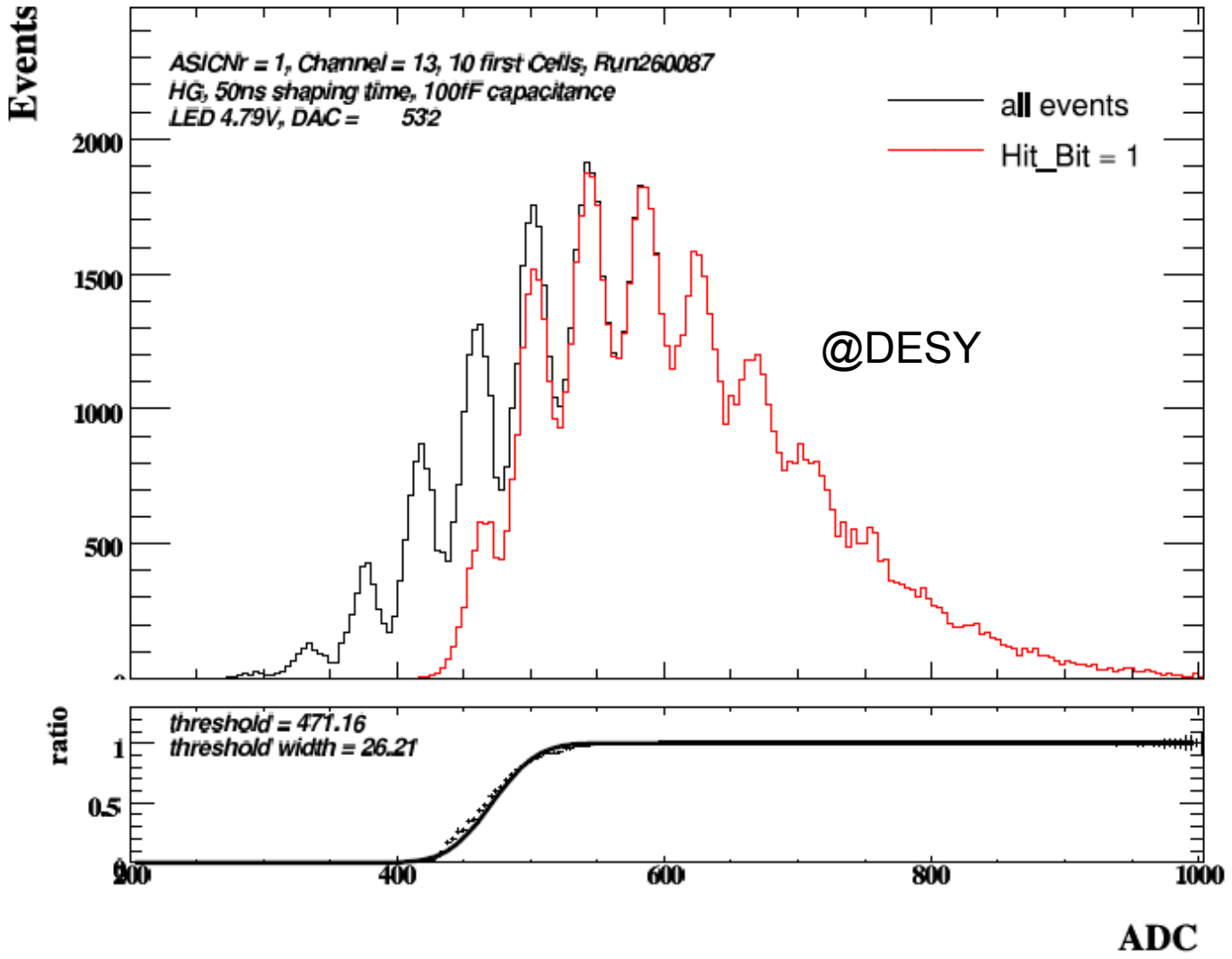




Single-Photon Peaks

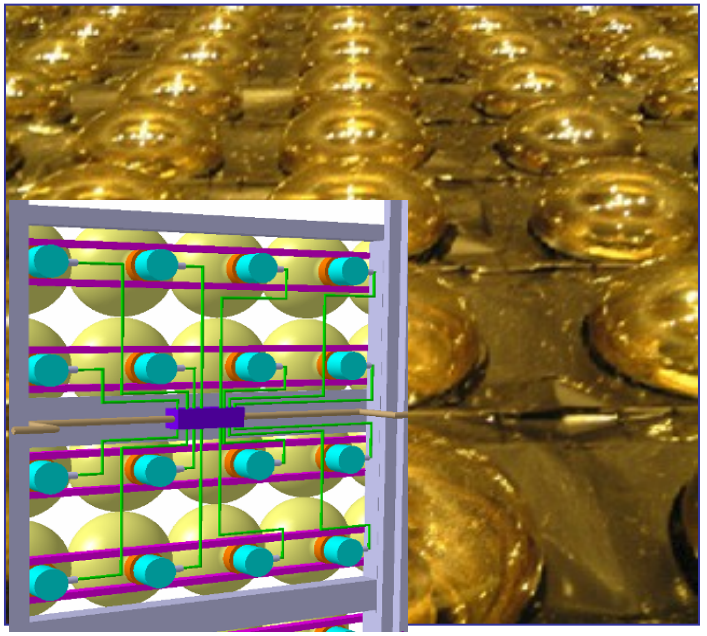


SiPM SPECTRUM with Autotrigger

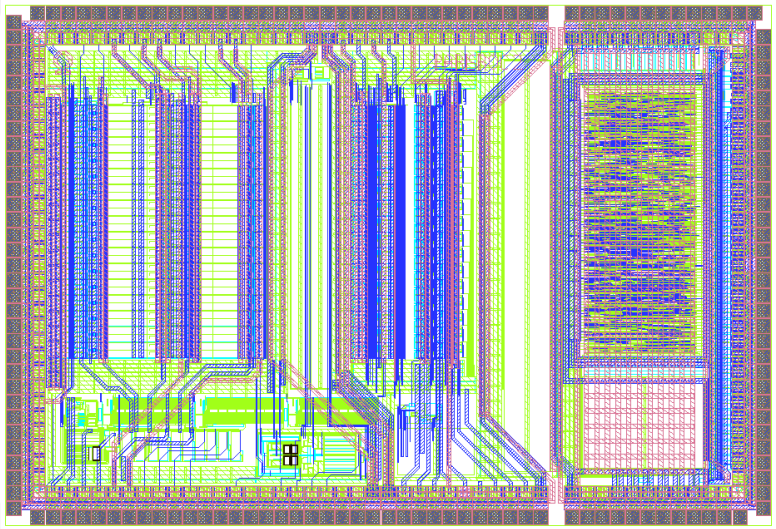


PARiSROC for PMm^2

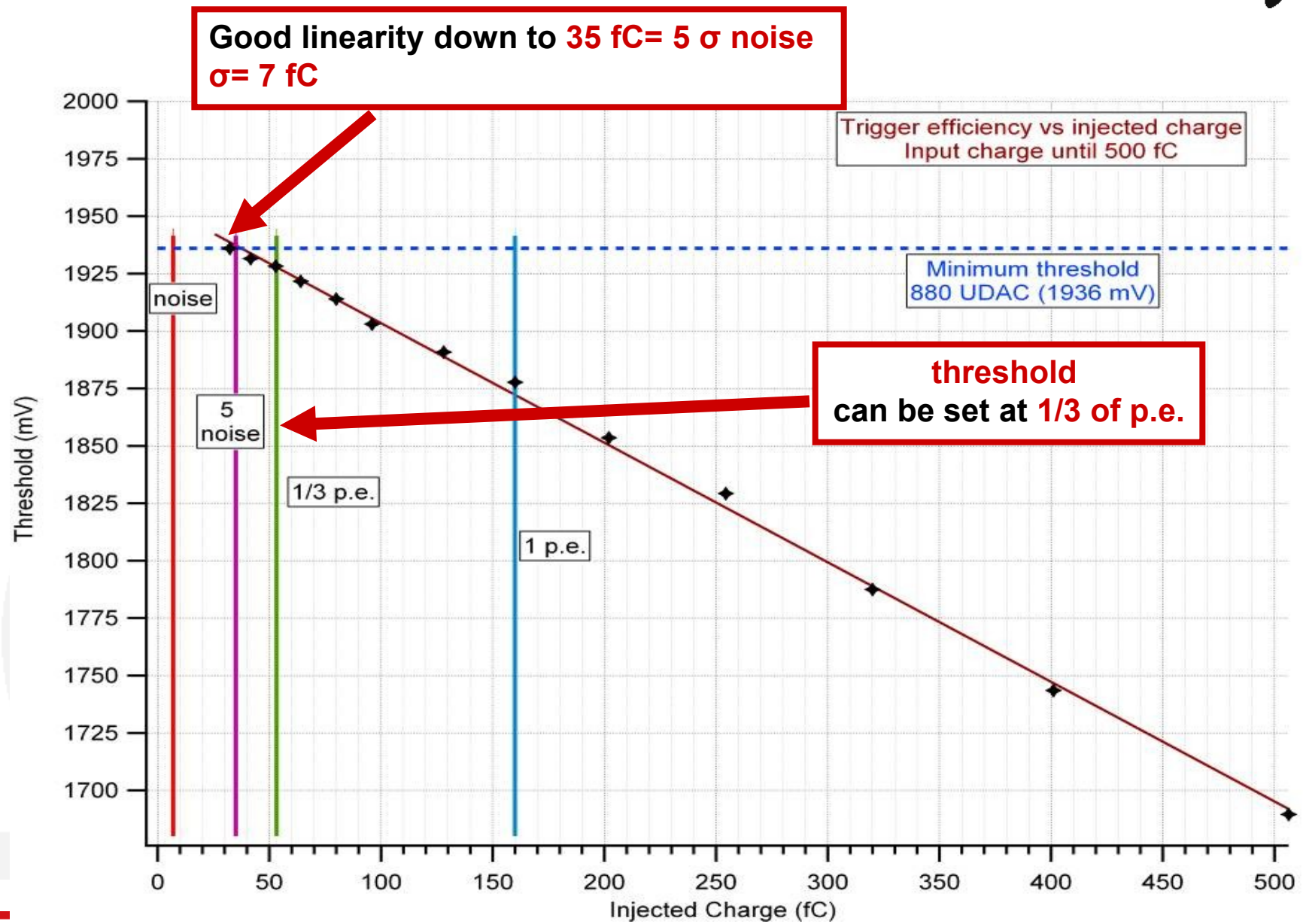
- Photomultiplier ARray Integrated SiGe Read-Out Chip
  - Replace large PMTs by arrays of smaller ones (PMm2 project)
  - Centralized ASIC 16 independent channels
  - Auto-trigger at 1/3 p.e.
  - Charge and time measurement (10-12 bits)
  - Water tight, common high voltage
  - Data driven : « One wire out »



Joël Pouthas IPN Orsay



Trigger efficiency



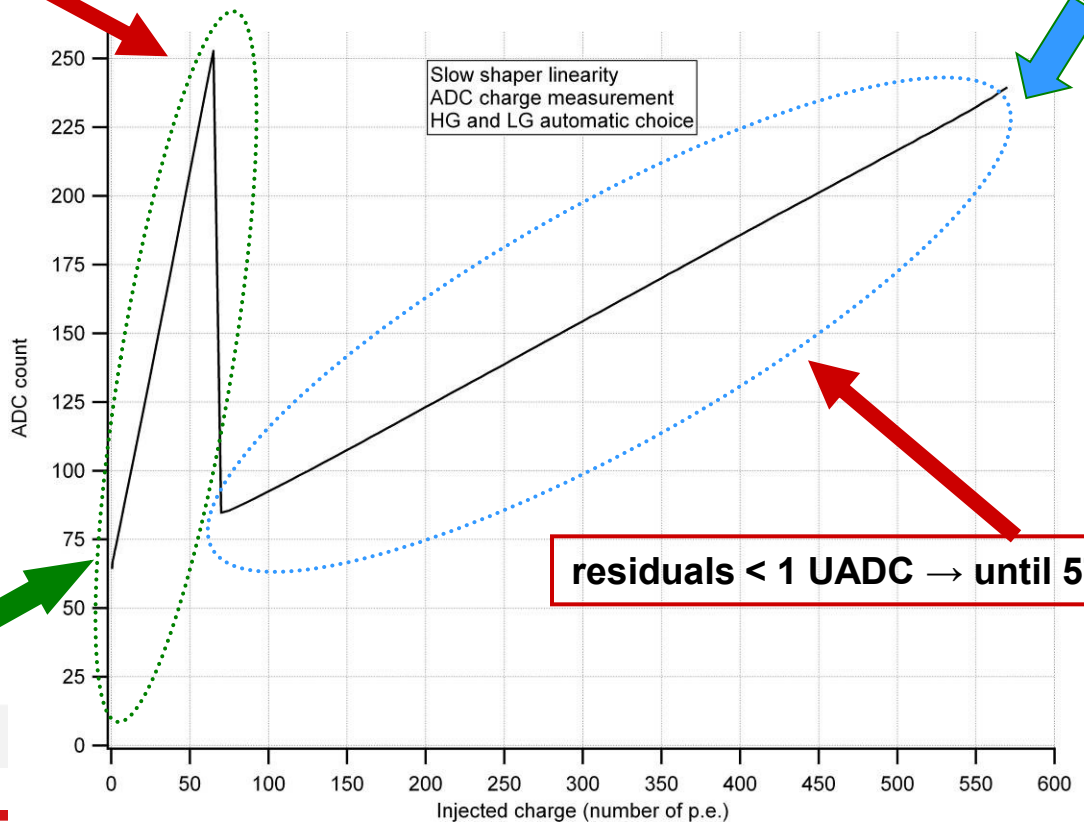
Auto-gain test (ADC measurements)

The whole chain is tested, injecting a charge at the input of the channel: the signal is amplified, auto-triggered, held in the SCA cell and converted by the ADC.

The charge measurements for different injected charges setting the gain threshold at 60 p.e.

residuals < 1 UADC → until 60 p.e.

Low gain Up to 570 p.e.



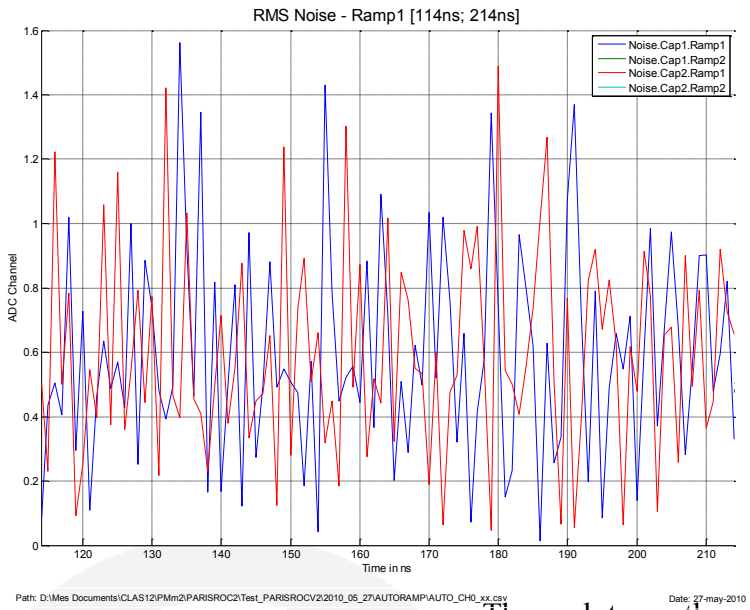
Automatic gain selection

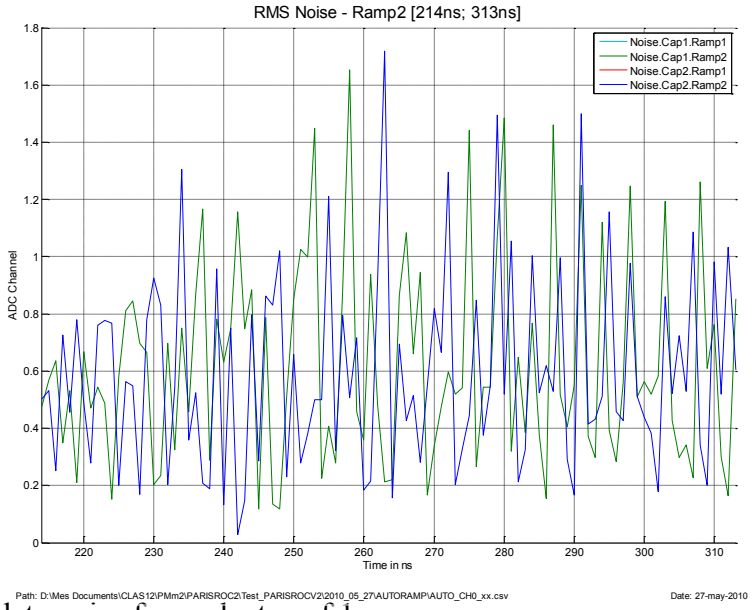
Good performance of the whole chain.

residuals < 1 UADC → until 570 p.e.

High gain Up to 60 p.e.

PARISROC TDC ramps Noise



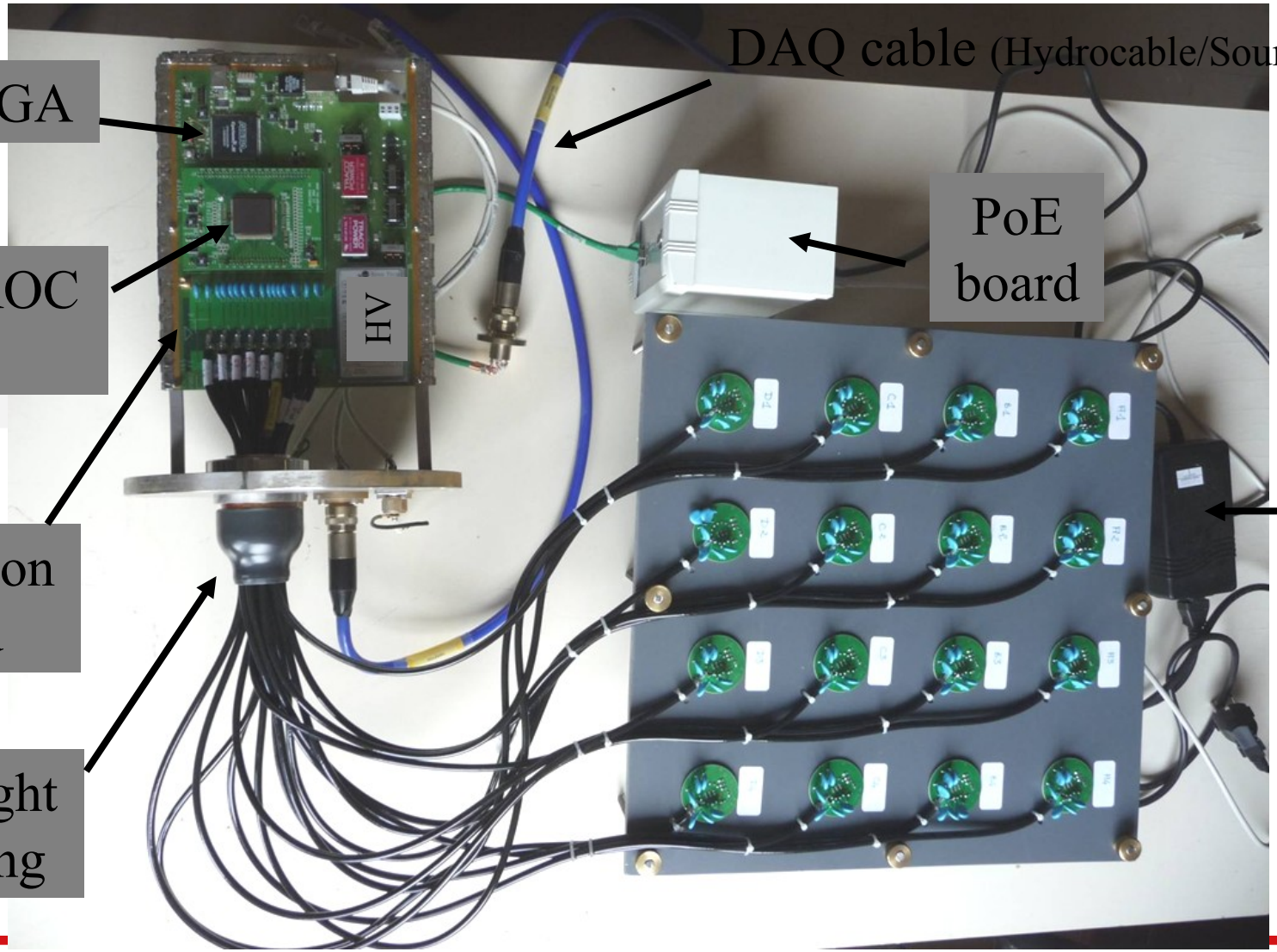


These plots are the row data noise for each step of 1ns.
Do not forget that the generator have a 107ps jitter.

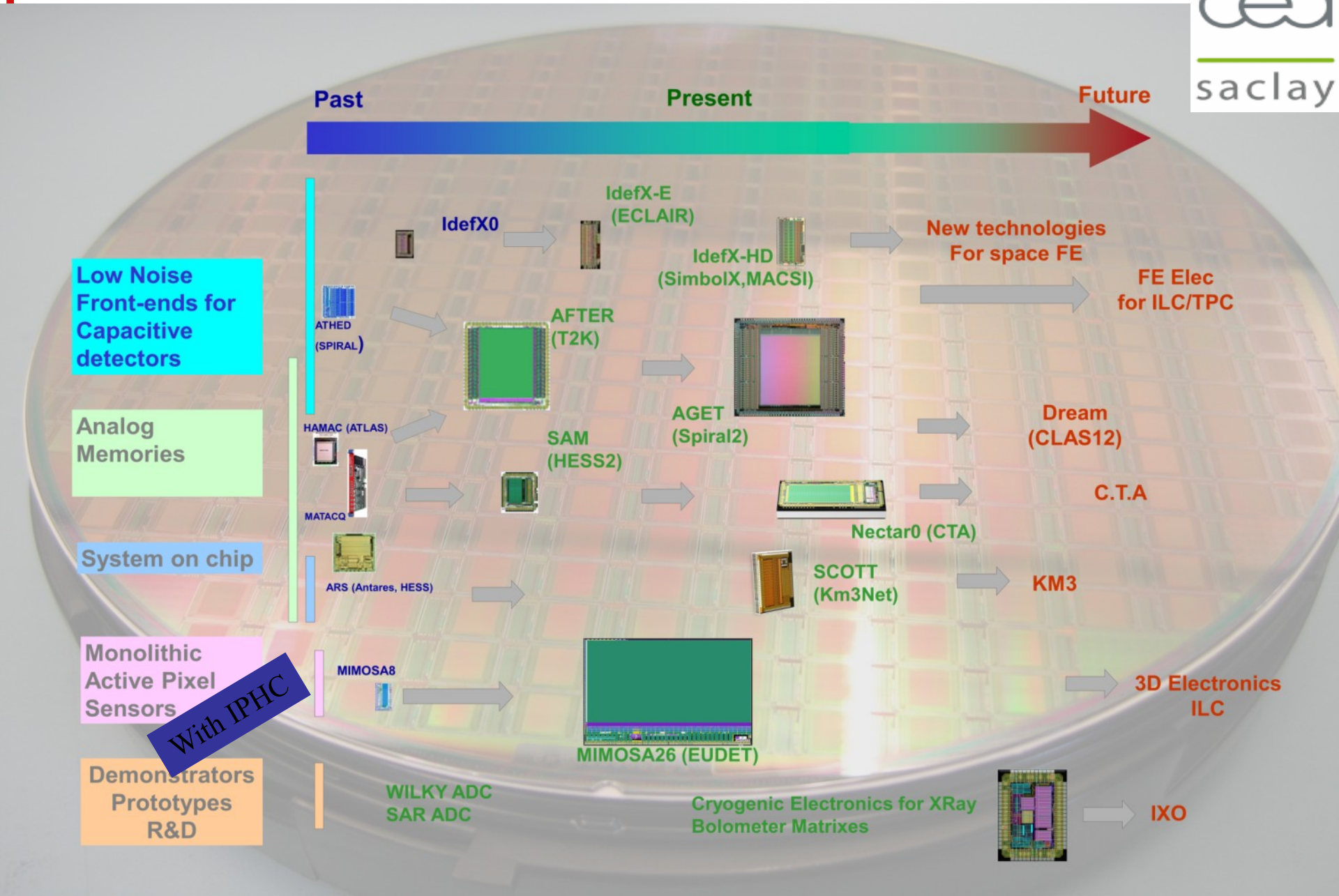
Capacitor	Row Noise (Quadratic Mean)	TDC Noise (Quadratic Mean)	Max TDC Noise
Ramp1.Cap2	0.68ch = 148ps	102ps	306ps
		111ps	
Ramp2.Cap2	0.68ch = 147ps	101ps	356ps

PMm2 demonstrator

IPNO+LAL+LAPP+ULB



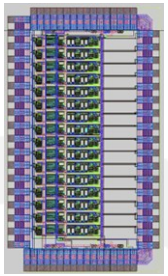
Asic ROADMAP @ Irfu Saclay

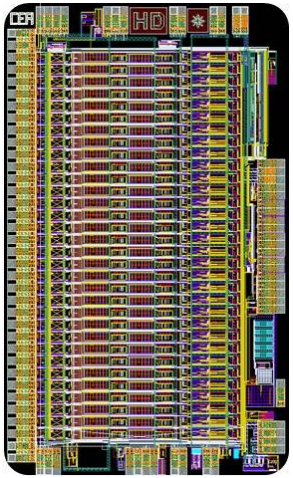


The Idef-X Family

COMMON BASIS => Idef-X family:

- **For low or very low capacitance detectors (CdTe , or Si & LXe)**
- **Same CSA, PZ, Filter, (discriminator, peak detector) architecture**
- **Detector leakage current compliant.**
- **Use of a custom digital library for latchup free design.**
- **technology tested for space environment: AMS 0.35µm**





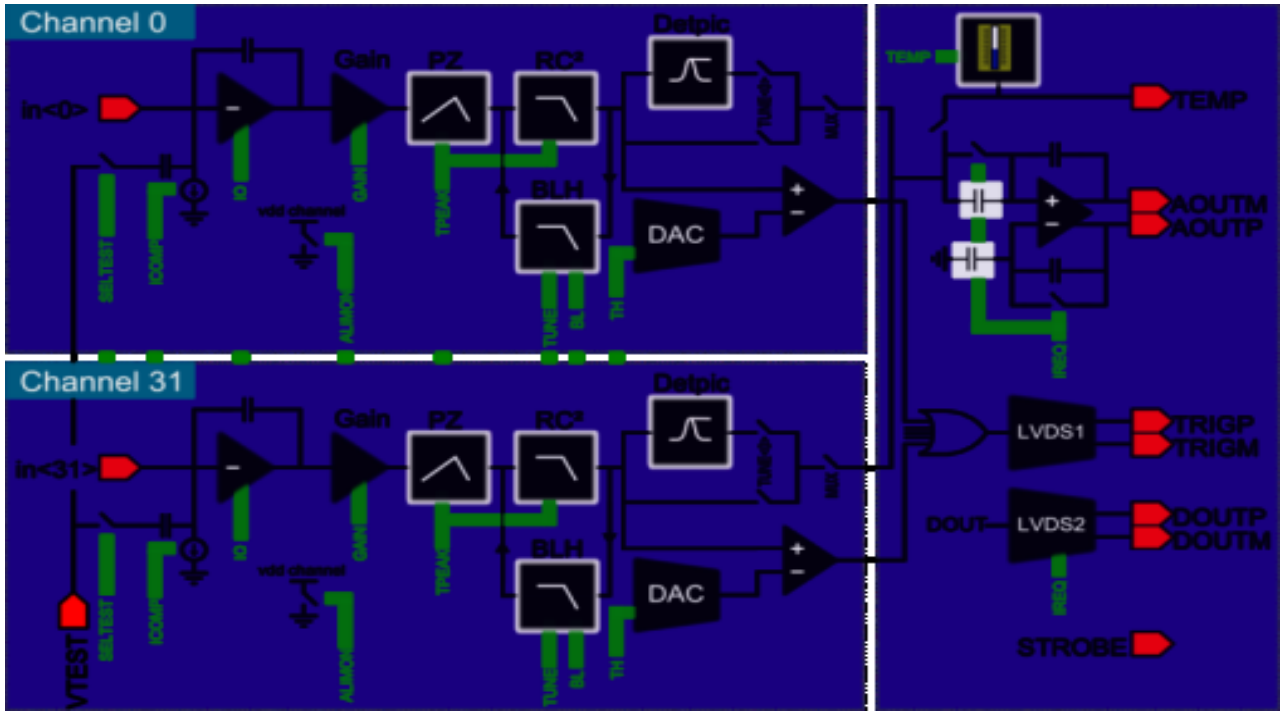
time

IdefX1.1:
16 channels.
Parallel analog outputs

IdefX-Eclairs:
32 channels.
Multiplexed outputs.
1 Range 200keV
<3mW/ch

IdefX-HD:
32 channels.
Multiplexed outputs.
4 Ranges up to 1.2MeV
Low power: 0.8mW/ch

IDeF-X HD (the more recent chip): Architecture



- 32 channels. Muxed output
- CSA (new concept)
- Gain (50, 100, 150, 200mV/fC)
- PZ cancellation
- RC² filter (T_{PEAK}=1 to 10µs)
- Base Line Holder (switchable)
- Peak detector

- 1 Threshold/ channel (6 bits)
- Dynamic up to 1.2MeV (CdTe).
- "OR" Trigger output.
- 3 modes of readout:
  - All channels.
  - Hit channels.
  - On demand

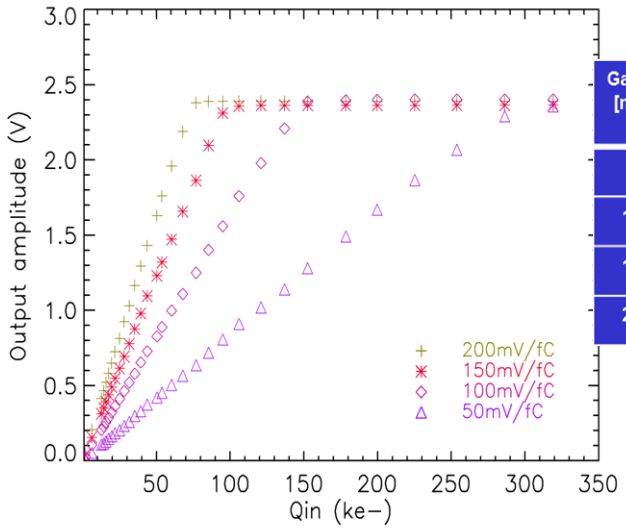
- Embedded temperature Sensor with absolute resolution of 0.5°C.
- Energy and T readout via differential output buffer.

- Slow Control
  - ü Multi ASIC interface
  - ü Gain
  - ü T_{PEAK}
  - ü I_{CSA}(23-100µA)
  - ü I_{LEAK}
  - ü Channel mask
  - ü Test mask
  - ü AlimON
- Power on reset
- LVDS input/output with tunable current
- Hardened digital standard cells

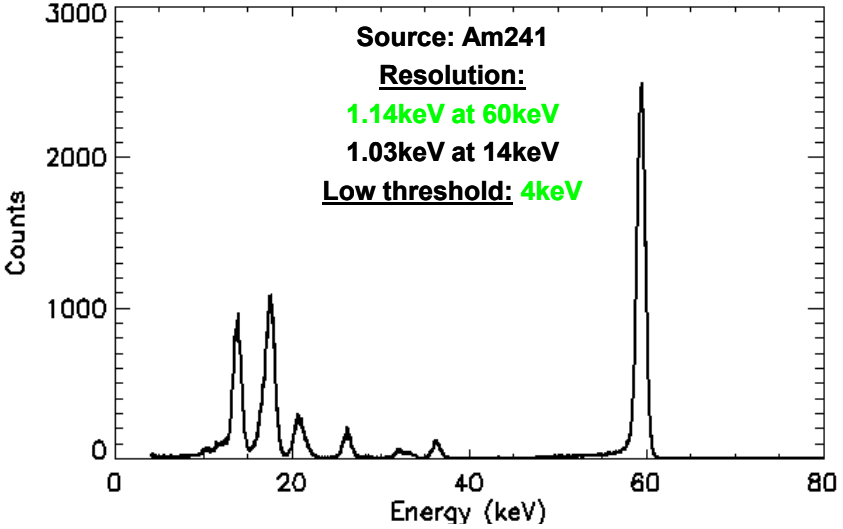
• Low power: 0.8mW /channel

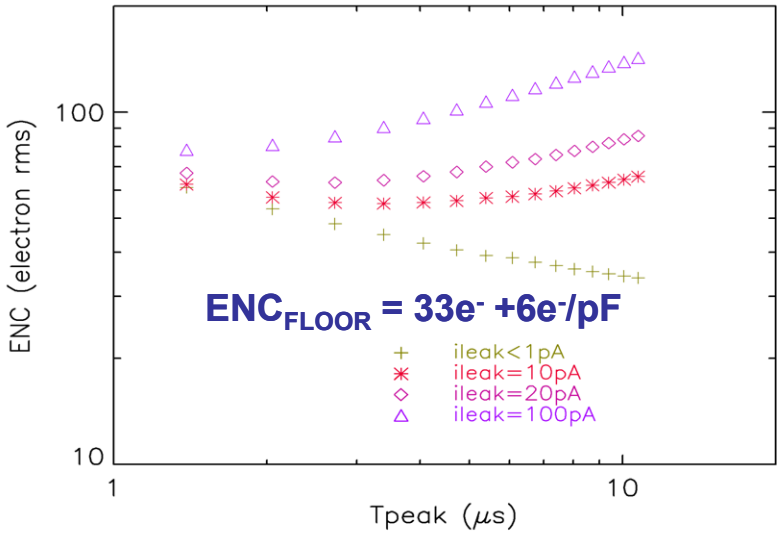
Idef-X HD: performances

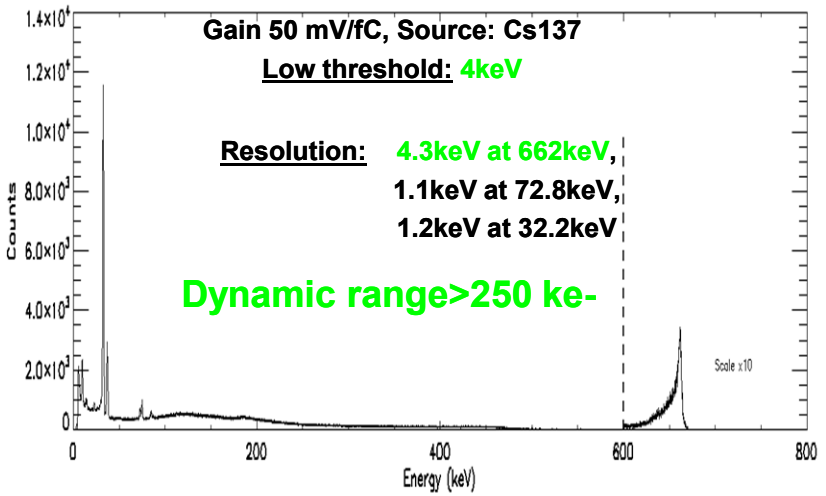
CdTe Schottky 2x(2x2xmm²), -10⁰C,



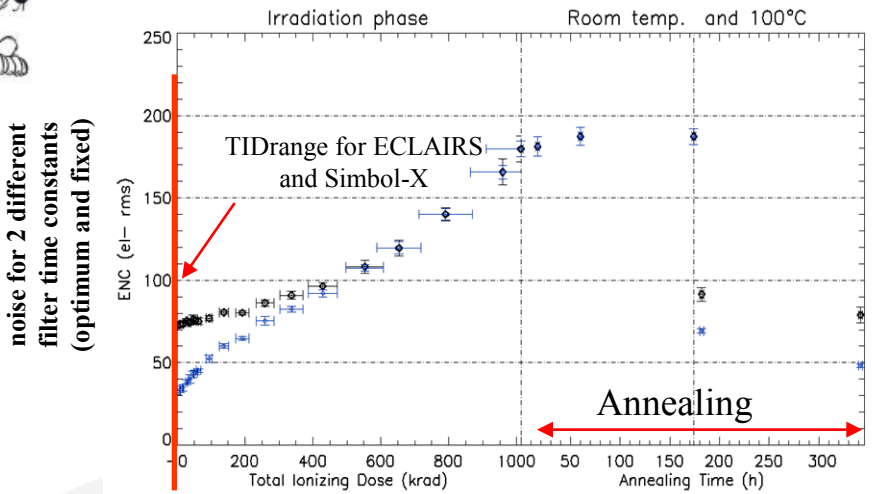
$Gain_{MEAS.}$ [mV/fC]	Dynamic range [fC]	Dynamic range CdTe [eV]	INL [%]
51.8	36	993 k	1.19
102.2	22	607 k	1.39
152.5	13.5	372 k	1.04
203.8	11	303k	1.16







– TID: Irradiation with 60CO @ 500rad/h



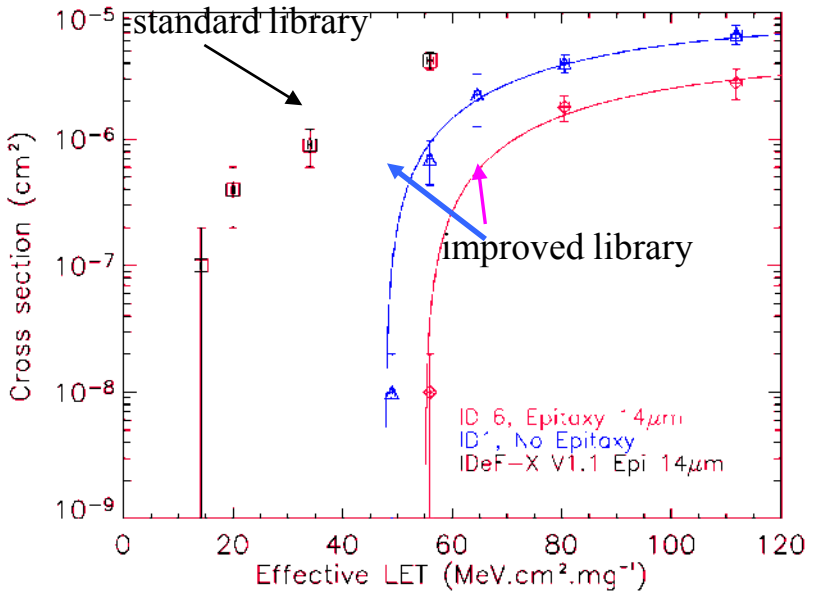
noise for 2 different filter time constants (optimum and fixed)

Irradiation up to 1 Mrad:

–only effect noise increase (cleared after annealing).

–Leakage on ESD diodes suspected

–The Spec for ECLAIRs and SIMBOL-X is only 10krad



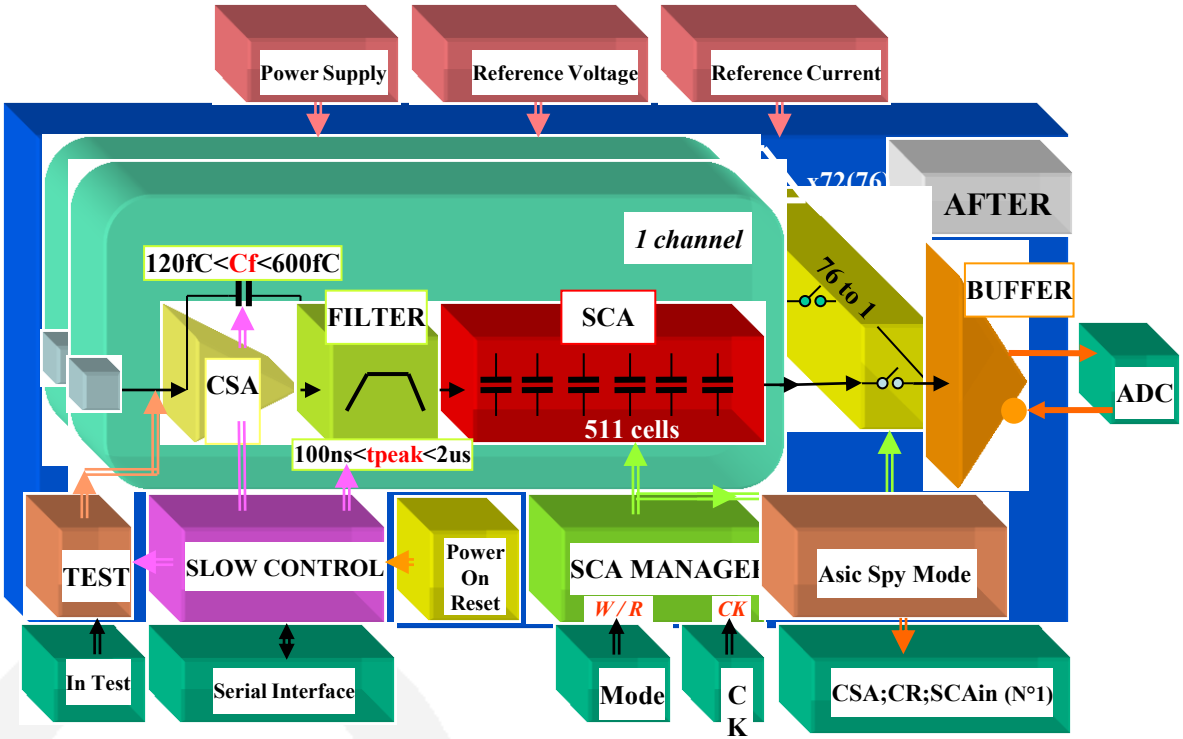
SEL Tests

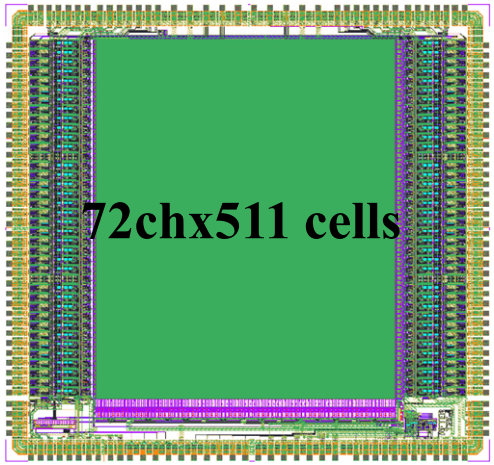
New digital library to improve hardness against Single Event Latchup:

Test on Idef-X V2.E => no anti latchup circuit required for the ECLAIRs mission.

No Latchup seen @ 110 MeV for IdefX HD.

AFTER: Asic For TPC Electronic Read-out





IEEE Trans. Nucl Sci, June 2008

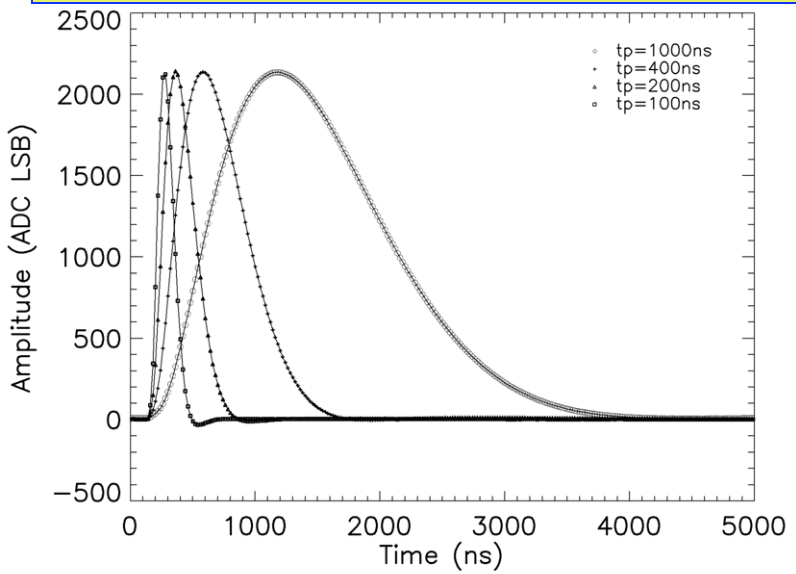
Main features:

- Input Current Polarity: positive or negative
- 72 Analog Channels
- 4 Gains: 120fC, 240fC, 360fC & 600fC
- 16 Peaking Time values: (100ns to 2µs)
- 511 analog memory cells / Channel:
  Fwrite: 1MHz-100MHz; Fread: 20MHz

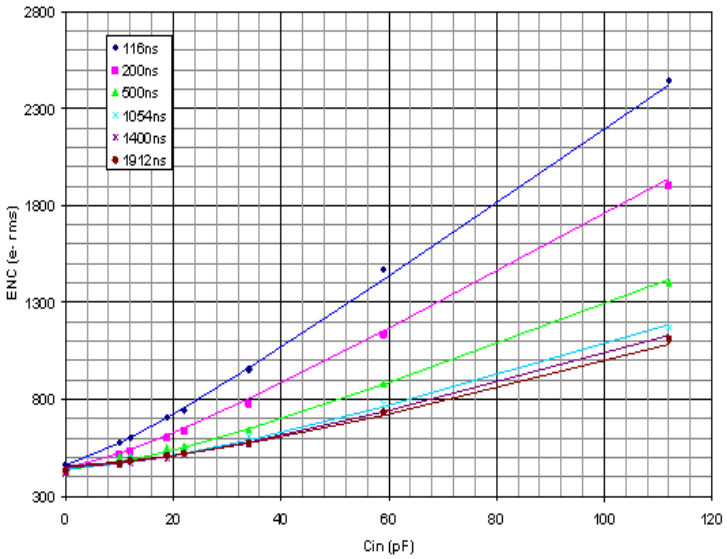
- Optimized for 20-30pF detector capa
- 12-bit dynamic range
- Slow Control
- Power on reset
- Test modes
- Spy mode on channel 1:
  CSA, CR or filter out

Pulse Shape + linearity

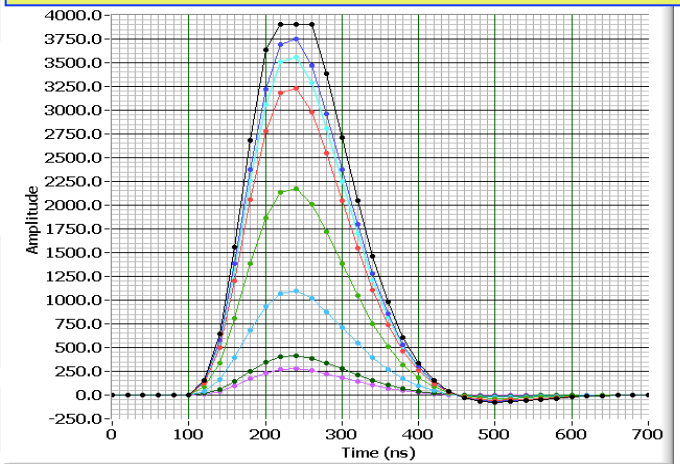
Digitized signal with various peaking time



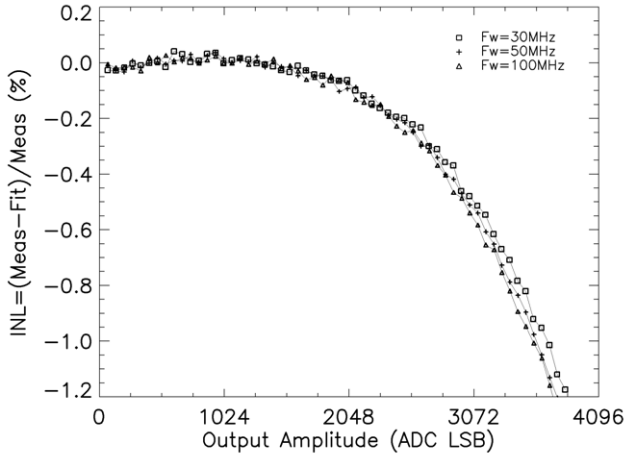
Good noise performance



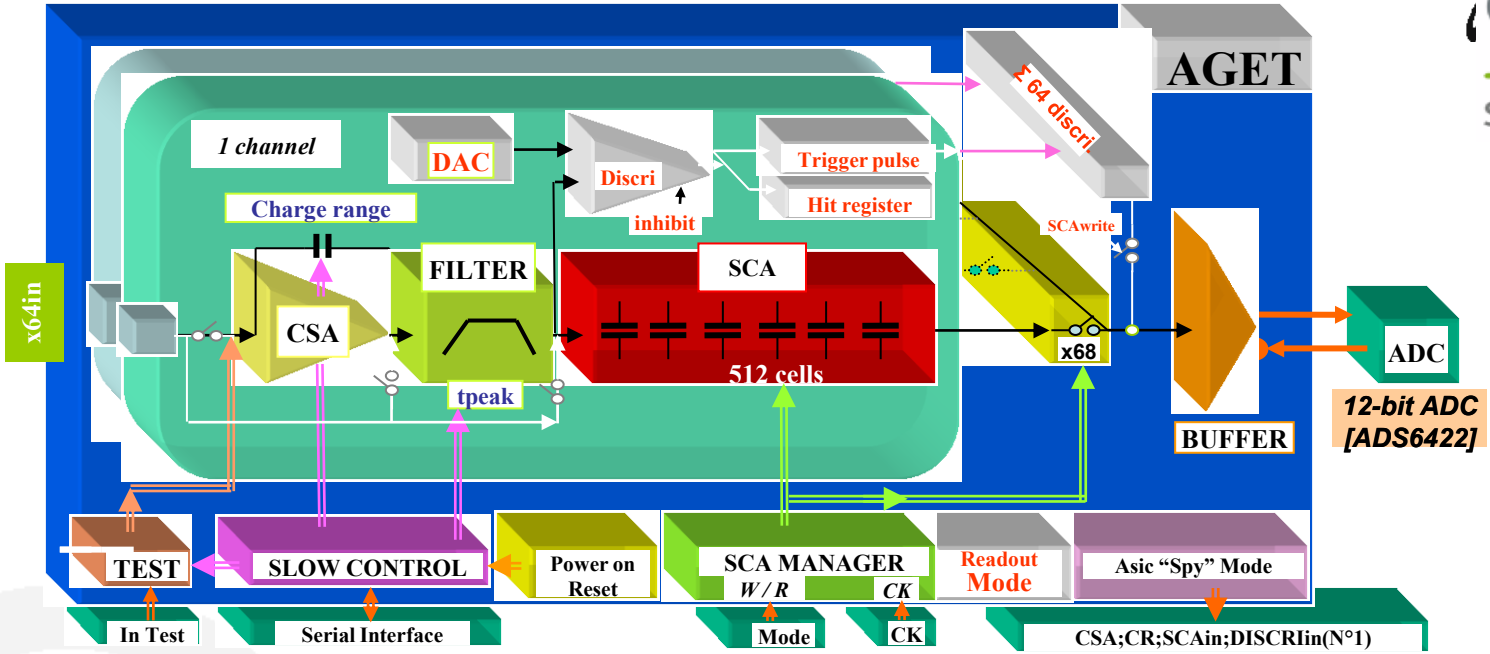
Pulse Shape Independent of amplitude



Integral Non Linearity <1.2%



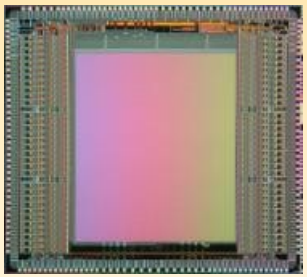
AGET: General ASIC for active target TPCs



- **64 Analog Channels: Analog part + Sampling Capacitor Array.**
- **CSA + PZC + Filter (semi-Gaussian order 2).**
- **SCA: 512 analog memory cells.**
- **AUTOTRIGGERING CAPABILITY**
- **Programmable Readout Offset**
- **Discriminator + Threshold DAC/Channel + mask.**
- **Digital Trigger output (LVDS)**
- **Multiplicity Output [Analog sum of the discri outputs.].**
- **High Charge range (10pC)**
- **Several SCA readout modes (all, zero-supress, on demand)**

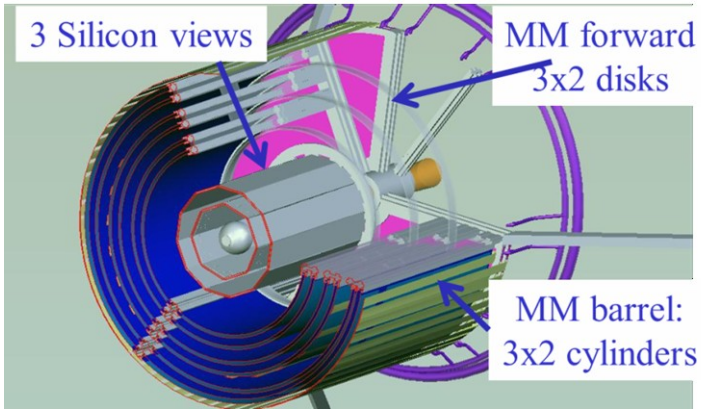
NEW

- **Slow Control.**
- **Power on reset.**
- **Test modes.**
- **Spy mode.**
- **Channel inhibit**



DREAM (Deadtimeless Readout Analog Memory)

Designed to read the ~20000 channels of a Micromegas tracker for the CLAS12 upgrade @ JLAB (Virginia).



More than 5m^2 of stripped detectors.
~30k channels

Based on AGET structure, but:

- **64 channels with "everything" tunable.**
- **Design for high detector capacity (ENC <1500 e- for t_p=150ns @200pF)**
- **Dead Time "Free" readout (APV-like structure) :**
  The 512 cell Switched Capacitor Array is used as a **circular analogue buffer** (both L1 latency buffer + derandomizing buffer).
- **No limit for the number of cells kept for an event.**
- **Normal operation with external trigger, but autotriggering capabilities available.**

- **Chip submitted in beginning of June 2011.**

NECTAR: a 3.2GS/s digitizer for CTA*

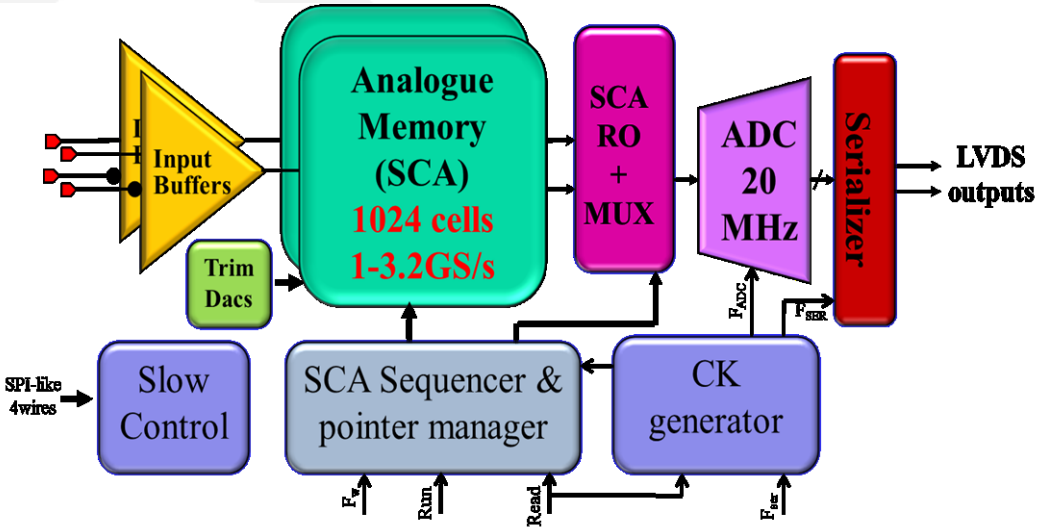
* Program supporrted by French ANR

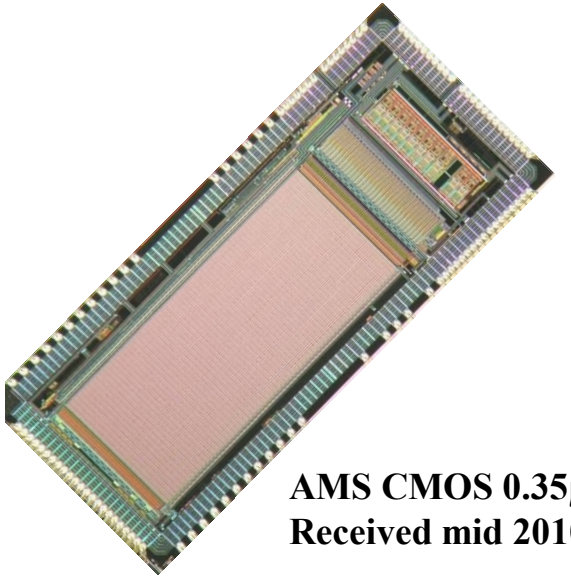
CTA:

- project of a large Atmospheric Cherenkov Telescope Array.
- 100 telescopes with each more than 1000 PMT. ~16 bit range required (2gains)
- Need for fast integration time (typ 6ns) to reduce the effect of Night Sky Background.
- Use of low cost and proven solutions (HESS, Magic 2) => use of fast analogue memories as L1 Buffer.

NECTAr:

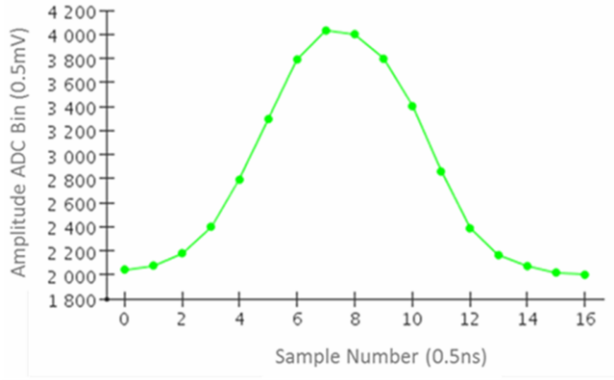
- 2 differential channels of 1024 cells SCA with 400 MHz bandwidth (DLL-matrix structure)
- Sampling rate in the 1-3GS/s range.
- Digitization of a window of interest by a 20 MS/s pipeline ADC (IP from IN2P3/LPSC) after a trigger is received.
- Serialization of ouput data @120MHz on 2 LVDS pair



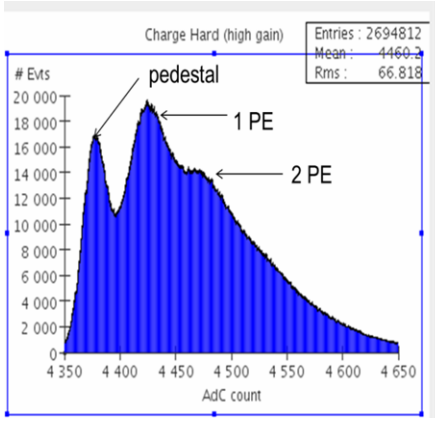


AMS CMOS 0.35µm
Received mid 2010

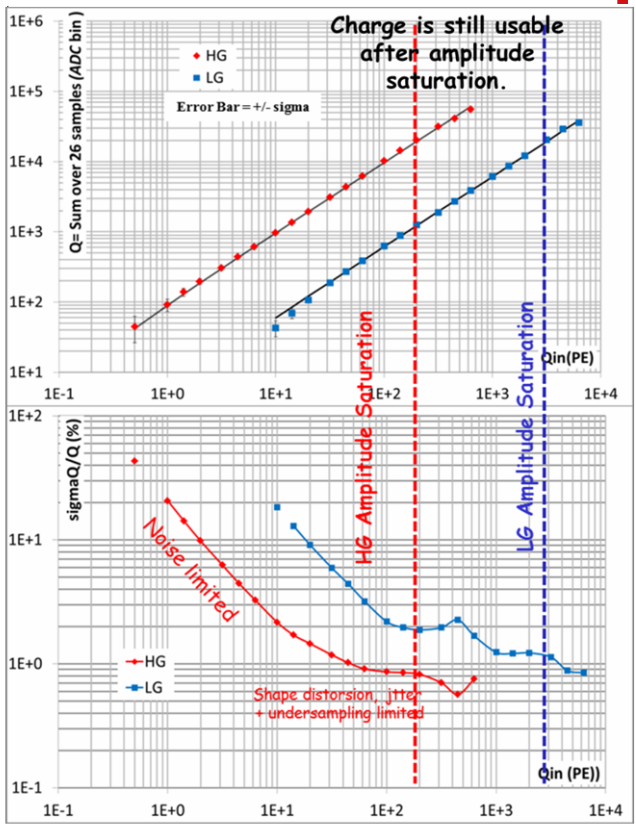
TAR: Performances



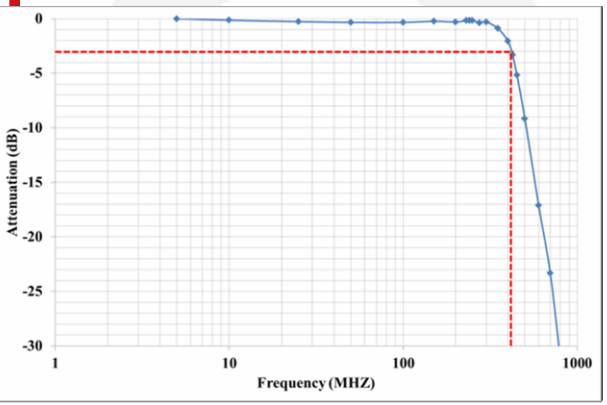
Photoelectron signal digitized by NECTAR:2.4ns FWHM,half range pulse sampled @2 GS/s



Photoelectron Spectrum with Hamamatsu R9619mod PMT (2E5 Gain + on board HG=16)



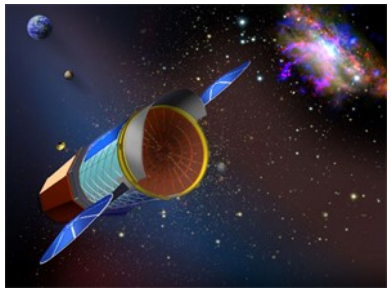
Charge Scan & Q resolution with simulated PE pulses, 2GS/s (the 2 Nectar channels are connected respectively to ampli with gain 1 and 16) . More than 10,000 usable range



-3dB Bandwidth is llarger than 400 Mhz For 0.8V peak-peak sinewave

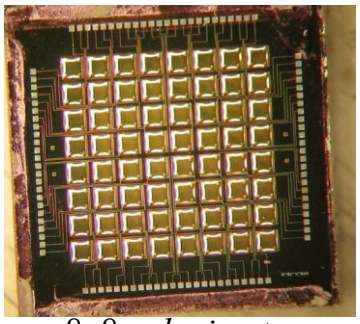
	Nectar0 performance	Unit
Power Consumption	< 300	mW
Sampling Freq. Range	0.5- 3.2 GS/s	GS/s
Analog Bandwidth	>400MHz	MHz
Read Out time for a 16 cell event (2 gains 1- cells)	<2	µs
ADC LSB	0.5	mV rms
Total noise (unchanged with frequency)	< 0.8mV	mV rms
Maximum signal (limited by ADC range)	2V	V
Dynamic Range	>11.3	bits
Crosstalk	4	per mil
Relative non linearity (integral)	<2% (quasi DC)	%
Sampling Jitter	< 40 rms (from resolution)	ps rms

Ultra Low Temperature Mux for XRAY micro calorimeter



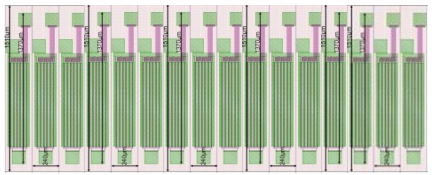
Satellite IXO

- **Target: IXO** satellite (ESA)
- **High resolution** (5eV @ 6kEV) **XRay spectro-imager**
- **fine pitch:** 4000 pixels
- Calorimeter Matrix manufactured by **CEA/LETI**
- Detector temperature : 50 to 100mK
- Photon by photon detection => high speed FE



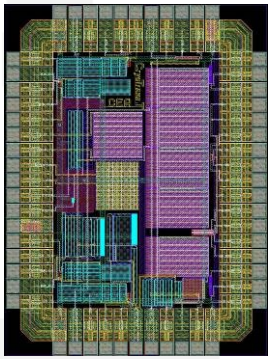
8x8 calorimeter matrix prototype

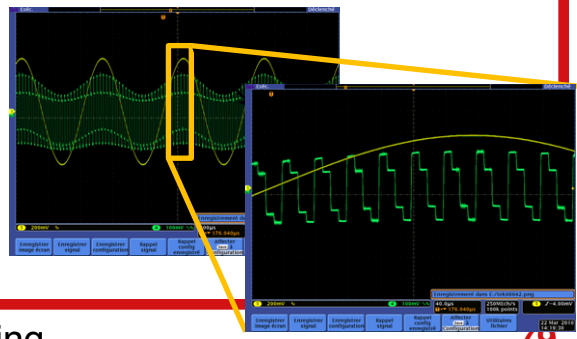
- Front_End electronics close to the detector:
- **Must operate @ 4K**
- Amplify and multiplex the detector pulses
- Low noise, low power **(30µW/channel)**
- **Technological choices:**



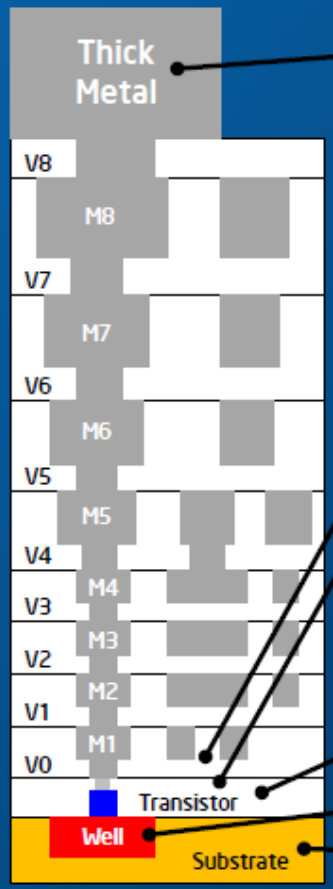
Multi HEMT chip.

  - HEMT (from CNRS/LPN) for the first stage (impedance adaptation + gain).
  - **AMS 0.35µm SiGe chip for extra gain and mulitplexing:**
    - Prototype circuit (8 channel Mux) submitted in July 2009
      => Analogue and digital working perfectly @ 4K
    - Design of an optimized 34 channel Mux in progress

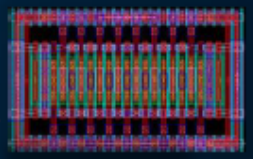


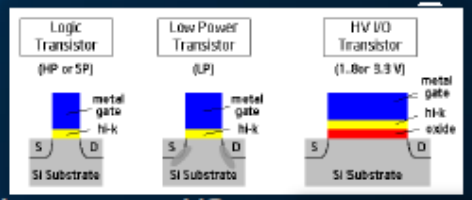


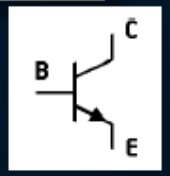
32 nm RF CMOS Technology

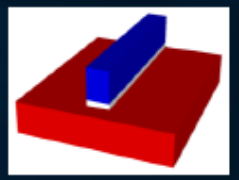


- TM1 Inductor: high Q and density
- Passives:
  - Precision Resistor
  - High Q Inductor
  - High Density Decap
- HV PA Transistor
- RF Transistor: Templates/Modeling
- Transistor:
  - Logic, low power, I/O
  - JFET, BJT
- Well: Triple Well/Deep Nwell
- Substrate: High Resistivity

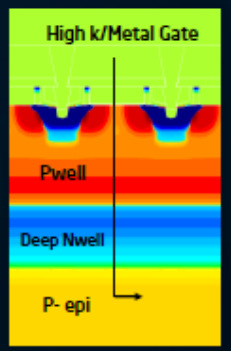








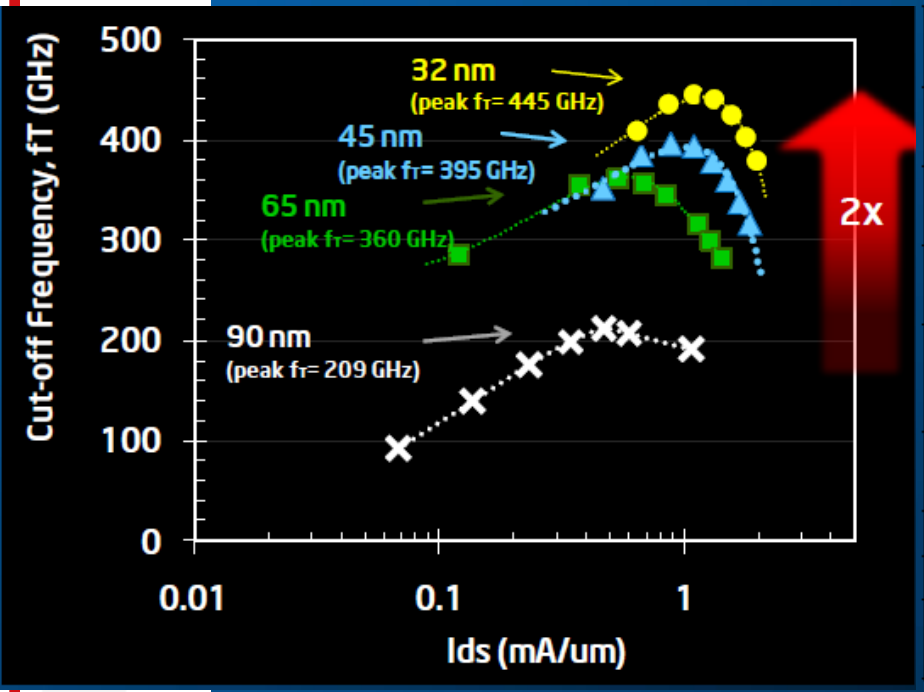
RF Models



Basic 32 nm CMOS technology is expanded with many more mixed signals/RF features to meet RF SoC requirements

C.-H. Jan, Dec/10 IEDM '10, San Francisco 5

RF CMOS Technology Performance Metrics



RF Devices	RF Circuits	Key Device Characteristics
Logic Transistor	MAC/BB, ADC, DAC	Idsat, Idlin, Vt, Ioff
Analog Transistor	ADC, DAC, MAC/BB	Gm, Rout, Matching, Linearity, Noise, NF_{min}
RF Transistor	PA, Mixer, T/R Switch	f_T, f_{max}, 1/f Noise, NF_{min}
PA Transistors	PA	Ron, Linearity, f_T, f_{MAX}, Efficiency, Breakdwn V,
Precision Resistors	ADC, DAC, BB Filter, others	R, σR/R, Matching
Linear Capacitors	PLL, VCO	C, Q, Matching
Varactors	PLL, VCO	Tuning Ratio, Q, Kv_{CO},
Inductor/ Transformer/Balun	PA, LNA, Mixer	L, Q

What are the impacts of CMOS scaling on these metrics ?

C.-H. Jan, Dec/10 IEDM '10, San Francisco 11

Conclusion

- 0.35 µm still widely used for good ratio performance/cost
- « acta est fabula » : talk is finished

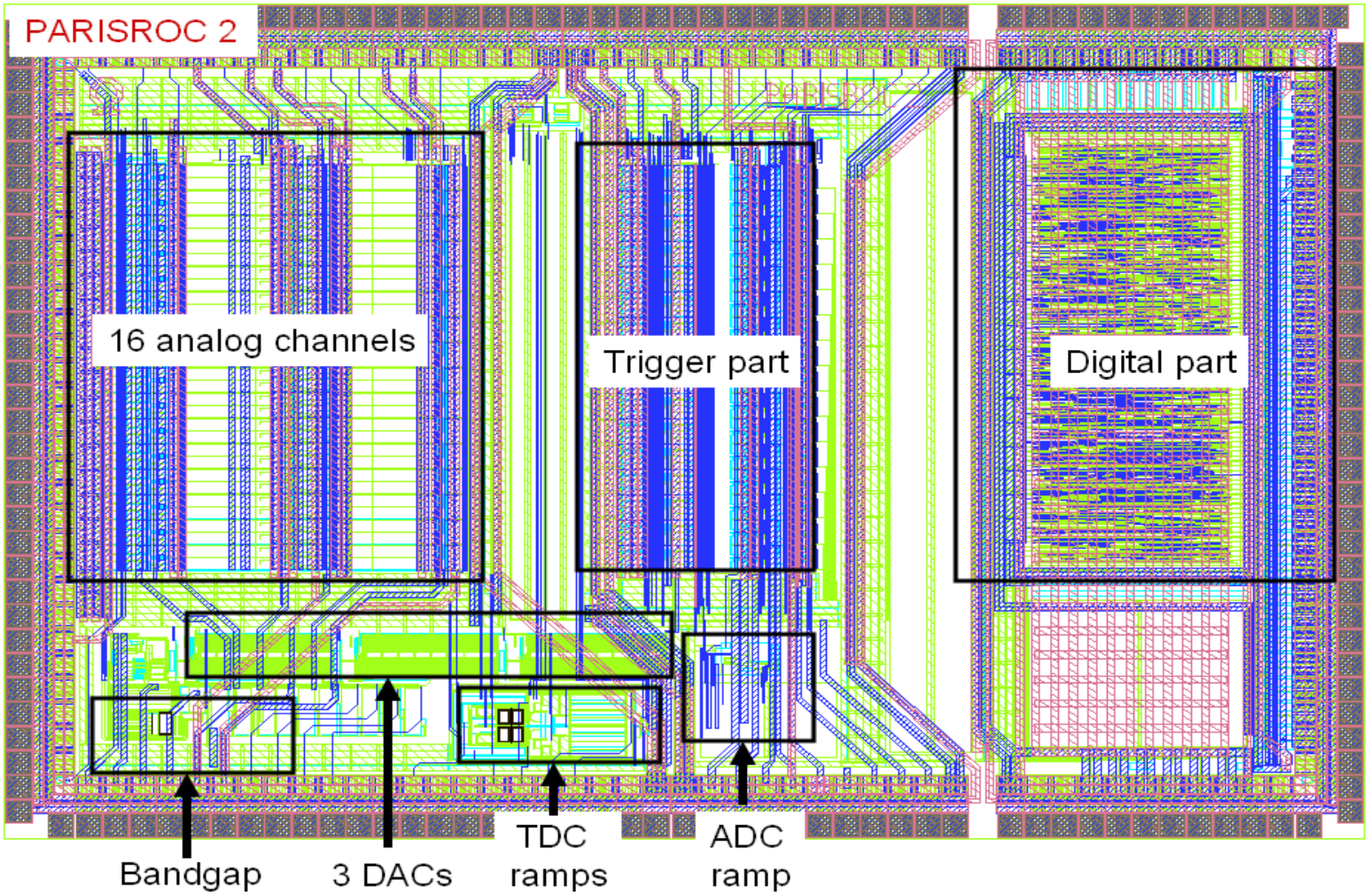
Backup slides

PARISROC2 layout

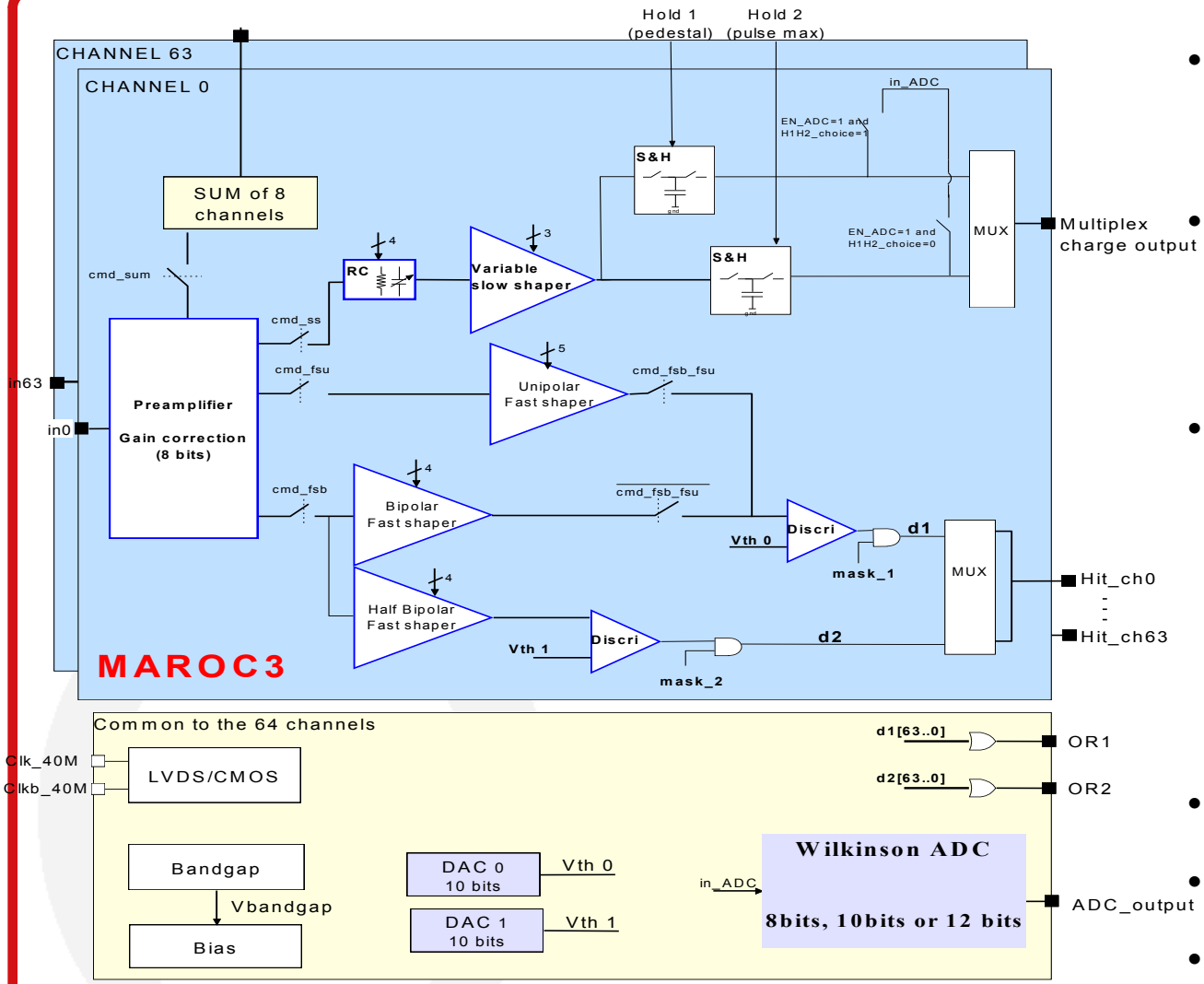
Technology: AMS SiGe 0.35 µm

Surface: 18 mm²

Package: CQFP160

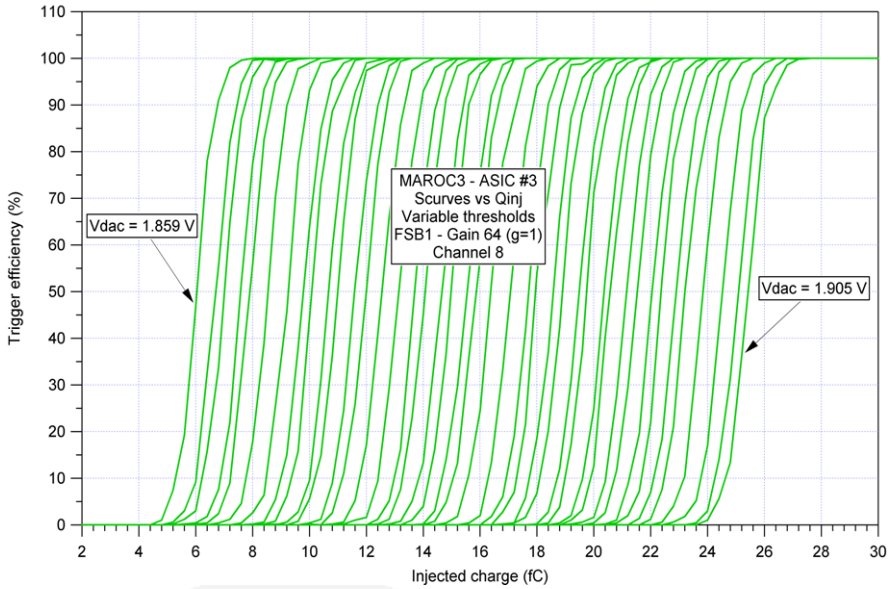


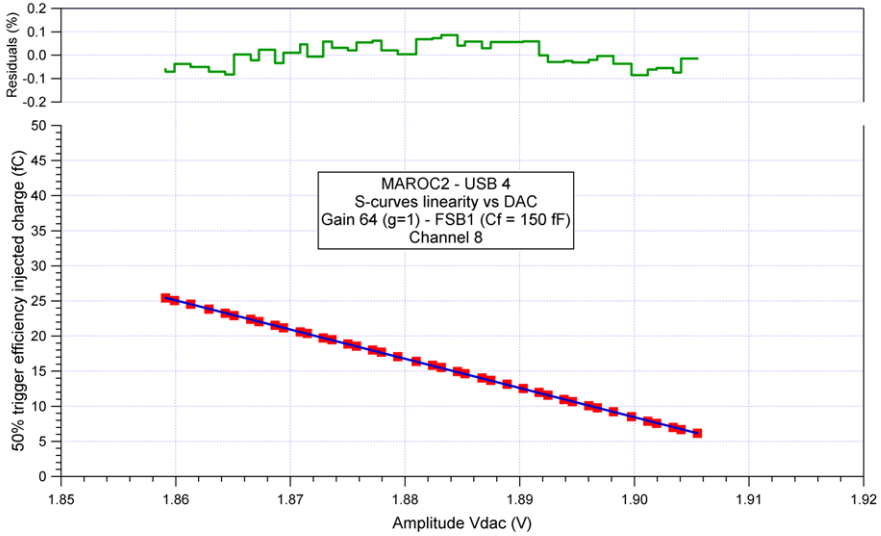
MAROC 3 – Main Features

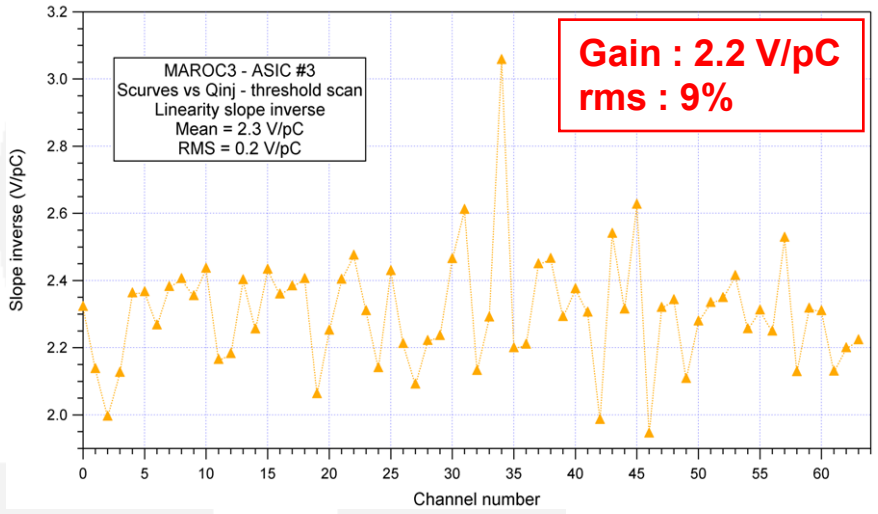


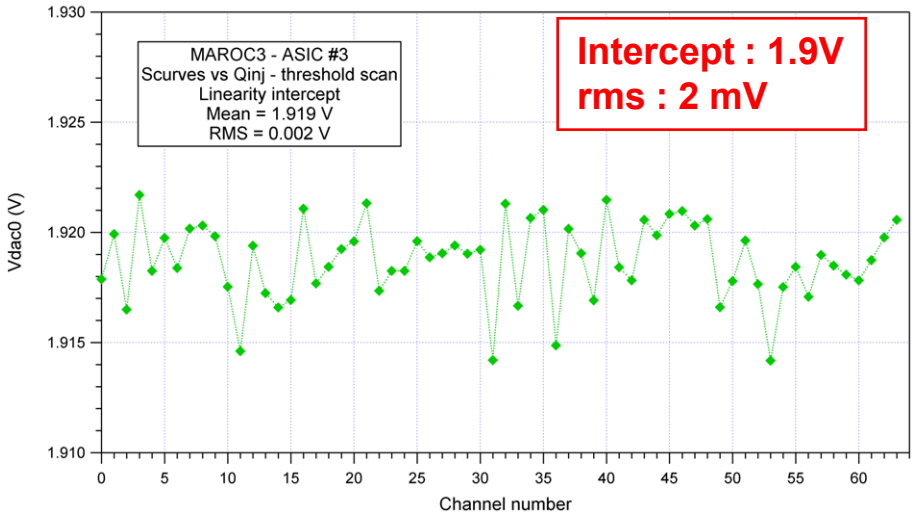
- **Gain adjustement:**
  - 8 bits (2,1,…,0.0156) instead of 6 bits (2,1,…,0.0625)
- **Charge measurement**
  - Variable charge gain
  - Dynamic range increased
  - 8 or 10 or 12 bits wilkinson ADC
- **Trigger measurement**
  - Bipolar fast shaper: 2 thresholds
  - Only 2 DAC
  - Mux instead of an encoder
  - 2 OR outputs
  - New digital output levels: Vhigh and Vlow
  - Mask
- **Internal reference**
- **P = 3 mW/ch**
- **828 slow control parameters!**

Scurves with FSB1



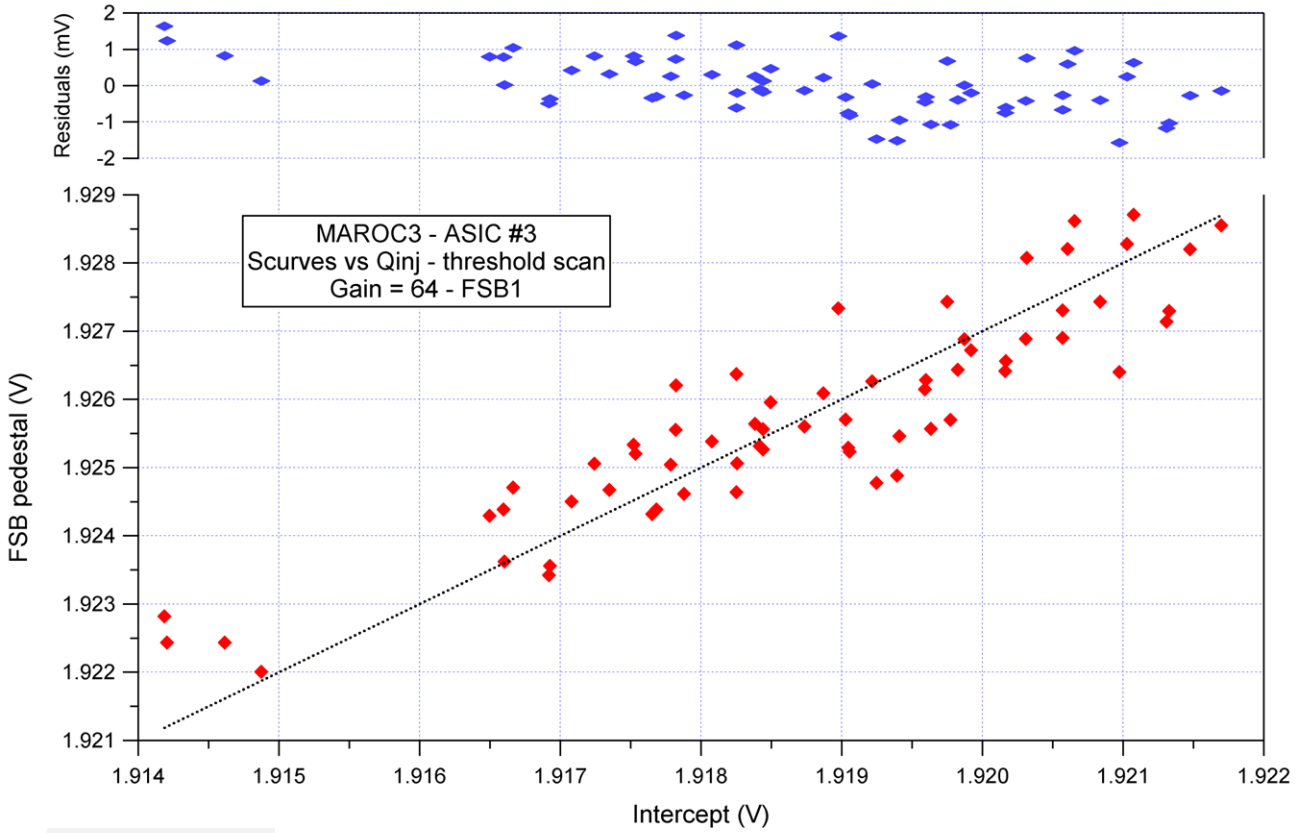






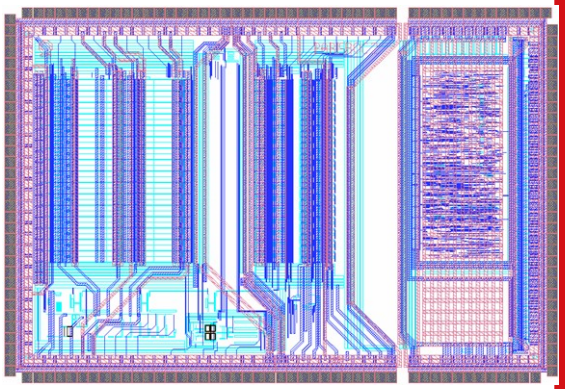
Discriminator offset

- SiGe BJT discriminator
  - Offset ~500 µV



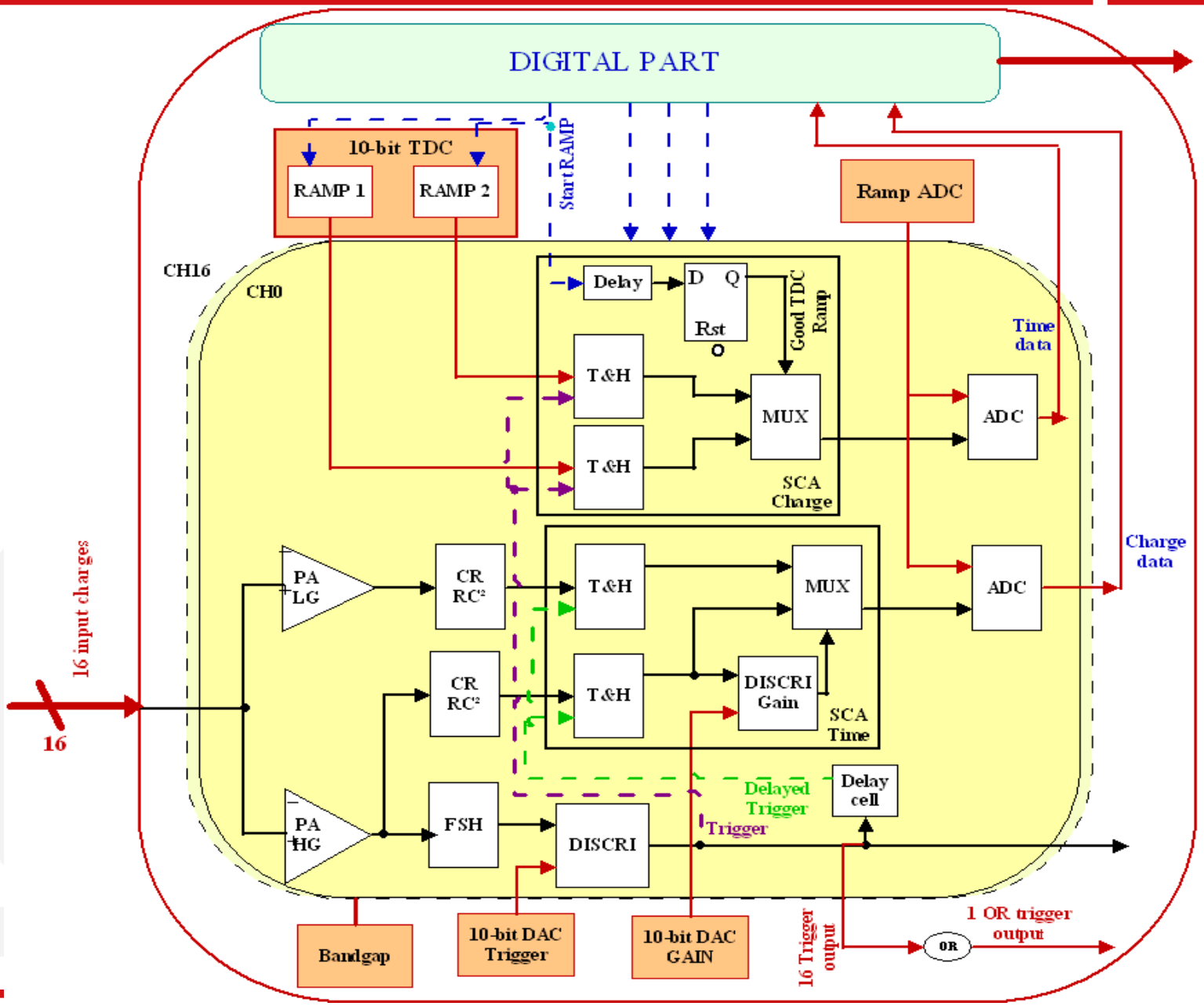
PARiSROC characteristics

- 16 preamplifier inputs
  - Input dynamic range : 0 ☐ 300 pe (0 ☐ 50pC) with 1% linearity good precision obtained by 2 preamps (high and low gain)
  - Variable gain by a factor 4 (8 bits) for PMTs gain adjustment
- 16 trigger outputs:
  - Fast shaper (t=15ns) + low offset discriminator
  - Threshold provided by common internal 10bit DAC
  - 100 % eficiency at 1/3 pe
  - "OR" of 16 triggers output
- 1 multiplexed charge output :
  - Slow shaper with variable shaping time :
    t =25ns,50n or 100ns
  - Dual Track & Hold
- 8 to 10-bit internal ADC (Wilkinson) for charge and fine time measurement
- Internal TDC : 24 bits counter (coarse) + fine 1 ns
- One serial data output : channel number + Charge + time coarse and fine
- **Dissipation** : 5mW/ch



PARISROC – 18 mm^2

PARISROC general schematic

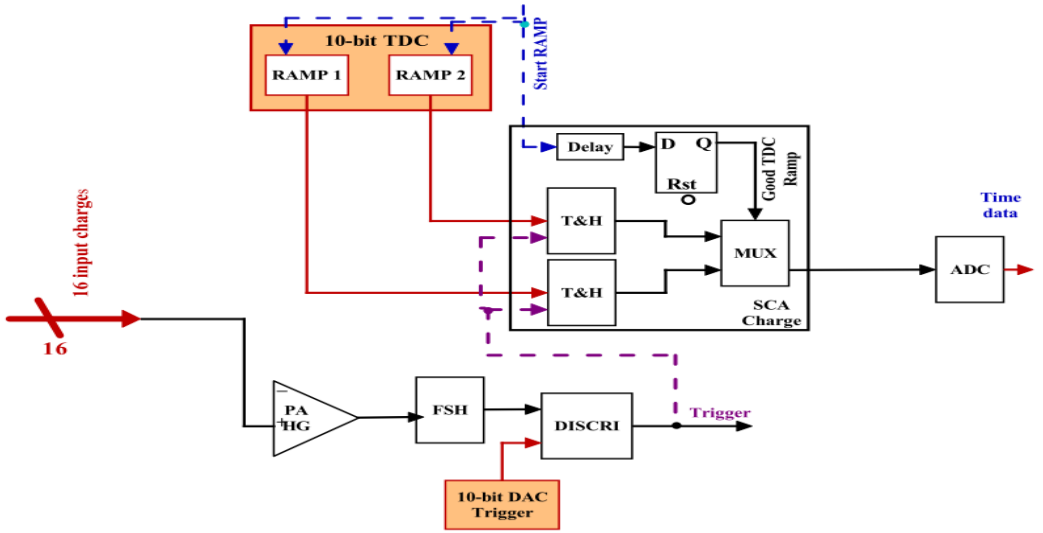


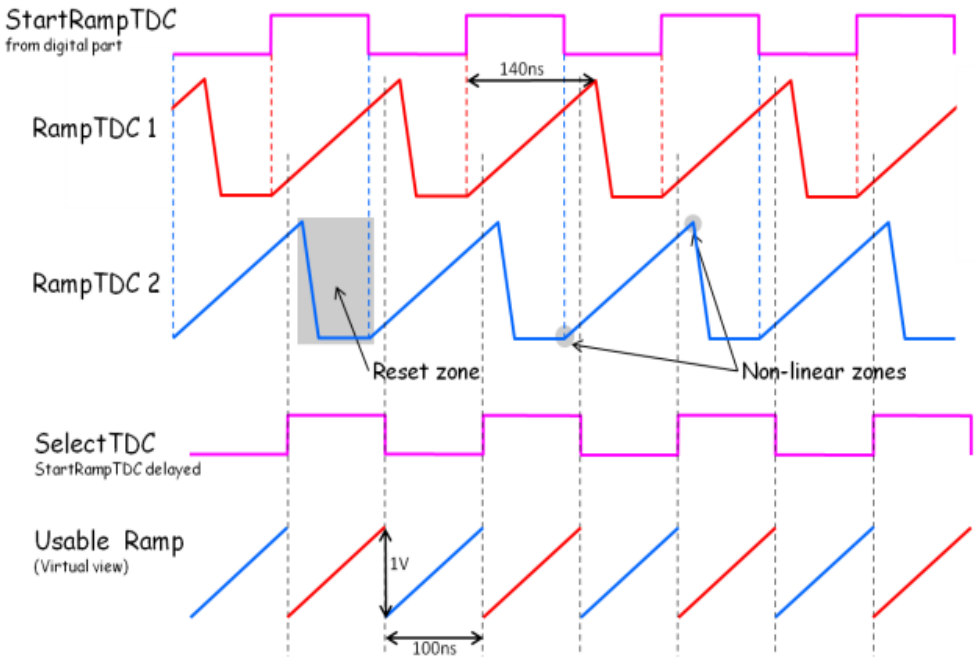
Time measurement

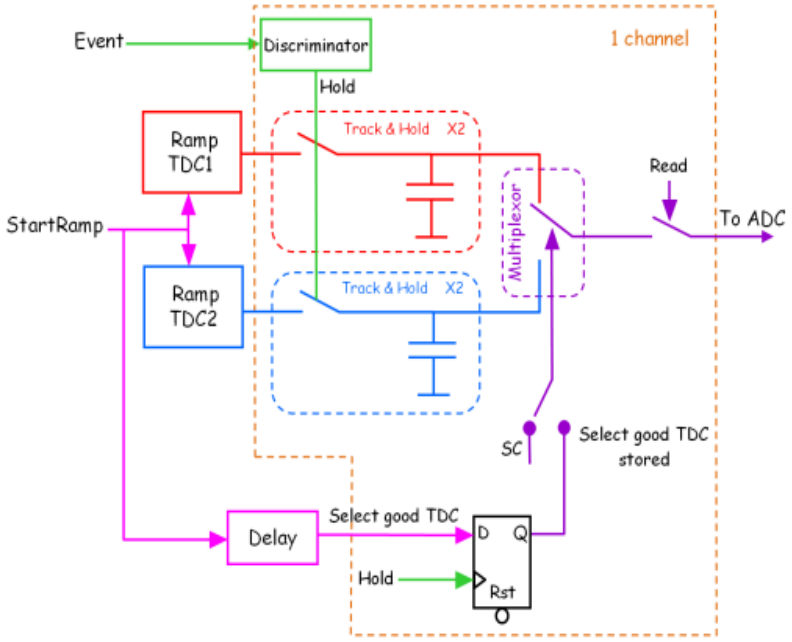
2 systems:

1. Coarse time by 24-bit gray counter
- working at 10 MHz
- with 1.67 s of dynamic
- 100 ns steps

2. Fine time by analog TDC
- 100 ns dynamic
- 100 ps step







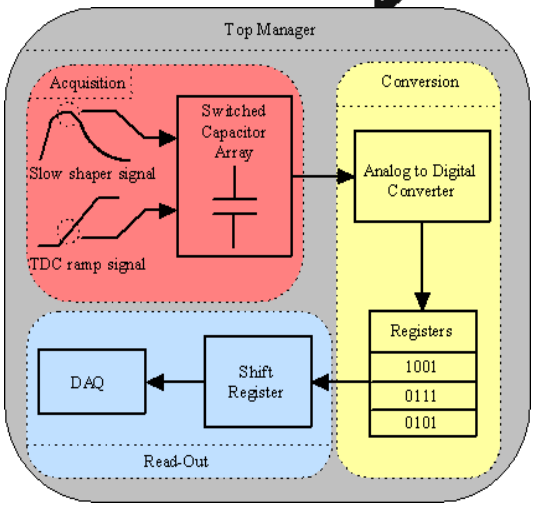
Digital part

4 modules: ***Acquisition, Conversion, Read Out and Top manager***.

Acquisition part manages the track & hold

Conversion part converts charge and time into 10 bits digital values saved in registers (RAM)

Read Out sends the data from memory to an external system



SELECTIVE READ OUT

- **Only hit channels are read**
- **Readout clock : 40 MHz**
- **Max Readout time (16 ch hit) : 25 µs**
- **51 bits of data / hit channel**

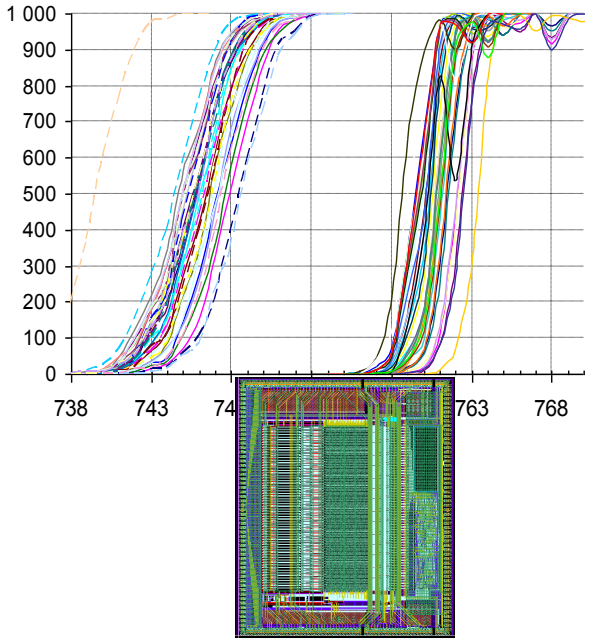
	PARIROC 2
Conversion Time	26 µs
Readout Time	25 µs
Total cycle duration	51 µs

	PARIROC version 2
Channel number	4
Coarse time counter	24
Extra Coarse time	1
Gain used	1
Charge converted	10
Fine time (TDC) used	1
Fine time (TDC) converted	10
Total	51 bits

SKIROC status

- SPIROC2 used as SKIROC emulator
  - only preamp differs
  - 36 channels instead of 64
  - Limited dynamic range (~500 MIPs)
  - Tests starting with FEV7 to address embedding issues
  - Noise tests on testboard proceeding (ENC ~ 1 ke-)

- SKIROC2 submitted with production run
  - 64 channels, 70 mm^2
  - Very large dynamic range: HG for 0.5-500 MIP, LG for 500-3000 Mip
  - Testability at wafer level

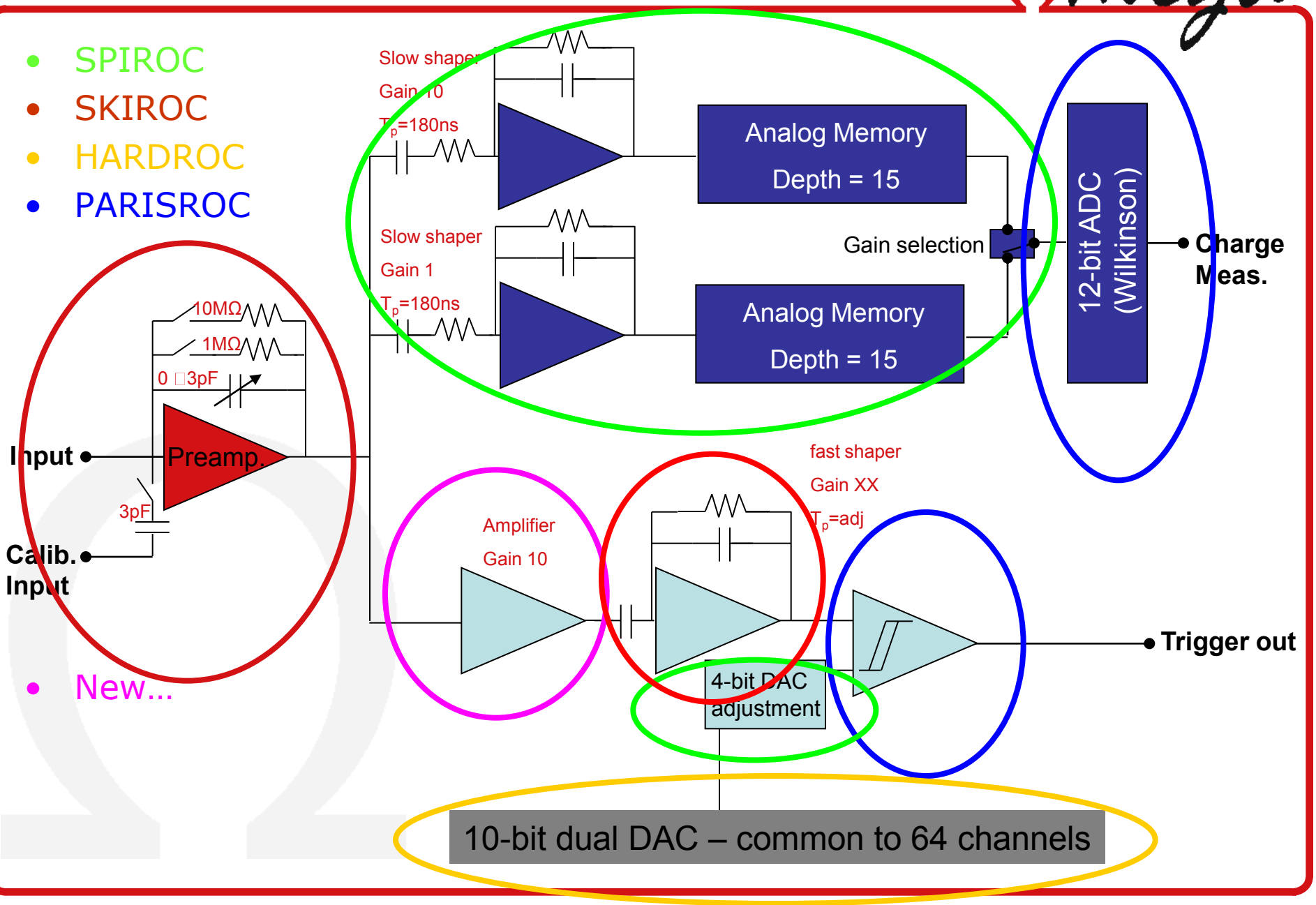


- Front End boards crucial element
  - Collaboration with Korea

S. Callier, *M. Cohen-Solal*, F. Dulucq, J. Fleury, N. Seguin

SKIROC2 One channel block scheme

- SPIROC
- SKIROC
- HARDROC
- PARISROC



- New…