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CMOS Technologies for HV applications

Microelectronics Users eXchange MUX-2011

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CERN, June 10th, 2011

Outline

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Let's scale down first

Introduction & Company Overview

Technology Integration

High Voltage Device Description

Low Voltage RF Device Description

Device Models

ESD, SOA and Reliability

Design Kit

Conclusions

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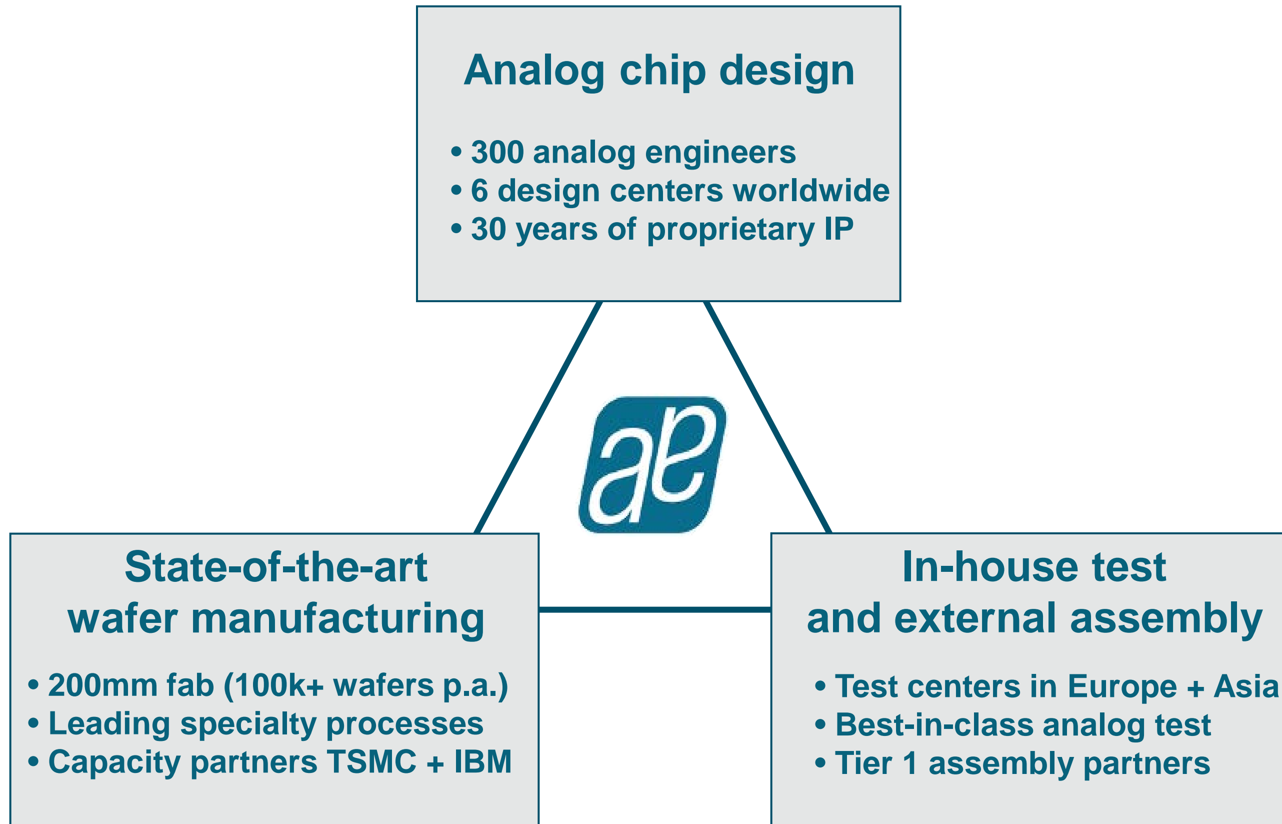
Full control over design and manufacturing



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Figures of Merit in High Voltage Technology

BVdss

- Initial Specification for LDMOS devices and defines usable voltage for circuit design
- Allows for adequate voltage margin to account for device hot-e degradation (reliability) and ESD robustness
- For H18, full device reliability lifetime is evaluated during technology qualification
- Statistical in line process control to avoid escapes below minimum value
- SOAC tool checking during design simulation alerts circuit designer to any inappropriate voltage use

Ron

- Minimum value is key for setting device size and overall circuit complexity
- For H18, device layout is optimized by device type to obtain a minimum Ron after meeting BVdss window as specified above

Process complexity

- Modularity to industry standard CMOS: H18 FET electrical specifications/models are identical to those of C18 technology for 1.8 and 5V LV FETs: easy porting of IP
- Minimal mask additions for HV devices: add of 2 masks compared with C18
- Maintain a rich HV device set: variety of BVdss and Vgs of HV LDMOS devices and specific HV devices include NPN, PNP, JFET, HV resistors and HV capacitors

Process flexibility and extendibility

- The single H18 process supports multiple BVdss specifications with scaled devices
- H18 is extendable without process changes to BVdss values as low as 10V and high as 120V
- Thus, designs completed now can be enhanced by addition of these extended voltage range devices in the future

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Si-Limit: On-Resistance vs. Blocking Voltage Tradeoff

A simple model for HV Transistors:

For a one sided junction the depletion layer width at breakdown is:

$$W = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot V_B}{q \cdot N_{drift}}}$$

and the breakdown voltage is:

$$V_B = \frac{W \cdot E_{crit}}{2} = \frac{W^2 \cdot q \cdot N_{drift}}{2\varepsilon_{si}}$$

Specific on-resistance is given by:

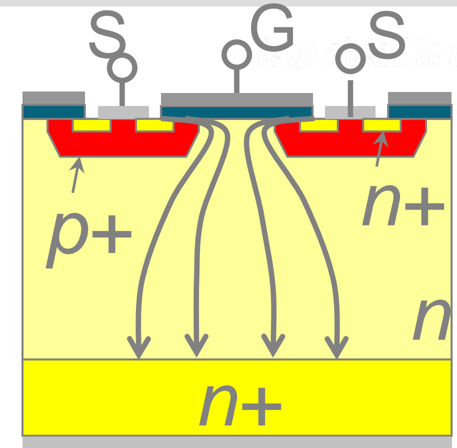
$$R_{on,sp} = \rho \cdot W = \frac{W}{q\mu N_{drift}} = \frac{W^3}{2\mu V_B \varepsilon_{si}}$$

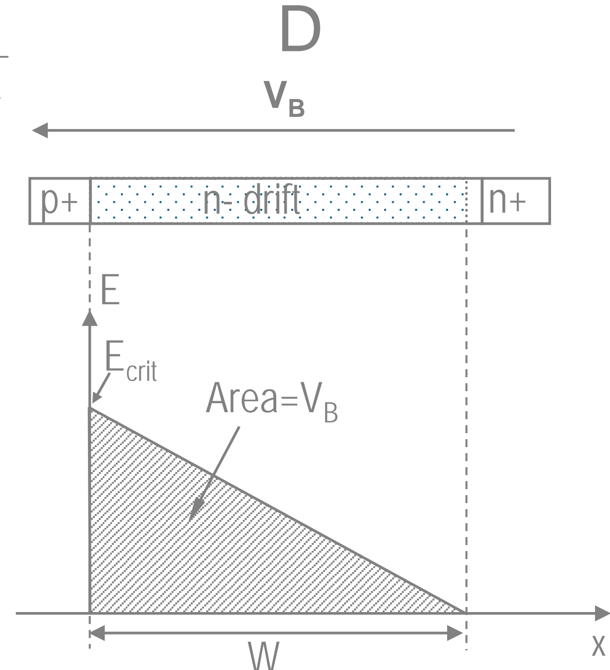
Breakdown occurs when the depletion layer reaches a certain thickness which is almost proportional to the breakdown voltage (avalanche effect):

$$W = 2.58 \cdot 10^{-6} \cdot (V_B)^{\frac{7}{6}}$$

Which finally yields:

$$R_{on,sp} \propto V_B^{\;2.5}$$





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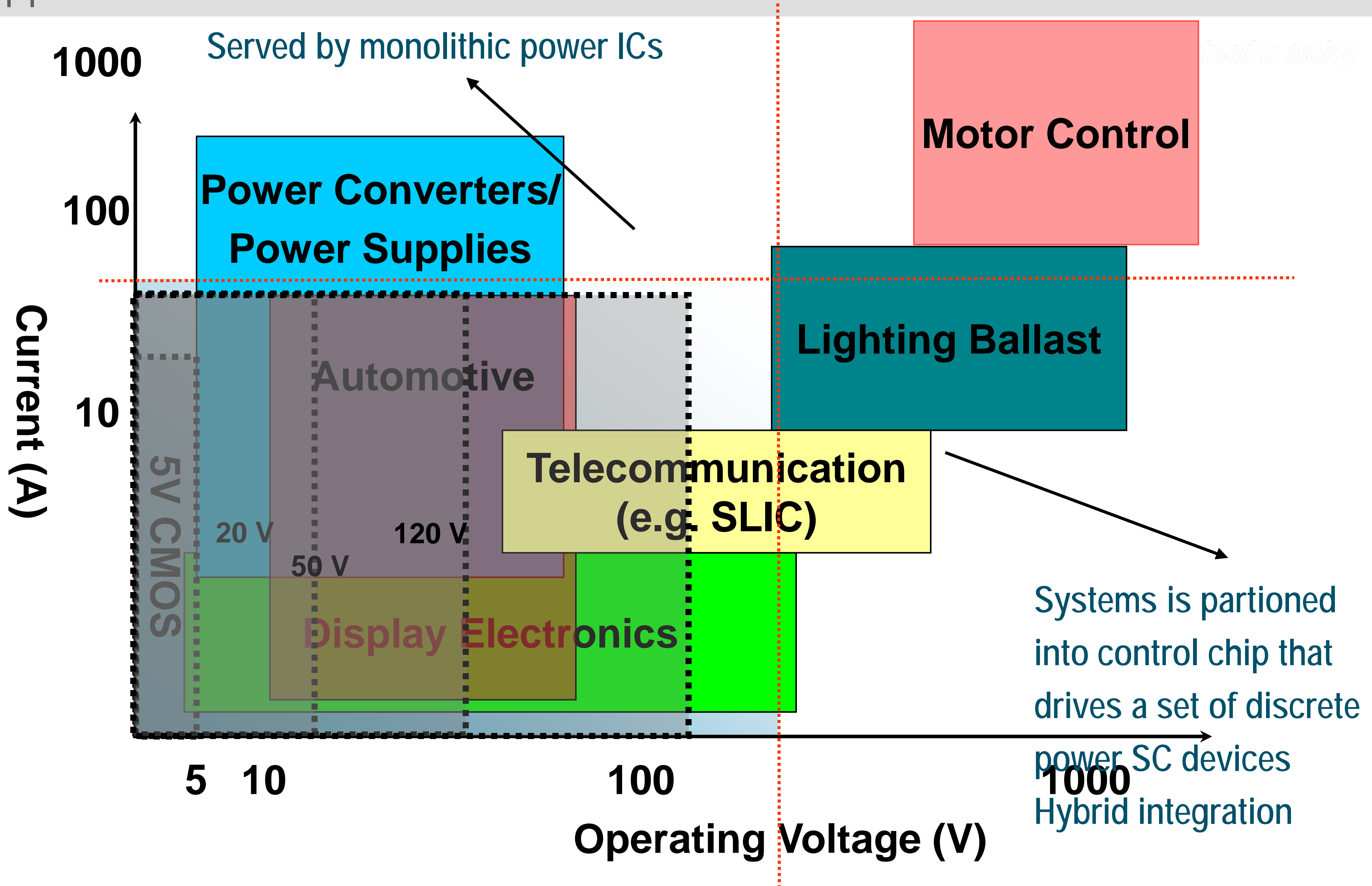
Application Areas of Power Devices



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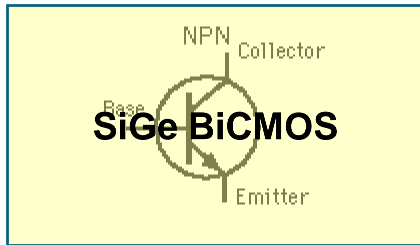
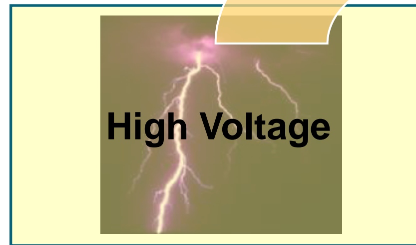
Process modularity on 0.35µm node

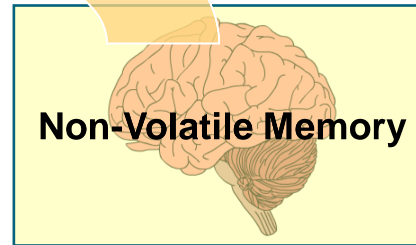
High flexibility through modularity:



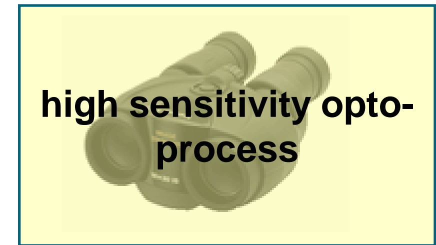
SiGe BiCMOS



High Voltage

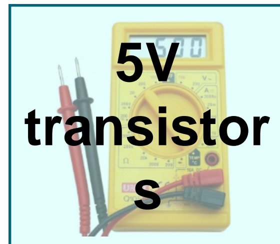


Non-Volatile Memory



high sensitivity opto-process

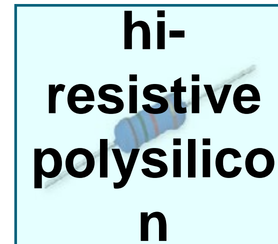
caps: poly & MIM



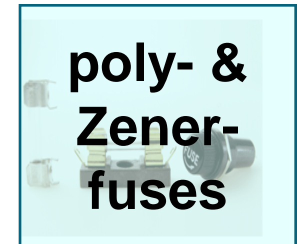
5V transistors

LVT transistors

3rd and 4th metal



hi-resistive polysilicon



poly- & Zener-fuses

C35 3.3V analog/mixed signal polycide process

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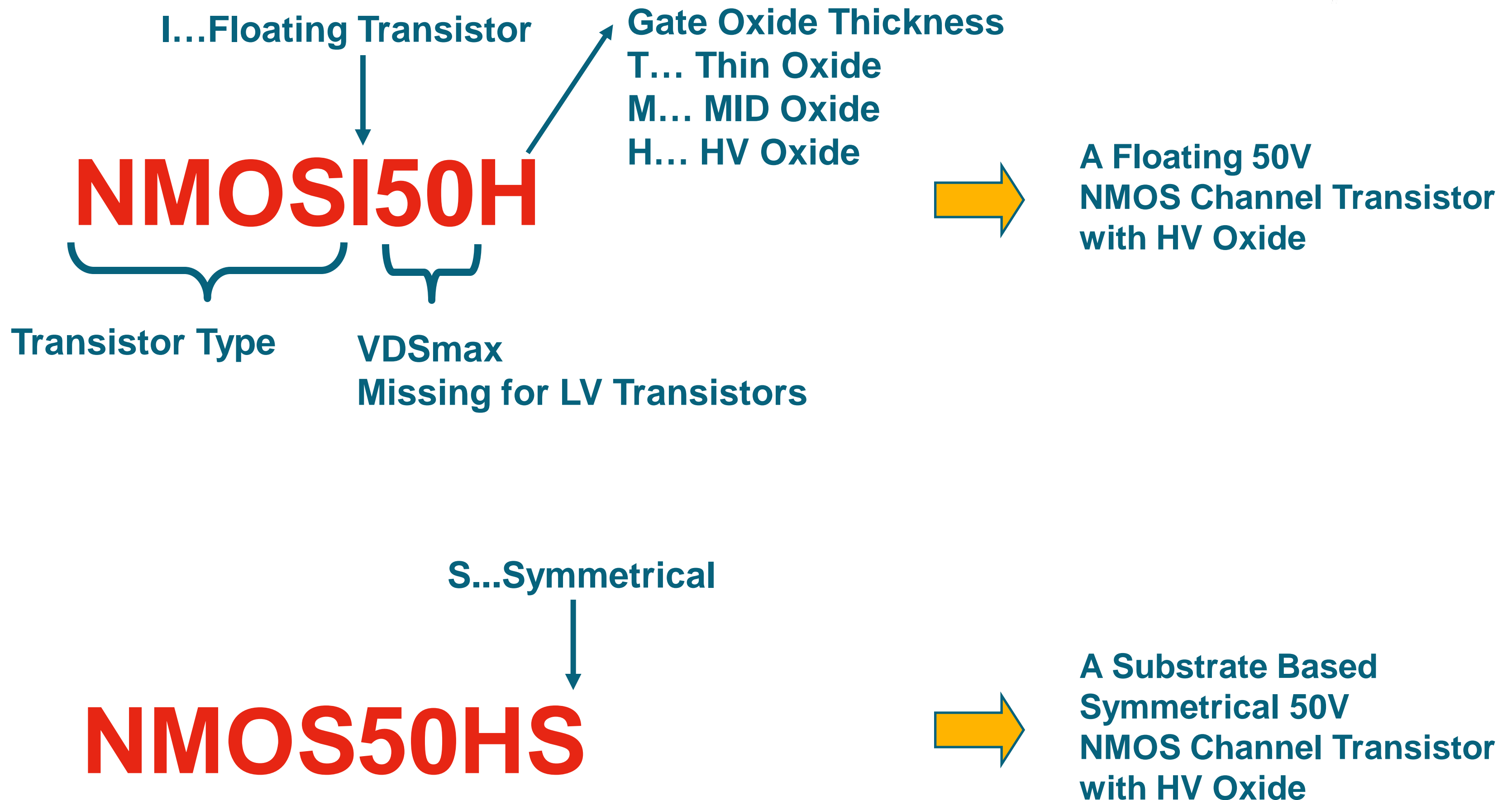
MOS transistor naming H35



© HGE

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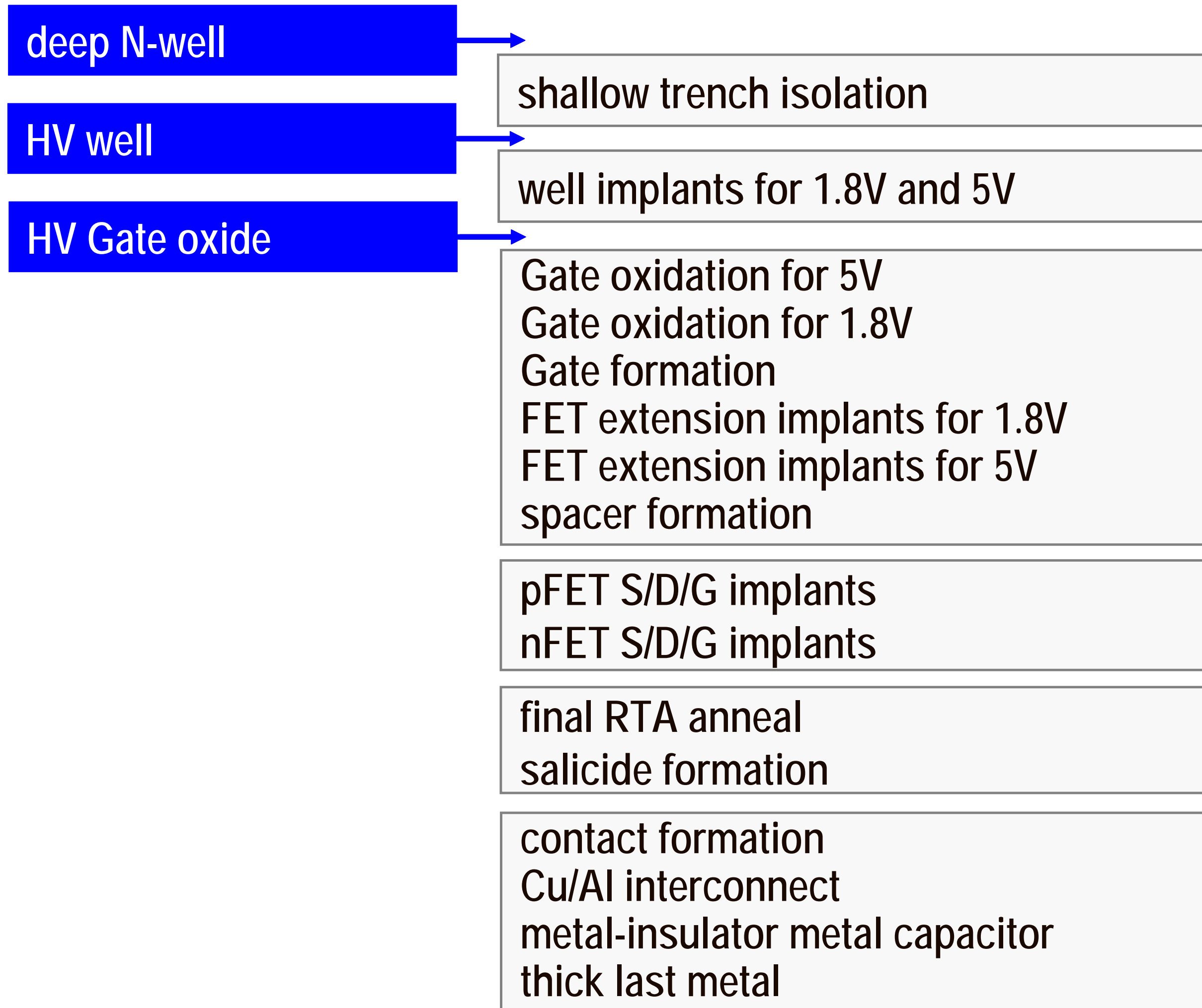
High Voltage Technology Process Flow



Net:

- **Triple gate process (1.8, 5 and 20V), but 1.8 and 20V optional**
- **2 additional HV masks to base CMOS**
- **Additional resistor masks optional**
- **3LM-7LM options**

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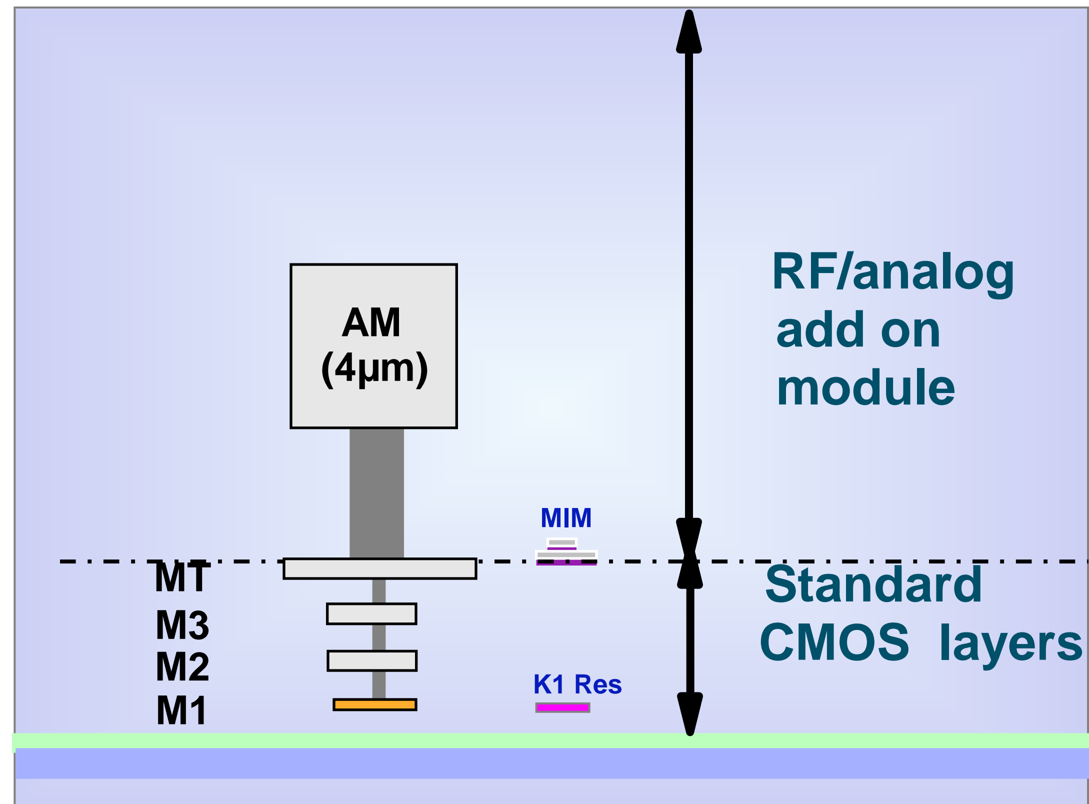
H18 metal stack options

	AM Last Metal Option				
# Levels	3	4	5	6	7
					MT
				MT	M5
Standard Al wiring Levels			MT	M4	M4
		MT	M3	M3	M3
	MT	M2	M2	M2	M2
	M1	M1	M1	M1	M1



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0.18µm HV CMOS - Key Technology Features

Currently available voltages	1.8 V / 5 V / 20 V / 25 V / 50 V
RON (20V & 50V) NMOS	15 & 105 mΩ mm^2
Operating Voltages	20 V / 25 V / 50 V
Blocking Voltages	30 V / 40 V / 70 V
Layout scalable devices	20 - 120 V (120 V demonstrated)

0.18µm HV CMOS - Process Modules

Back end process modules

- 3 - 7 metal
- Power metal (4 µm thick)
- Poly resistor
- High resistive poly
- MIM (metal insulator metal) capacitance

Front end process modules

- 1.8 V Gates
- 5.0 V Gates
- 20 V Gates
- Isolated low voltage NMOS and PMOS (1.8 V / 5.0 V)

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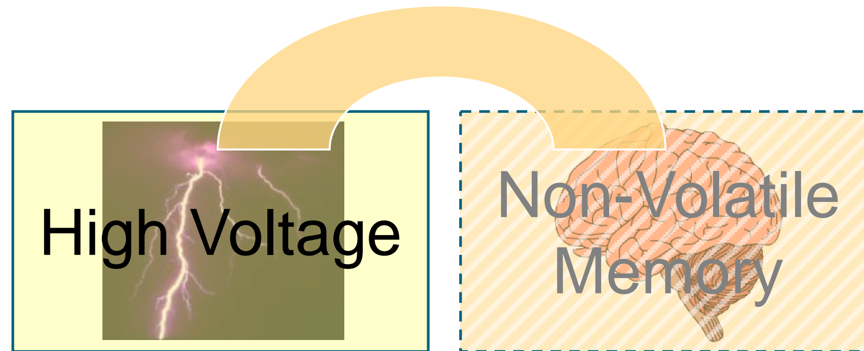
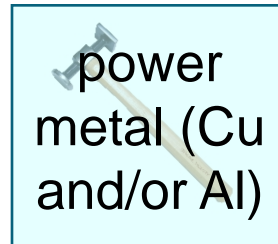
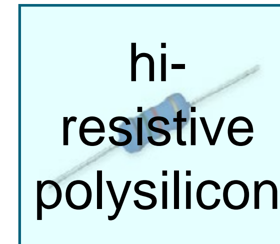
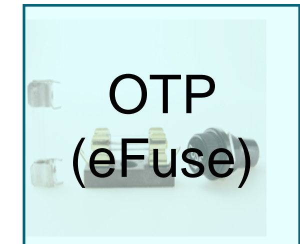
Process modularity of H18

High flexibility through modularity:









C18 1.8V silicide process

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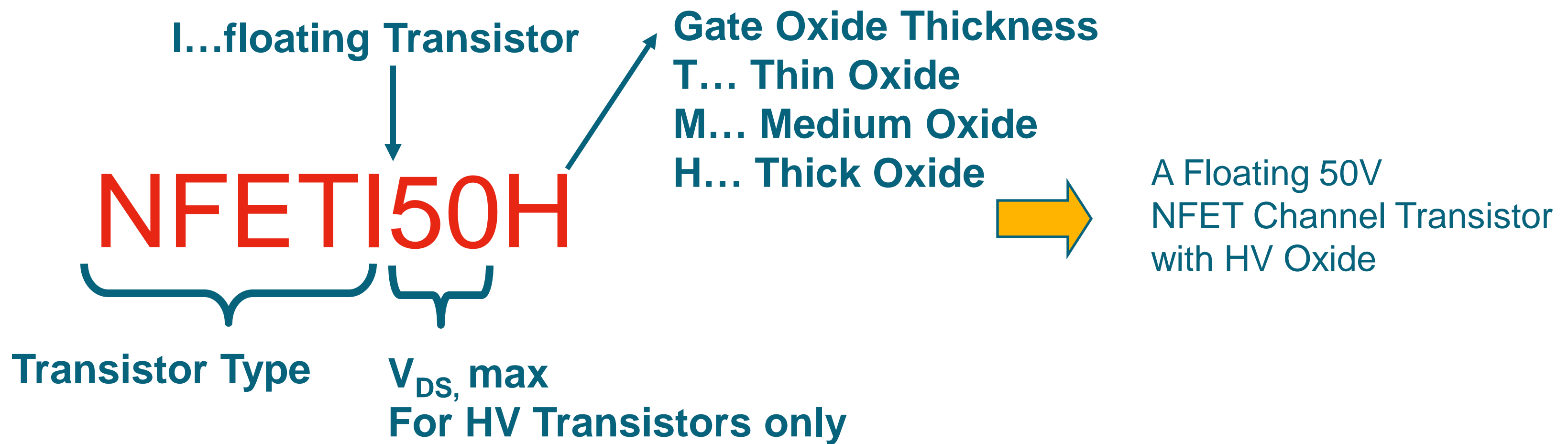
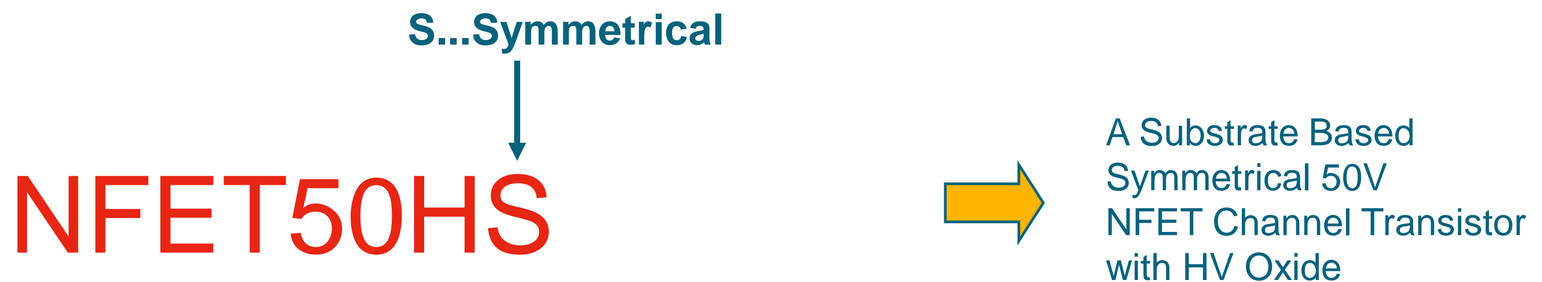
HV MOS Transistor Naming Convention Cheat Sheet





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H18 device list

Existing C18 Devices

Thin oxide NFET/PFET 1.8V
Medium oxide NFET/PFET 5V
High Vt NFET/PFET 1.8V
N+ diffusion resistor
P+ diffusion resistor
N+ poly resistor
P+ poly resistor
K1 BEOL resistor
High resistivity poly resistor
precision poly resistor
Single Nitride MIM
Dual Nitride MIM
HighK MIM
PCDCAP thin ox
Vertical parallel plate capacitor (VNcap)
Schottky Barrier Diode
Efuse
Bondpad

Modifications to existing devices for HV process:

Thin oxide NFETi/PFETi 1.8V in HV wells
Medium oxide NFETi/PFETi 5V in HV wells
High Vt NFETi/PFETi 1.8V in HV wells
N+ diffusion resistor in HV well
P+ diffusion resistor in HV well

New Devices:

Thin oxide NFETi/PFET 20V
Thick oxide NFETi/PFET 20V
Thick oxide NFETi/PFET symmetric 20V
Medium oxide NFETi 20V
Medium oxide NFETi/PFET 25V
Thin oxide NFETi/PFET 50V
Medium oxide NFETi/PFET 50V
Thick NFETi/PFET 50V
Thick NFETi/PFET symmetric 50V
3 terminal JFET
Parasitic VPNP (high V)
Parasitic VNPN (isolated)
NWell resistor in HV well
PWell resistor in HV well
High Voltage VNcap

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Suite of FETs with three gate oxide thicknesses

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- Low Voltage (LV) fets for standard 1.8 and 5V CMOS
- LV fets in HV well for high voltage isolation to substrate
- HV asymmetric fets for High Voltage applications
- 3 gate oxide thicknesses, 2 maximum drain bias choices
- HV symmetric fets for specialty applications (transmission gate)

	LV fets		LV fets in HV well		HV asymmetric fets in HV wells		HV symmetric fets (nfet in Substrate)	
Vds / Vgs	1.8V	5.0V	1.8V	5.0V	20V**	50V	20V	50V
1.8V (3.5nm)	nfet* pfet* nfethvt pfethvt		nfeti* pfeti* nfetihvt pfetihvt		nfeti20t pfet20t	nfeti50t pfet50t		
5.0V (12nm)		nfetm pfetm		nfetim pfetim	nfet20mh nfeti25m pfet25m	nfeti50m pfet50m		
20V (52nm)					nfeti20h pfet20h	nfeti50h pfet50h	nfet20hs pfet20hs	nfet50hs pfet50hs

* RF layout available ** 25V Vds for nfeti25m,pfeti25m

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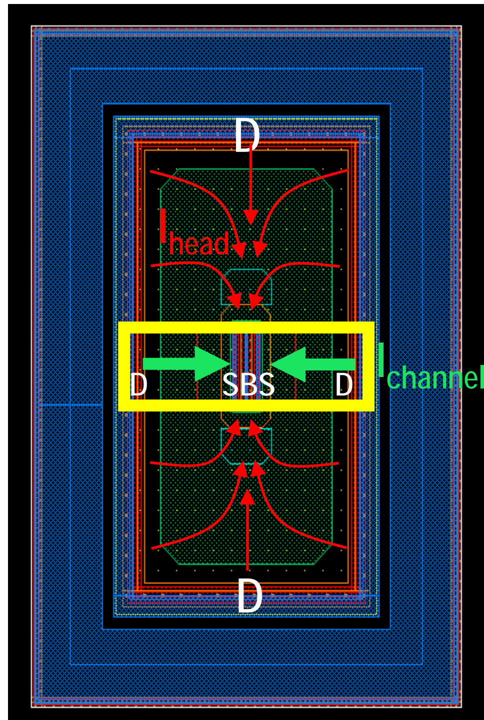
Wide vs. Small Devices: The Transistor Head effect

Parasitic head currents can't be 100% eliminated (up to 20uA)



Parasitic head currents

I_{head} = ∑ of all current through the head

Current trough the channel

$I_{channel}$ = ∑ of all current through the channels

$Ids = I_{channel} + I_{head}$

$Ron = Vds/Ids = Vds/(I_{channel}+I_{head})$

Parasitic head currents can't be neglected for low channel Currents (narrow devices)
If channel currents are high (wide devices), parasitic head current can be neglected
For simple calculation there are two different Ron [Ohm um] values for narrow and wide transistors

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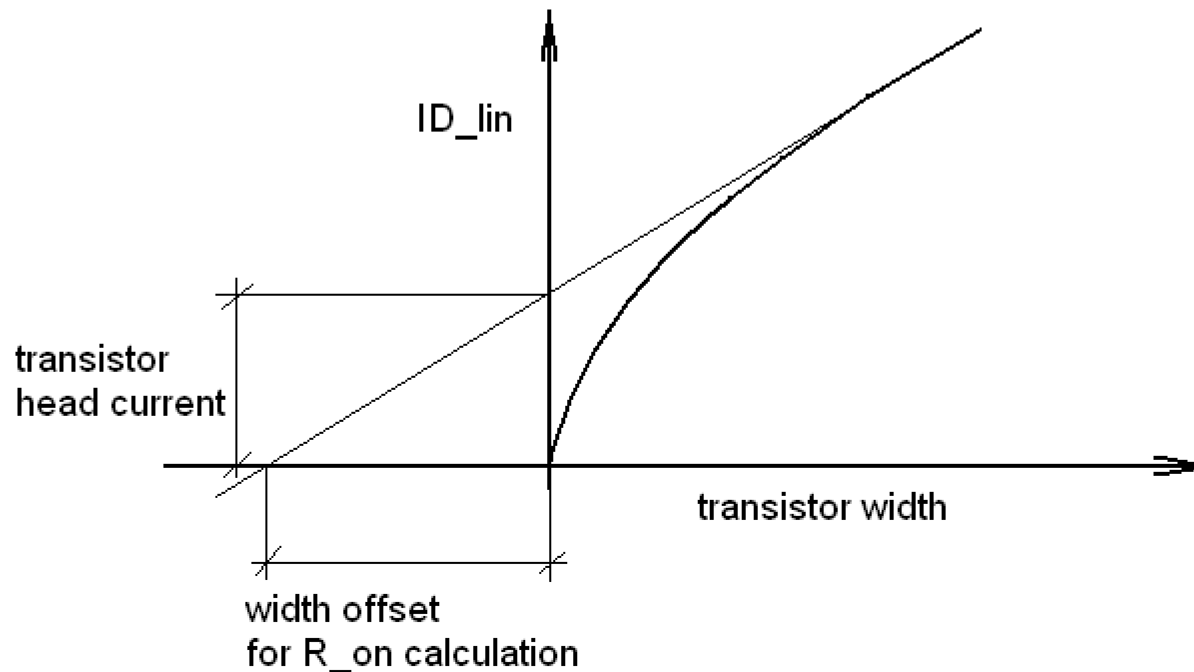
Transistor head current



For small W devices the transistor current increases faster than for a large W device.

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H18 High Voltage NFETs

	Asymmetric, thinnest oxide, isolated well		Asymm., med. oxide in substrate	Asymmetric, medium oxide, isolated well		Asymmetric, thickest oxide, isolated well		Symmetric, thickest oxide, in substrate	
Parameter	nfeti20t	nfeti50t	nfet20mh	nfeti25m	nfeti50m	nfeti20h	nfeti50h	nfet20hs	nfet50hs
Min Drain-source breakdown (V)	29	83	27	33	73	28	79	32	85
Tox (physical, nm) / Max VGS (V)	3.5 / 1.98	3.5 / 1.98	12 / 5.5	12 / 5.5	12 / 5.5	52 / 20	52 / 20	52 / 20	52 / 20
Ldrawn (µm)	0.2	0.2	0.4	0.4	0.4	0.5	0.5	0.7	1.3
V_T (short wide V)	0.43	0.40	0.80	0.71	0.72	2.0	2.14	2.15	2.15
IDsat (µA/ µm)	200	172	400	343	266	580	353	340	230
On Resistance mΩ-mm^2	35.1	168	17.1	45.2	143	29.5	138	47.1	316
On Resistance mΩ-mm^2 (butted)*	29.8	155	14.4	39.2	132	25.5	128		

Pitch for R_{sp} on resistance calculation includes full drain, source, *and* independent body contact (*mh devices butted source contact)

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H18 High Voltage PFETs

	Asymmetric, thinnest oxide		Asymmetric, medium oxide		Asymmetric, thickest oxide		Symmetric, thickest oxide	
Parameter	pfet20t	pfet50t	pfet25m	pfet50m	pfet20h	pfet50h	pfet20hs	Pfet50hs
Min Drain-source breakdown (V)	-30	-70	-32	-70	-35	-70	-28	-70
Tox (physical, nm) / Max VGS (V)	3.5 / 1.98	3.5 / 1.98	12 / 5.5	12 / 5.5	52 / 20	52 / 20	52 / 20	52 / 20
Ldrawn (µm)	0.2	0.2	0.6	0.6	0.6	0.6	2.0	3.0
V_T (short wide V)	-0.35	-0.35	-0.51	-0.52	-2.48	-2.52	-1.80	-1.80
IDsat (µA/ µm)	140	123	220	204	345	309	250	160
On Resistance mΩ-mm^2	53.0	187	66.0	194	63.0	183	129	630
On Resistance mΩ-mm^2 (butted)*	41.8	166	53.8	174	51.7	166		

Pitch for R_{sp} on resistance calculation includes full drain, source, *and* independent body contact (*mh devices butted source contact)

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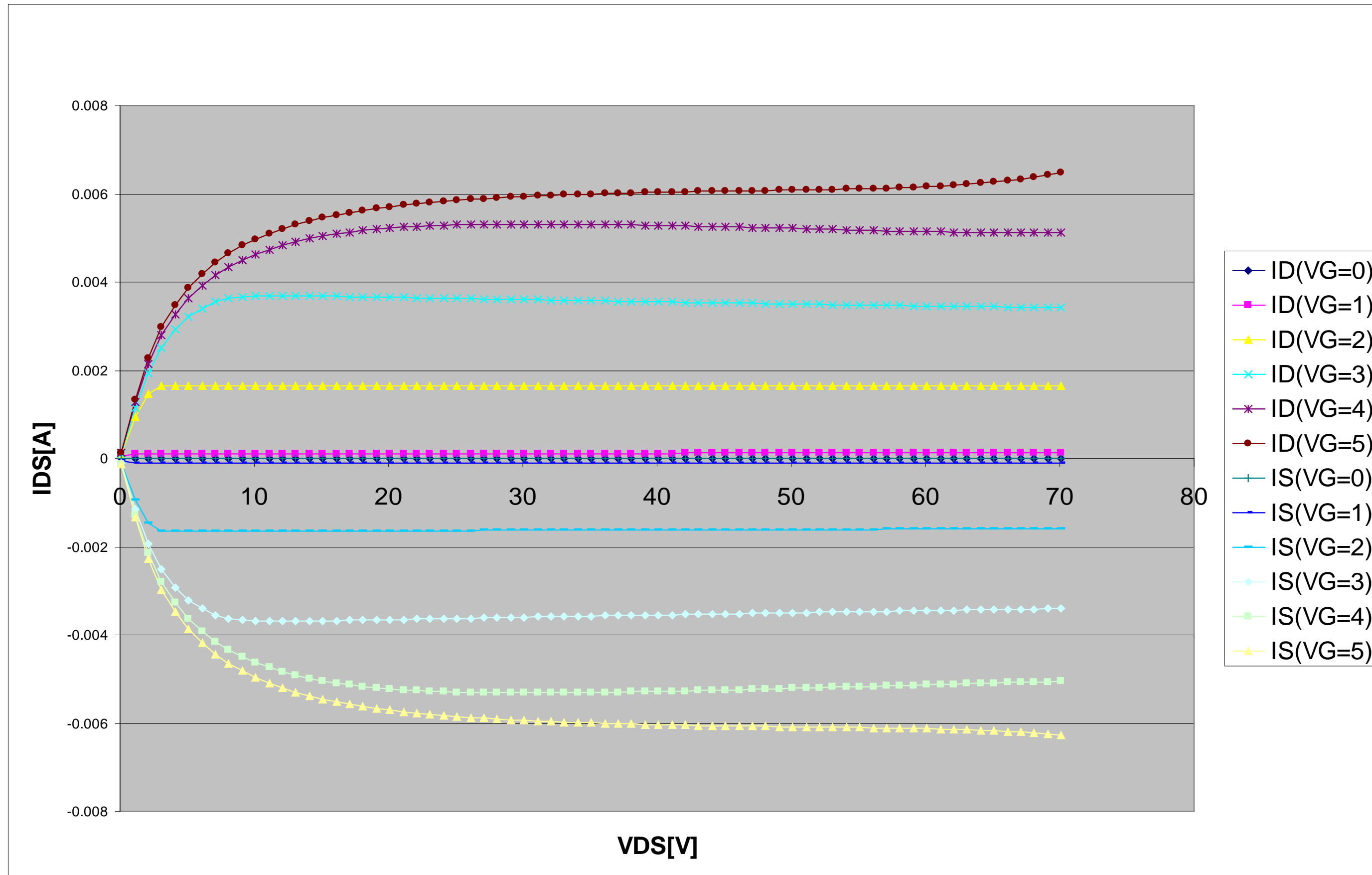
H18 Devices: NFETI50 Device Family



Note the active breakdown for the stationary curve tracing is for the 50V devices higher than 70V.

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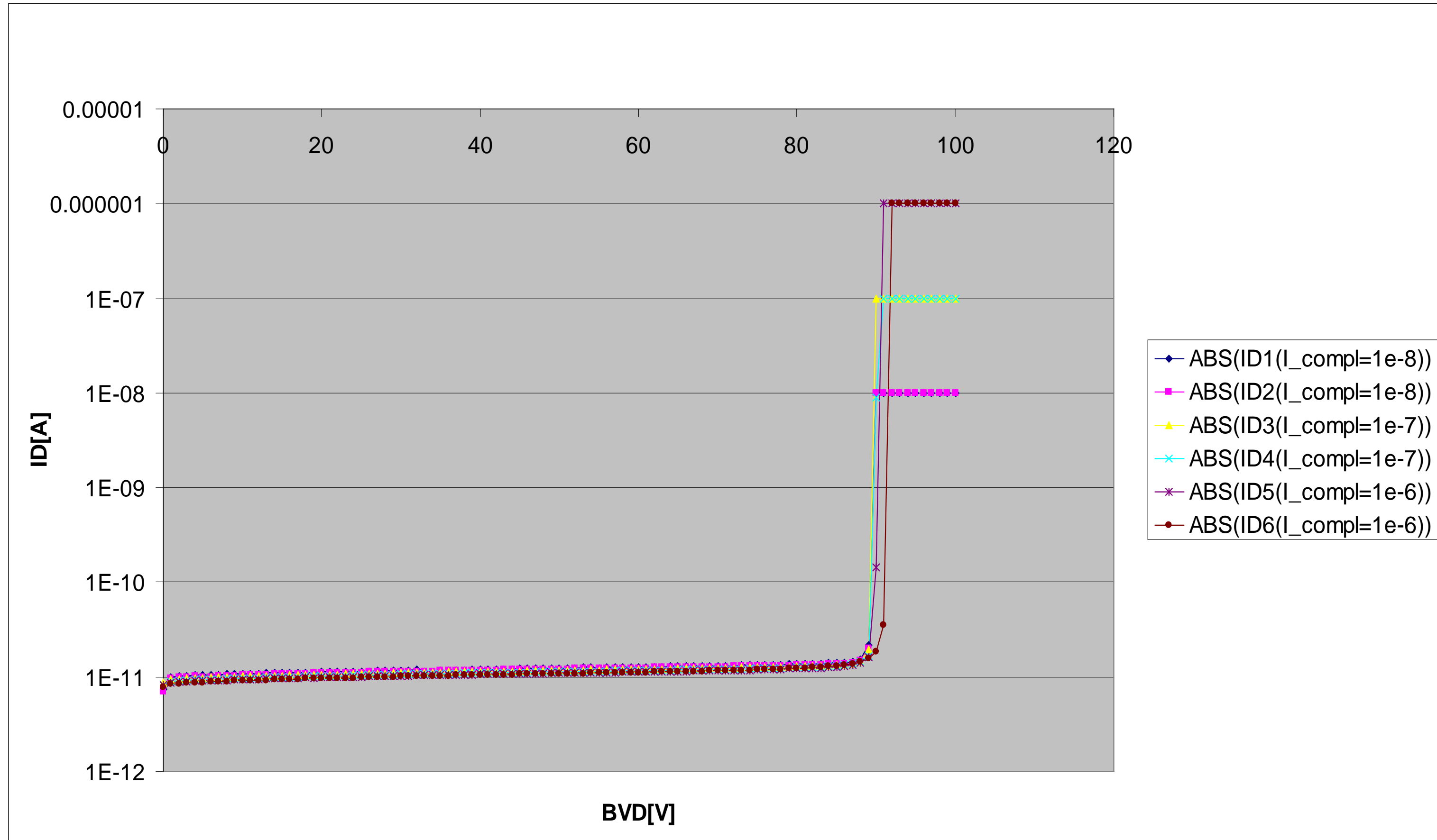
H18 Devices: NFETI50 Device Family

NFETI50M blocking curve



The breakdown should start abrupt without any premature leakage current

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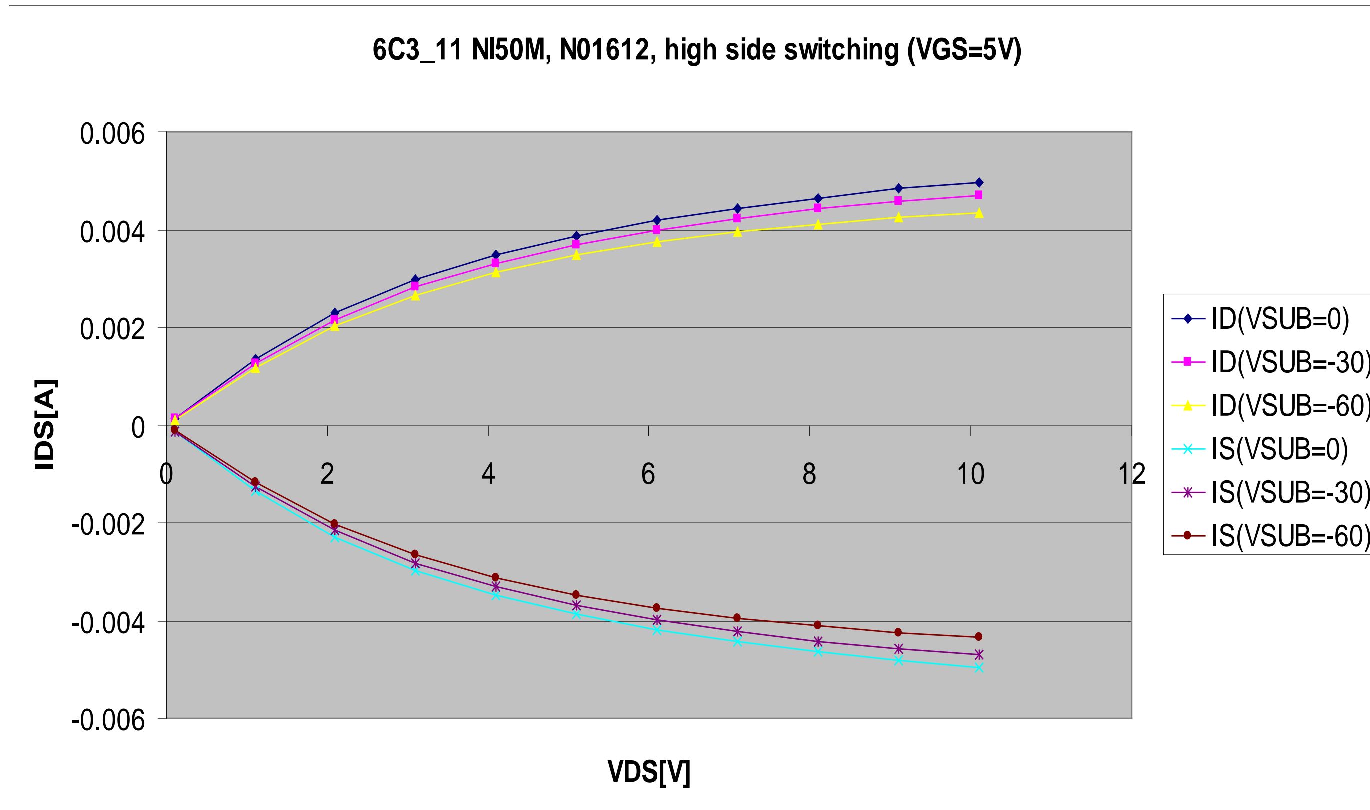
H18 Devices: NFETI50 Device Family

NFETI50M high side switching behavior



Note: The drain voltage in the curve with the lowest current is 60+10=70V above substrate potential.

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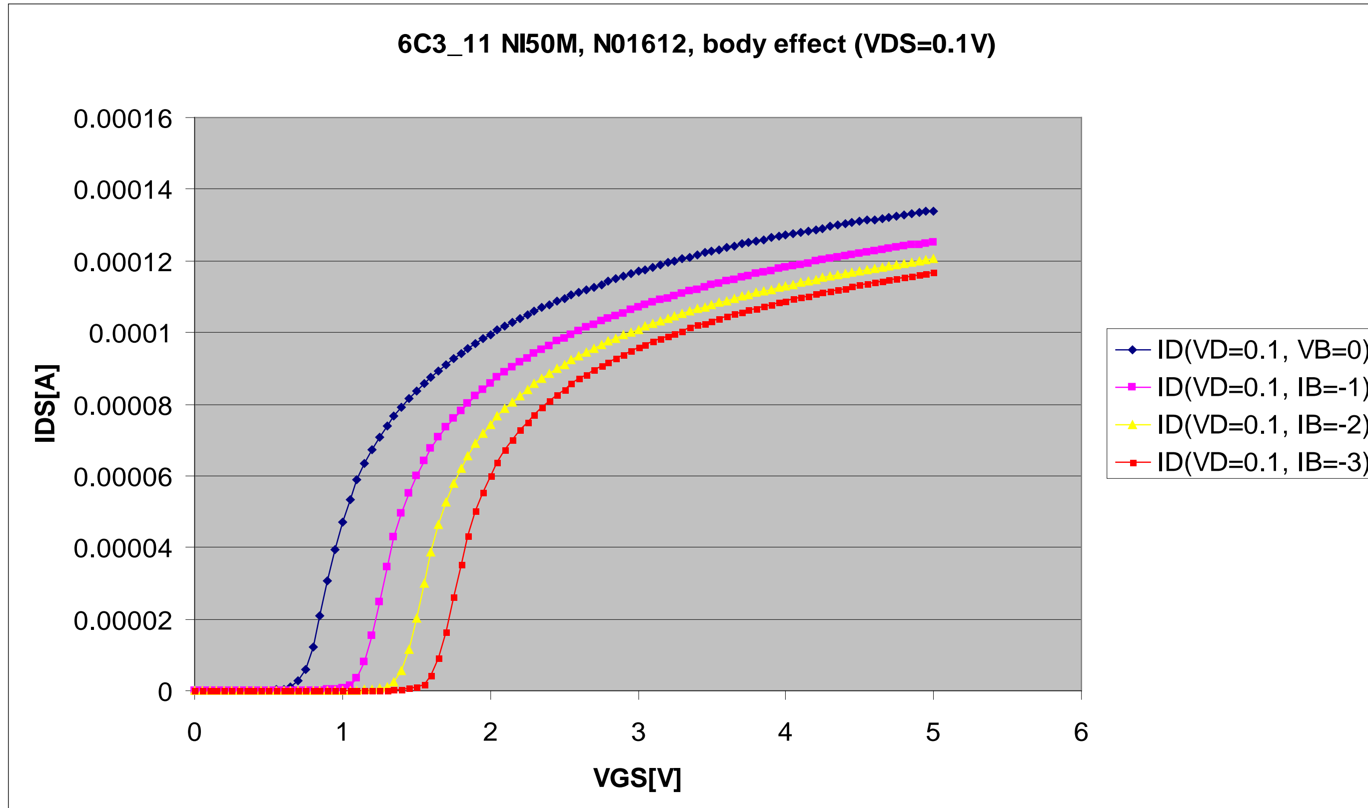
NFETI50M body effect



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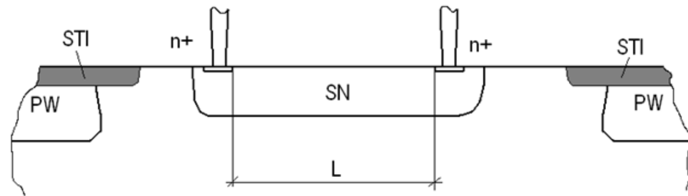
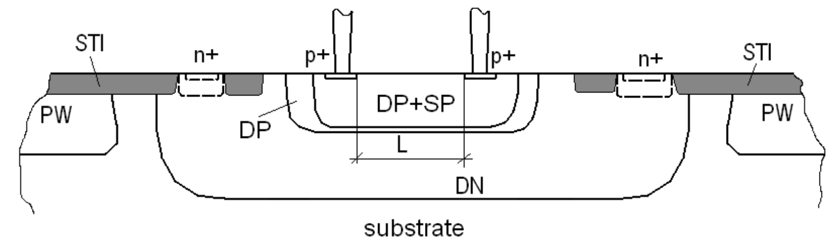
H18: HV Resistors

NW Resistor



- Linear current-voltage relationship over wide range of applied voltage
- Resistance scales with width

PW Resistor



- The pinch-off characteristic for high current density is modeled
- Weff calculated from various W/L

	Rs (Ω / sq)	Temp Coeff (linear) 10^{-3} / K	Temp Coeff (quad) 10^{-3} / K
HV NW Resistor	3074	5.14	1.47
HV PW Resistor	725	2.32	0.53

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H18: Low Voltage FET Options

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Device Description	H18 Spec Target Value Vt (mV)	Id sat (µA/µm)	Vdd (V)	Library Name
Thin ox NFET	355	600	1.8	nfet
Thin ox NFET in HV isolation	355	600	1.8	nfeti
Thin ox PFET	420	260	1.8	pfet
Thin ox PFET in HV isolation	420	260	1.8	pfeti
High Vt NFET	525	500	1.8	nfethvt
High Vt PFET	520	210	1.8	pfethvt
5V Medium ox NFET	625	630	5.0	nfetm
5V Medium ox NFET in HV isolation	625	630	5.0	nfetim
5V Medium ox PFET *	650	345	5.0	pfet
5V Medium ox PFET in HV isolation *	650	345	5.0	pfeti

All specifications match those found in C18
* Corresponds to shorter (0.5µm) gate length device

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Design Documents

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Basic Design & Process Information

Process Parameters Documents
- Operating conditions
- Structural & geometrical parameters
- Electrical parameters
- Figures of merit (e.g. FT ,FMAX)

Compact Modeling Documents
- SPICE Models
- Features and Limitations

Design Rule Documents
- Rules, Guidelines, Recommended
- Layout Structures

Element Layout Documents
- Element specification
- Internal only

RF-Design Documents
- RF-Devices
- RF Modeling
- Figures of merit (e.g. Qmax)

Noise Documents
- Noise Measurements
- Noise Modeling

Matching Documents
Matching Measurements
Matching Modeling

Parasitic Modeling
Parasitic diodes and
Bipolar Tr. for HVMOS

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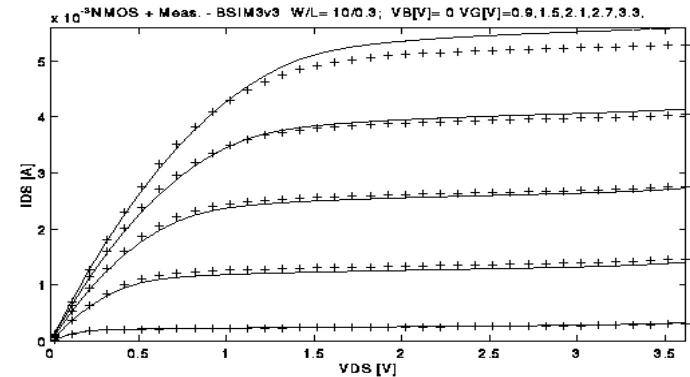
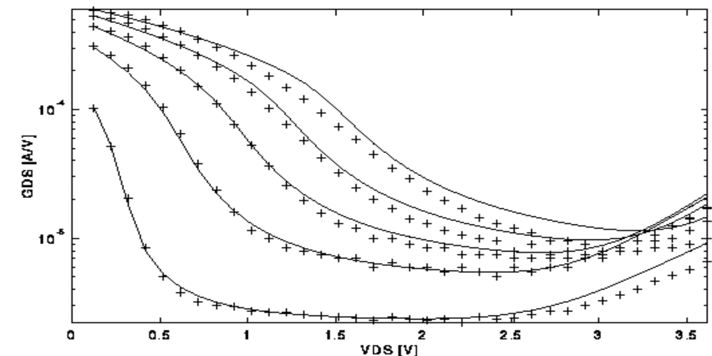
Compact modeling for the CMOS Process

- PSP & BSIM3v3 for std. MOS transistor
  - Scalable, physical, predictable.
- High voltage transistor modeled as sub-circuits
- JFET models for all diffusion resistors
- SGP model for all pnp (Vert,Lat)
- Voltage and Temp. dependent capacitance & resistor modeling
- Mismatch modeling for all devices
- Noise modeling (1/f & thermal noise)
- RF- modeling for MOS, Res, Cap, Varactor.





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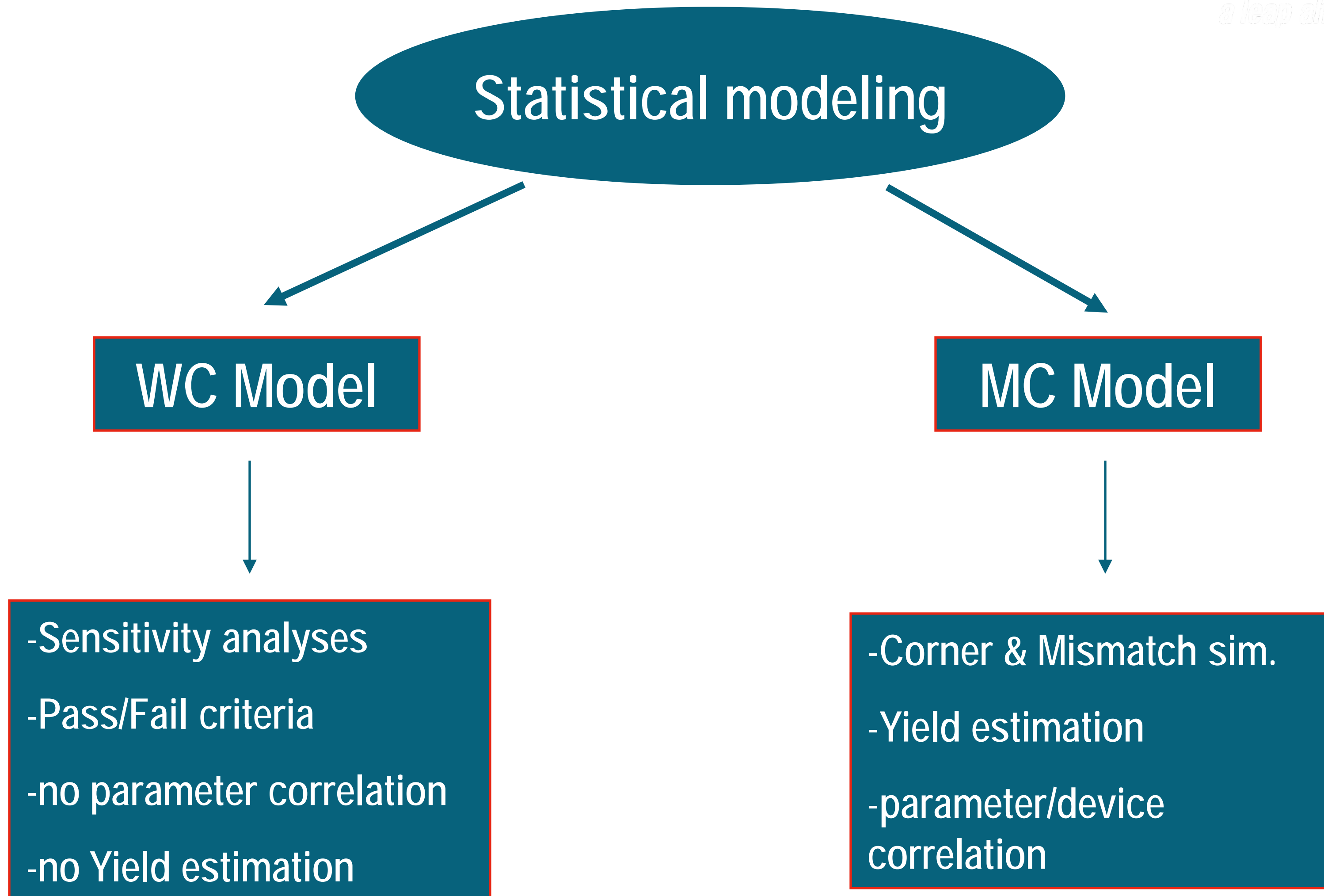
Process variation overview



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H35 120V Devices (Compact Modeling)

Model Features							
Device	Scalable Model	1/f noise*)	Temp. Modeling -40 – 180° C	Worst Case Model	Monte Carlo Model	Mismatch Parameter*)	parasitic model*)
NMOSI120M	x	x	x	x	x	x	x
NMOSI120H	x	x	x	x	x	x	x
PMOS120M	x	x	x	x	x	x	x
PMOS120H	x	x	x	x	x	x	x

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H35 120V Characteristic Curves

7.1 NMOSI120M

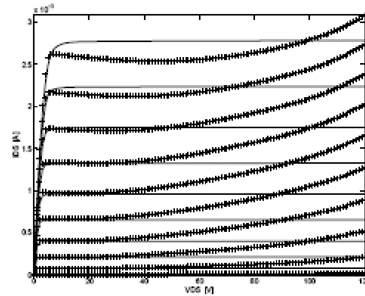

Fig.7.1.1 NMOSI120M output characteristic of a typical wafer. W/L=40/10, VGS= 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 V, VBS=0 V. + = measured, -- = BSIM3v3 model

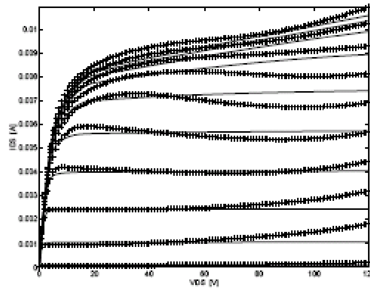

Fig.7.1.2 NMOSI120M output characteristic of a typical wafer. W/L=40/0.5, VGS= 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 V, VBS=0 V. + = measured, -- = BSIM3v3 model

7.2 NMOSI120H

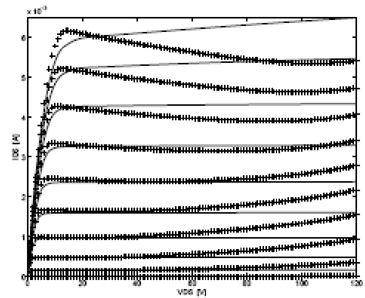

Fig.7.2.1 NMOSI120H output characteristic of a typical wafer. W/L=40/10, VGS= 2.9 4.8 6.7 8.6 10.5 12.4 14.3 16.2 18.1 20 V, VBS=0 V. + = measured, -- = BSIM3v3 model

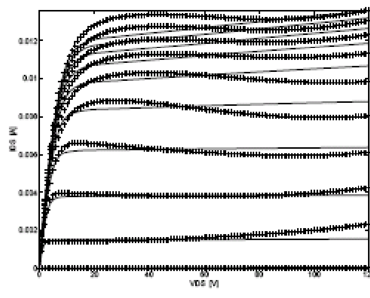

Fig.7.2.2 NMOSI120H output characteristic of a typical wafer. W/L=40/0.5, VGS= 2.9 4.8 6.7 8.6 10.5 12.4 14.3 16.2 18.1 20 V, VBS=0 V. + = measured, -- = BSIM3v3 model

7.3 PMOS120M

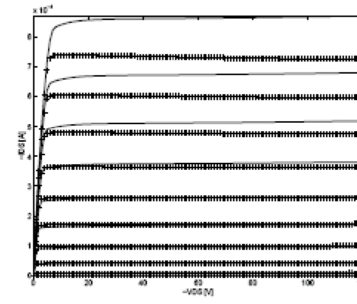

Fig.7.3.1 PMOS120M output characteristic of a typical wafer. W/L=20/5, VGS= -1.0 -1.5 -2.0 -2.5 -3.0 -3.5 -4.0 -4.5 -5.0 -5.5 V, VBS=0 V. + = measured, -- = BSIM3v3 model

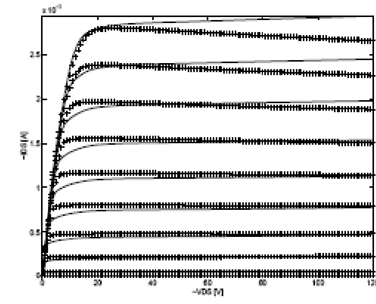

Fig.7.3.2 PMOS120M output characteristic of a typical wafer. W/L=20/1, VGS= -1.0 -1.5 -2.0 -2.5 -3.0 -3.5 -4.0 -4.5 -5.0 -5.5 V, VBS=0 V. + = measured, -- = BSIM3v3 model

7.4 PMOS120H

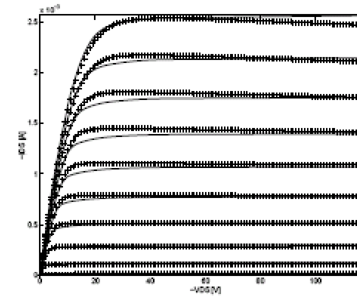

Fig.7.4.1 PMOS120H output characteristic of a typical wafer. W/L=20/5, VGS= -2.9 -4.8 -6.7 -8.6 -10.5 -12.4 -14.3 -16.2 -18.1 -20 V, VBS=0 V. + = measured, -- = BSIM3v3 model

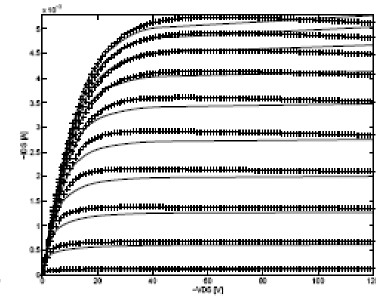

Fig.7.4.2 PMOS120H output characteristic of a typical wafer. W/L=20/1.2, VGS= -2.9 -4.8 -6.7 -8.6 -10.5 -12.4 -14.3 -16.2 -18.1 -20 V, VBS=0 V. + = measured, -- = BSIM3v3 model

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HiSIM-HV Model for HV LDMOS

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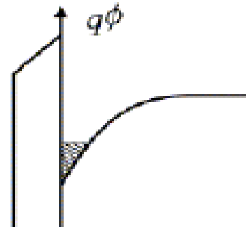
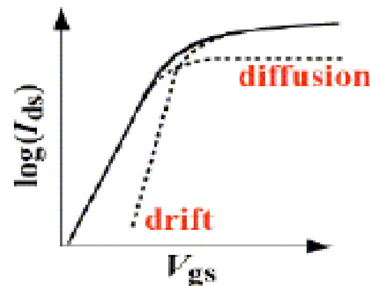
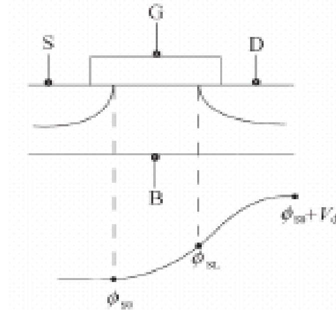
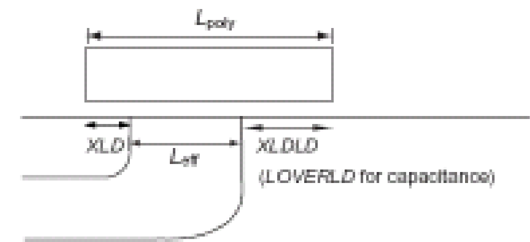
- Developed as extension of HiSIM: Complete surface potential based model
=> unified description of device characteristics for all bias regions
- Based on drift-diffusion theory using charge sheet and gradual channel approximation







- Capable of modeling symmetrical and asymmetrical devices: COSYM= 0/1
- Self-heating effect modeling: COSELFHEAT=0/1
- Substrate current modeling: COISUB=0/1



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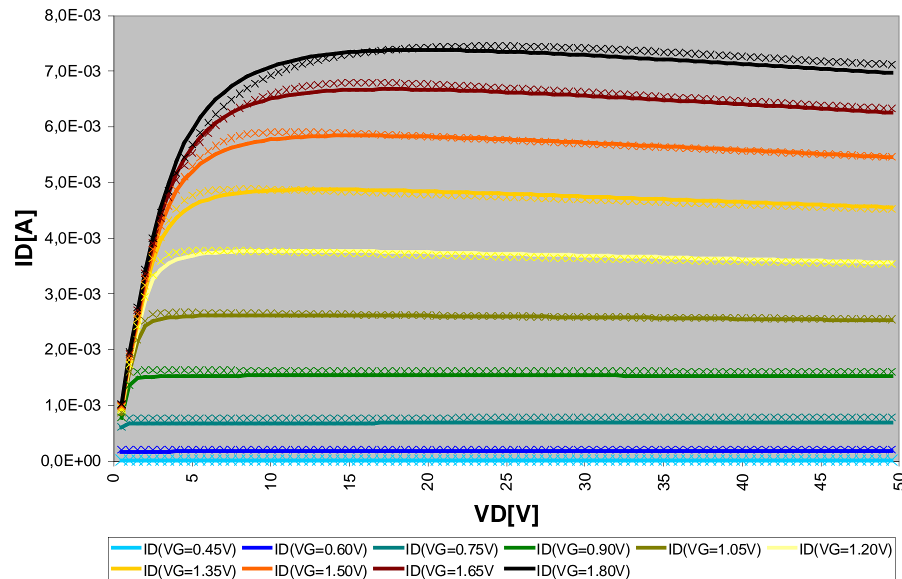
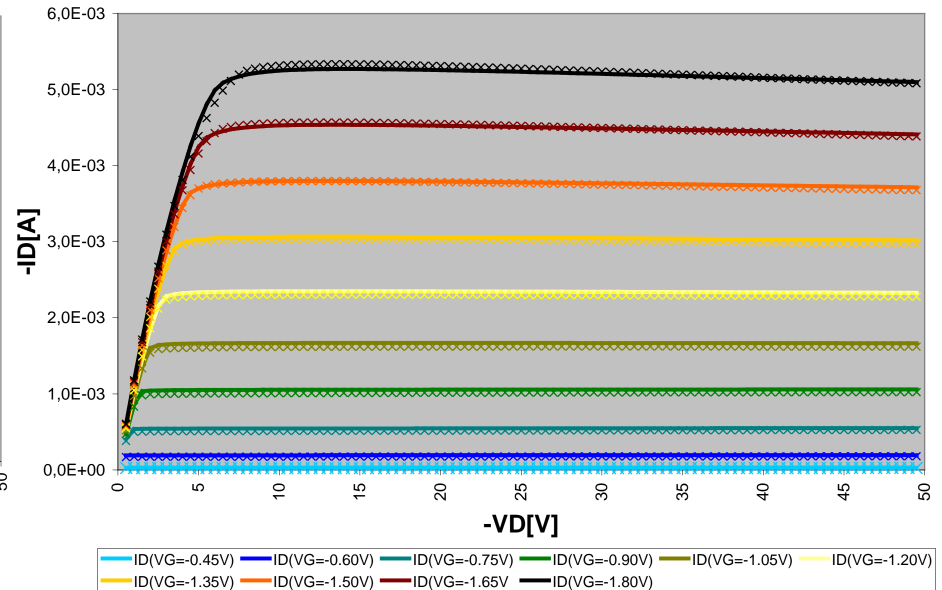
HV HSIM_HV Model to Hardware Results





Excellent agreement between measured results and HiSIM_HV SPICE model.

Model features include:

- Surface potential iterative calculation used for an accurate description of drift region
- Self-heating included
- Simulation speed and accuracy is improved compared BSIM (SPICE) + subcircuit.

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Outline

Let's scale down first

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Technology Integration

High Voltage Device Description

Low Voltage RF Device Description

Device Models

ESD, SOA and Reliability

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Conclusions

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H18: LV and HV ESD Protection

Strategies for 1.8V and 5.0V Applications:

- Power Supply Protection Devices
  - 1.8V or 5.0V RC-Triggered Power Clamp
  - 1.8V or 5.0V Silicide-Blocked NFET
- I/O ESD Protection Devices
  - P^+/NW Diodes
  - N^+/PW Diodes
  - 1.8V or 5.0V Silicide-Blocked NFET
- ESD protection devices are offered in standard well and in HV Well

Strategies for 20V, 25V and 50V:

- Power Supply Protection Devices
  - HV Clamp based on 20V, 25V or 50V HV-PFETs
- I/O ESD Protection Devices
  - 25V Forward Diode
  - 50V Forward Diode

Characterization

- Use 100ns TLP, 30ns and 1ns TLP to emulates device behavior under HBM, MM and CDM conditions
- Also wafer level testing with HBM tester

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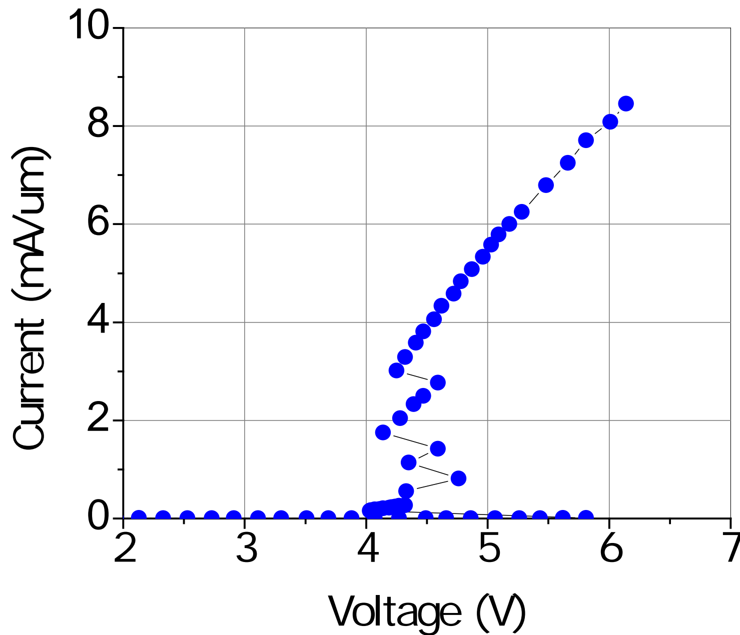
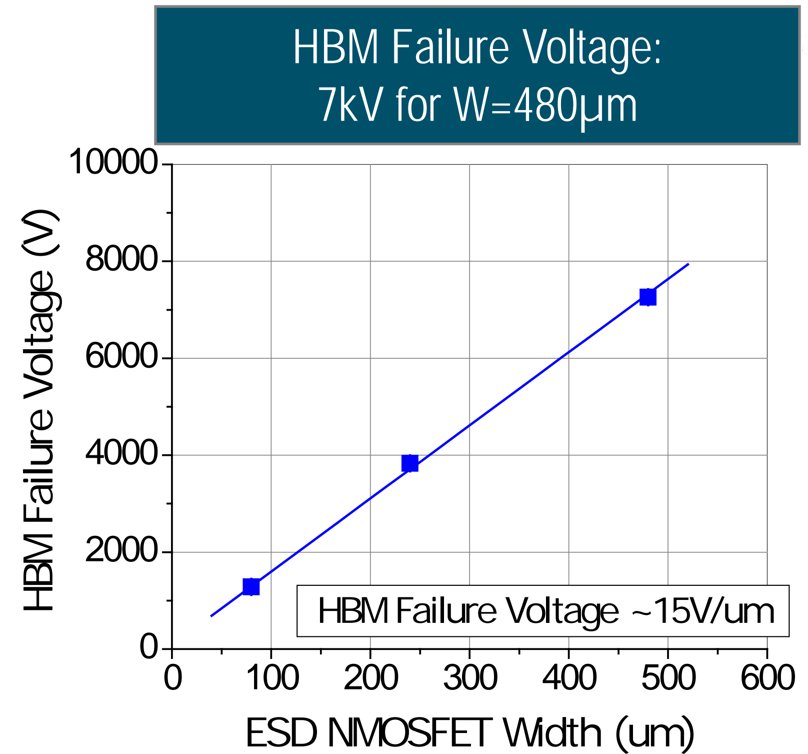
LV Silicided 1.8V NFET Scalability

HBM Failure Voltage:
7kV for W=480µm





– 100ns TLP I-V of a 1.8V, gate-grounded silicide-blocked NFET with drain silicide-block length of 2µm

– HBM data shows good scaling of failure voltage ~15V/µm of device width

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H18 ESD Solutions

– ESD protection devices are available in H18 HIT-Kit for protection of **low voltage and high voltage devices**

– ESD devices are designed to be **fully scalable** to enable a area optimized solution

– Detailed recommendations and ESD data summary is available in **ESD Reference Guide** that is provided with the HIT-Kit

– **ESD Design review** is provided upon request for all designs

– Demonstrated scalable ESD solutions (**HBM 2-8kV)**

– Failure currents of protections exceed tester capability

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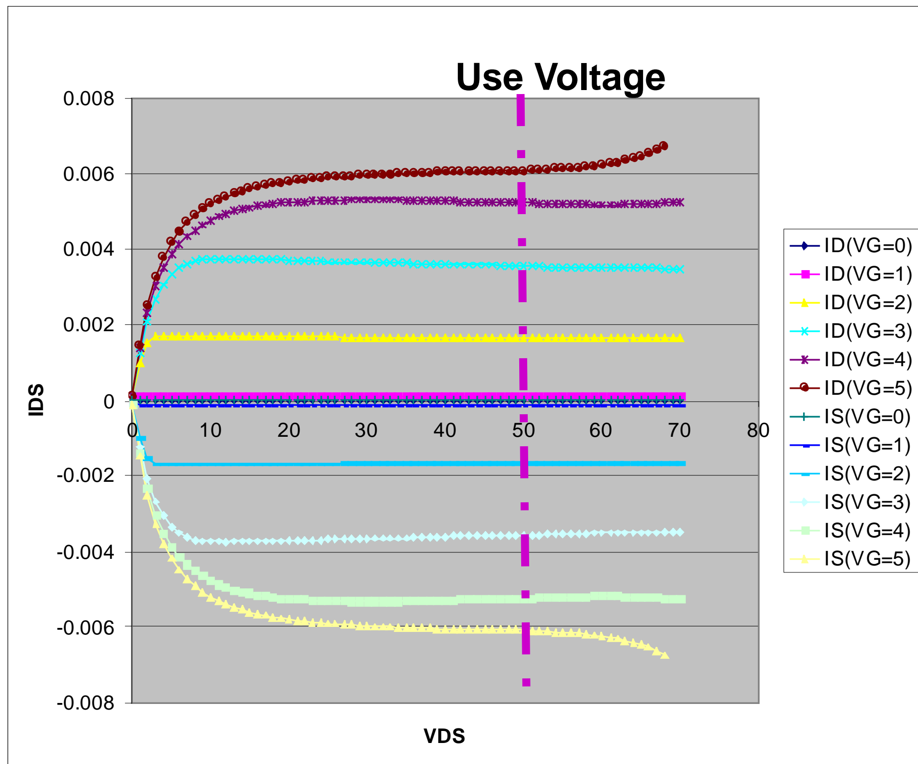
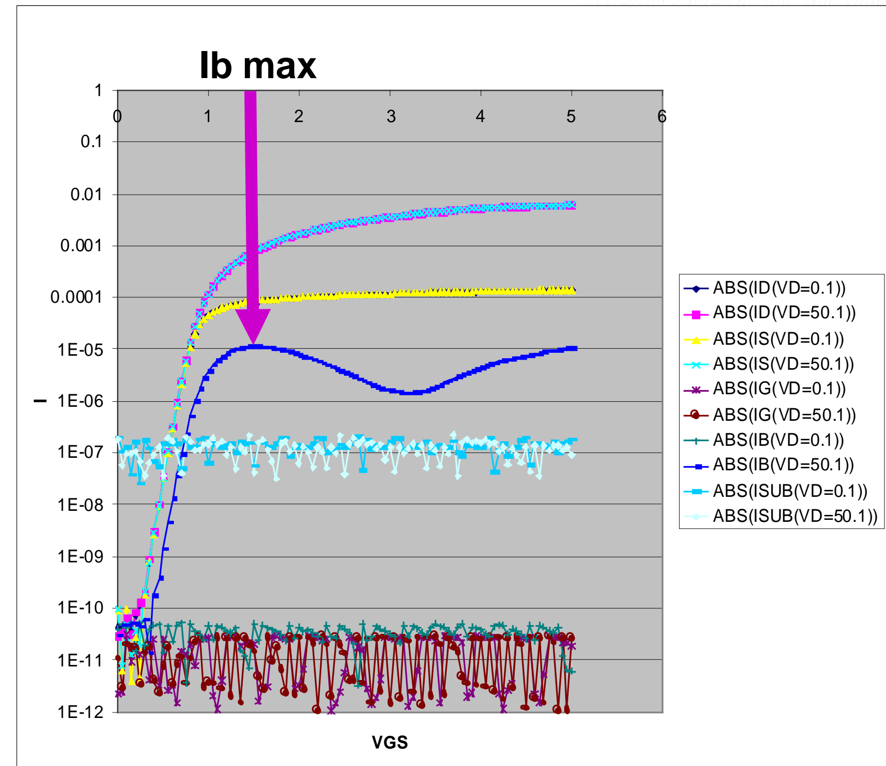
HV NFET SOA and Reliability





Forward IV and body current plots for isolated HV NMOS NFETI50M

- Output current stable (Ids) beyond use voltage
- Body current (Ib) peaks at Vgs~1.5V

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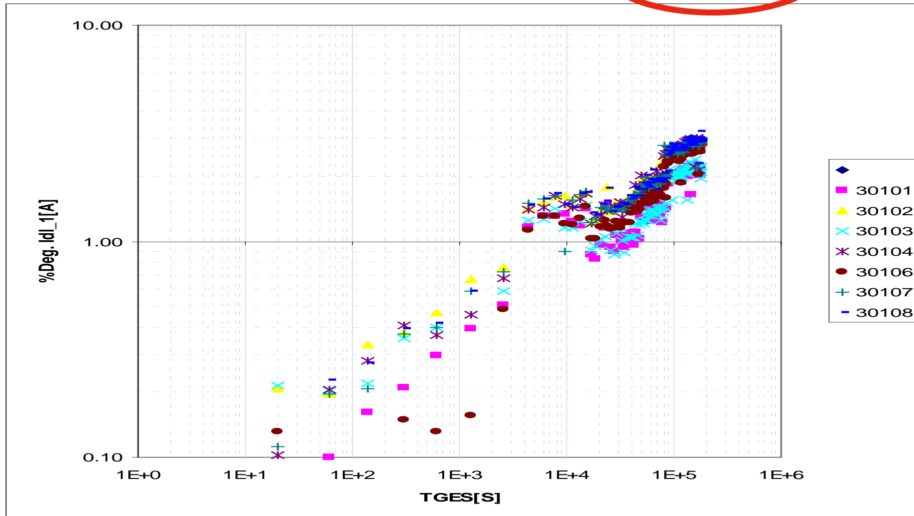
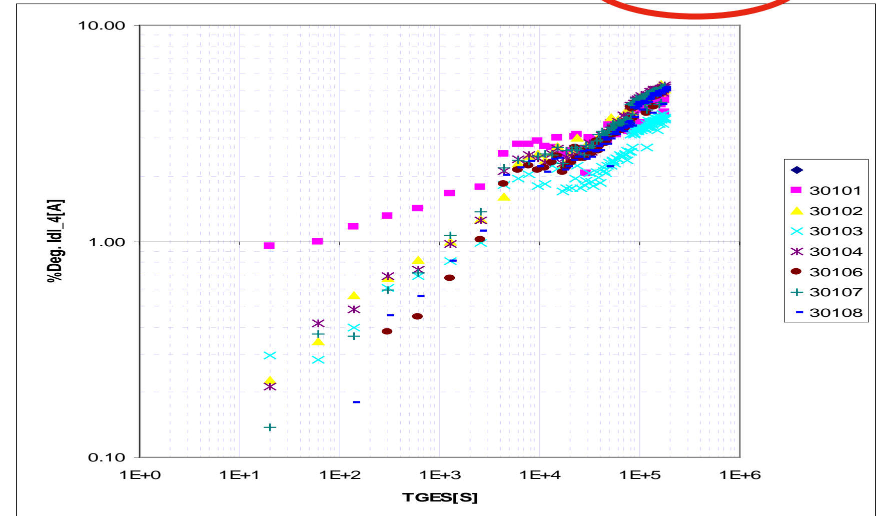
HV Isolated NFET Idlin Stability (NFETI50M)

Stress Vd=50, VG= 1.5
Delta Id lin at Vd=0.1, VG=1.3V



Stress Vd=50, VG= 1.5
Delta Id lin at Vd=0.1, VG=4.3V



- Id_{lin} parameter shift with (stress time) is key for power applications
- Measure Id_{lin} stability after stress at Vds=50V, Vgs=1, 1.5V (worst case)
  - Gm, Vt, Id_{sat} drift << Id_{lin}
- Use data to construct SOA tradeoffs with respect to L, Vd,% shift (lifetime)
- Id_{lin} lifetime > 10 years ; ***industrial*** and ***automotive*** grade stability
- Id_{lin} lifetime @60V stress exceeds ***consumer*** grade stability

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Qualification Strategy - Overview

Temperature lifetime profile: (-40 … +125)° C for 15 years

(-40 … +150)° C for 10 000 hours

Voltage levels: VG…1.98V/5.5V/20V

VD…1.98V/5.5V/20V/50V

Oxides: Defect Density: <1 Defect/cm^2

max. oxide area: 5mm^2

ESD: ESD Library up to 4kV HBM*

*** According to MIL-STD-883C method 3015.7 and JESD22-A114 and ANSI/ESD STM5.1**

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Design Environment: HIT-Kit

Analog/Mixed Signal High Performance Interface Tool Kit

The AMS HIT-Kit enables product developers to concentrate on their core competence IC design rather than on setting up and mastering the EDA environment

This leads the Partner to:

- **Shorter Time to Market**
- **Complete Environment for First Time Right Designs**
- **More Efficient Designs (Die Size, Performance, Yield)**

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LTacc – LifeTime Acceleration Factor for Simulation

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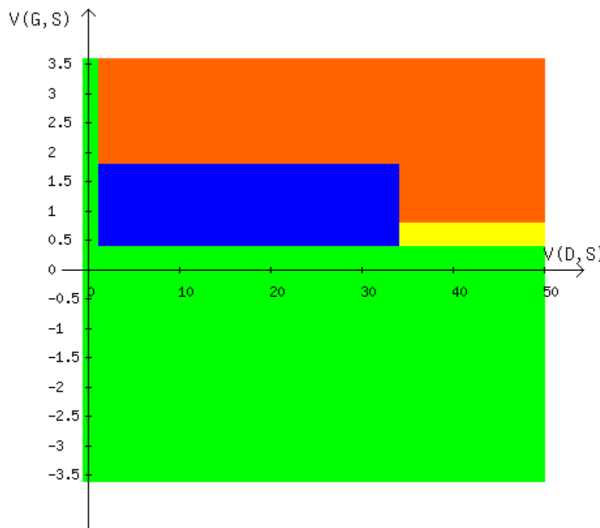
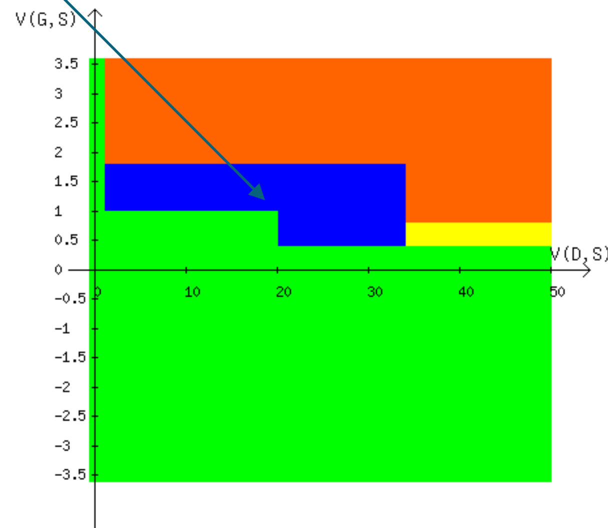
LTacc defined in the Process Parameter Document:

HV NMOS Transistors	Device name	max. VGS [V]	max. VDS [V]	max. VGB [V]	max. VDB [V]	max. VSB [V]	LTacc	Device length [µm]	Note	
High voltage NMOS with thin gate oxide	NMOS50T	1.8	34	3.6	50		100	0.5	Q1,Q4,Q5	Digital
		0.8	50			3.6	600			
		1.0	20	1.2	20		1	2.5	Q2,Q4,Q5	Analog
		3.6 (5)	50 (55)	3.6 (5)	50 (55)	3.6 (5)	2000	0.5	Q1,Q4,Q5	Digital

Digital





Analog

* Taken a very bad device a example

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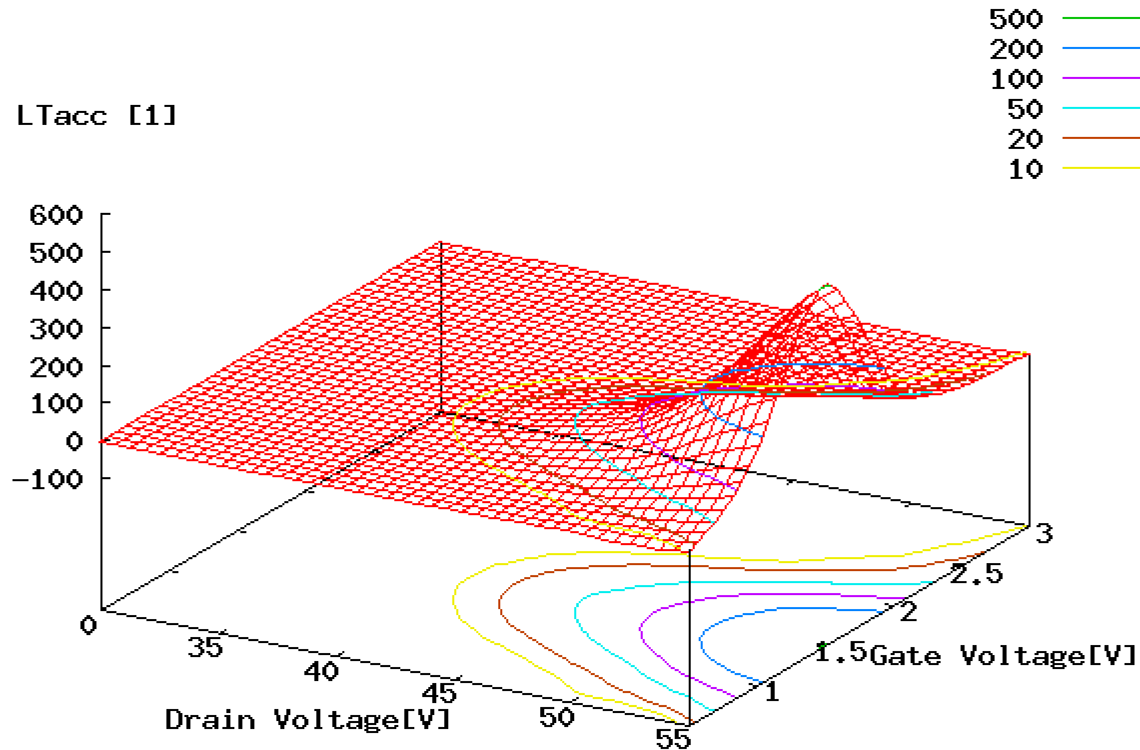
NMOS50T HC Reliability Model

-Acceleration Factors for NMOS50T based on self-heating and operating conditions analysis.



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HIT-Kit Benefits

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- “Plug and Play” for IC designers
- All major EDA tools supported
- All process technologies supported with latest versionsof EDA tools
- All devices supported throughout the whole design flow
- Complete modeling of active and passive devices

(high accuracy, Monte Carlo, corner, mismatch, noise, HDL, IC package, up to system level)

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HIT-Kit Benefits (cont.)

- **Supports complete flow for RF, Mixed Signal and High Voltage design**
- **Additional Userware for special Tasks**
  (Bonding-Diagram Editor,Safe Operating Area Check, Revision Block Generator etc.)
- **Full Mixed-Signal Library Concept**
- **HIT-Kit is fully compliant with QS9000 quality certificate**
- **HIT-Kit developers provide technical support**

DNV

CERTIFICATE

DNV ZERTIFIZIERUNG UND UMWELTGUTACHTER GMBH

certifies, that the company

austriamicrosystems

austriamicrosystems AG

at the site

Schloß Premstätten
A-8141 Unterpremstätten

has established a quality management system in conformity with the standard

QS-9000 : 1998
(based on and including EN ISO 9001 : 1994)
Semiconductor Supplement, 2nd edition

The company has been audited in accordance with the requirements of QS-9000 Appendix B, Code of Practice for Quality System Registrars.

This Certificate is valid for:

Design, manufacturing and sales of ASICs (Application Specific Integrated Circuits) and ASSPs (Application Specific Standard Products) and systems solutions

This certificate is valid until:

Certificate Registration No.:

Essen, 2002-06-17 — M. Fröhlich, Manager

Essen, 2002-06-17 — Operations Manager

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Customer Support

Hotline

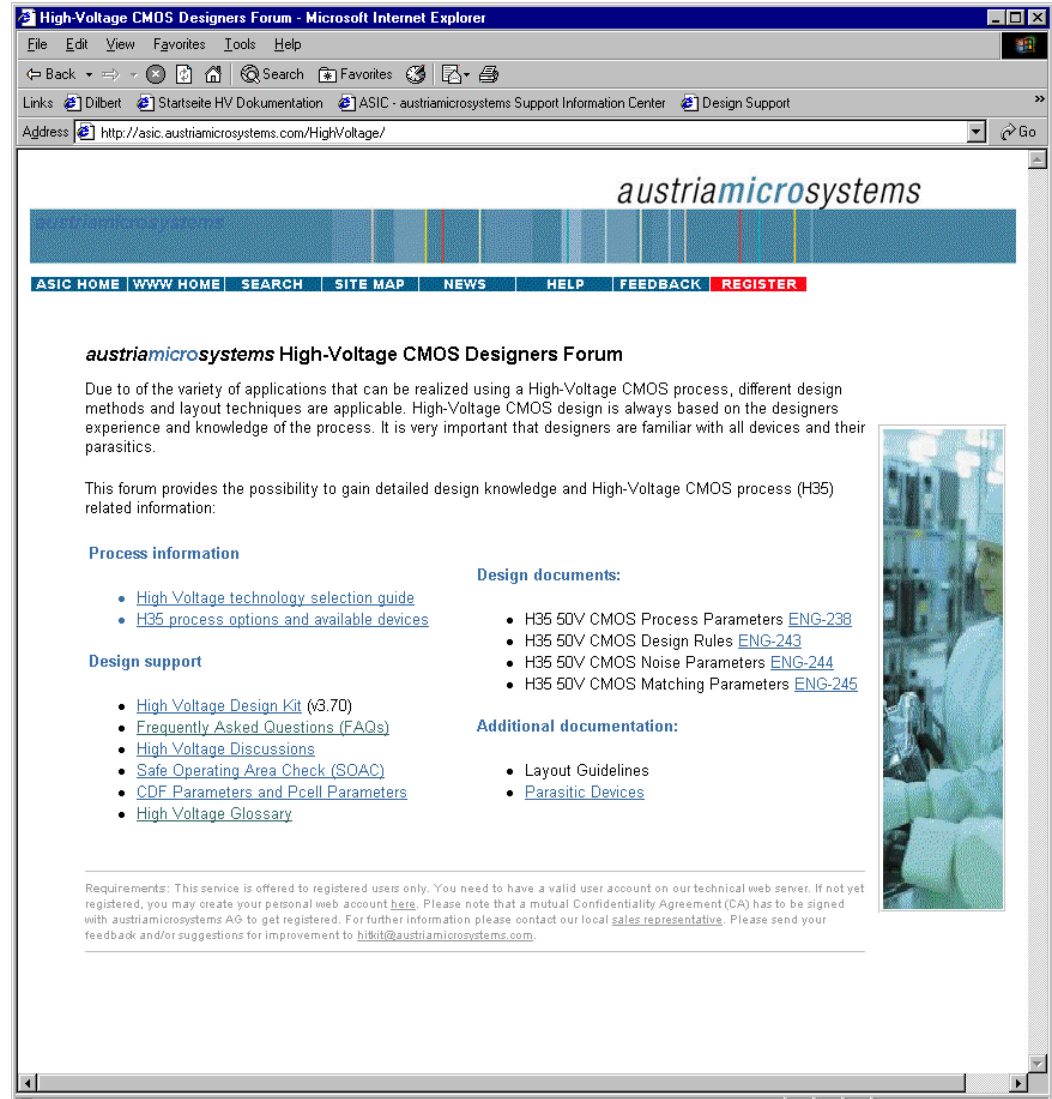
Online Documentation

http://asic.austriamicrosystems.com

- Data sheets
- Design Documents
- HIT-Kit Information
- Tool usage
- News & Alerts
- Download area

Special High-Voltage Designer Forum

Training & Tutorials



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Summary and Conclusions

- H35/H18 is a HV CMOS power management platform which exceeds or matches BCD technology performance at lower process complexity (cost).
  - HV n- and p-channel specific on-resistance is lower than all foundry offerings from 30V-80V BV_{ds}
  - offers a rich suite of HV FETs, bipolars, JFETs and SBDs in a triple-well triple-gate oxide process
- H35/H18 supports a rich suite of passive components including precision resistors, capacitors, varactors, ESD components
- H35/H18 LV devices are IP-compatible to the CMOS 350/180nm platform (C35/C18) for IP re-use across derivative nodes
- H35/H18 device library is hardware verified with full reliability qualification
- We offer a long experience of High-Voltage CMOS process development and design to our customers.

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Some famous last words....

Do you have it in smaller size?

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