SILICONGATE

Powering Your Success

Designing Charge Pump Based Converters

JUN 2011

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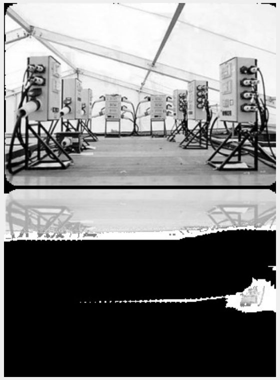
CHARGE PUMPS



Advantages

No coils!

Low EMI (if well designed)

Fully integrated (if you only need a few 1uA)

Digital control (when regulation is needed)

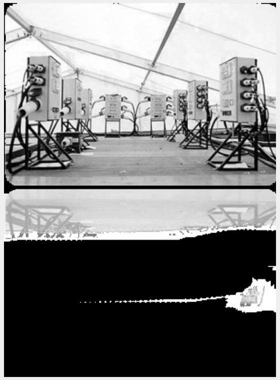
Disadvantages

Lower efficiency (if you need to regulate the output voltage)

More switches and more silicon area

Large inrush currents (if badly designed)

CHARGE PUMPS



When to use?

When you cannot use coils

Extra silicon area is not a problem

System has long standby periods

Pins are available

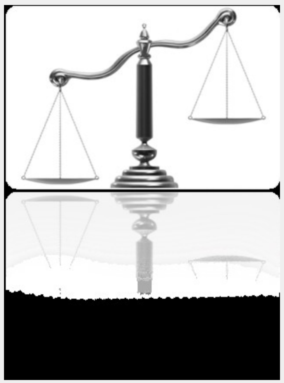
Output current range is medium 10 mA – 1 A*

Or

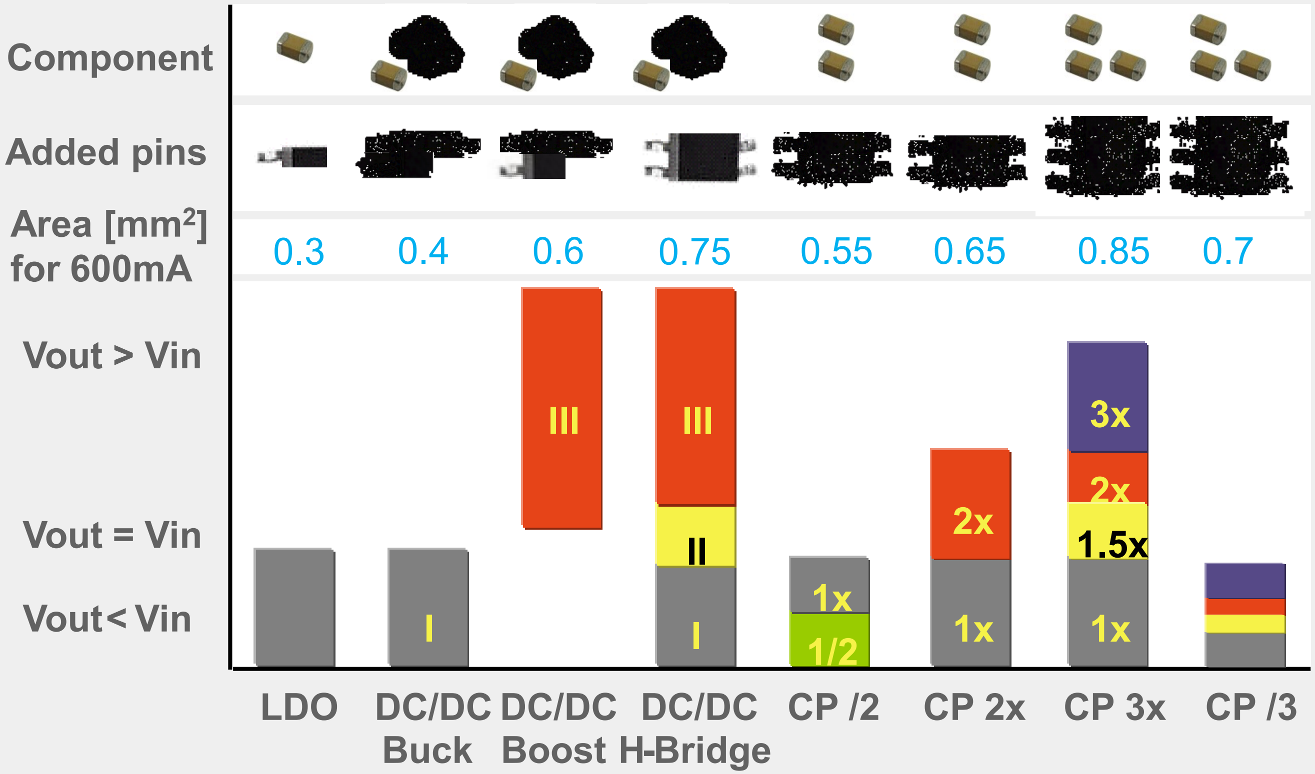
Fully integrated

Small currents <100 uA

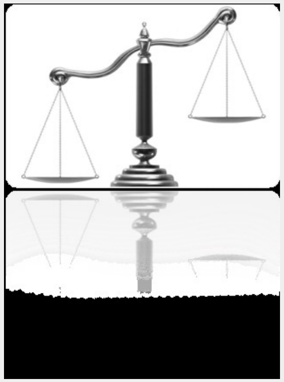
CHARGE PUMPS

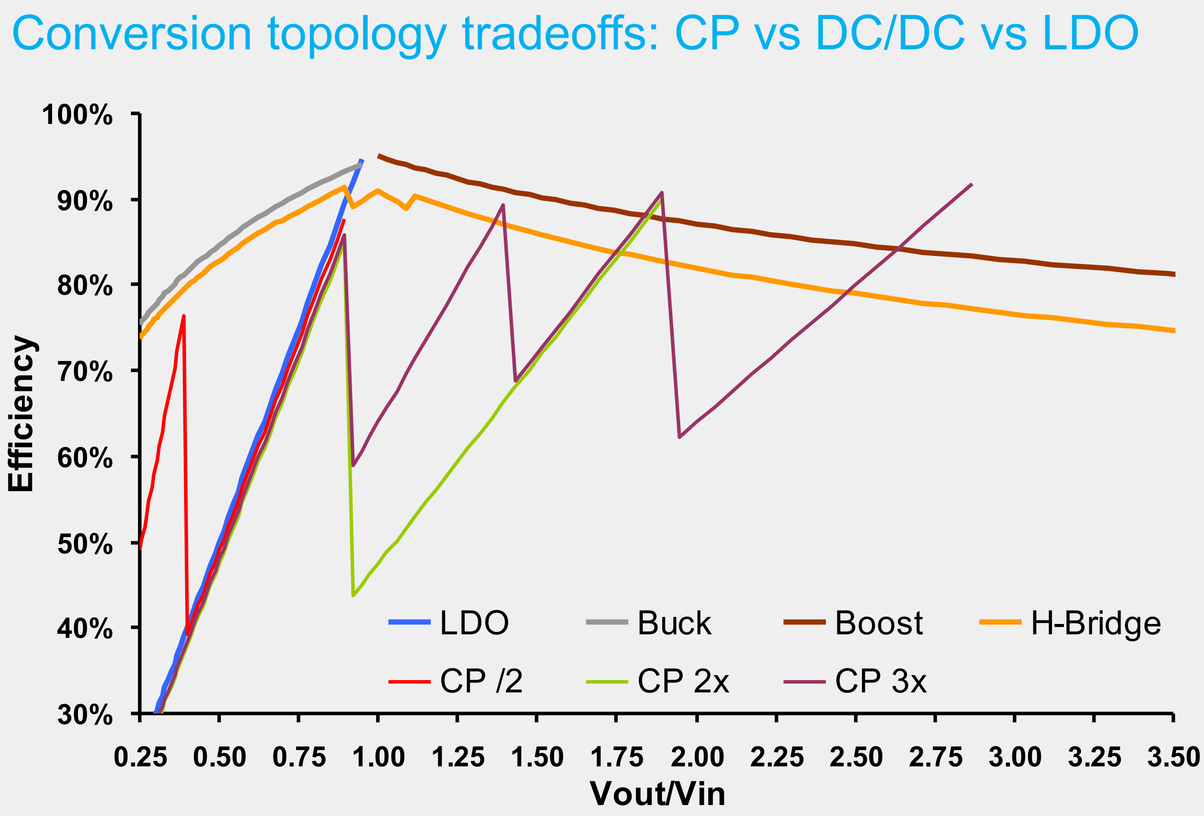


Conversion topology tradeoffs: CP vs DC/DC vs LDO



CHARGE PUMPS





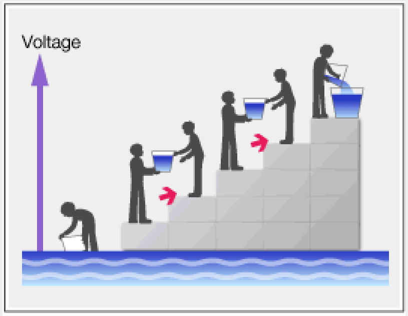
CHARGE PUMPS

In principle

Easy to understand

Simple to design

Very quick to develop



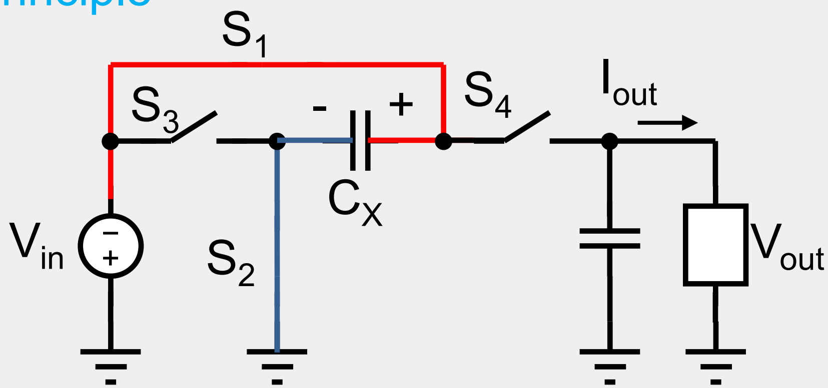
Working image of charge pump circuit
(www.sii.co.jp)

At the end

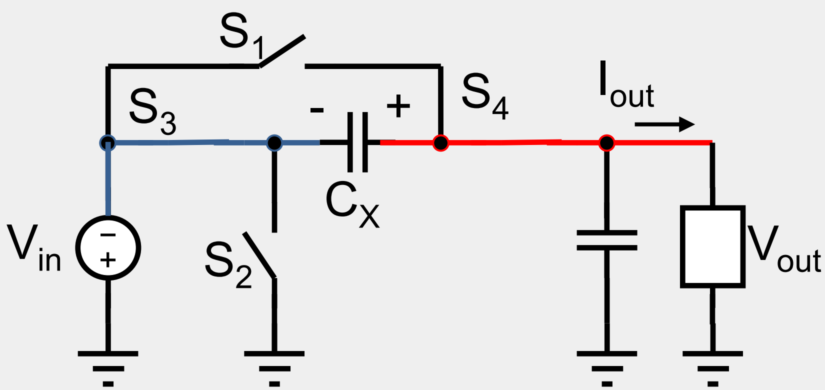
As complex as any engineer might like ☺

CHARGE PUMPS

In principle

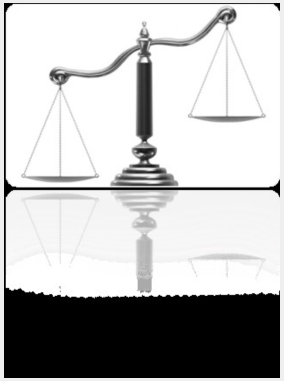


$V_{cx}=V_{in}$



$V_{out}=V_{cx}+V_{in}=$
$=2.V_{in}$

CHARGE PUMPS



Ideally

Fixed voltage gain

(G= 1/3, ½ , 2/3, 1x, 2x, 3x)

$$V_{out} = G \cdot V_{in}$$

$$I_{out} = \frac{1}{G} \cdot I_{in}$$

$$\eta = 100\ \%$$

In reality

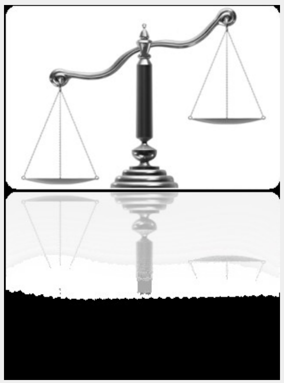
Looses so output voltage drops with load

$$V_{out} = G \cdot V_{in} - I_{out} \cdot R_{eq}$$

$$I_{out} = \frac{1}{G} \cdot I_{in}$$

$$\eta = 1 - \frac{R_{eq} \cdot I_{out}^2}{V_{in} \cdot I_{in}}$$

CHARGE PUMPS



Ideally

No voltage control

$$V_{out} = G \cdot V_{in} - I_{out} \cdot R_{eq}$$

$$I_{out} = \frac{1}{G} \cdot I_{in}$$

$$\eta = 1 - \frac{R_{eq} \cdot I_{out}^2}{V_{in} \cdot I_{in}}$$

In reality

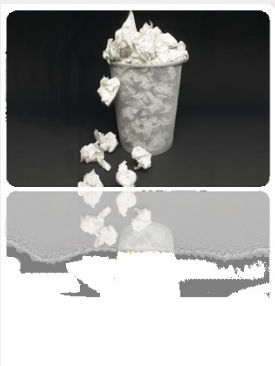
Voltage control is required (usually a system requirement and also pulse skipping reduces switching losses at light loads)

$$V_{out} = V_{prog} < G \cdot V_{in} - I_{out} \cdot R_{eq}$$

$$I_{out} = \frac{1}{G} \cdot I_{in}$$

$$\eta = \frac{V_{out}}{G \cdot V_{in}}$$

CP PROB & SOL



Need regulation

High quiescent current

High ripple

High inrush current

Large Vi range

Noise

Pulse skipping control

Slow turn-on switches

Current limited switches

Incomplete charging with digital control

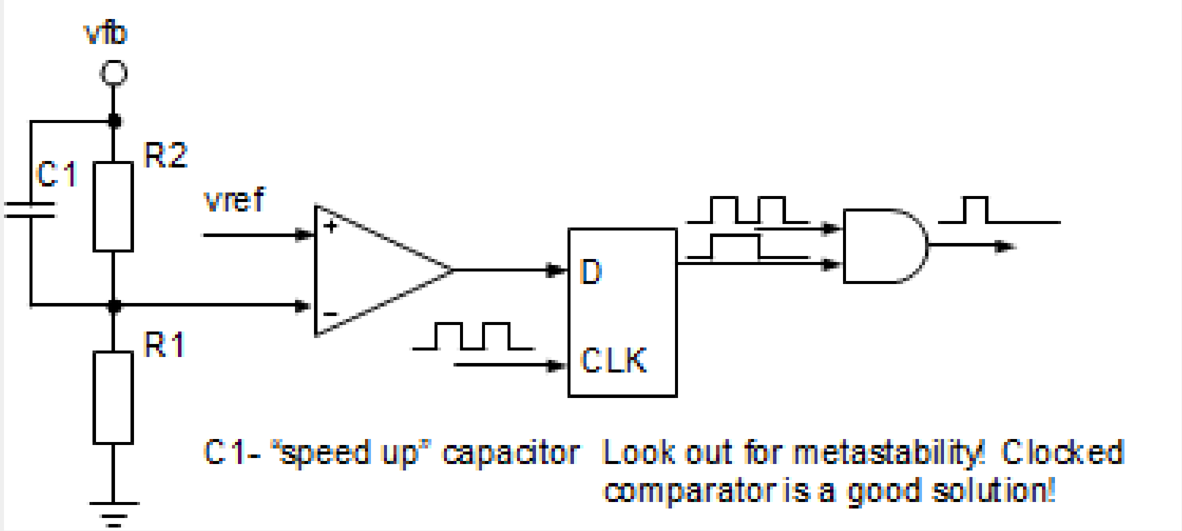
Over current comparator

Multi-mode digital control

Avoid PMOS body diodes turn on

NEED REGULATION

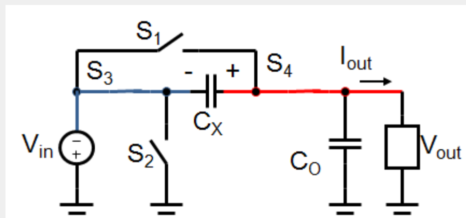
Pulse skipping as simple as it gets ☺



If you use this simple version you will probably get large ripple output!!

HIGH RIPPLE

As bad as it gets at full charge/discharge with regulation ☹



$$C_X > \frac{I_{out} \cdot T}{(2 \cdot V_{in} - V_{out})}; \quad C_O >> C_X$$

$$V_{ripple\ 1} \approx (2 \cdot V_{in} - V_{out\_n-1}) \frac{C_X}{C_X + C_O}$$

Might be

$$V_{ripple} \approx (2 \cdot V_{in} - V_{out}) \frac{ESL_{CO}}{ESL_{CX} + ESL_{CO} + L_{bond}} >> V_{ripple\ 1}$$

or

Might be

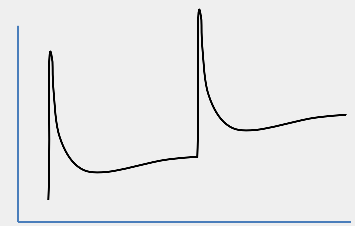
$$V_{ripple} \approx (2 \cdot V_{in} - V_{out}) \frac{ESR_{CO}}{ESR_{CX} + ESR_{CO} + R_{bond} + R_{SW}} >> V_{ripple\ 1}$$

HIGH RIPPLE

Inductive dominated ripple

$$V_{ripple} \approx (2 \cdot V_{in} - V_{out\_n-1}) \frac{ESL_{CO}}{ESL_{CX} + ESL_{CO} + L_{bond}}$$

Slow turn-on switche



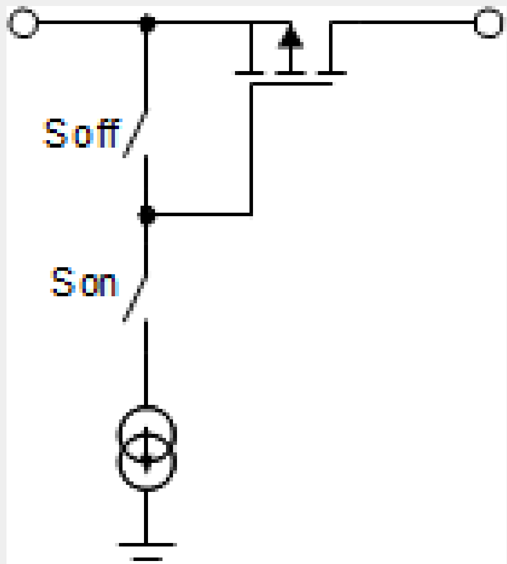
Resistive dominated ripple

$$V_{ripple} \approx (2 \cdot V_{in} - V_{out\_n-1}) \frac{ESR_{CO}}{ESR_{CX} + ESR_{CO} + R_{bond} + R_{SW}}$$

Current limited switches OR Incomplete charging

SLOW TURN-ON SW

Good solution for inductive dominated ripple and EMI reduction

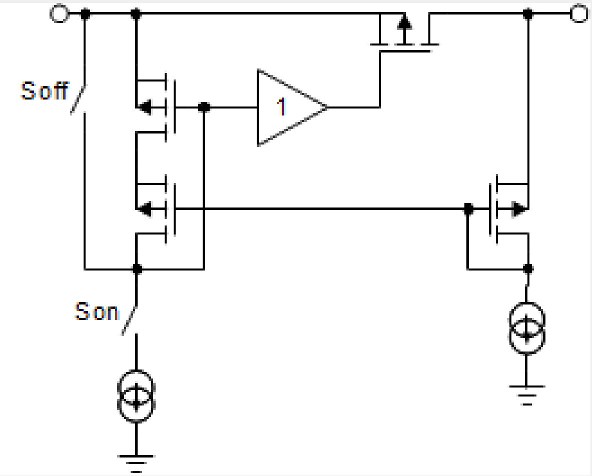


Simple but effective slow turn-on switch

(do not use ideal current sources)

CURRENT LIMITED SW

Good solution for resistive dominated ripple and current limitation



Stability needs to be checked with bond wire and capacitor parasitic

Improves incomplete charging digital control (better solution than using Rdson or additional resistors to limit charging current)

INCOMPLETE CHARGING

With digital control

Simple

Effective

Lower ripple

Maintains fast response to load transients

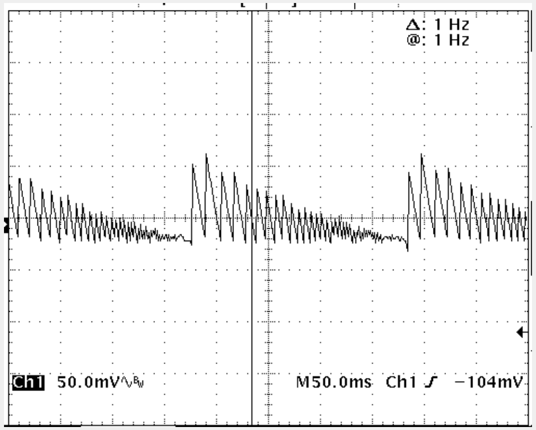
Requires larger flying capacitor

Requires some type of current limitation:

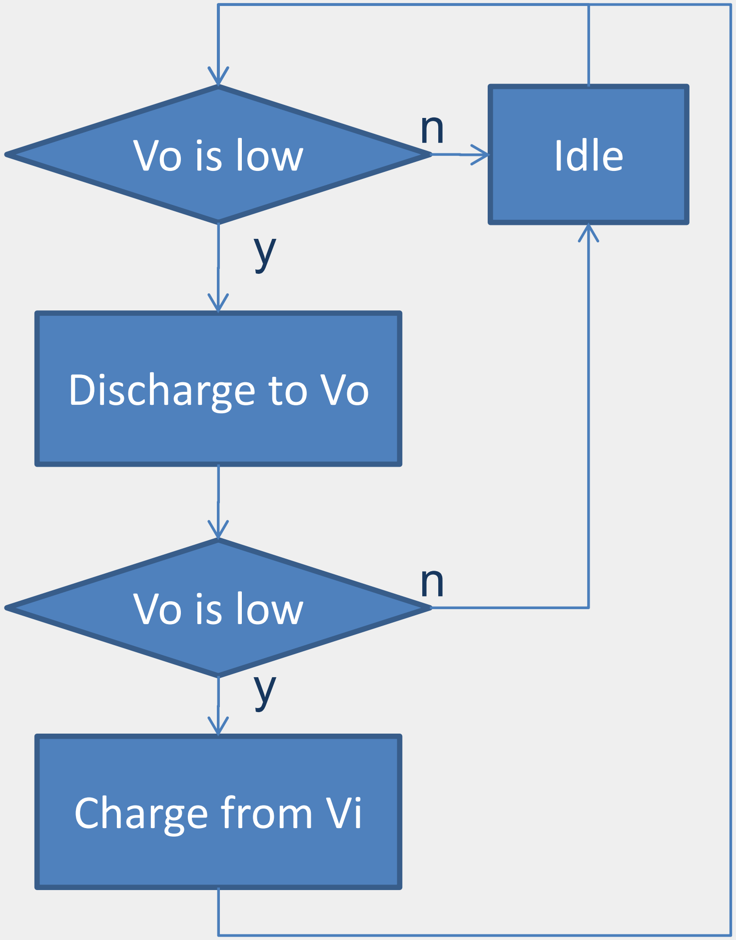
Rdson; additional R; current limited switches

INCOMPLETE CHARGING

Digital control of flying capacitor states and R limited charging/discharging



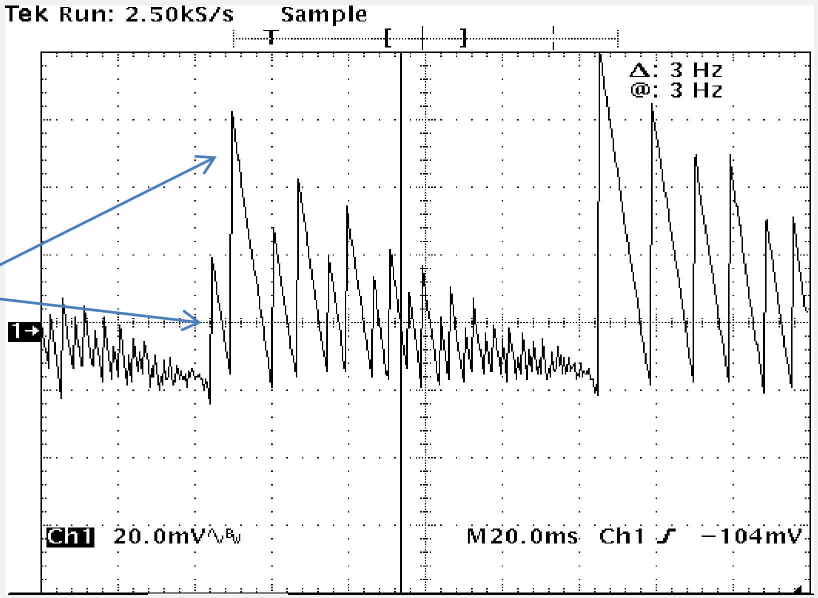
Resulting ripple



INCOMPLETE CHARGING

Bad load balancing (CP with two flying capacitors)

Unbalanced capacitor charge

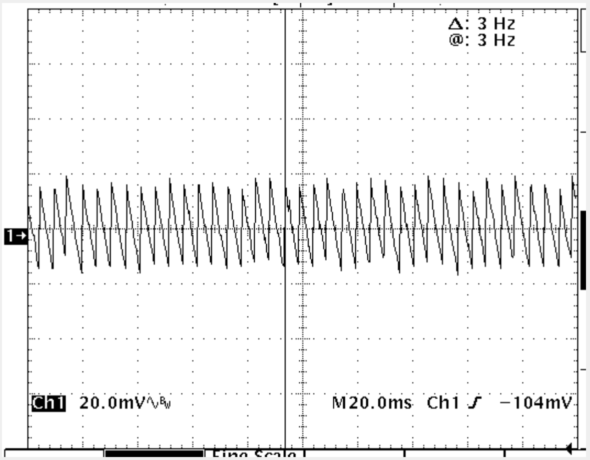


Simple solution: use complete charging on the flying capacitors and limit the discharge current for partial discharges

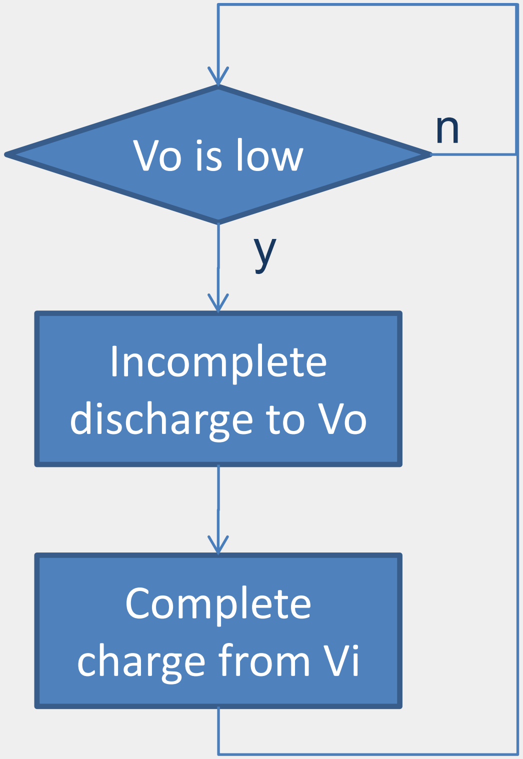
INCOMPLETE CHARGING

Improved control with

limited discharge current



Resulting ripple

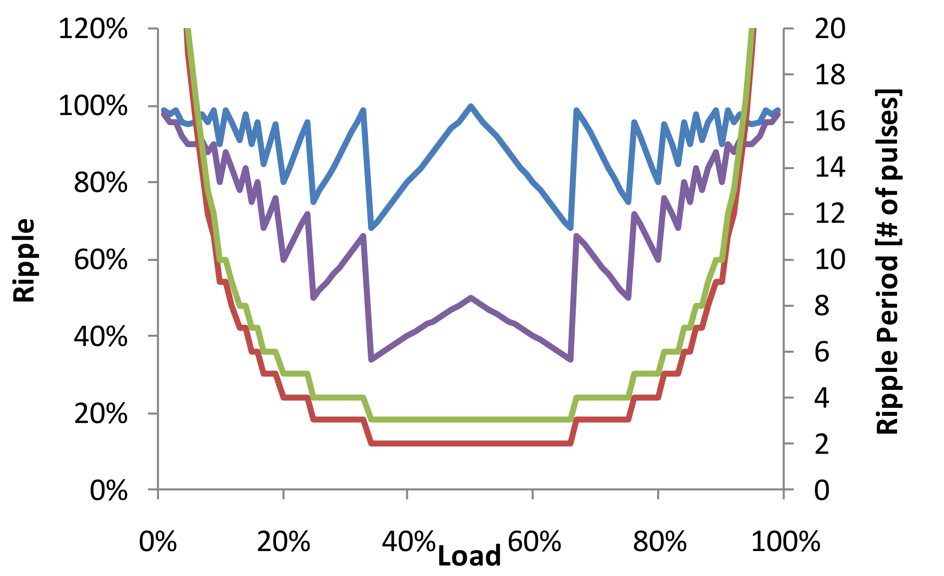


INCOMPLETE CHARGING

Improved control with

limited discharge current

$$V_{ripple} \approx \frac{I_{SW} \cdot T_{ON}}{C_O}$$

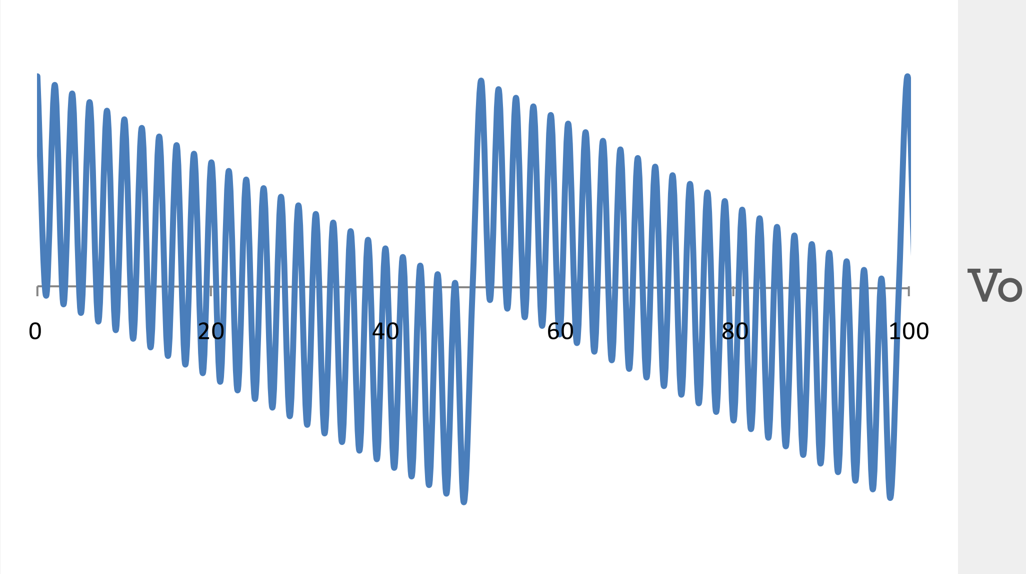


Min period is 2 pulses (1 charge pulse + 1 discharge pulses)

Plus the effects of Limit Cycle Oscillations

INCOMPLETE CHARGING

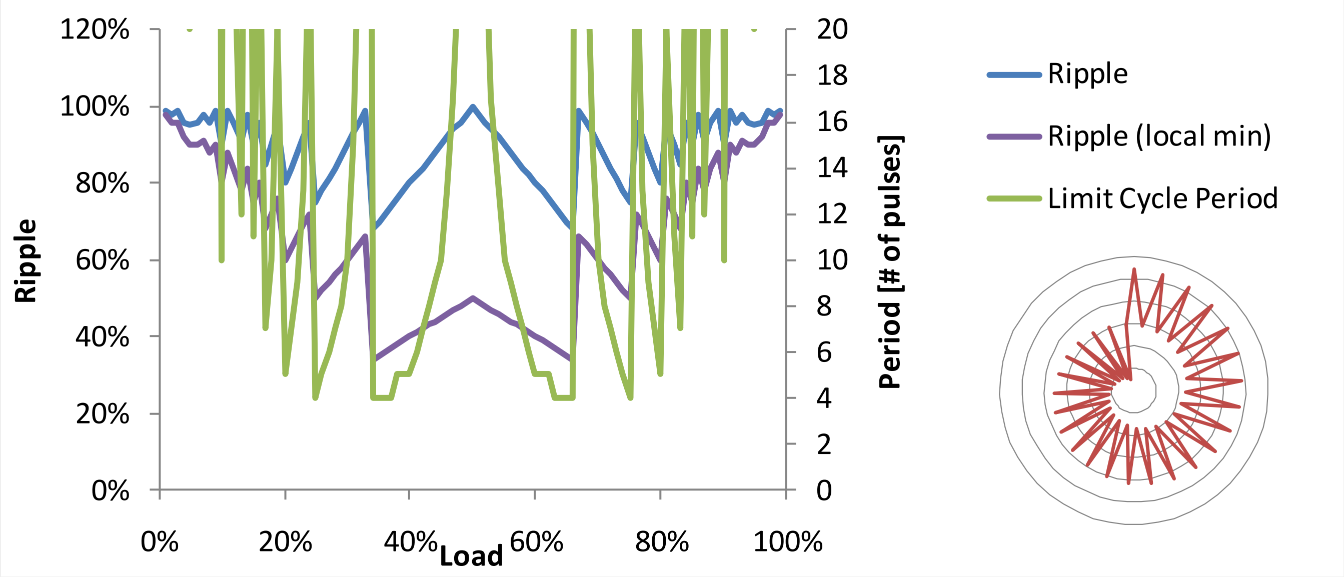
Limit Cycle Oscillations



Same as for any other pulse skipping control…

INCOMPLETE CHARGING

Limit Cycle Oscillations

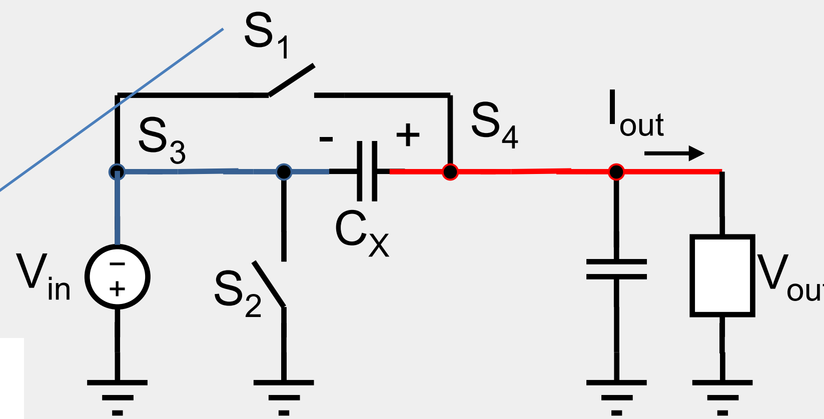


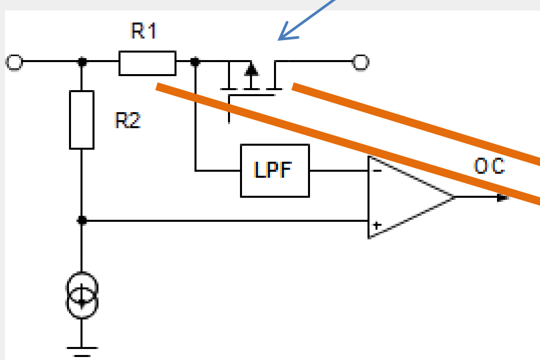
HIGH INRUSH CURRENT

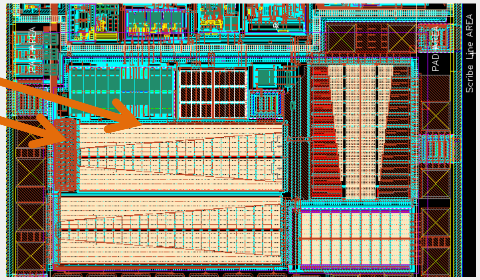
Current limited switches

or

Over current comparator







LARGE VI RANGE

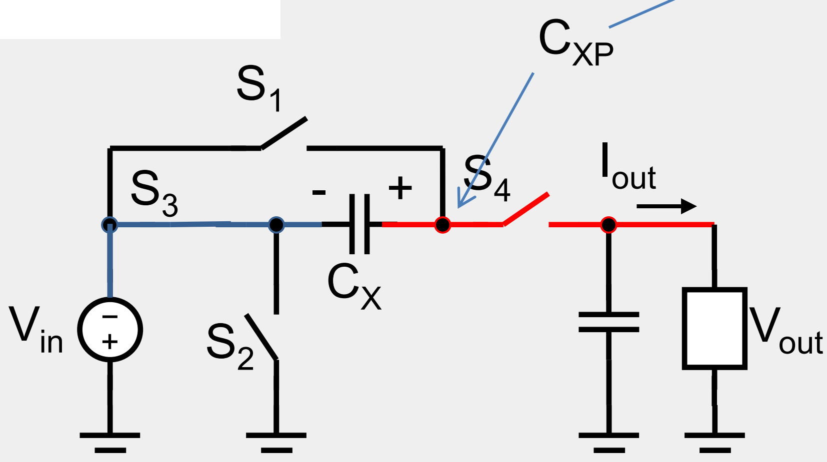
Multimode auto switching

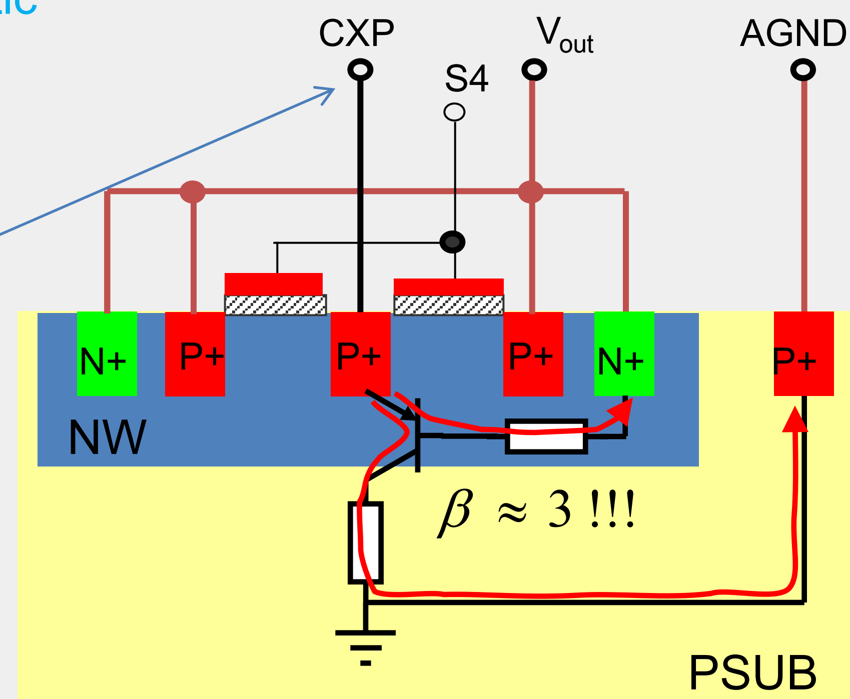
Lots of modes and conditions but simple digital implementation

														Next State			
													Table1	if		else	
Mode	Cx1	Cx2	State	S1	S2	S3	S4	S5	S6	S7	S8	S9	S1..9	!cp	cp	!cp	cp
	CH	OFF	0	1	0	0	1	0	1	0	0	1	100101001	1	0	1	0
	OFF	OFF	1	0	1	0	0	0	1	0	0	0	010001000	2	0	11	8
	OFF	OFF	2	0	1	0	0	0	1	0	0	0	010001000	2	0	3	0
1	OFF	OFF	3	0	1	0	0	0	1	0	0	0	010001000	3	0	3	8
	DIS	OFF	4	0	0	0	1	1	0	0	0	1	000110001	5	6	5	6
	OFF	DIS	5	0	1	0	0	0	1	0	1	0	010001010	5	6	5	6
	DIS	OFF	6	0	0	0	1	1	0	0	0	1	000110001	7	16	7	16
	OFF	DIS	7	0	1	0	0	0	1	0	1	0	010001010	7	6	7	6
	CH	CH	8	1	0	1	0	1	0	1	0	0	101010100	11	9	11	0
	DIS	DIS	9	0	0	0	1	0	1	0	0	1	000101001	11	8	11	0
	OFF	OFF	10	0	1	0	0	0	1	0	0	0	010001000	11	9	11	9
	OFF	OFF	11	0	1	0	0	0	1	0	0	0	010001000	18	9	18	9
	CH	OFF	12	1	0	1	0	0	0	0	0	0	101000000	13	15	13	9
	OFF	OFF	13	0	1	0	0	0	1	0	0	0	010001000	13	15	13	12
	OFF	OFF	14	0	1	0	0	0	1	0	0	0	010001000	14	15	14	12
	OFF	CH	15	0	0	0	0	1	0	1	0	0	000010100	18	16	18	9
	DIS	DIS	16	0	0	0	1	0	1	0	0	1	000101001	17	12	17	8
	OFF	OFF	17	0	1	0	0	0	1	0	0	0	010001000	18	16	18	20
	OFF	OFF	18	0	1	0	0	0	1	0	0	0	010001000	18	16	19	16
2	OFF	OFF	19	0	1	0	0	0	1	0	0	0	010001000	19	16	19	20
	CH	OFF	20	1	0	1	0	0	1	0	0	0	101001000	21	22	21	28
	OFF	OFF	21	0	1	0	0	0	1	0	0	0	010001000	21	22	21	22
	OFF	CH	22	0	1	0	0	1	0	1	0	0	010010100	23	20	23	24
	OFF	OFF	23	0	1	0	0	0	1	0	0	0	010001000	23	22	23	22
	CH	DIS	24	1	0	1	0	0	1	0	1	0	101001010	26	28	26	4
	DIS	OFF	25	0	1	0	1	0	1	0	0	0	010101000	26	28	39	28
	OFF	OFF	26	0	1	0	0	0	1	0	0	0	010001000	26	25	27	25
	OFF	OFF	27	0	1	0	0	0	1	0	0	0	010001000	28	25	28	37
	DIS	CH	28	0	1	0	1	1	0	1	0	0	010110100	30	24	30	4
	OFF	DIS	29	0	1	0	0	0	1	0	1	0	010001010	30	24	43	24
	OFF	OFF	30	0	1	0	0	0	1	0	0	0	010001000	30	29	31	31
3	OFF	OFF	31	0	1	0	0	0	1	0	0	0	010001000	31	28	31	41
	CH	CH	32	1	0	0	0	0	0	1	0	1	100000101	34	33	34	24
	DIS	DIS	33	0	1	0	1	0	1	0	1	0	010101010	34	32	34	24
	OFF	OFF	34	0	1	0	0	0	1	0	0	0	010001000	35	32	35	32
	OFF	OFF	35	0	1	0	0	0	1	0	0	0	010001000	35	33	44	38
	CH	CH	36	0	1	0	0	0	1	0	0	0	010001000	39	38	39	33
	DIS	OFF	37	0	1	0	1	0	1	0	0	0	010101000	39	38	39	32
	DIS	OFF	38	0	1	0	1	0	1	0	0	0	010101000	39	41	39	32
	OFF	OFF	39	0	1	0	0	0	1	0	0	0	010001000	39	37	39	37
	OFF	OFF	40	0	1	0	0	0	1	0	0	0	010001000	40	37	40	37
	OFF	DIS	41	0	1	0	0	0	1	0	1	0	010001010	43	42	43	32
	OFF	DIS	42	0	1	0	0	0	1	0	1	0	010001010	43	36	43	32
	OFF	OFF	43	0	1	0	0	0	1	0	0	0	010001000	43	41	43	41
4	OFF	OFF	44	0	1	0	0	0	1	0	0	0	010001000	44	41	44	41

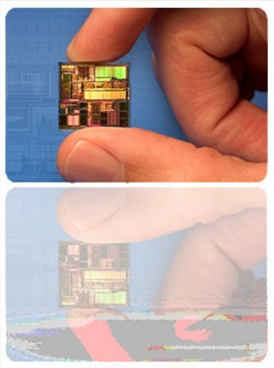
NOISE

Avoid turn on of parasitic diodes

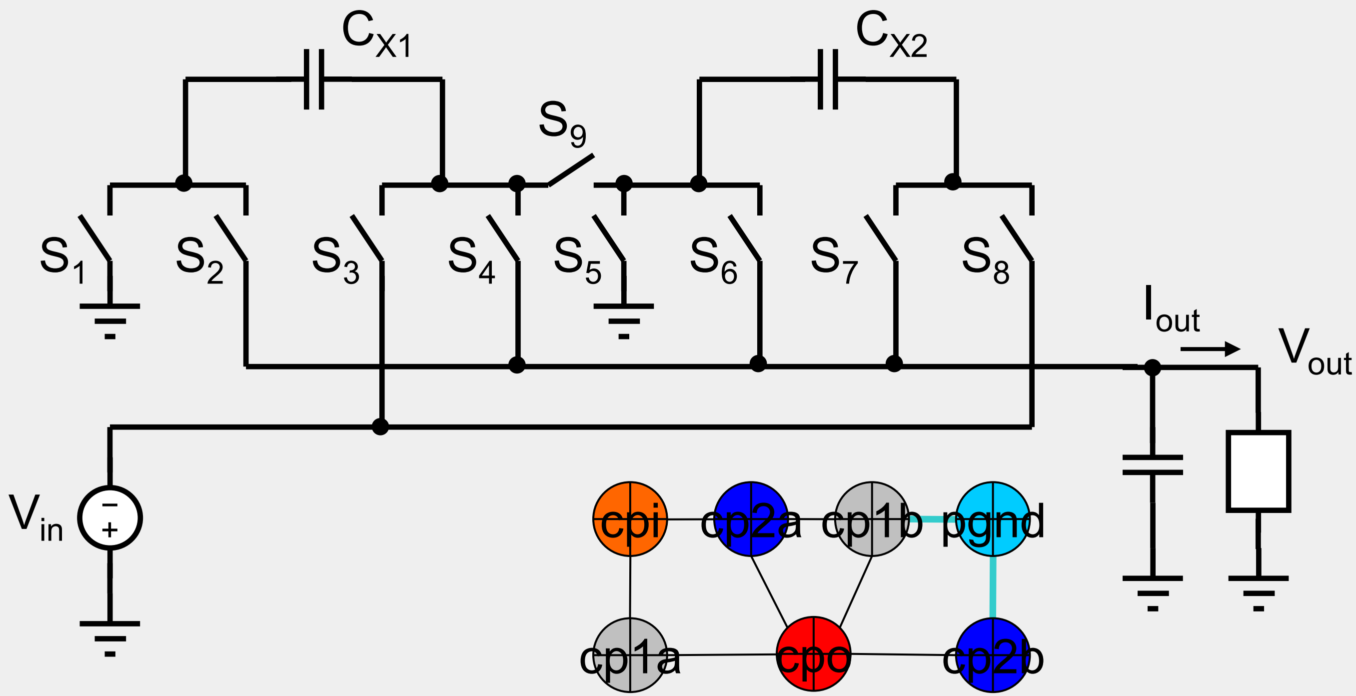




FRAC CP EXAMPLE

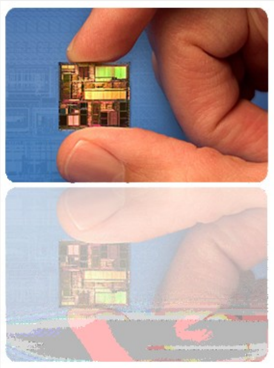


9 sw multimode topology

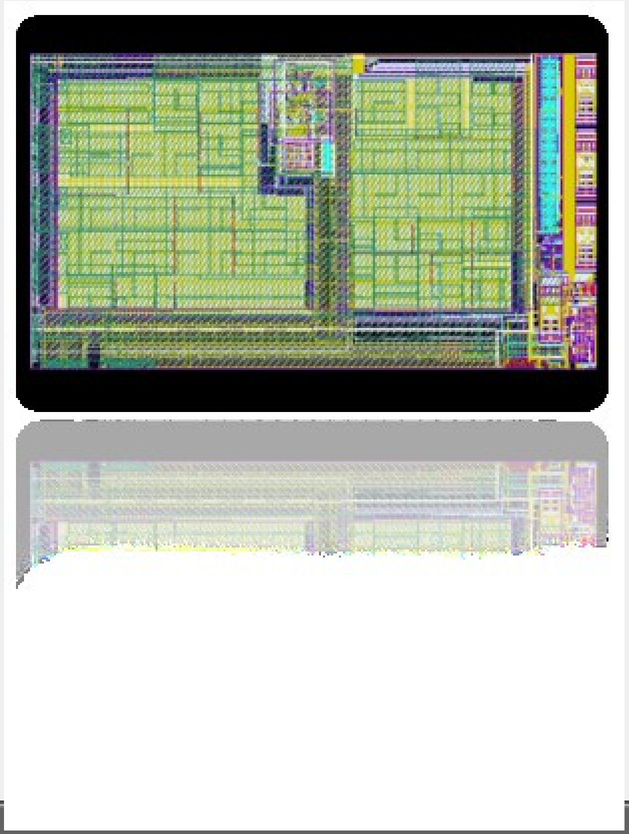


Gains: 1/3; ½; 2/3; 1

FRAC CP EXAMPLE



Layout



Fractionary CP

10 μA consumption

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