

# WG 7-1

## Data density and power efficiency

S. Michelis on behalf of WG7.1.b collaboration:

M. Karagounis, FH-Dortmund, Germany

K. Klein, L. Feld RWTH Aachen, Germany

A. Michalowska-Forsyth, TU Graz, Austria

S. Saggini, UNIUD University of Udine, Italy

F. Arteché, Itainnova, Spain

S. Michelis, G. Ripamonti CERN, Switzerland

M.Lazzaroni and A. Andreazza, UNIMI University of Milan+INFN



# WP 7.1b: power efficiency

Next-generation, large-area, high-granularity particle detectors consume significantly more power at reduced voltages compared to current systems.

This project aims to improve power efficiency of detector systems at reduced material budget.

For this purpose, two powering options will be investigated:

## Parallel Powering (DCDC)

Contribution from:

- CERN
- FH Dortmund
- RWTH Aachen
- TU Graz
- UNIUD
- UNIMI+INFN

## Serial Powering

Contribution from:

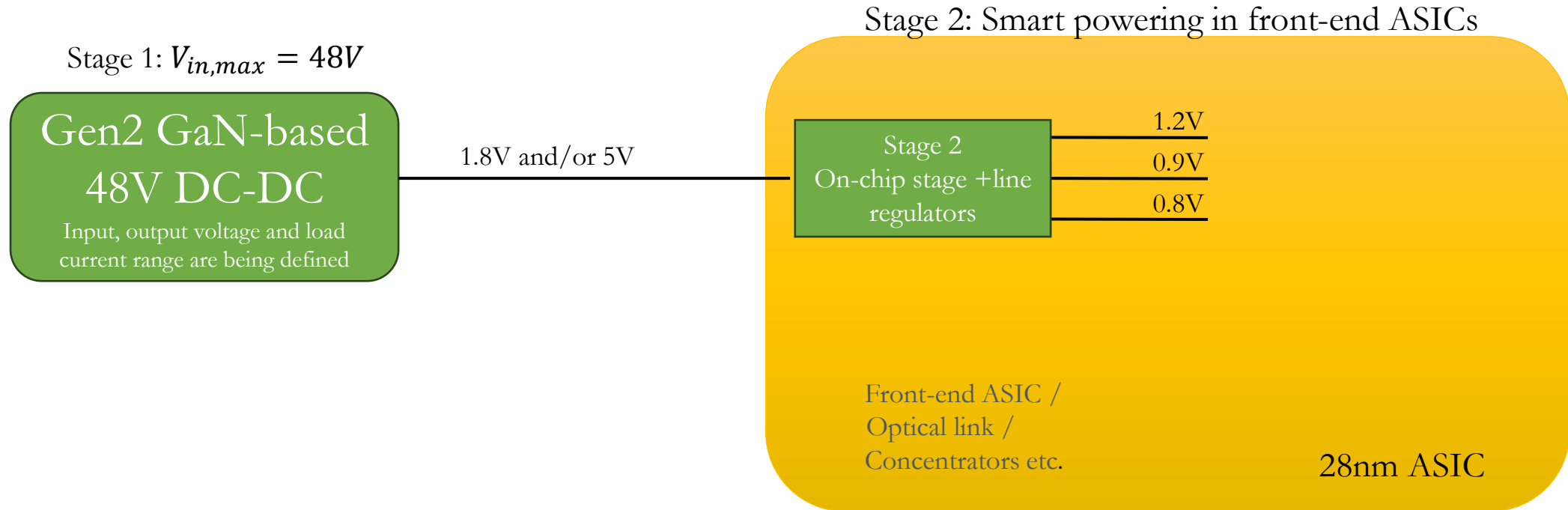
- FH Dortmund
- ITAINNOVA
- UNIMI+INFN

The project is a joint effort of experts in power electronics, IC and PCB design, thermal management, EMC, reliability and particle detector systems.

# Available and requested funds

	Granted Funds		Requested funds	
Institute	FTE / Monetary funds	Funds granted by	FTE / Monetary funds	note
CERN	2.5 / 270kCHF (over 5 years)	Granted by CERN EP-RD WP2 and EP-RD WP5.4		
FH Dortmund	1.33 / 110 kCHF (over 3 years)	BMBF as part of two projects (05H21PRCA9 & 05H21PRRD1)	1	Submitted to transnational funding agencies.
ITAINNOVA	1.5 / 100 kCHF (over 3 years)	GanCAP4CMS, PC Fisica-MMR and AIDAinnova		
RWTH Aachen	0.4		0.67 / 35 kCHF	Submitted to the BMBF on June 30th 2023
TU Graz	0.33		1 / 50 kCHF	Submitted the Austrian Science Fund FWF
UNIUD	0.7		1	Request will be done to INFN if DRD approved
INFN and UNIMI	0.5		0.5	Request will be done to INFN if DRD approved

# WP 7.1b: parallel power (DCDC)

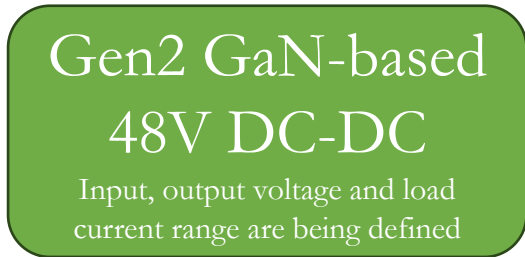


Stage 1 based on HV CMOS technology and GaN power stage

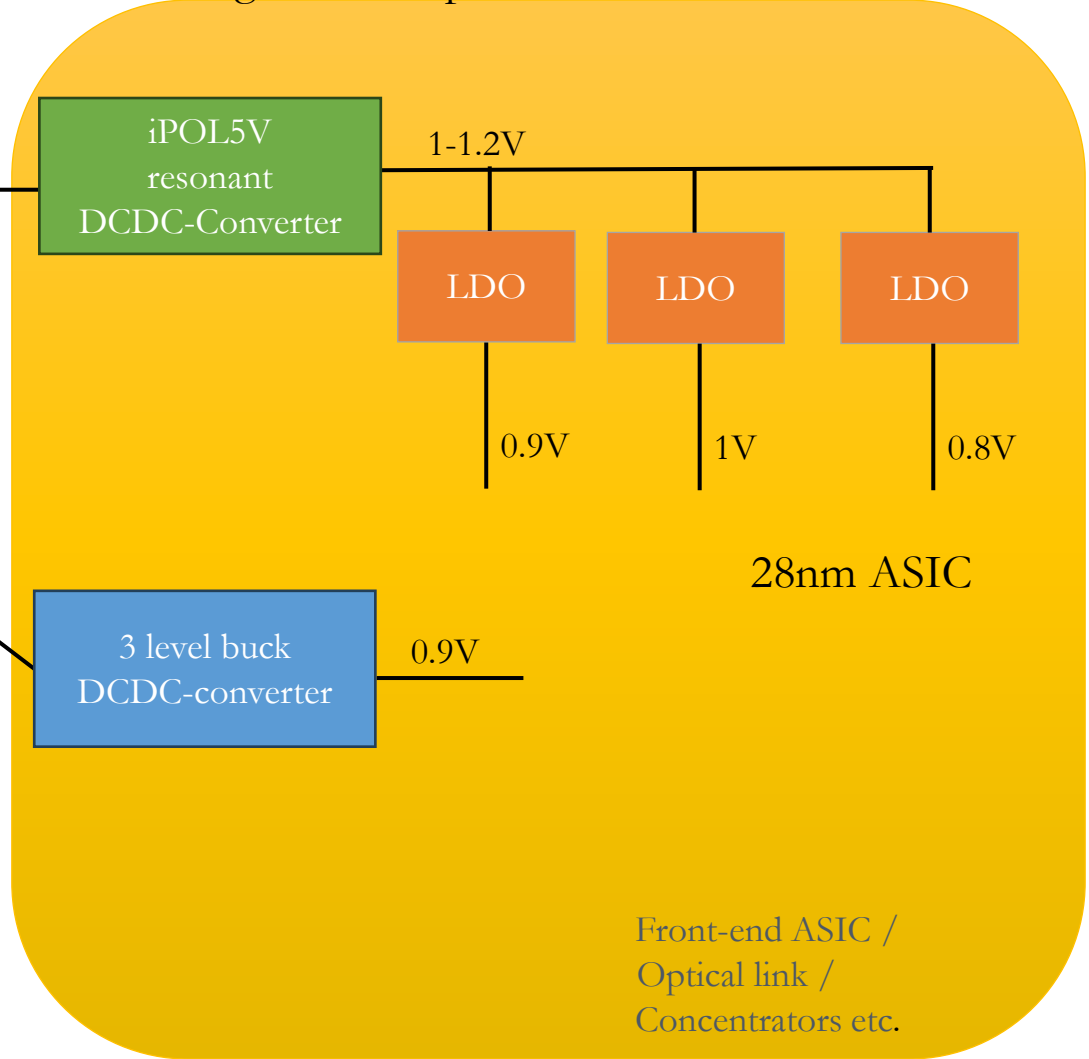
Stage 2 is a fully integrated solution with all components inside the 28nm ASIC

# WP 7.1b: parallel power (DCDC)

Stage 1:  $V_{in,max} = 48V$



Stage2: Smart power in front-end ASICs



5V

1.8V

Developed by:



CERN + UNIUD



TU Graz



FH Dortmund

# Stage1: high voltage technologies and 48V DCDC

We need to find suitable technologies (both High Voltage CMOS and GaN) which are available in long term

HV CMOS technology must be found:

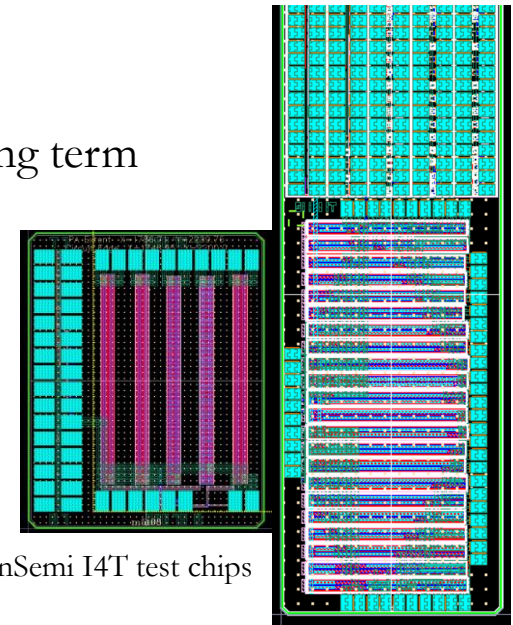
- The radiation characterization of the OnSemi I4T is being finalized. (Test chips designed in 2020).
- As an alternative solution, the ST 0.16 BCD SOI will be tested.
- Future HV technologies must be tested

GaN

- Survey of commercial components (EPC, Infineon, ST, GaN System)
- Test of accessible GaN process for radiation (IMEC GaN technology)

Low mass, high efficiency and high conversion ratio DCDC converter are in development

- Example bPOL48V from 48V to 5V



OnSemi I4T test chips



5cmx2.5cmx3mm 48Vto5V 6A 85% eff

# Stage2 iPOL5V: 5V-input resonant DC-DC converter

iPOL5V is a **fully integrated** resonant DC-DC converter developed in a 28 nm CMOS technology that can be integrated as a Macro Block in more complex ASICs .

R&D has started in Q4, 2021.

The target  $V_{out}$  is 0.9 – 1V, with a tentative maximum current of 500 mA.

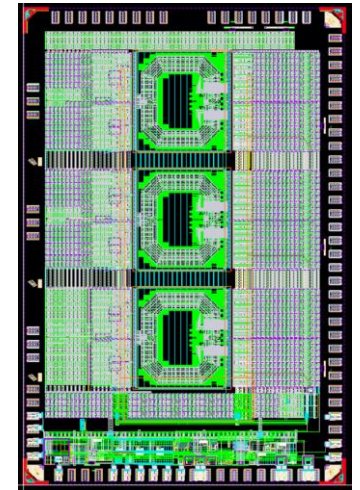
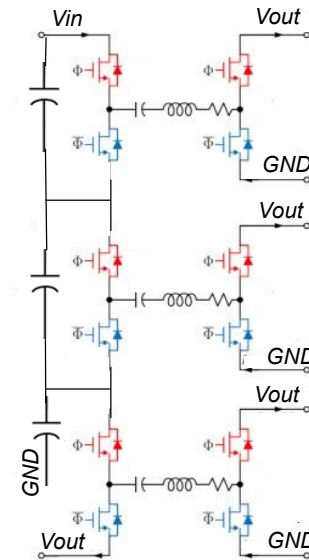
Added value:

- ultimate solution for low mass: no external components
- unprecedented radiation hardness for DC-DC converters: target TID tolerance is 1 Grad
- large reduction of input current (factor  $\approx 4$ )
- a fully integrated solution relaxes the PCB design

Design started, submission of the first prototype in Q4 2023.

A full PicoPix could be powered by parallelizing several iPOL5V cells.

Design done in collaboration with Udine



3.2 x 2.1 mm

# Stage2 : LDO low drop-out linear regulator

A fully integrated linear regulator (capless) is under design in TU Graz with these specifications

Input Voltage  $V_{IN} = 0.9V - 1.2V$

Output Current  $I_L = 150mA$

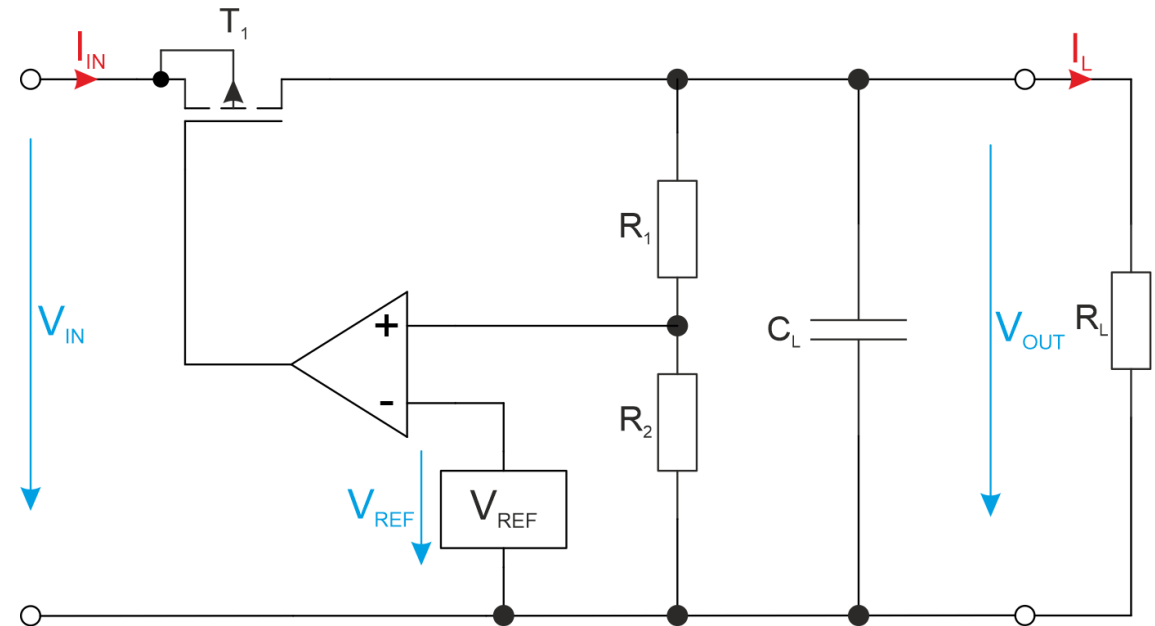
PSRR  $>10dB @ 1Hz < f_{ripple} < 1GHz$

Minimum Drop Voltage  $V_{drop,min} = 50mV$

Max. TID 1 Grad

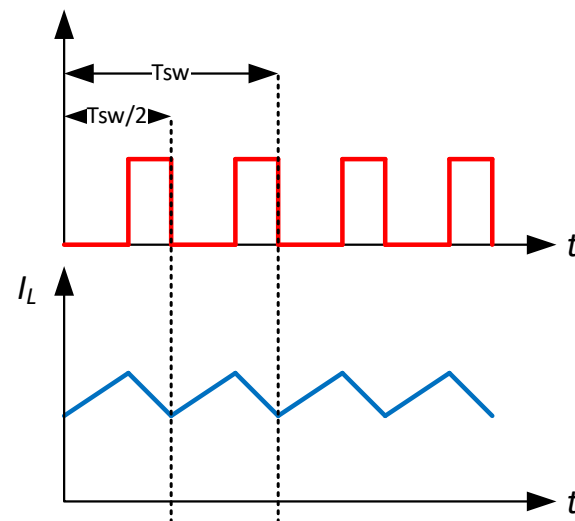
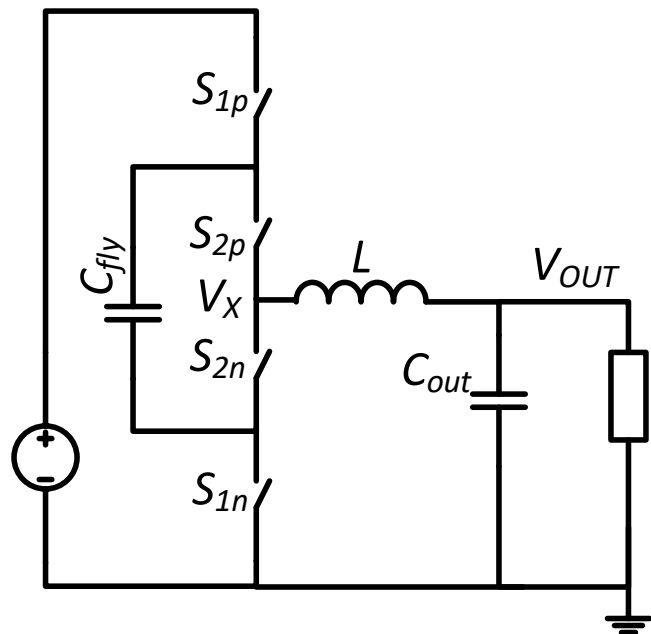
Mainly using core transistors

First prototype Q4 2023





# Stage2 3-Level FCML DC-DC converter



- $C_{fly}$  stores  $V_{in}/2$  (Gate driver necessary)
- For  $D < 0.5$ :  $V_X$  switches between  $V_{in}/2$  and GND)
- For  $D > 0.5$ :  $V_X$  switches between  $V_{in}$  and  $V_{in}/2$
- 4 Switching Phases
- Resonant mode possible

Advantages:

**High power density** because of better utilization of passive components

**Multimode operation** (resonant, quasi resonant, inductive) Enables **soft switching** which reduces switching losses and device stress

**Smaller output voltage ripple** compared to a conventional (2 level) buck converter

Challenges:

**Reliable startup** is necessary to precharge the flying capacitor(s) and ensure that the switches operate within their voltage limits until steady state is reached

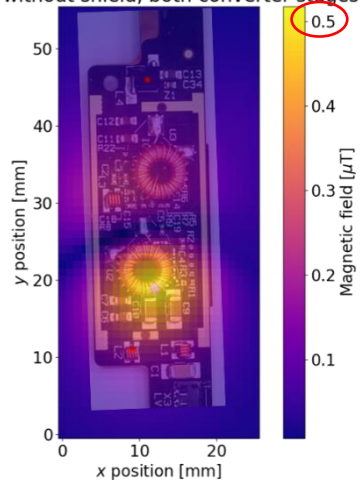
**Voltage imbalance** across flying capacitors due to various disturbances (input impedance, switching delays in driver network) Requires additional circuitry to maintain voltage balance

# Testing of the DCDC converter

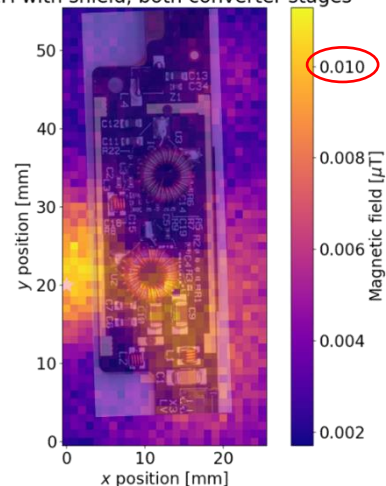
Objective is the characterization of novel DC-DC converters, both standalone and in-system

- Efficiency, line and load regulation (RWTH)
- conducted and radiated noise, thermal aspects, module noise performance (RWTH)
- Radiation testing (TU Graz)
- electromagnetic compatibility testing (immunity - EMI and emissions - EME) at PCB and IC level (TU Graz)
- Reliability and aging testing (TU Graz)

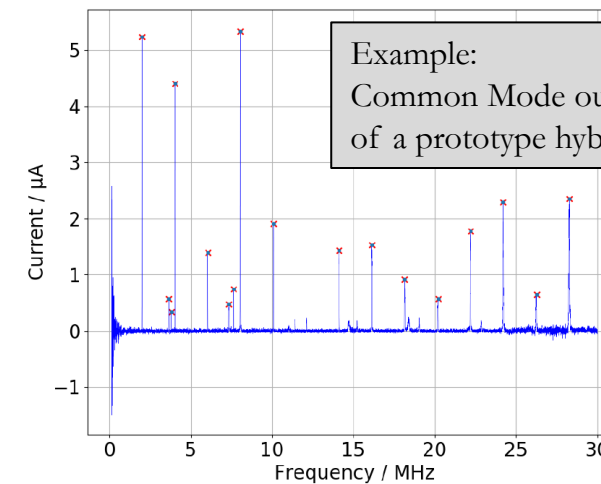
SEH without shield, both converter stages



SEH with shield, both converter stages



Example:  
Radiated noise without (left)  
and with (right) shield –  
reduction by factor 50

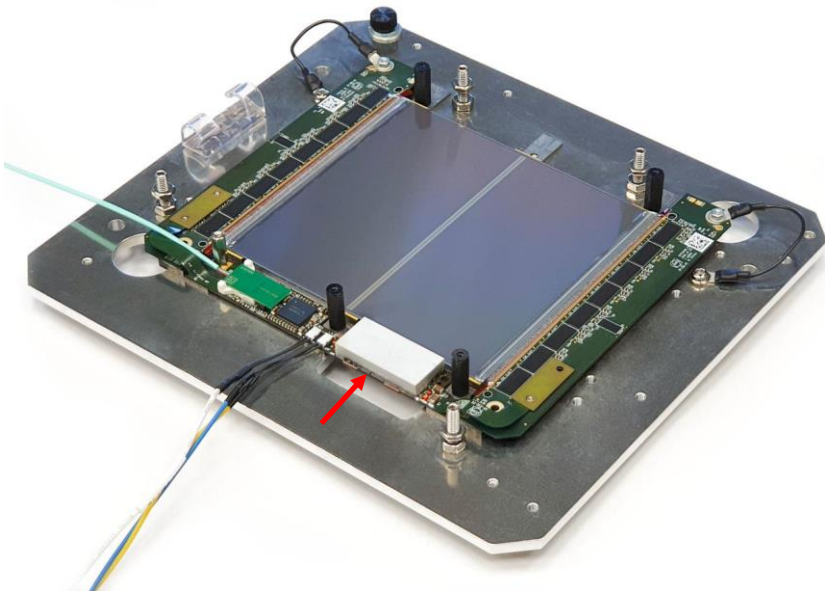


Example:  
Common Mode output noise spectrum  
of a prototype hybrid without shield

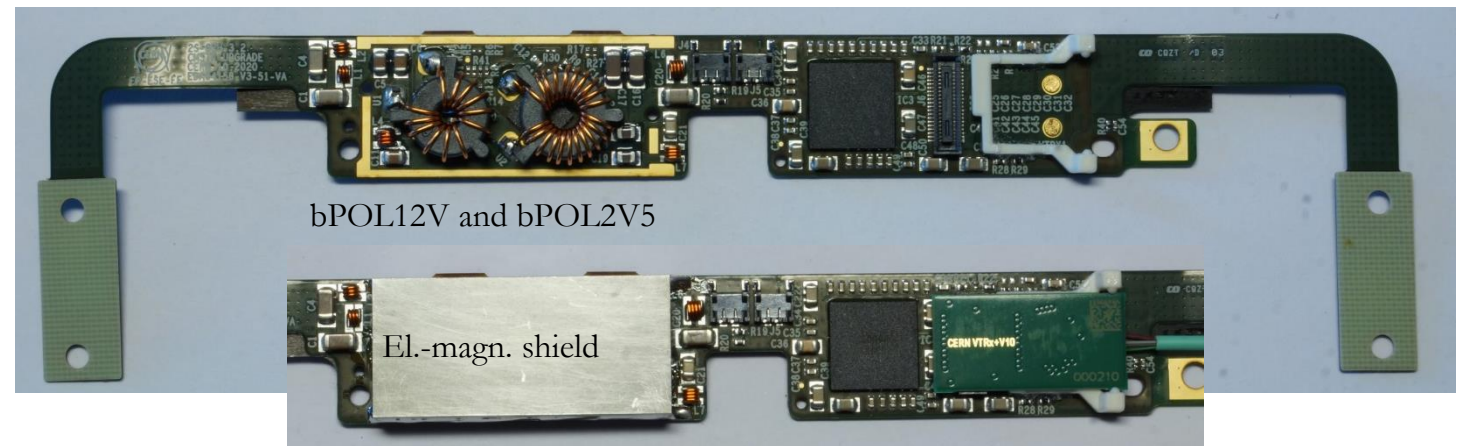
# Plans of RWTH Aachen University

Tentative workplan:

- Using the bPOL48V DC-DC converter:
  - Step 1: Characterization of the CERN bPOL48V board, standalone and with a CMS module (replacing the bPOL12V)
  - Step 2: Development of a small, lightweight optimized board that can be integrated into the CMS module
  - Step 3: Integration of the bPOL48V directly into the CMS tracker hybrids
- Characterization of an on-chip DC-DC converter, designed by Fachhochschule Dortmund

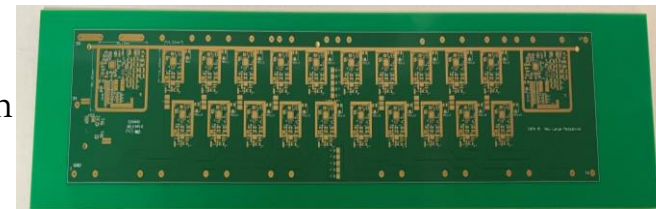
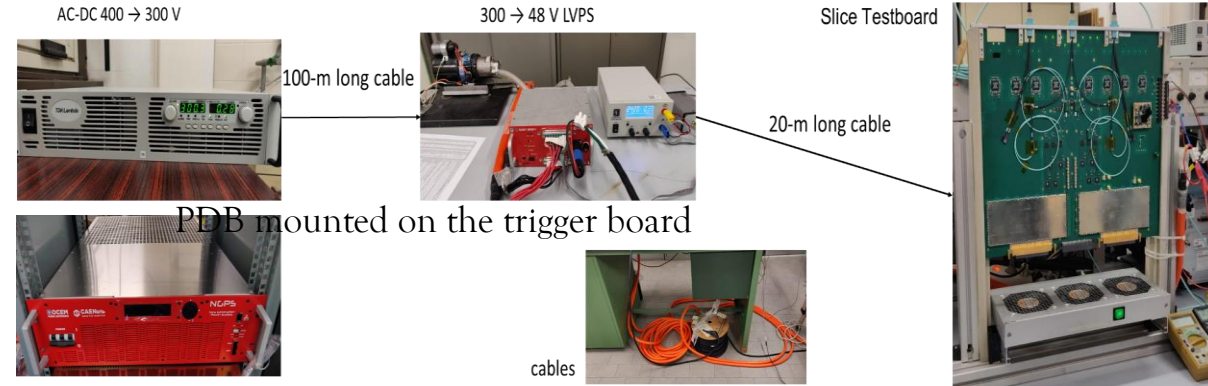


CMS Phase-2 strip module featuring a 2-step DC-DC scheme

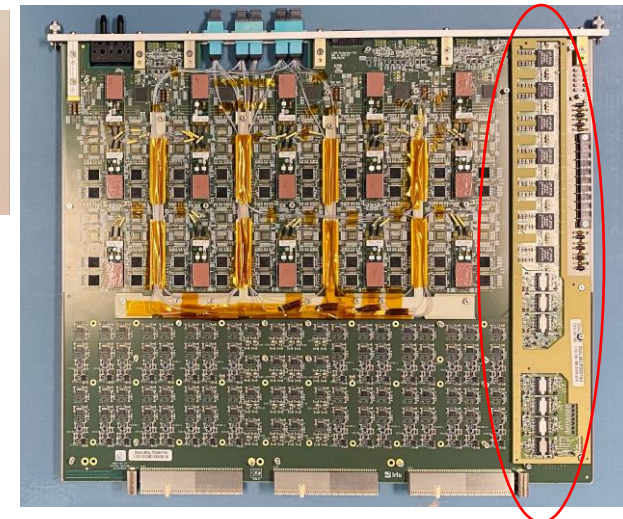


# Plans of UNIMI and INFN Milan

- Activity on Power Distribution Systems from  $\sim 300\text{V}$  to  $24 - 48\text{V}$  with MainConverters
- Final/local DC-DC conversion  $24 - 48\text{V} \rightarrow 1 - 5\text{V}$  with DC-DC and PoL (solutions using CERN devices and commercial devices)
- Issues:
  - Mechanical: Devices integrated on-board or Mezzanine.
  - Reliability (long term operations)
  - ATLAS: Magnetic Field, Radiation, Temperature (Device  $\rightarrow$  Room)
  - Other experiments: cryogenic temperature (LAr and  $\text{N}_2$ ), Room  $\rightarrow$  Device
  - Test
- Interesting results on ATLAS – LAr Calorimeter (see pictures, research and commissioning) and in DUNE experiment (more recently, research)
- Investigation about ASIC devices and Power over Fiber (PoF).
- Interest for different technologies



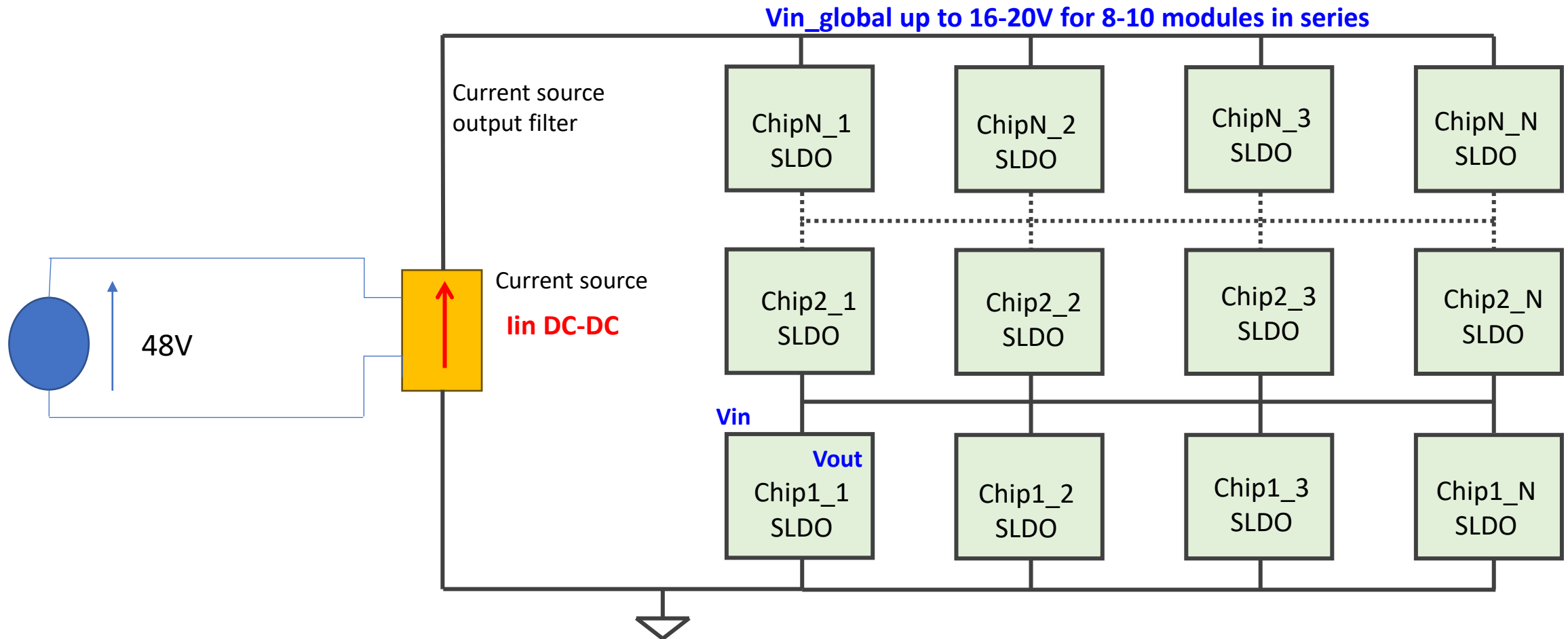
Power supply mezzanine for a board (FEB2 for Lar Calorimeter): on going



Power supply mezzanine for a board (LTDB for Lar Calorimeter): done



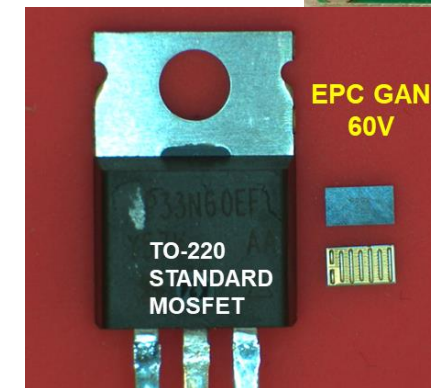
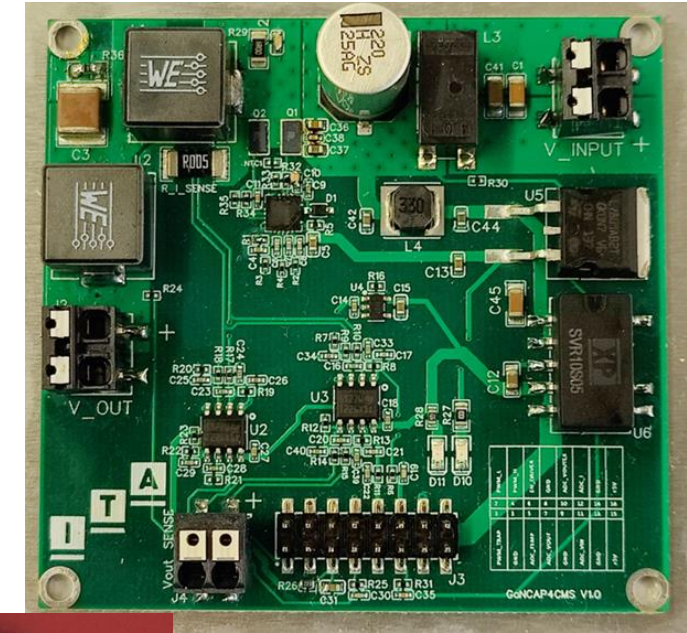
# WP 7.1b: serial power



# GaN based power converter for Serial Powering

The main goal of this task is to assess the feasibility of utilizing GaN-based DC-DC converters (current source) for serial powering applications.

- Several critical issues have been identified to optimized the design of these units
  - Design implications associated to GaN switching
    - High frequency (MHz) and short transition times (ns)
    - Control & deadtimes
  - EMI filter design : Filter embedded in the PCB
  - Magnetic components (air-core/other)
  - Power converter PCB layout
  - Radiation hardness
  - Explore Modular/Multiphase concept



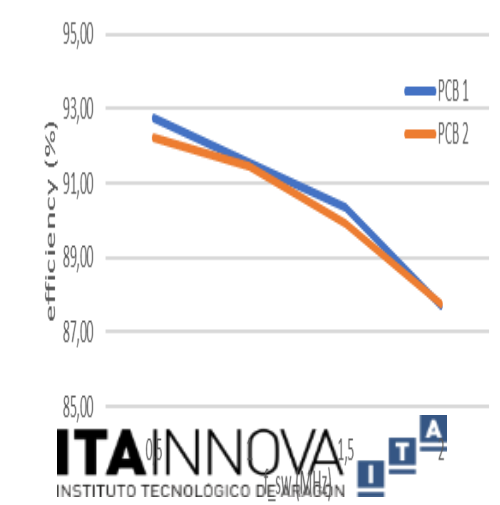
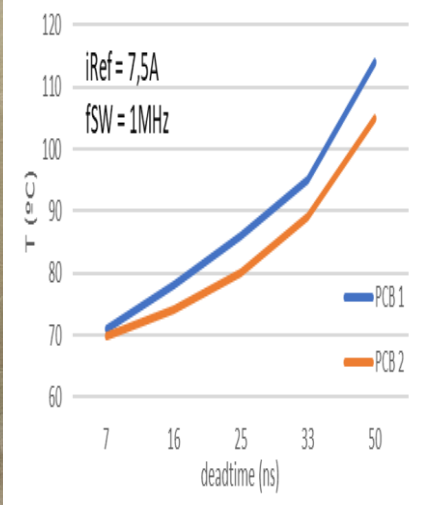
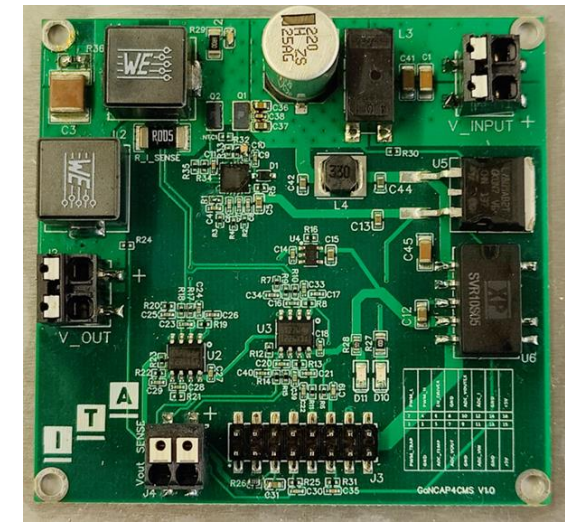
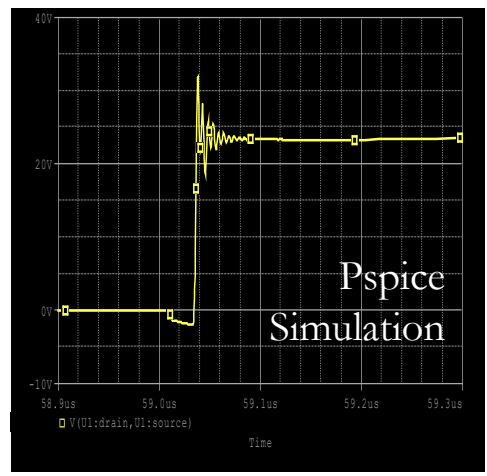
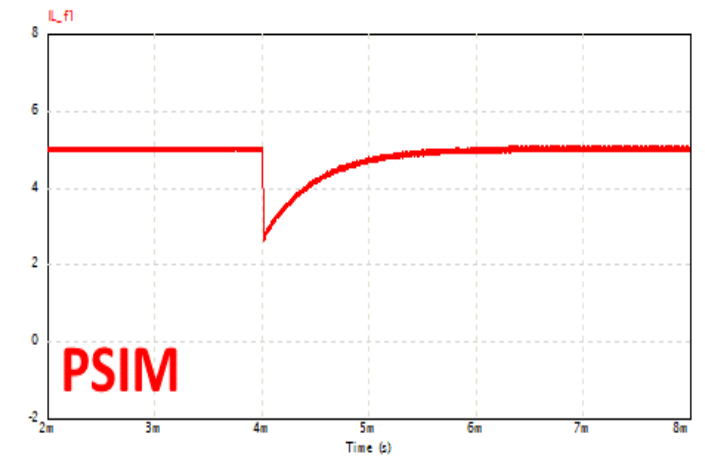
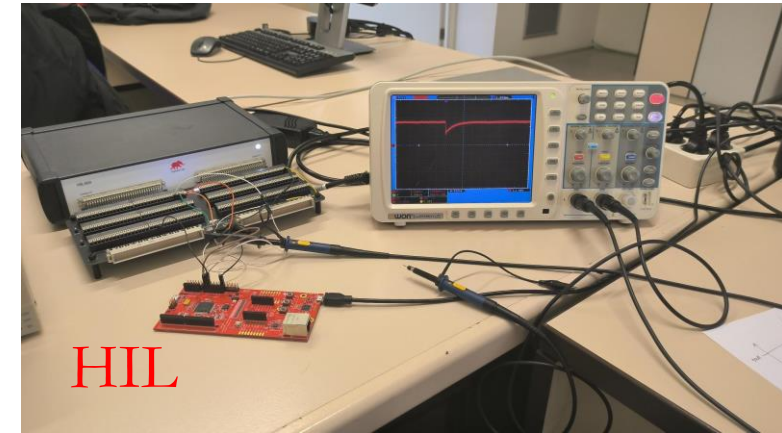
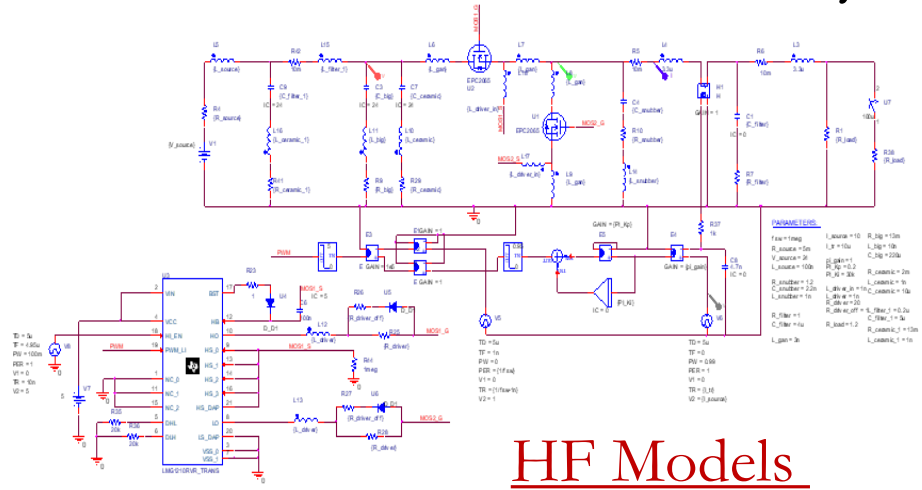
# GaN based power converter for Serial Powering

- In order to analyze some of the critical issues mentioned above, several activities focused on the development of 200W / 2MHz GaN-based DC-DC have been planned
  - Design & Develop a preliminary prototype, which includes (2023):
    - HF simulation models.
    - HIL models to enhance control and protections.
  - Perform a performance evaluation, encompassing efficiency and EMI testing (2024)
    - This evaluation will also involve combined EMI testing in radiation environments.
  - Design printed circuit boards (PCBs) that incorporate embedded filters and magnetic components.
  - Design & develop a new prototype based on a modular concept, incorporating identified improvements.(2025)
- This activities are supported with projects and facilities:
  - GanCAP4CMS: Design and development of a protection system based on GaN based DC-DC and integrated UCAPs for future detectors (Ref: LMP239\_21). (2022-2023).
  - Physics PC: Advanced technologies for the exploration of the universe and its components (2022-2025).
  - AIDAINNOVA -Advancement and Innovation for Detectors at Accelerators (Ref: 101004761). (2021-2025).
  - ITAINNOVA EMC & Power Lab

# GaN based power converter for Serial Powering

Some activities have been already started

HIL Models

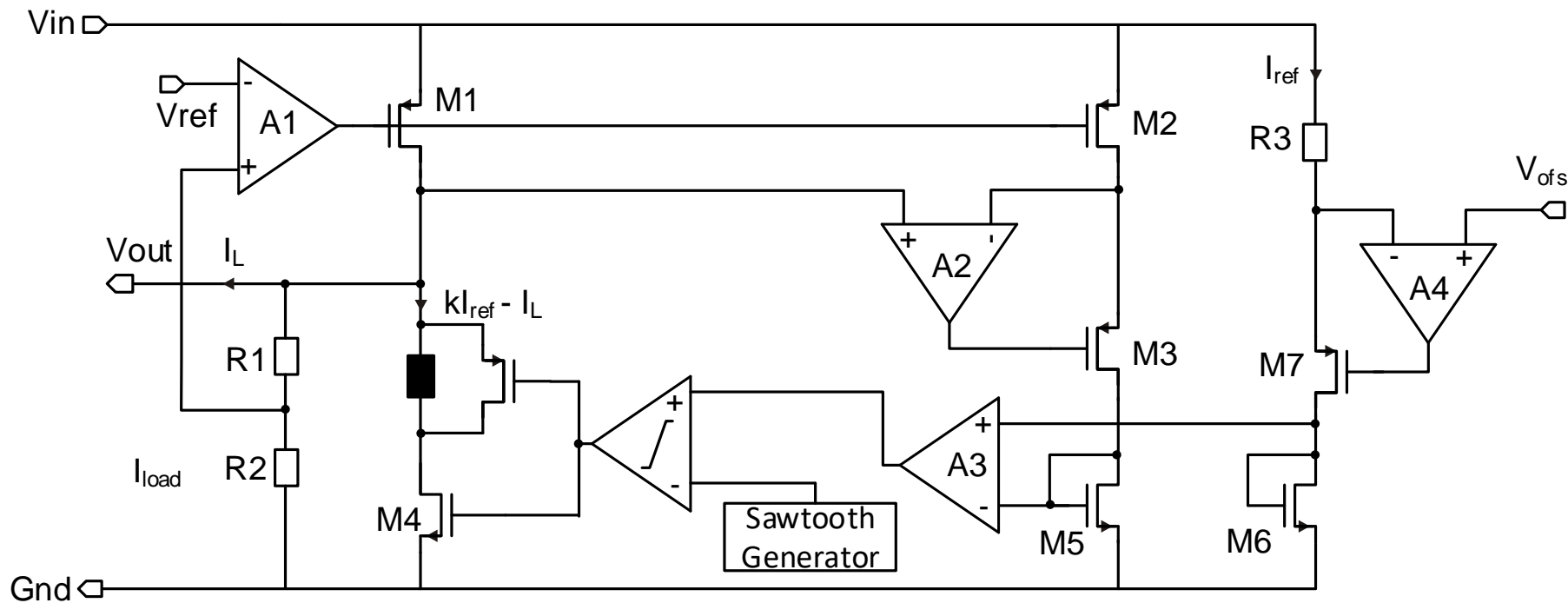


Prototype characterization



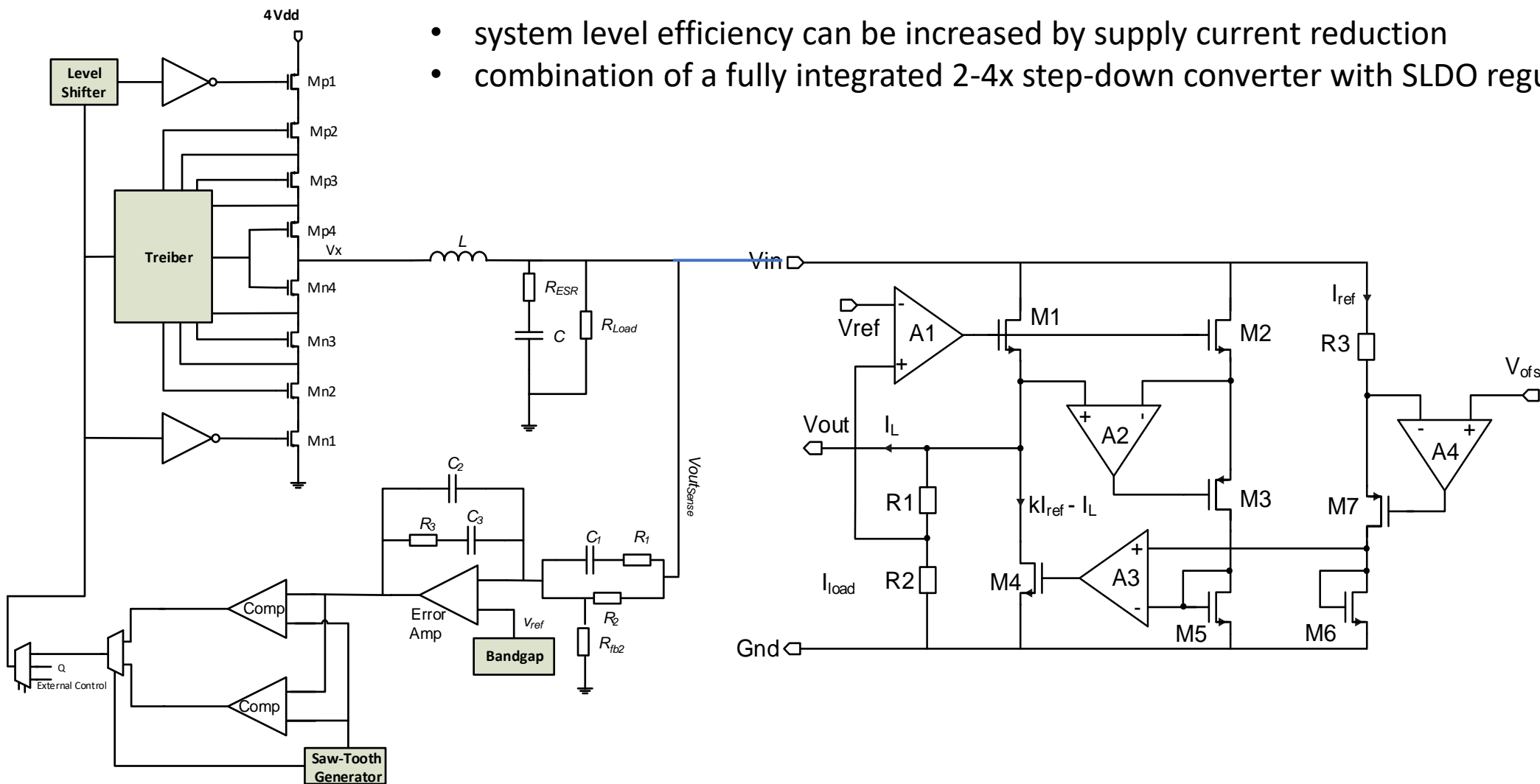
# High-Efficiency Shunt-LDO Regulator

- study of innovative architectures to increase efficiency on system and regulator level
- regulator level efficiency can be increased by switch-mode shunt element
  - Connected either at the output (see diagram) or the input of the regulator



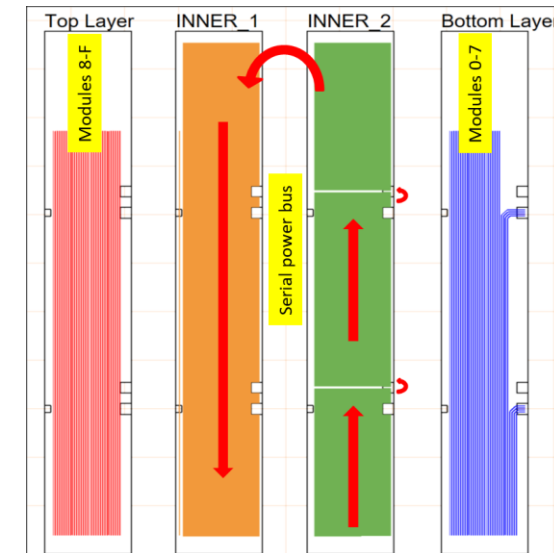
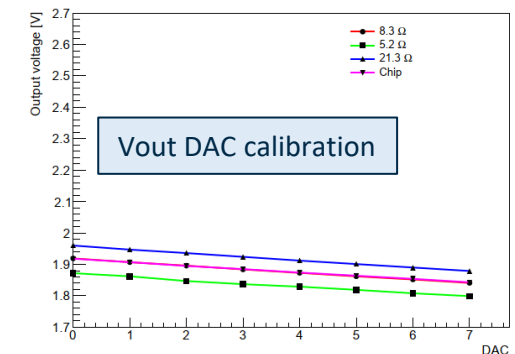
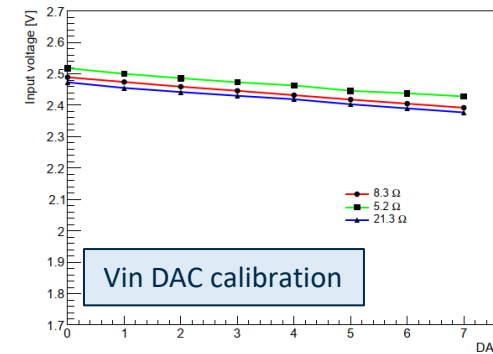
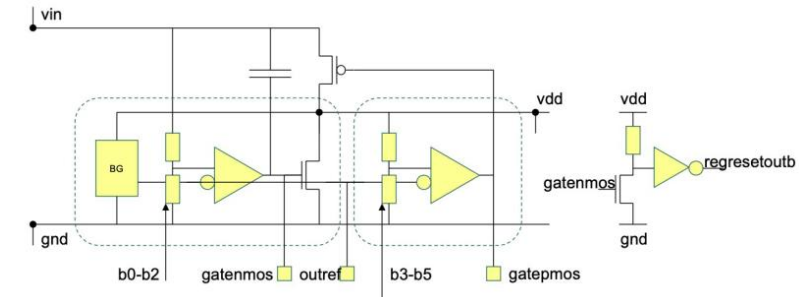
# High-Efficiency Shunt-LDO Regulator

- system level efficiency can be increased by supply current reduction
- combination of a fully integrated 2-4x step-down converter with SLDO regulator



# Serial Powering for FCCee

- Minimize detector material and number of connections for future lepton colliders
- DMAPS may be a suitable options for large area tracker
- Serial powering accessible for HV-CMOS technologies
- Some results on ATLASPIX3 chips with integrated SLDO:
  - no degradation of noise and threshold performance
  - tunable within some tens of mV range
- Planning for multi-module chain with low-mass power buses
- Interest for other technologies like the LF110nm platform (DRD7.6.1)



# Summary

Large community is building up around powering solutions for HEP applications

Investigate both parallel and serial power distribution solution with low mass, radiation hardness and high efficiency specifications

Main building blocks are:

GaN DC-DC Converter and GaN DC-DC Current Source, with use of high voltage CMOS and GaN technology up to 48V  
Resonant Converter, 3-level Buck Converter, Capless-LDO and SLDO designed in 28nm technology, aiming 1Grad

Full characterization of each block:

- Electrical and thermal performances
- Radiation hardness
- EMC and reliability assessment

Funding is granted already for CERN, FH Dortmund, Itainnova

Request for funds are pending or to be done for RWTH Aachen, TU Graz, UNIUD, UNIMI+INFN