Radiation Tolerant RISC-V processor and SoC platform

Implementing DRD7: an R&D Collaboration on Electronics and On-detector Processing.

2nd workshop

25 September 2023

Kostas Kloukinas

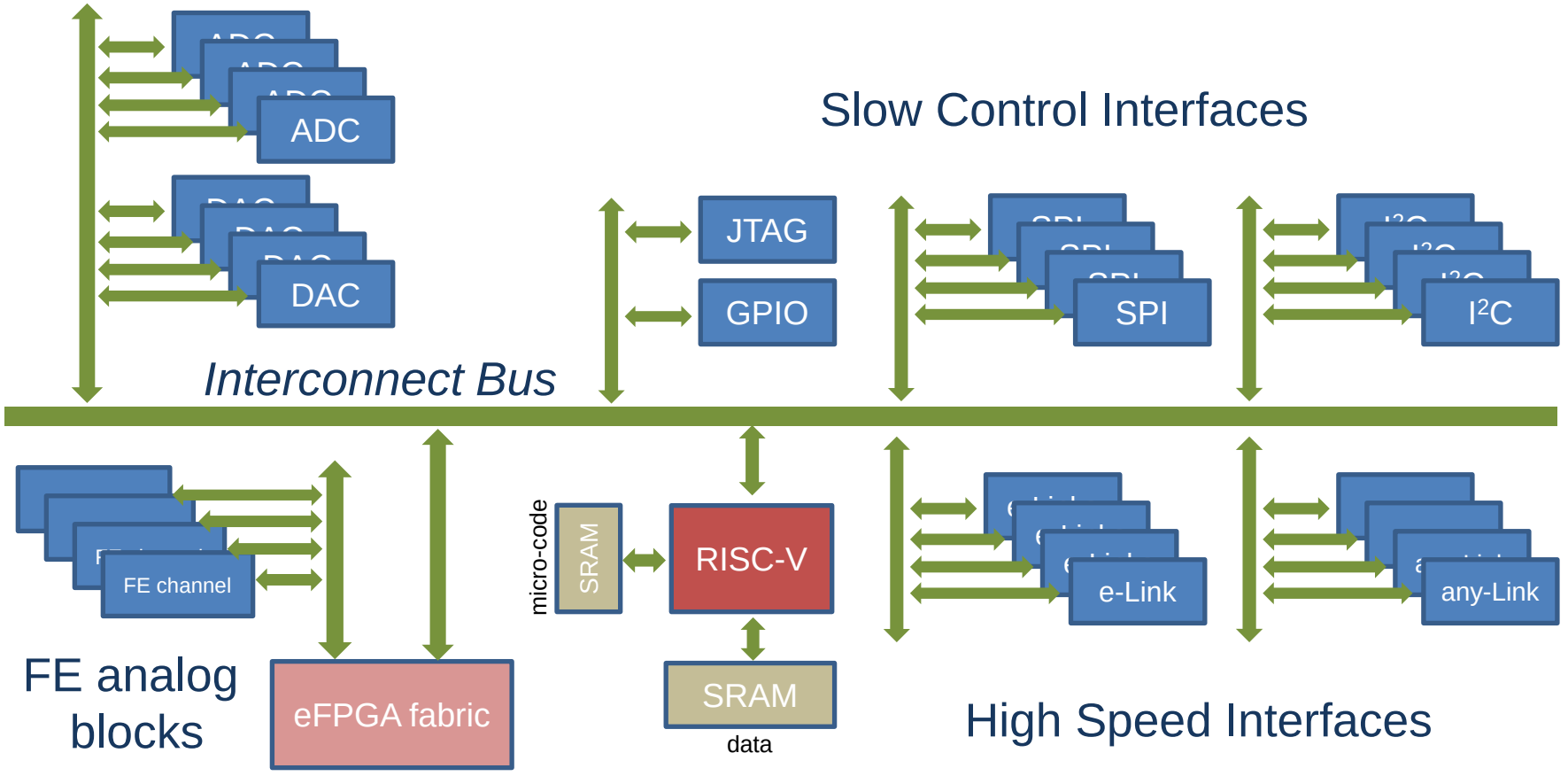
Introduction

- Project intentions
  - Rad-Tol RISC-V based System-on-Chip design
- Participating institues, as of today
  (in order of presentations)
  - CERN
  - KU LEUVEN
  - Fachhochschule Dortmund
  - UK Consortium

- **EP-R&D WP5.2** Rad-Tol SoC Ecosystem activity
  - Motivation
    - Tackle design complexity in future experiments
    - Control development cost on advanced nodes
    - Facilitate on-detector “intelligence”
    - Enable reconfigurable, retargetable FE ASICs
  - Propose a SoC ASIC design methodology
    - Introduce an abstract design methodology
    - Develop reusable IP blocks
    - Standardized interconnects for IP blocks
    - Replace state machines with a control processor (RISC-V based)
    - Programmable, flexible logic blocks (SoC Ecosystem, cores, eFPGA, NoCs)
    - Enhance Hierarchical Digital Implementation and Verifications

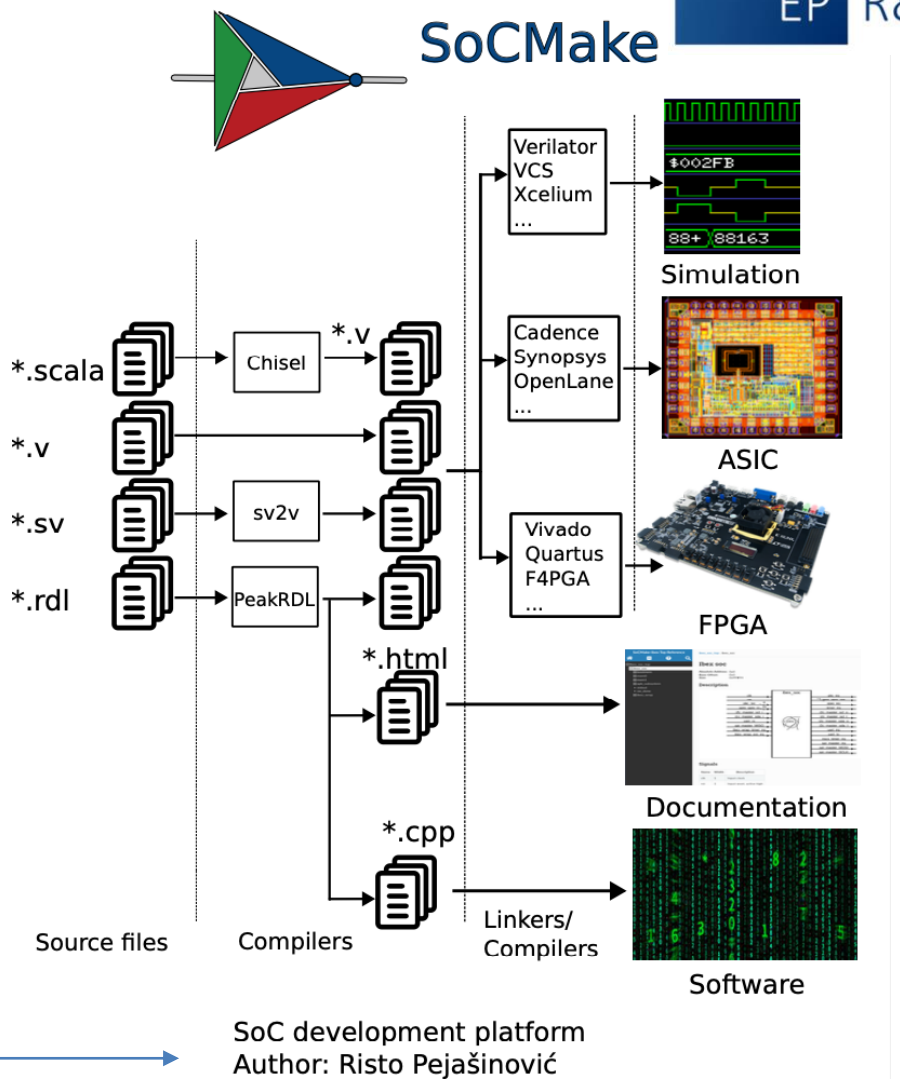
SoC Radiation Tolerant Ecosystem

Conceptual Diagram



SoC Generator Tool

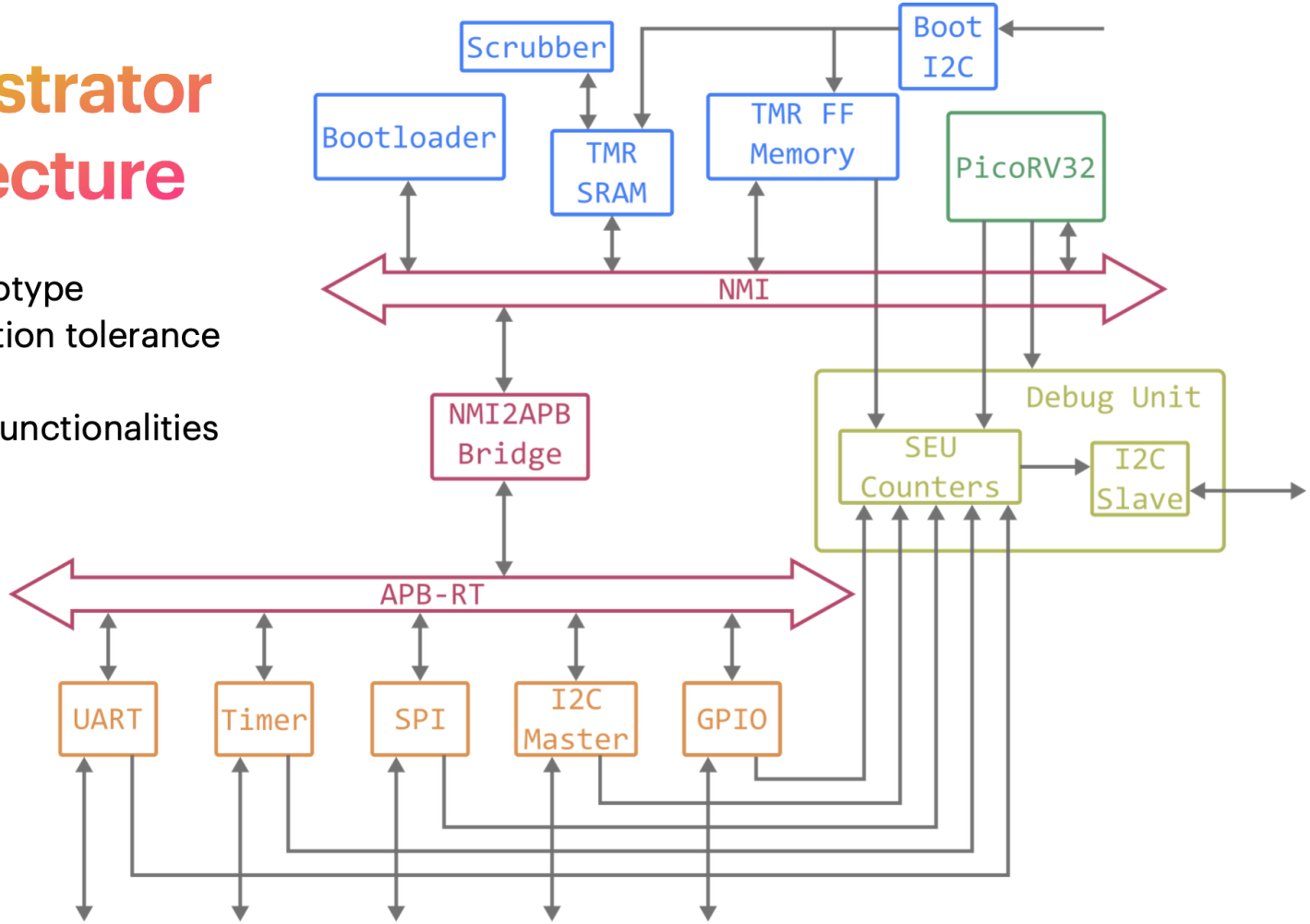
- SoCMake
  - SoC generator tool
  - *SystemRDL* language to automatize the generation of:
    - Hardware design
    - Software toolchain
    - Verification platform
    - Documentation
  - Generate custom SoCs
  - Rapid SoC prototyping
  - Work in progress



Demonstrator ASIC

Demonstrator architecture

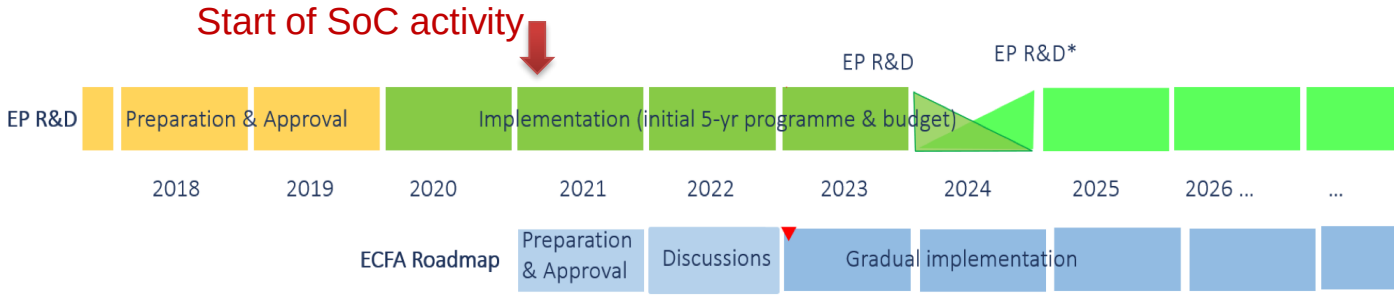
- First ASIC prototype
- Focus on radiation tolerance testability
- Limited set of functionalities



Alessandro Caratelli
Marco Andorno
Anvesh Nookala
Davide Ceresa
Risto Pejasinovitc

Plans & Resources

- Timeline
  - SoC activity started in 2021, during EP R&D phase I
  - Approved to continue in phase II, for *at least* four more years



- Scope
  - Open platform for Rad-Tol SoC ASIC design
  - SoC & core architecture, Verification, Implementation
- Resources
  - 1 fellow, 2 students, 3 part-time staff

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DRD7 Workshop

Radiation Tolerant RISC-V Processors

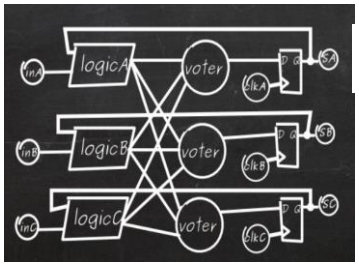
Levi Mariën
Electronic Circuits and Systems (ESAT)
Advanced Integrated Sensing Lab (ADVISE)

Motivation behind our research

- Spatial redundancy techniques
  - TMR, DMR, dual lockstep systems, ...

- Simple to understand
- Reliability failure reduces by orders of magnitude
- Can be automatized

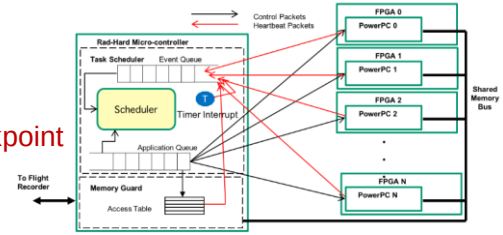
- Large area and power overhead (> 2x/3x)
- difficult to implement (RTL and physical constraints)



- Low area overhead
- Low critical path delay overhead
- Can be fully implemented in software

- Significally complicates the software stack
- Performance loss (lost cycles)
- Memory requirement for checkpoint recovery

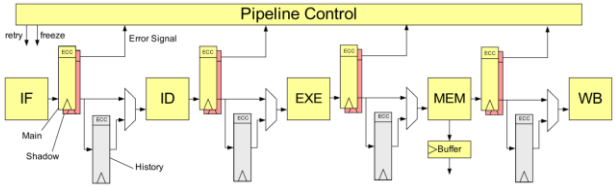
- Radiation hardening by software techniques
  - Instruction replay or checkpoint recovery



- Pipeline rollback
  - Register encoding/decoding
  - Pipeline rollback when non-recoverable error occurs

- Low area overhead
- Can mitigate SETs and SEUs

- Increases critical path delay
- Latency penalty when rollback
- Complex to implement



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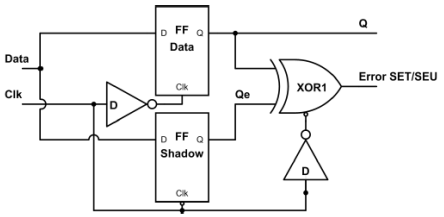
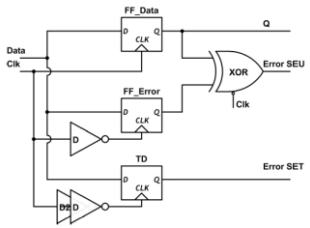
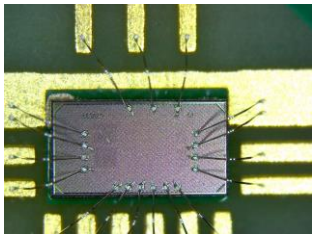
In-situ SEE error detection and correction

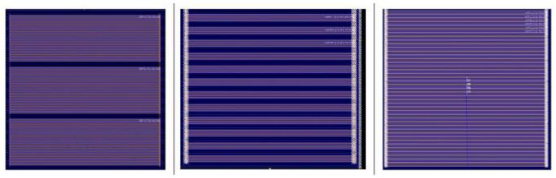
- Single-Event Effect (SEE) error detection
  - Double sampling error detection flip-flop
  - Parallel error detection flip-flop
  - Test chip created
- Single-Event Effect (SEE) error correction
  - Fully configurable

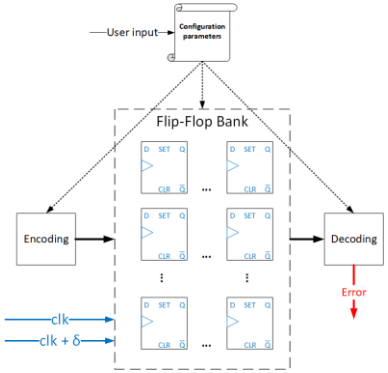






σ (cm^2)	Parallel EDFF	Double Sampling EDFF
σ_{SET}	1.6x10^{-8}	N/A
σ_{SEU}	7.4x10^{-8}	4.6x10^{-8}
σ_{data}	1.3x10^{-8}	1.1x10^{-8}
False Negative	0.12x10^{-8}	0
False Positive	7.9x10^{-8}	3.5x10^{-8}

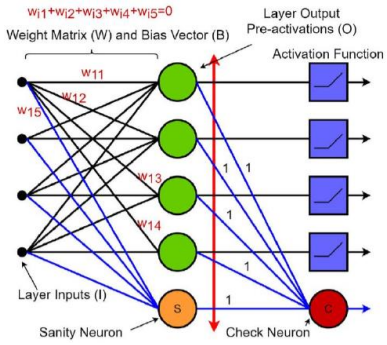


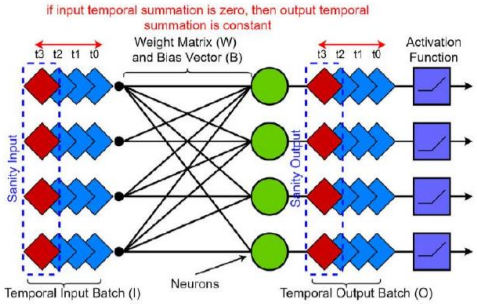


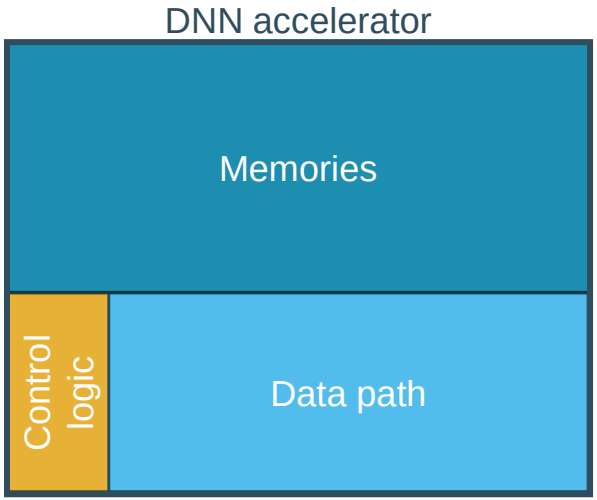
	EDFF 1	EDFF 2	DFF	TMR	Glitch
Static Power (nW)	5.5	3.4	1.4	11.1	5.2
Dynamic Power (fJ)	4.3	4.9	1.6	8.4	5.5
Propagation Delay (ps)	65.5	65.4	62.5	103	568
Area (μm^2)	12.3	8.9	3.1	10.1	10.8

SEE mitigation in DNN accelerators

- Memories: 50-70% area
  - SEC-DED code to harden
- Data path: 30-50% area
  - Software/hardware mitigation
  - Software-based DNN tolerance
  - Hardware checker neurons
- Control logic: 2-5% area
  - TMR

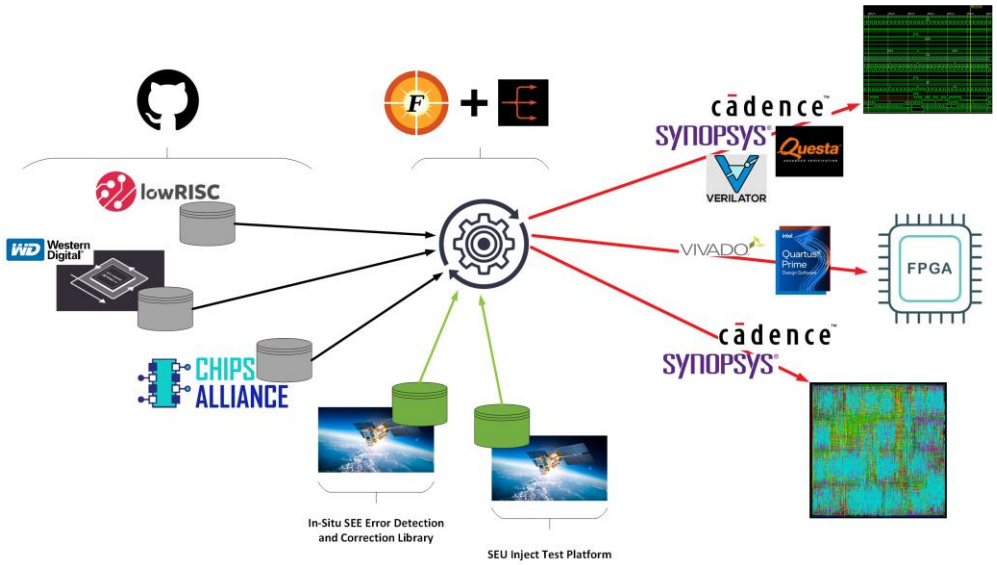


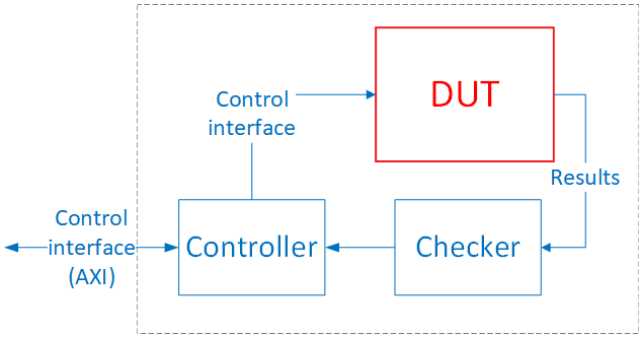




Long term goal

- Any RISC-V core can be targeted
  - Hell, any design for that matter
- Fueled by FuseSoC and Edalize
  - Achieving the power of vendor and tool independence
- In-Situ SEE error detection and correction library
- SEU inject test platform
  - In simulation testing
  - At runtime (FPGA) testing
  - Formal verification?





Contributions and resources

- Contributions
  - Rad-hard RISC-V SoC development on TSMC 28nm HPC+ or 22nm FDSOI technology
- Resources
  - 5 person team for 3 years
    - 3 persons already funded
      - 3 * 3FTE, resources already available
    - 2 persons to be funded
      - 2 * 3 FTE, resources considering asking

Fachhochschule
Dortmund
University of Applied Sciences and Arts

A radhard RISC-V micorocontroller implementation

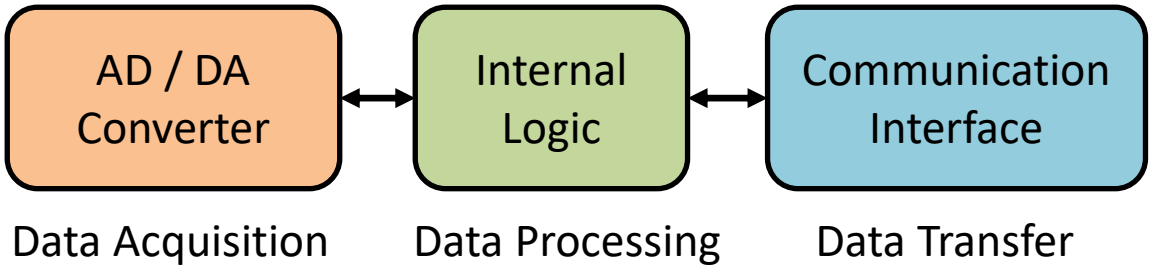
25.09.2023

2nd DRD7 workshop

Michael Karagounis

Motivation

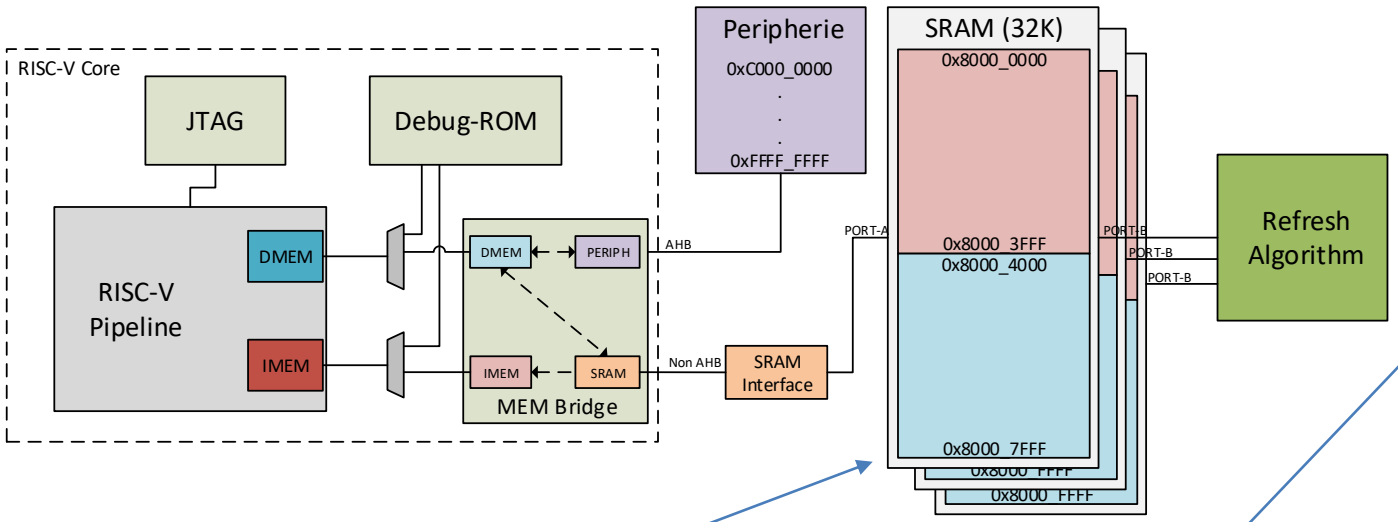
- First thoughts about the usefulness of a radiation-hard µC arose during the development of the MOPS (Monitoring of Pixel) chip
  - MOPS digitizes pixel module voltage and temperature and communicates via CANOpen
  - CANOpen is usually implemented in software but was implemented in hardware for MOPS
- Many custom ASICs have a similar structure:

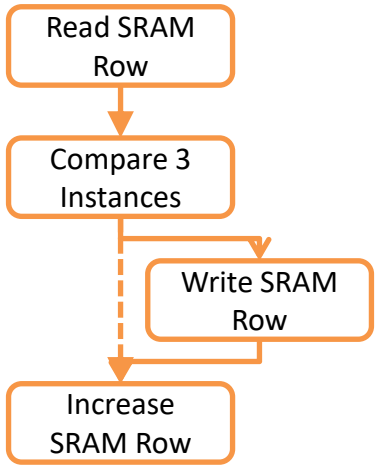


- Design of hardwired custom ASIC is complex and time consuming
  - Big verification effort
  - Bugfixes detected in silicon need redesign and new production cycle
- Adaptation to new projects is difficult
  - hardwired logic needs full redesign
- **Idea**: replace internal data processing logic with radiation-hard RISC-V core
  - Adaptation to new application and bugfixes via software updates

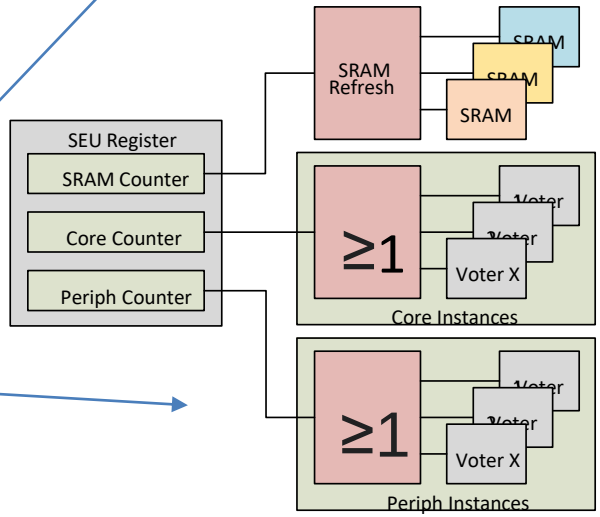
Design of TMR protected RISC-V microcontroller

- Fully TMR protected RV32-IMC Core designed in TSMC 65nm
  - 3 stage pipeline with multiplication and compressed instruction set extension
- 1.2V Core & I/O supply and 50 MHz clock





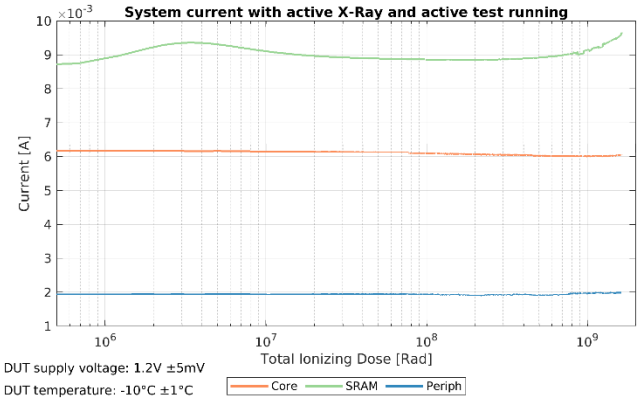
- three SRAM instances protected with scrubbing algorithm

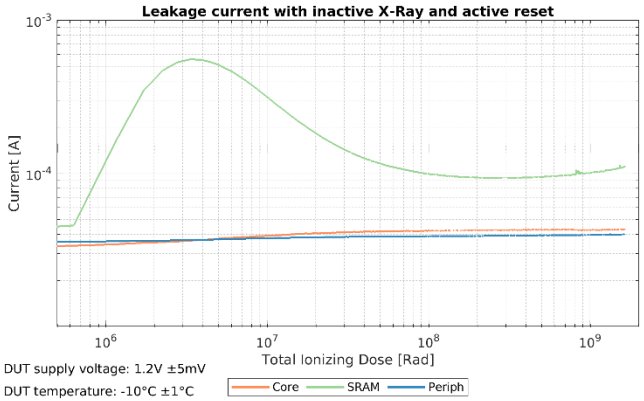


- SEU detection & counting logic

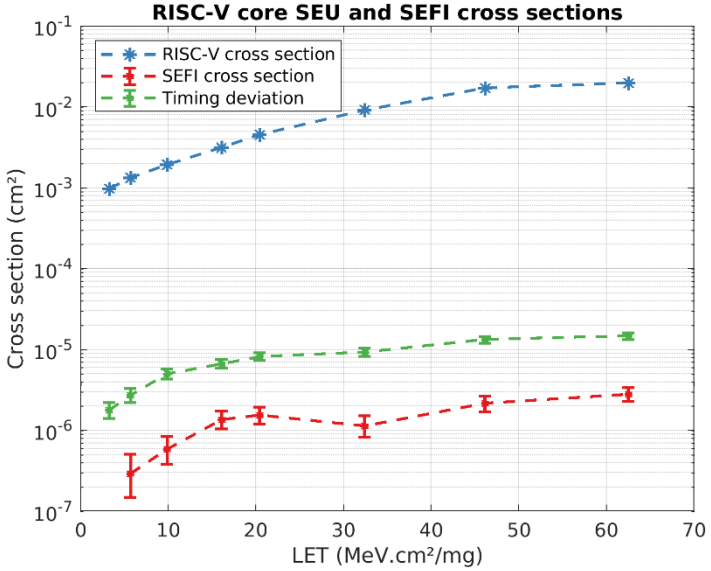
TID & SEE Characterization

- X-ray irrdiation at -20°C
- TID of 1 Grad reached
- SRAM leakage current main driver of increased current consumption





- Heavy ion irradiation for study of SEE



- cross section of corrected SEUs extracted by SEU counter circuit
- SEFI cross section is three orders of magnitude smaller than SEU cross section

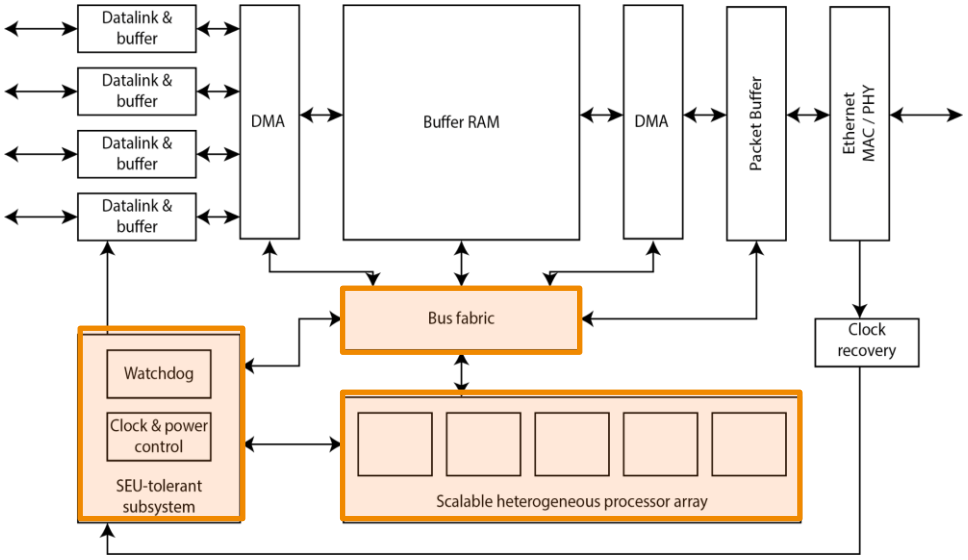
A. Walsemann, M. Karagounis, A. Stanitzki, D. Tutsch, **A radiation hard RISC-V microprocessor for high-energy physics applications,** Nuclear Instruments and Methods in Physics Research Section A, vol. 1056, p. 168633, 2023

Futur Plans & Resources

- Overall project goal is an open-source Zero SEFI microcontroller at LHC inner layer SEE rates
  - Are there additional architecture level protection measures necessary apart from TMR?
- Development of a well-elaborated verification suite
  - Verification of functionality and TMR implementation
  - study of cycle accurate golden models and/or virtual prototypes
- Improve diagnose capability during SEE radiation testing
  - Not only detect SEFIs but also cause of SEFIs
- Resources
  - 0.67 FTE (PhD student) for 1+3 years
  - Funds for Submission of chip prototypes

UK Consortium Contribution

- UK (STFC) Consortia
  - Royal Holloway, Birmingham, Warwick, Bristol, Manchester, RAL.
- Motivation
  - Develop common interface ASIC to couple a range of specialised FE ASICs to a common industry-standard off-detector interface.
- Plans for DRD7.2.b
  - Study/design of processor
  - Verification/testing of cores
  - Evaluate SoC platform
  - Software Ecosystem
- Contribution
  - Q4 2023: requests for funds
  - >1 FTE for 4 years



Proposed common interface ASIC for detector readout, timing, and control

Science and Technology Facilities Council · Royal Holloway University of London · The University of Manchester · Warwick · University of Birmingham · University of Bristol

Towards a Project Proposal

- Develop a Rad-Tol RISC-V based SoC ASIC design platform for HEP experiments
  - Standardized Architectures
  - Implementation Methodologies
  - Verification Methodologies
  - IP block Repository
  - Propose standardized solutions to the HEP community
- Establish regular meetings
  - Kick-off meeting in late October 2023
  - Identify areas of expertise
  - Define fields of contribution
- Finalize Project Proposal


Thank You