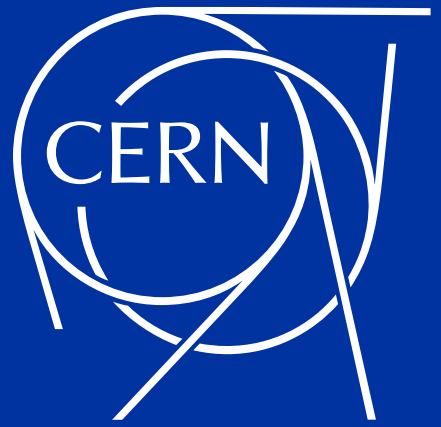


PixESL:
A virtual Electronic System Level prototyping framework

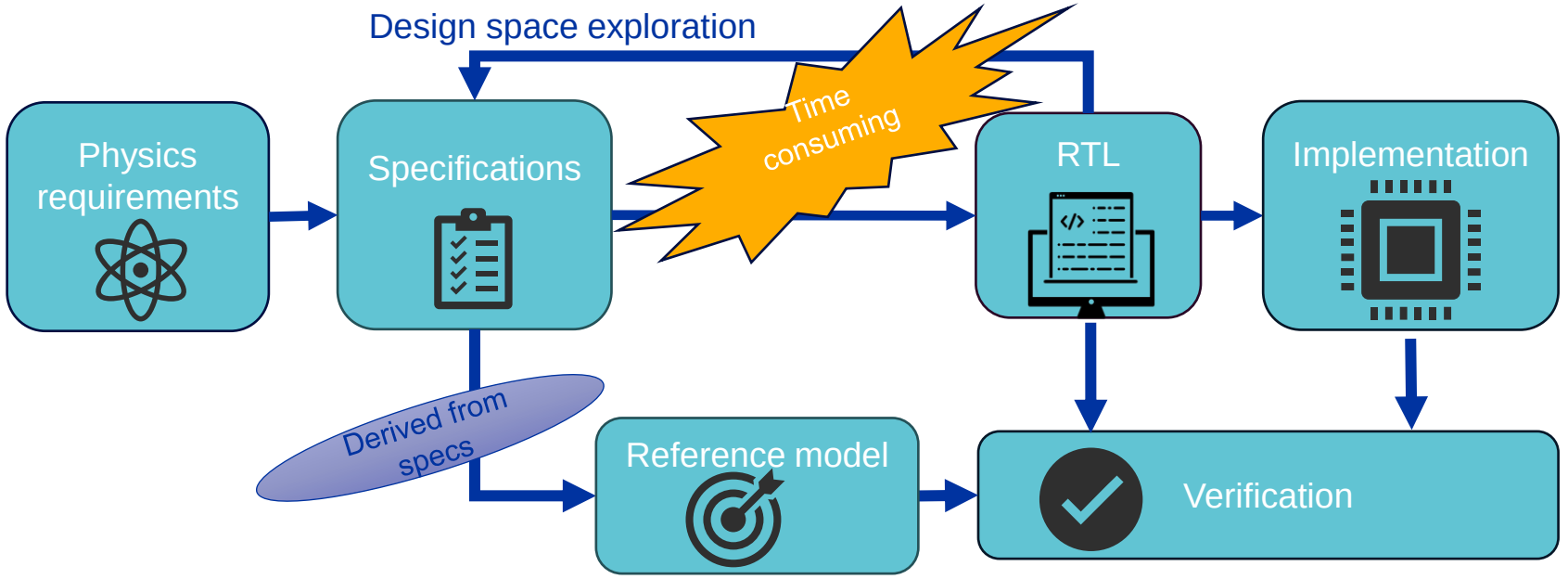
Jashandeep Dhaliwal on behalf of the EP R&D Work Package 5

25/09/2023

Detector Design Flow

Limitations

- the **design space exploration** requires:
  - HDL description of the system
  - Verification environment
  - Long simulation and iteration time
- The reference model has to be **derived from the specifications**

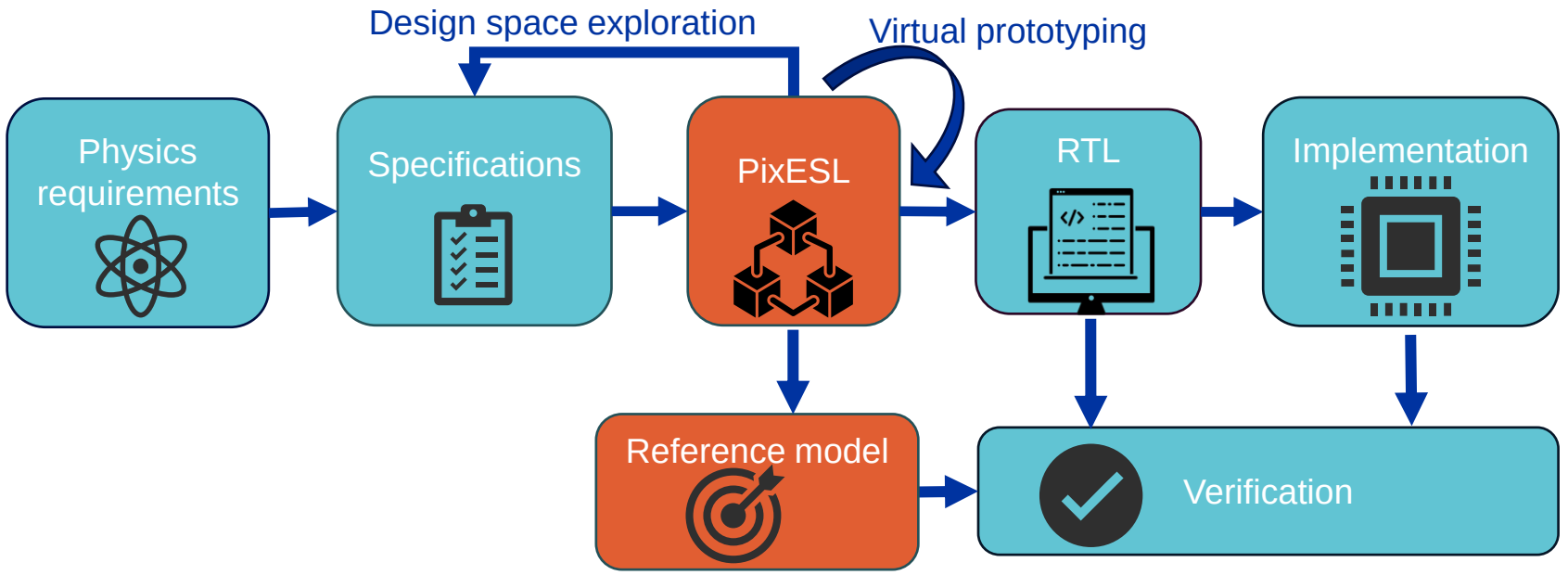


Detector Design Flow with PixESL

Goals

Develop a **high-level description of the system**, from front-end to back-end, to:

- Refine **specifications** and **performance evaluation** during prototyping
- Provide a **reference model** for verification
- Provide a **virtual prototyping environment** for new features development



PixESL - methodology

Open-source:

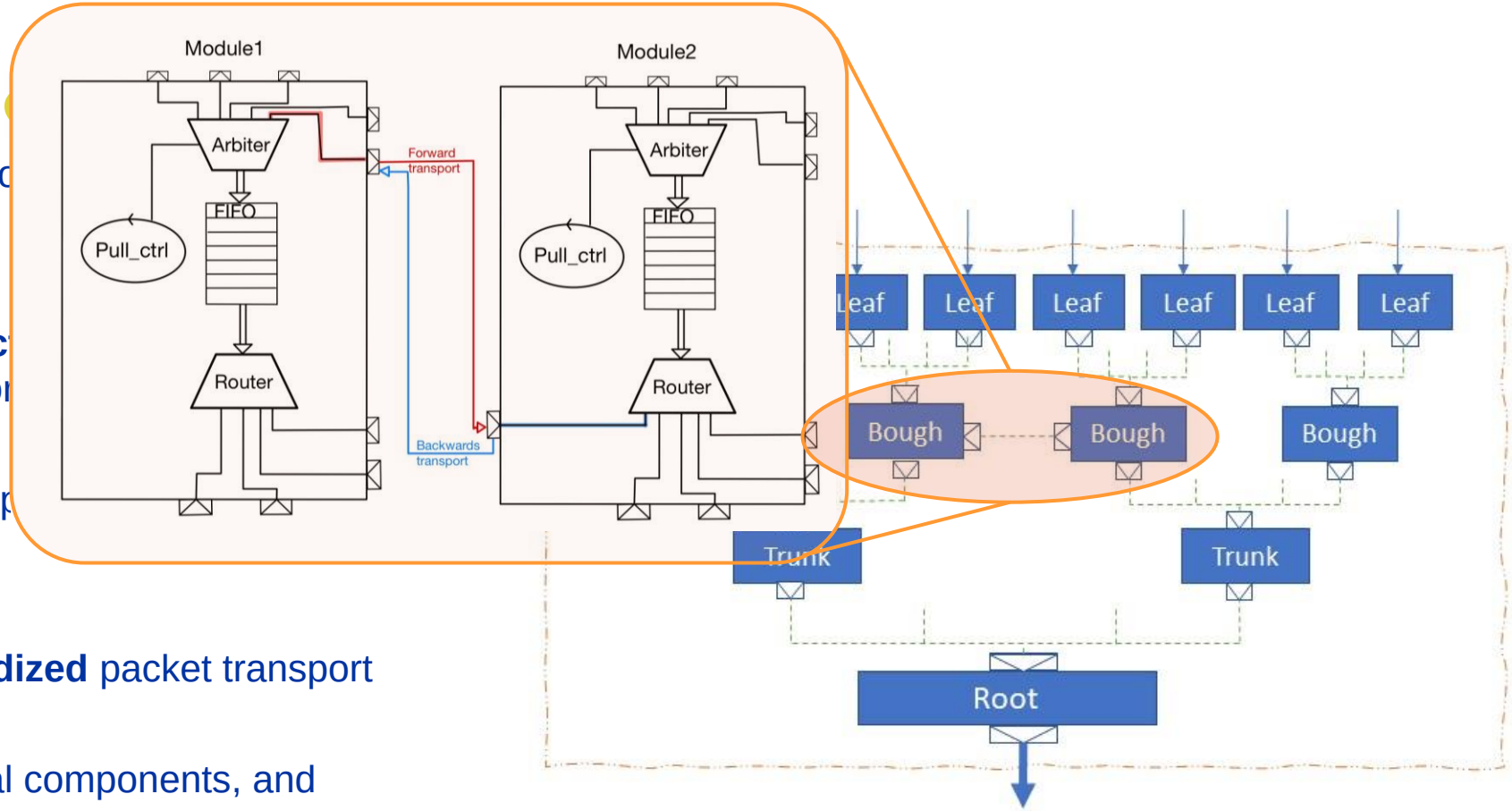
- The model is based on **C++** and
- Performance analysis are based c

User-friendly:

- The framework supports **architec**
  configurability (structure, memor
  interconnections)
- **User** and **developer** roles are sep

Reusable:

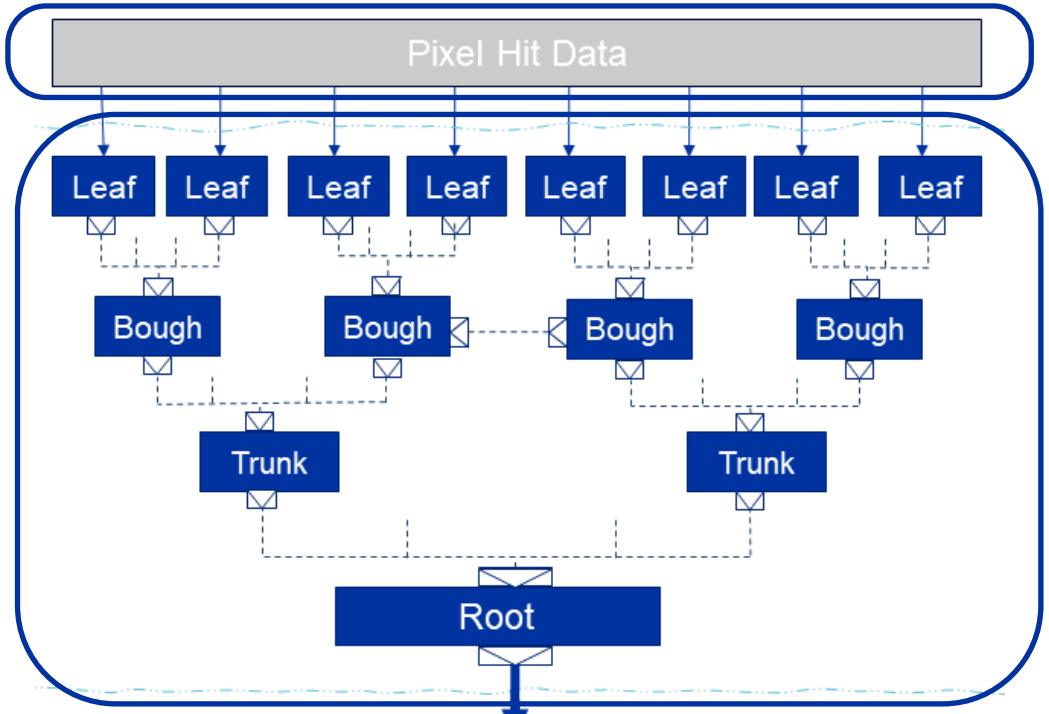
- **Generalized** layers and **standardized** packet transport (TLM)
- A **library** of layer types, functional components, and packet transport types
- Common integrated **metrics analyzer**



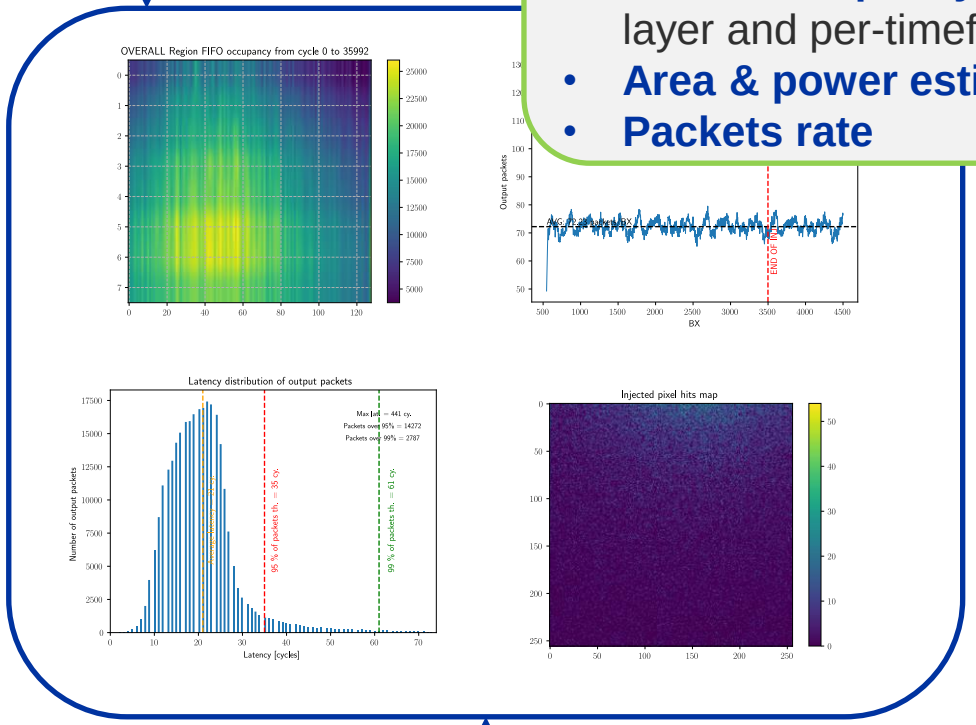
PixESL –Framework Diagram

Input data
(physics data / event generator)

Pixel FE model



Read-out model

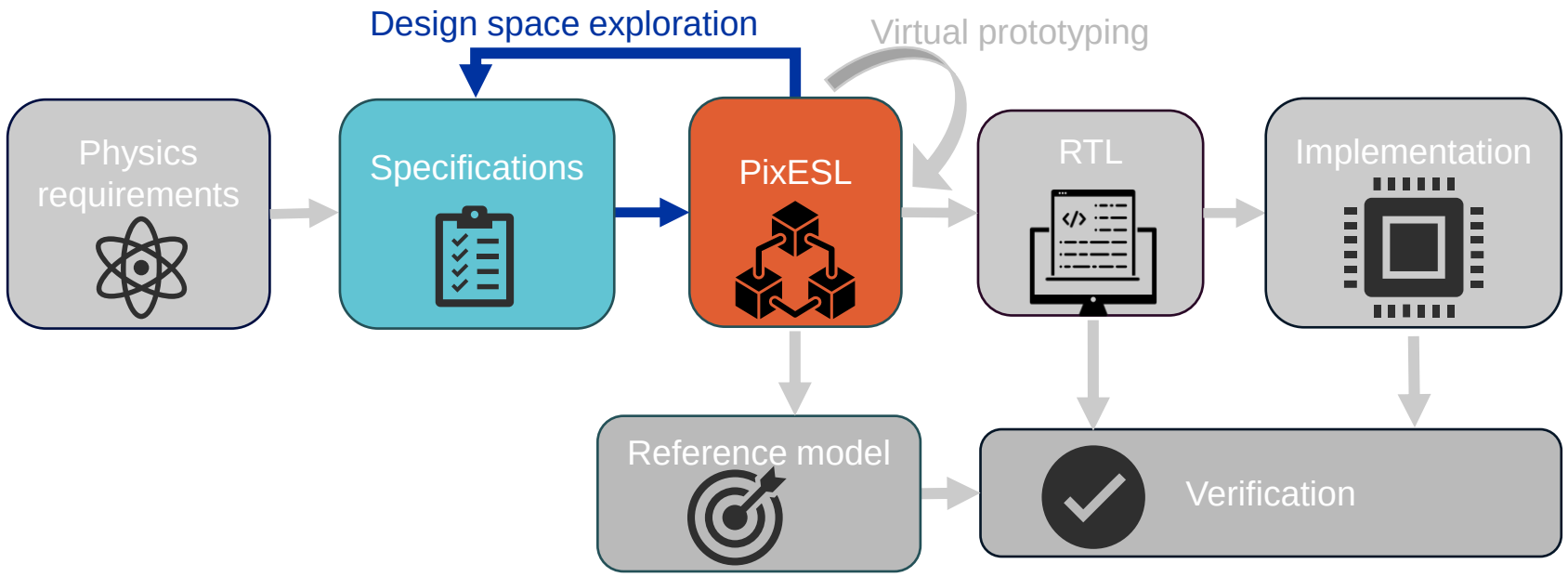


Metrics analyzer
(python scripts)

Metrics analyzer shows:

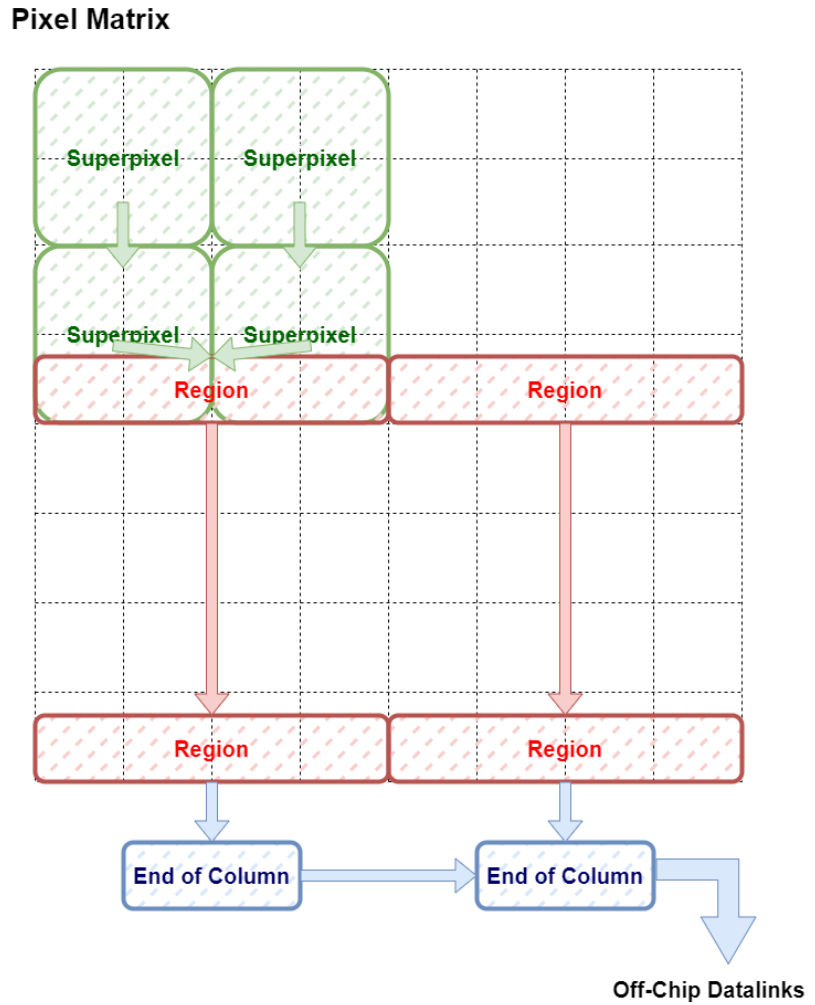
- **Readout efficiency**
- **Latency**
- **FIFOs occupancy** per-layer and per-timeframe
- **Area & power estimation**
- **Packets rate**

Design space exploration



LHCb Velopix2

- Velopix2 has been chosen as the first **case-study**: it is the upgrade to the pixel detector in the primary LHCb tracker
- Develop a **data-driven readout architecture**
- Based on **physical events**
- Main challenge: **higher occupancy** (x2 Velopix1)



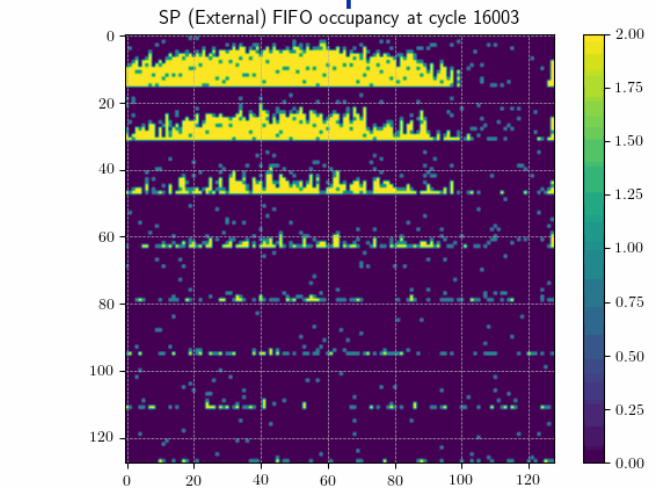
Thanks X. Llopart and S. Esposito for the support!

LHCb Velopix2 - Results

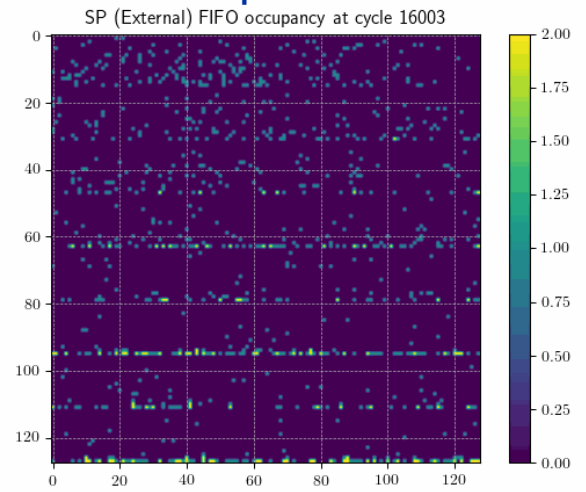
	Velopix1	Proposed
Pixel	256x256	256x256
SP	128x128	128x128
Regions	64x8	128x8
EoC	64 (8 ch.)	128 (16 ch.)

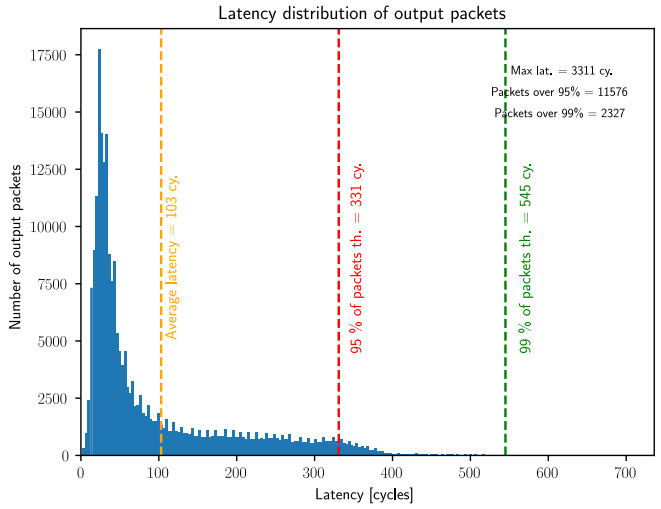
Readout eff.	80 %	99.5 %
Avg. latency	~100 cy.	~20 cy.

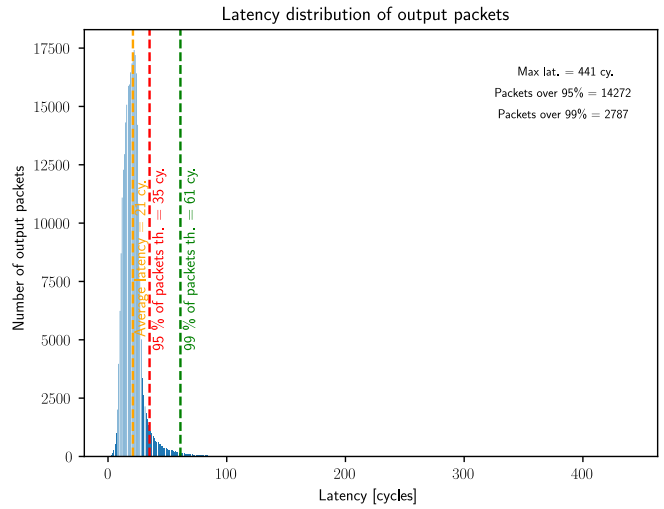
Velopix1



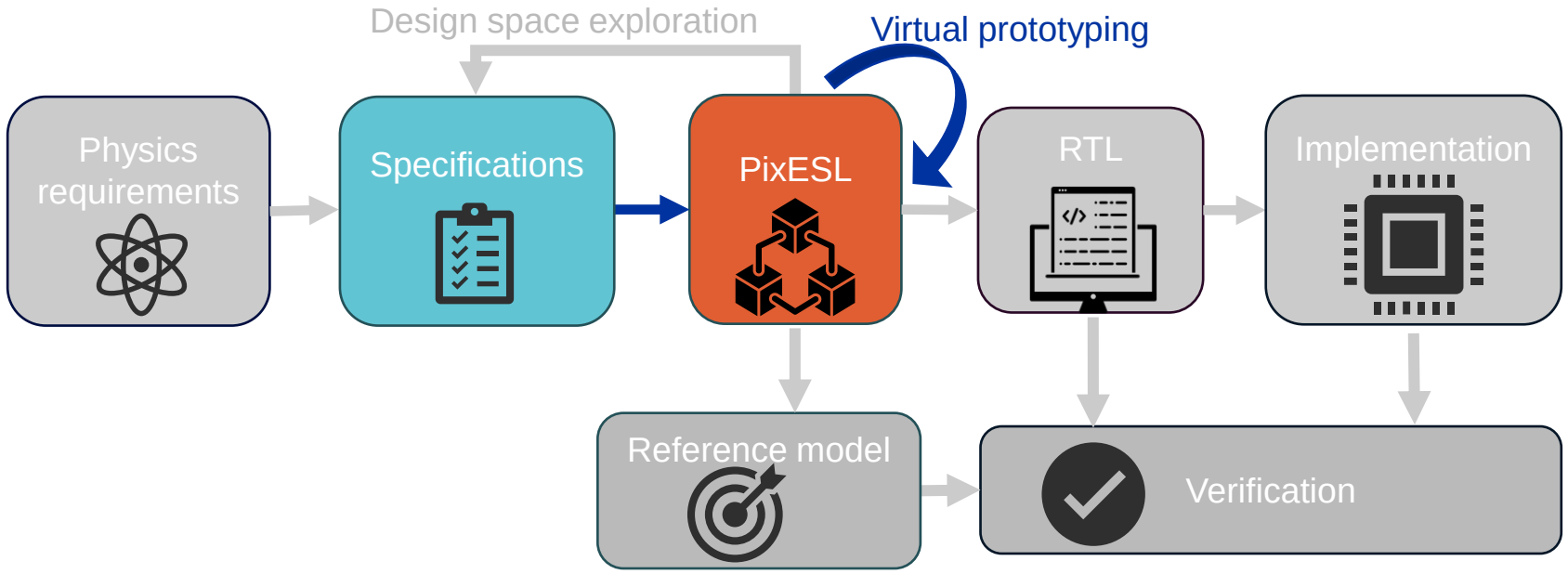
Proposed







Virtual prototyping



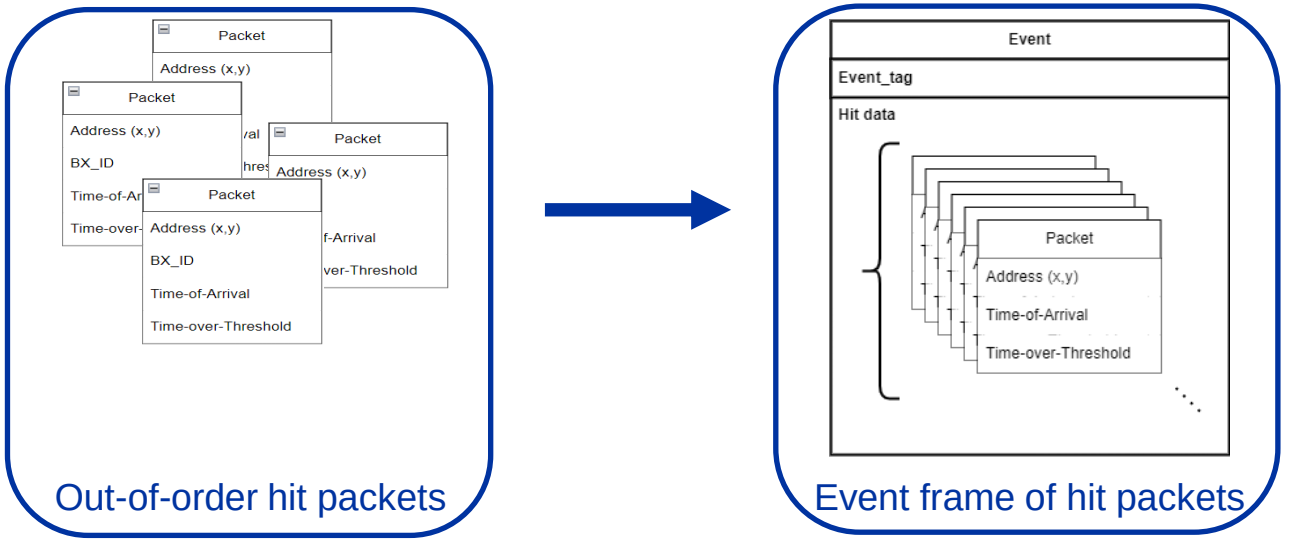
Sort&Bin – Virtual prototyping

Sort&Bin module:

- **ASIC** module, placed between the EoC and off-chip data links of **Velopix2**
- **Accumulates** hit packets over time and **groups** them in bins based on event tag (BX)

Goals:

- **Data reduction (**~20 %**)**
- **Fixed latency**
- **Power savings**

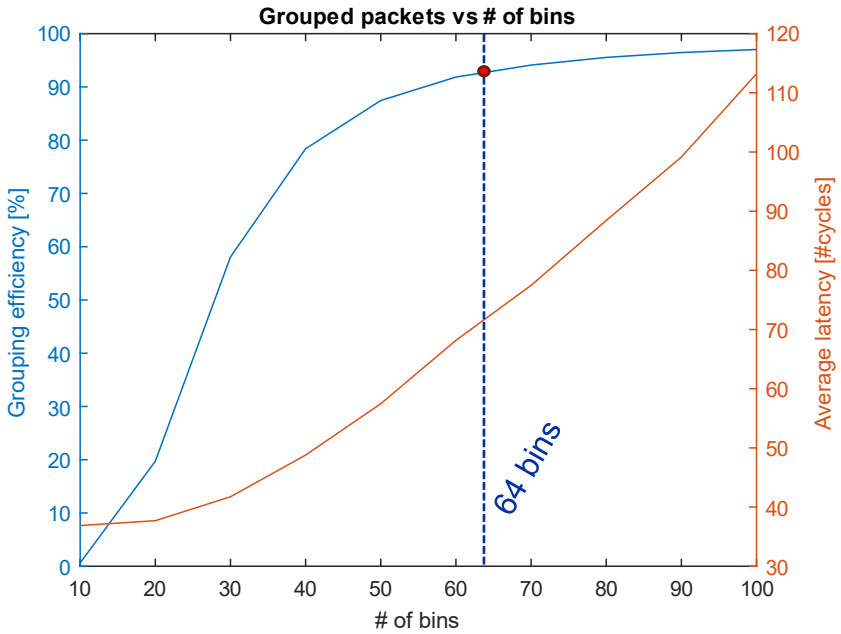


Sort&Bin – Virtual prototyping

Method:

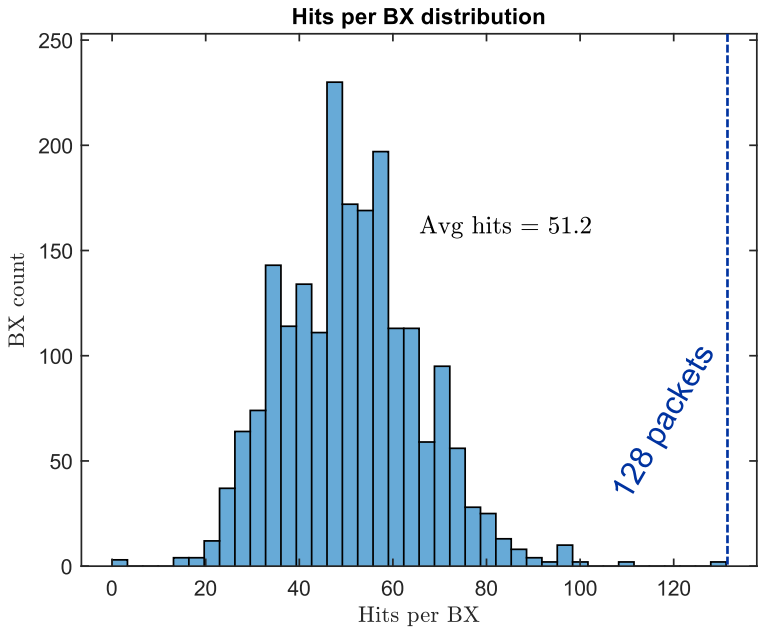
- Develop a **SystemC description** of the module
- Study the **performance with PixESL**

Number of bins



Target: >90% grouping

Bin size

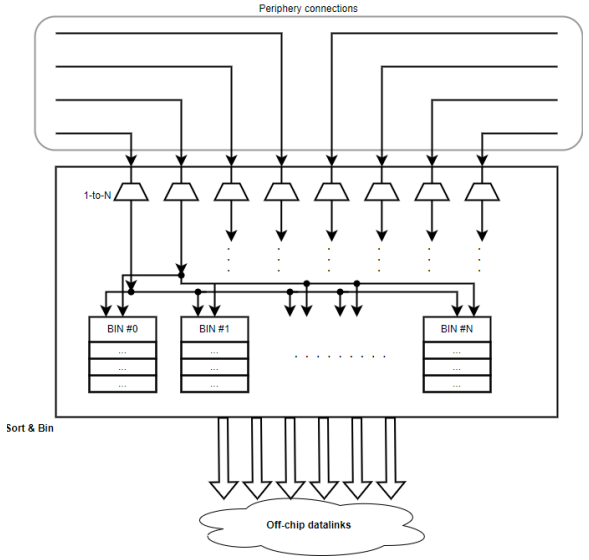


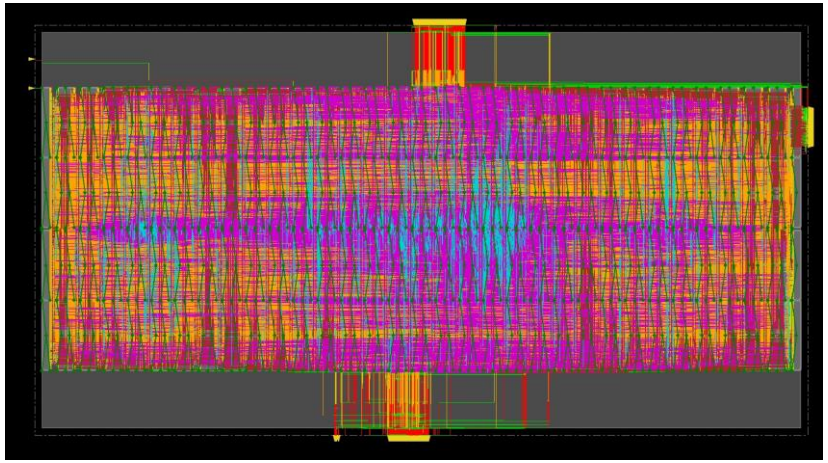
Target: Bin size > Max packets per event

Sort&Bin – RTL & PnR

Sort&Bin:

- **64 Bins** with 128 packets per bin
- **RTL**: DP-SRAM-based module





Virtual prototyping:

- facilitates the creation of a **new feature** in the **early stages of the development** process
- provides a **self-contained prototyping environment**
- provides a **reference model for RTL validation**

- Implemented in 28nm
- Power consumption: ~50 mW
- Area: 3.6 mm^2

Conclusions

- PixESL is a valid tool for high-level modelling and architectural analysis

- The framework presents an effective and quick prototyping approach:
  - Workforce: ~2 FTE for 3 years (2023-25)
  - Development time: ~3 months
  - Modelling of Velopix2: ~1 month
  - Modelling of Sort&Bin: ~1 week
  - Runtime: ~15 BX/s

- Metrics analyzer allows us to find bottlenecks and limitations

- New features can be developed by virtual prototyping

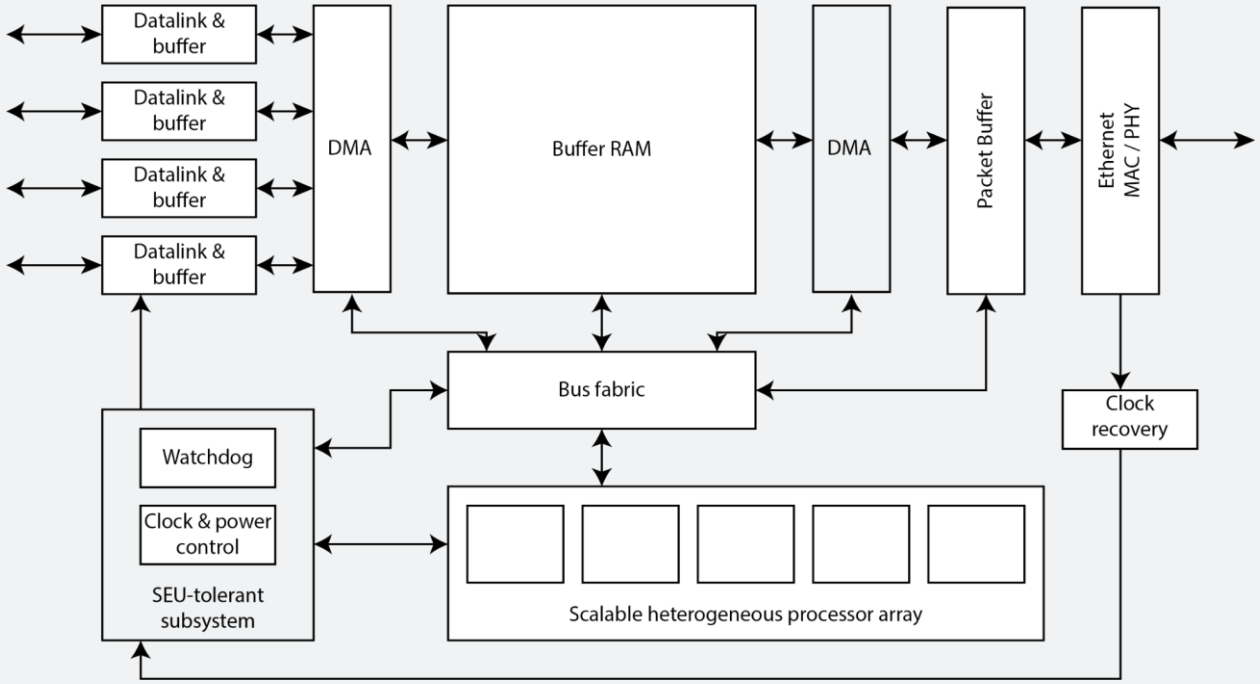
Team:

- Project mgmt. – Davide Ceresa (davide.ceresa@cern.ch)
- Developer – Jashandeep Dhaliwal (jashandeep.dhaliwal@cern.ch)
- Developer – Francesco E. Brambilla (francesco.enrico.brambilla@cern.ch)

CONTRIBUTORS & PLANNING

UK Consortium Contribution

- UK (STFC) Consortia
  - Royal Holloway, Birmingham, Warwick, Bristol, Manchester, RAL.
- Motivation
  - Develop common interface ASIC to couple a range of specialised FE ASICs to a common industry-standard off-detector interface.
- Plans for DRD7.2.c
  - Virtual Framework User
  - Evaluation and feedback
  - Possibly more…
- Contribution
  - Q4 2023: requests for funds
  - ~1.2 FTE for 4 years



Proposed common interface ASIC for detector readout, timing, and control

Science and Technology Facilities Council
ROYAL HOLLOWAY UNIVERSITY OF LONDON
MANCHESTER 1824 The University of Manchester
WARWICK THE UNIVERSITY OF WARWICK
UNIVERSITY OF BIRMINGHAM
University of BRISTOL

Virtual Electronic System Level prototyping project

Key notions:

- Abstraction
- Exploration
- Reusability
- Accessibility

Applications:

- Detector readout architecture
- On-chip processing prototyping
- Front-end/sensor modeling (?)

Institutes / Resources:

- Confirmed: CERN / 2 FTE, STFC / 1.2 FTE
- To be confirmed: IPHC Strasbourg /1 FTE, PSI / ?

Plan:

1. Identify participants (technical contacts)
2. Kick-off meeting in late October 2023
   a. User/developer roles
   b. Development Plan
      i. More study cases
      ii. Framework extension
      iii. New tools development
   c. Task assignment
3. Project proposal with deliverables