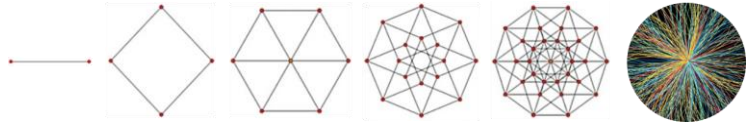


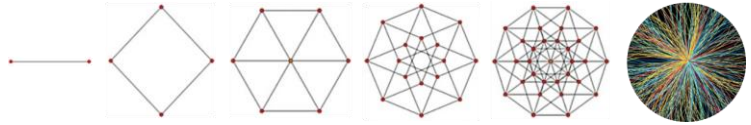
7.3.b Timing measurements and distribution

7.3.b-2 Timing distribution techniques and systems

sophie.baron@cern.ch

On behalf of the 7.3.b-2 contributors

Proto Project ID Card



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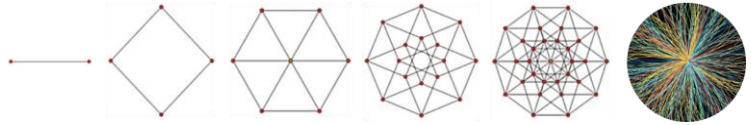
DRD7 Working Group	7.3: 4D & 5D techniques
Proto Project Reference	7.3.b: Timing measurements and distribution
Sub Project Title	7.3.b.2: Timing distribution techniques and systems
Subtitle	COTS characterization, Distribution Architectures and systems
Description	
Innovative/strategic vision	
Performance Target, deliverables and timeline	
Multi-disciplinary, transversal content	
Contributors and areas of competence	
Available material and human resources	
Existing R&D framework and available funding	
Additional resources to be requested	

- This Project is the second leg of the “Timing measurement and distribution” Proto Project
  - The first leg is “Strategies for characterizing and calibrating sources impacting time measurements”
- ID Card Represents a first «project Intention»
- Written by the conveners & initial contributors of the initiative
- Still at the intention level: Will be extended and completed with additional contributions from incoming institutes

Project Description & Vision



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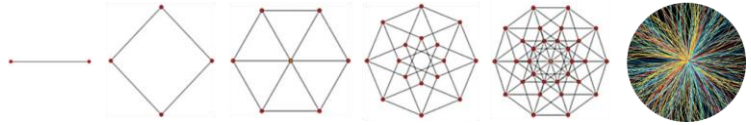
- Increasing need of timing detectors with very high resolution
- Very high precision and stability (o(ps)) of clock signal distribution
- “exotic” requirement, not a high priority of COTS manufacturers.

→ Common effort of the community to explore limits of COTS and reach ambitious timing precision not targeted by commercially available solutions

- Explore limits for these solutions
  - Develop and compare implementations on different COTS and custom platforms. Assess their ultimate performance.
- Carefully study and optimize implementation
  - Study and implement solutions to improve phase stability and mitigate non-determinism.
- Explore alternative ways of distributing timing

Performance Target



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Several parallel and complementary studies are proposed by the participating institutes:

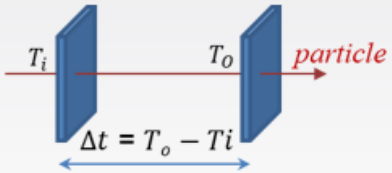
- Precise & deterministic timing distribution studies with FPGAs and Backend-boards
  - Microsemi PolarFire FPGAs (BE & FE interest as rad tol <300 Gy)
  - Intel FPGAs / PCIe400
  - Xilinx FPGAs / Felix
- White Rabbit
  - WR based Clock Distribution system prototype for 4-D detectors
  - Implementation of WR nodes on Intel FPGA
- Solutions for precise and deterministic clock distribution with not fully deterministic COTS
  - FW IPs and HW solutions to measure and mitigate phase changes
- New protocol development for precise & deterministic clock and timestamp distribution for future non LHC experiments, and implementation study for on-detector ASICs
- Nice to have (but not funded for the moment) - in collaboration with WG7.1: custom timing ASICs to reach targeted performance if not guaranteed by COTS

An Example: WR for 4-D detector

ToF Computation in 4-D Detectors based on WR technology

We want to compute:

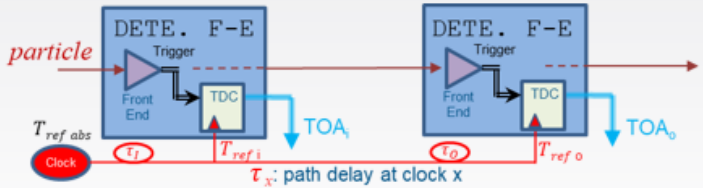
Δt: *Time of Flight* (TOF)



Δt: TOF between detector planes
T_i, T_o: absolute times

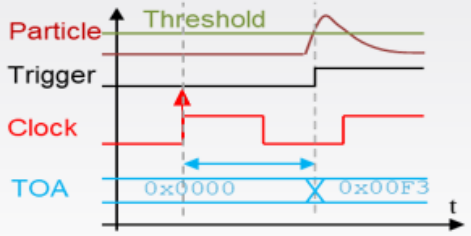
We measure:

2x Time Of Arrival (TOA) w.r.t ref. clock



τ_x: path delay at clock x
T_{refx}: local ref. clock at node x

We use a local reference clock T_{refx}

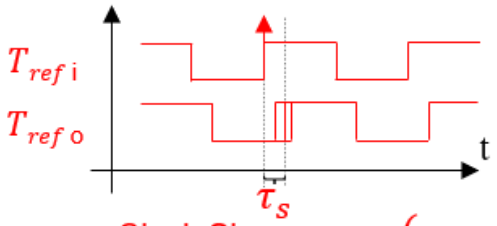


T_{ref} needs to be a common synchronized reference among all nodes

$$T_x = T_{ref\ x} + TOA_x$$

We need clean Clock distribution ensuring accuracy, precision and coping skew

Phase of the Ref clock at Detectors



Clock Skew $\tau_s = (\tau_0 - \tau_i)$

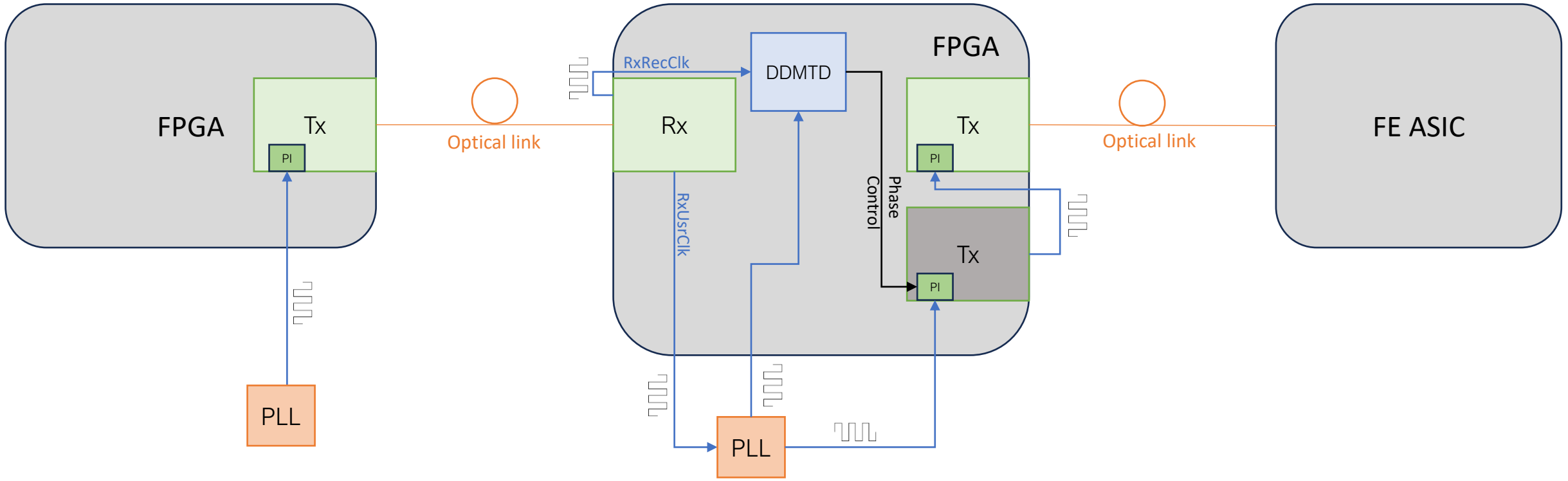
IEEE 1588 standard – High Accuracy profile???

This task plans to assess the feasibility of utilizing white rabbit technology for the creation of a distributed timing architecture for 4D detectors:

- WR Learning curve (as user and developer), System performance achieved…
- WR technology has been developed at CERN – Accelerator area

Courtesy: Fernando Arteche

Another Example: mitigating non determinism of Xilinx receivers



Tx — Temperature Compensation (TCLink) Transmitter

Tx — Transmitter used as a clock fine phase shifter

DDMTD — Phase measurment

PI — Phase Interpolator (ie Phase shifter)

Example of investigation: using features of Xilinx transceivers to monitor phase drifts/jumps and compensate for them

Deliverables & Timeline

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- Q4 2023-Q3 2024:
  - Regular reports on studies for generic solutions to mitigate non-determinism of COTS
    - To be extended if funding obtained
- 2024-2025: Prototyping and first results on
  - White Rabbit studies:
    - WR for Muon detectors
    - WR implementation on Intel Agilex/PCIe400 prototype
  - FPGA & Platforms
- 2025: Reporting
  - Reports for:
    - Analysis and limitations of WR technology in 4D detectors
    - FPGAs / platforms evaluation
    - New Protocol implementation in ASIC

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Precise & deterministic timing distribution study with FPGAs (PolarFire, Xilinx)

GOBIERNO DE ESPAÑA · MINISTERIO DE CIENCIA, INNOVACIÓN Y UNIVERSIDADES · Ciemat Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

Nikhef

Precise & deterministic timing distribution study with Intel FPGAs & WR implementation

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis

New protocol development for clock and timestamp distribution for future non LHC experiments

University of BRISTOL

White Rabbit Clock distribution system prototype for 4-D detectors

ITAINNOVA INSTITUTO TECNOLÓGICO DE ARAGÓN

IFCA Instituto de Física de Cantabria

CNM Centro Nacional de Microelectrónica · IMB

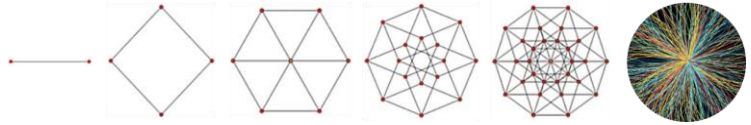
Solutions to mitigate COTS' nondeterminism

CERN

*Some other institutes communicated their firm intention to contribute via the survey and are being contacted for consolidation

Contact us if you wish to contribute!

Resources and Organization



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- Resources
  - Manpower and Funding currently being consolidated
    - So far, we start small… ~5 FTE / year
    - Several institutes have limited resources on this activity for the moment and are currently requesting funds to gain momentum (CERN, Bristol, ..)
    - Additional institutes planning to request funds and join the WG
  - Additional contribution proposals under study
- Organized as
  - A Forum
  - Rotating Chair
- Strong link with
  - WG 7.3.b.1 (Timing simulation) and 7.5.c (Generic backend)
  - WG 7.1 when it comes to potential FE ASIC design
  - HPTD interest Group (High Precision Timing Distribution)

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