Cooling: Cooling plates

On behalf of the 7.4c collaborators

7.4: EXTREME ENVIRONMENT AND LONGEVITY

IMPLEMENTING DRD7:

AN R&D COLLABORATION ON ELECTRONICS AND ON-DETECTOR PROCESSING

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Introduction

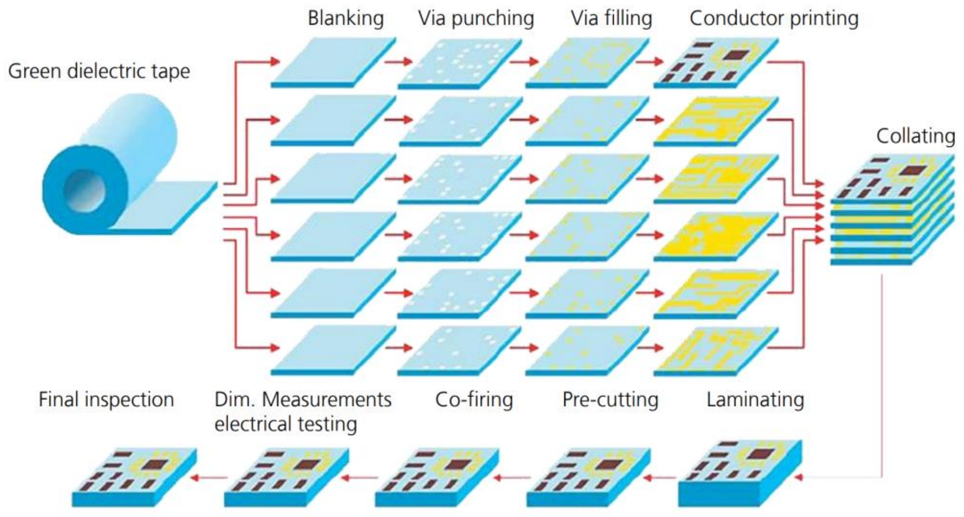
- No single solution for the cooling structure nor coolant
  - Different material budget constraints, power dissipation, …

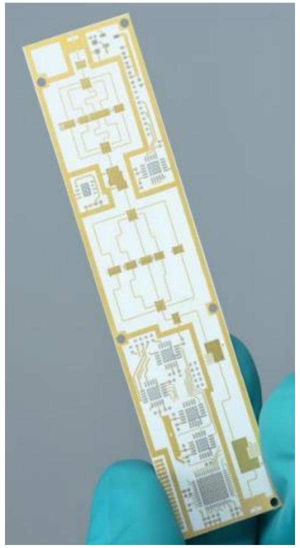
- Three (sub-)projects will be described today:
  - Ceramics cooling plate (UoM)
  - Microchannel cooling and active interconnection developments (CNM, DESY, IFIC)
  - Microchannel cooling manufacturing via thermocompression (CPPM)

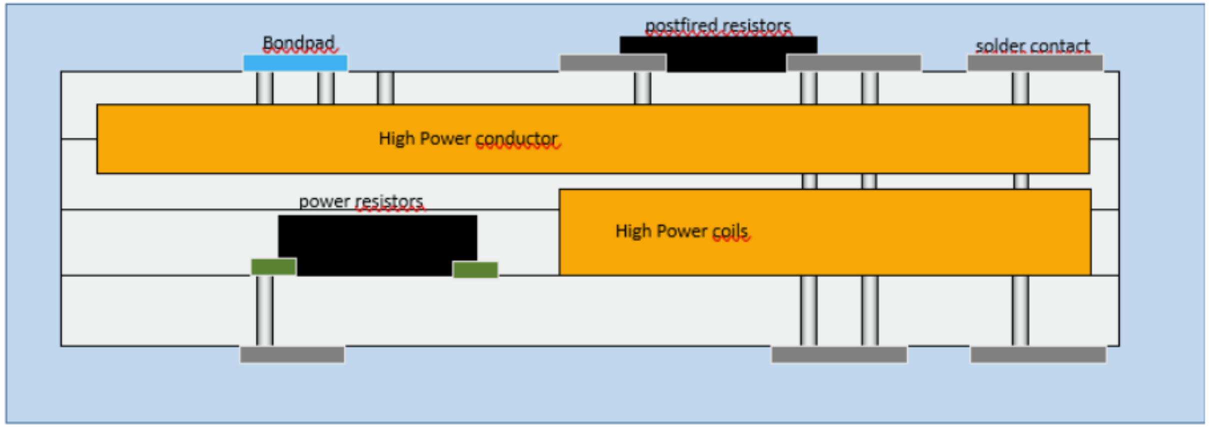
- More applications and contributors are welcome
- Potential future overlap with the DRD8:
  - DRD7.4c – "covers the cooling structures in direct contact with electronics"
    - Cooling plates are included (e.g.: coolant R&D not included)

Ceramics

- Potential collaboration with Fraunhofer IKTS (Germany)
- Different base materials: YSZ, Al_2O_3, AlN, … including SiC
- Manufacturing based on several layers
- <u>Why?</u>
  - Robustness, reliability, stability in ultra-high-vacuum
  - Possible to embed conductive layers in between ceramics layers and metalize the surface
    - Potential to integrate electronics or high conductivity elements
  - Mechanically robust and compatible with high ultra vacuum







Ceramics

- Experience with fluidic applications
- First prototype
  - Initial channel with $70\mu m$ width (restrictions)
  - Channels height $100\mu m$
  - Overall dimensions: $40 \times 60 mm^2$
  - Based on alumina (Al_2O_3)
    - Possible to move to SiC afterwards
- Encouraging results from FEA studies
  - Geometry based on the VELO Upgrade I design (5 mm overhang)
  - For $2W/cm^2$, $\Delta T \sim 9°C$

- Goal: Manufacture and validate initial prototypes in the coming years to high pressure, leak tightness and cooling performance
  - Benchmark: LHCb VELO Upgrade 2 requirements (High pressure 186 bar, leak tight (vacuum operation) and excellent thermal performance)

MANCHESTER 1824
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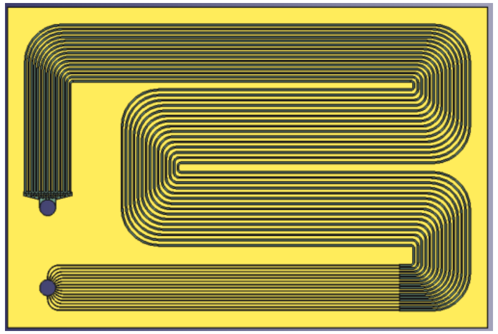
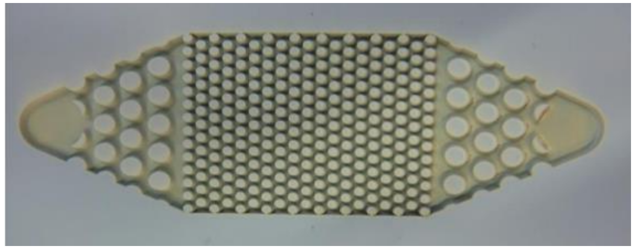


SNAKEI based design to optimize printing parameters/test feasibility



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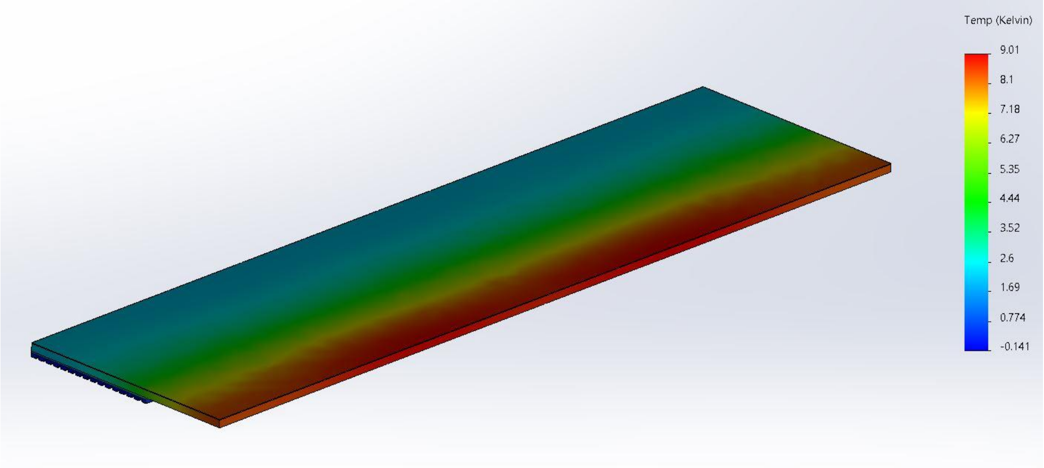


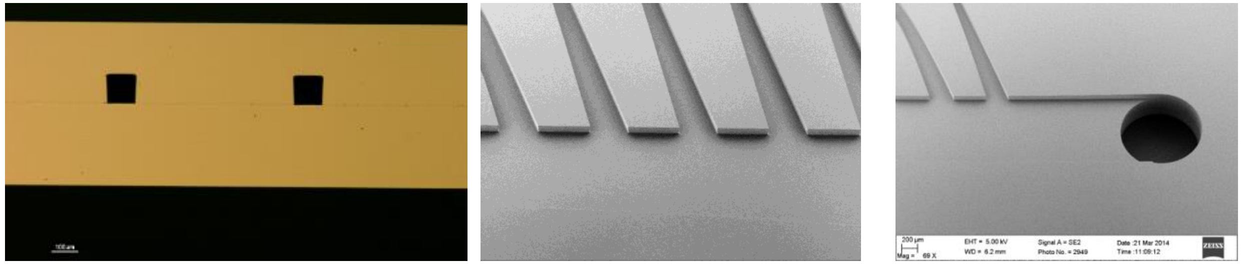
Simplified FEA focusing on the 5 mm overhang. Substrate in alumina and heat conduction on one side of the cooling plate and Stycast (100um).

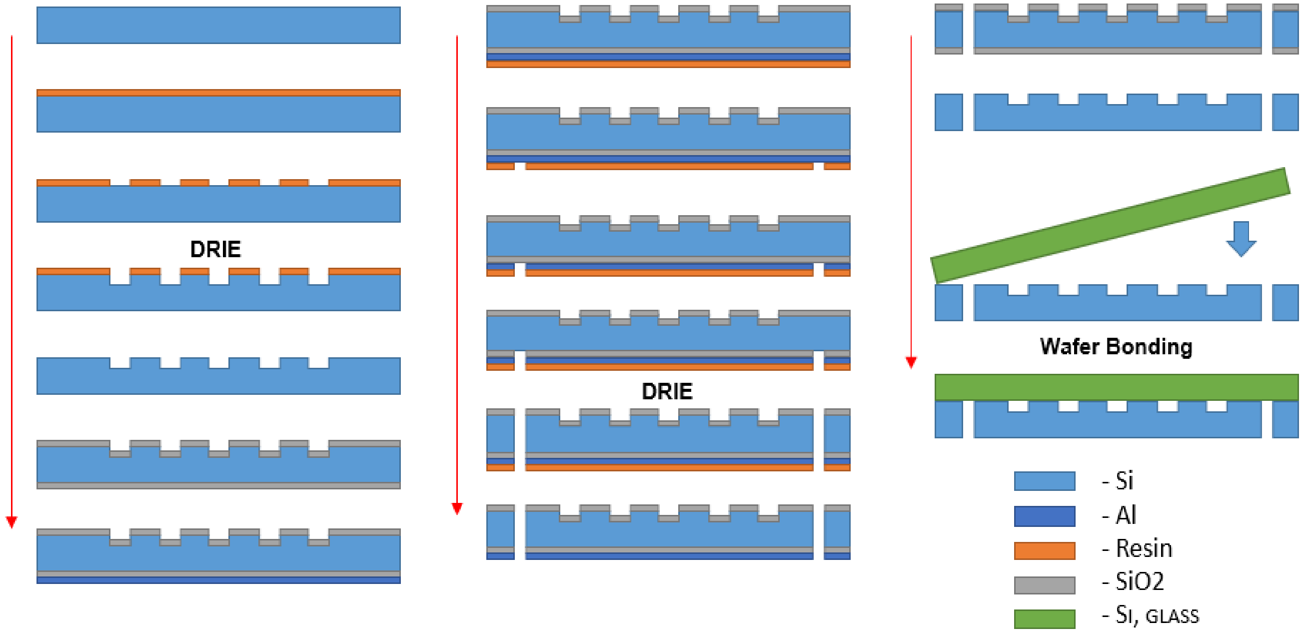
Microchannel cooling and active interconnection developments

- **Miguel Ullán (IMB-CNM, CSIC)**, Carlos Mariñas (IFIC-UV, CSIC), Marcel Vos (IFIC, CSIC-UV), Ingrid Gregor (DESY), Sergio Díez (DESY)
- In the past, we developed a technology of micro-channel cooling for High Energy Physics detectors
  - N. Flaschel, et al. ”Thermal and hydrodynamic studies for micro-channel cooling for large area silicon sensors in high energy physics experiments”, NIMA, vol. 863, pp. 26-34, 2017. http://dx.doi.org/10.1016/j.nima.2017.05.003
  - Ph.D Thesis: Micro-channel Cooling For Silicon Detectors. Nils Flaschel. Hamburg University. 2017

Microchannel cooling and active interconnection developments

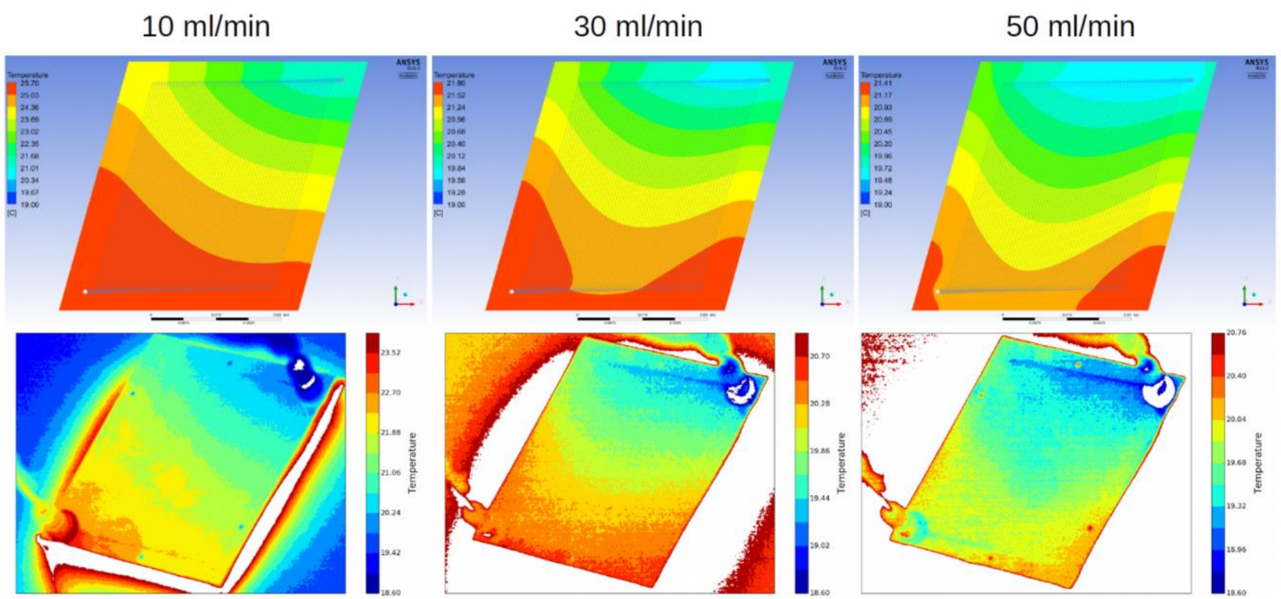
- Technological process for buried micro-channels at IMB-CNM
- Creation of microchannels:
  - Deep Reactive ion etching (DRIE)
- Buried micro-channels:
  - Wafer bonding



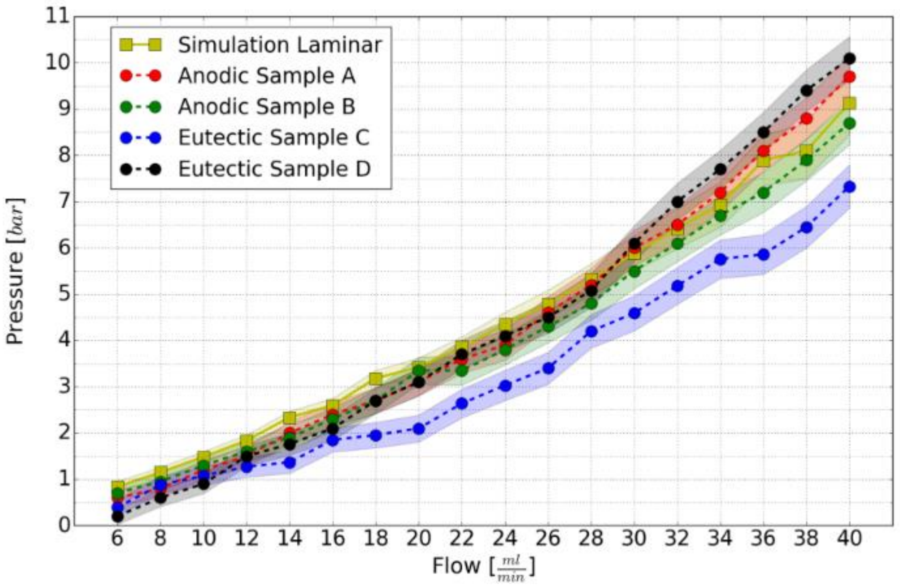


Centro Nacional de Microelectrónica CSIC

Microchannel cooling and active interconnection developments

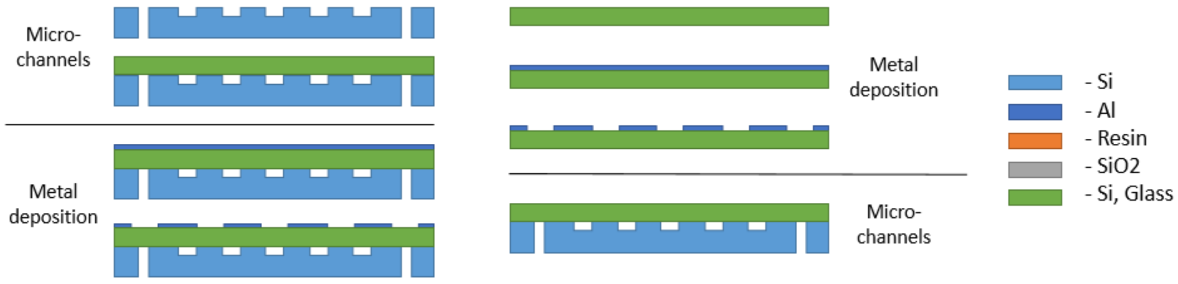


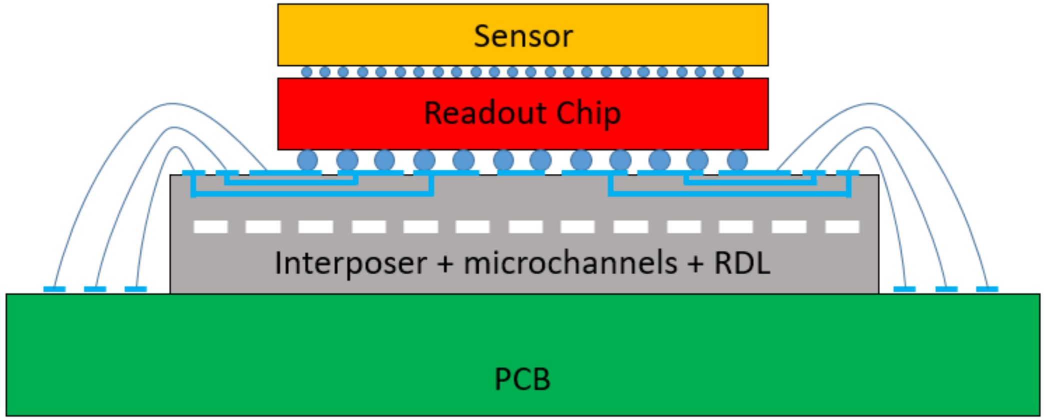
- Previous results on fluidic and thermal tests
- Laminar flow
- Good agreement with simulation
- Thermal homogeneity across the sample, < ±1 ºC (for lowest flow rate)



Microchannel cooling and active interconnection developments

- Main Objective I: Integration of micro-channels in silicon interposers with integrated signal and power routing (RDL)





Main Objective II: Full integration of the sensor (CMOS technology) with the microchannel cooling in a single silicon piece

- Full integration of DMAPS chip with the microchannels in a single monolithic piece
- Post-processing at wafer level with a CMOS compatible process
- Following the "post-processing" technique developed previously
- Additional technological developments
  - ✓ Low temperature ($350°C$) anodic bonding
  - ➢ Microchannels created on glass substrates (isotropic wet etching)
  - ➢ Eutectic and/or fusion bonding
  - ➢ Improve post-processing compatibility
  - ➢ Full demonstrator

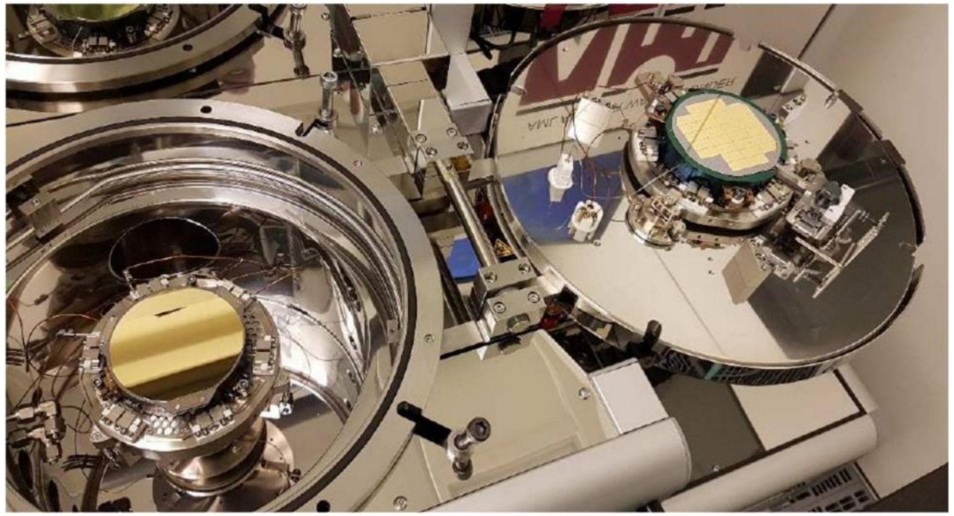
Microchannel cooling manufacturing via thermocompression

R&D to develop a low-cost micro-channel production process

As an alternative to the complicated and costly direct Si/Si bonding, investigate bonding techniques with intermediate thin layers:

- Anodic bonding with glass (BF33)
- Thermocompression with gold

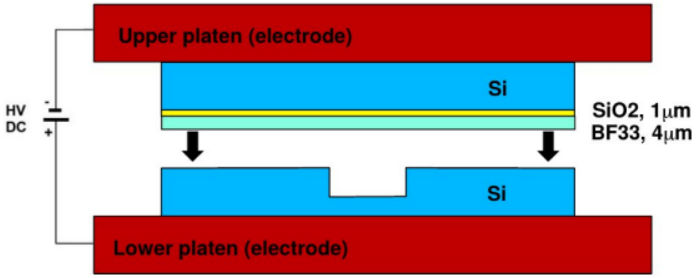
Bargiel et al., Micromachines 2023, 14, 1297

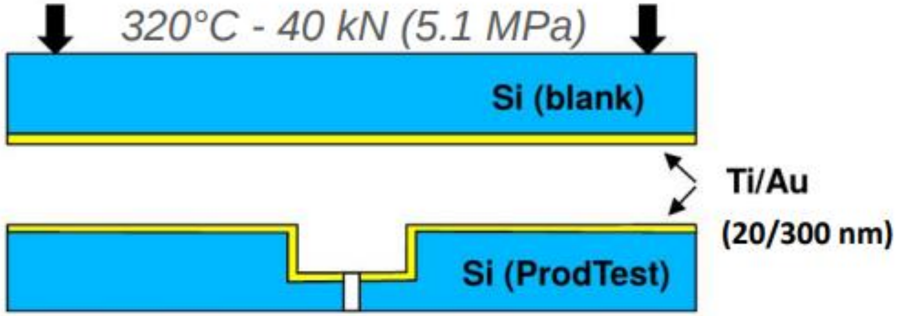


Thermocompression

Anodic bonding

50V - 400°C - 50kg





Microchannel cooling manufacturing via thermocompression

[Bargiel et al., Micromachines 2023, 14, 1297]

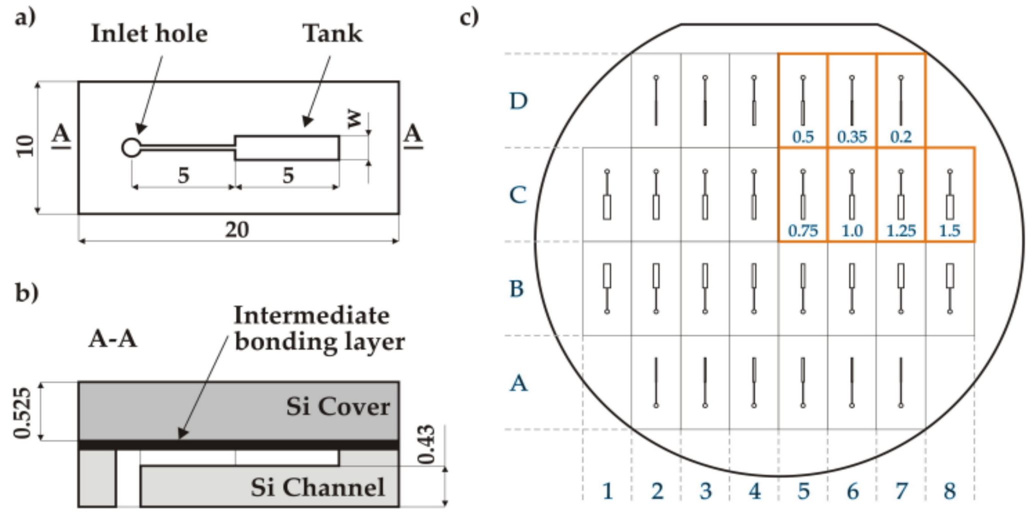
CPPM — CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE

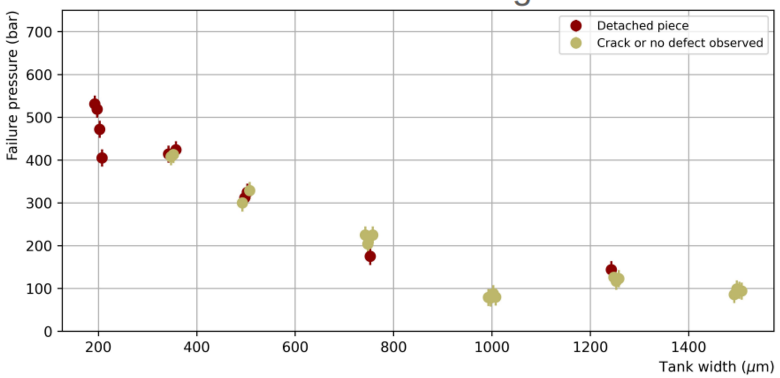
Bonding strength evaluated through a series of destructive pressure burst tests, recording the maximum pressure reached in microfluidic test structures before breakage (à la LHCb)

⇒ Test chips produced both with the anodic and with the thermocompression bondings can sustain very high pressure

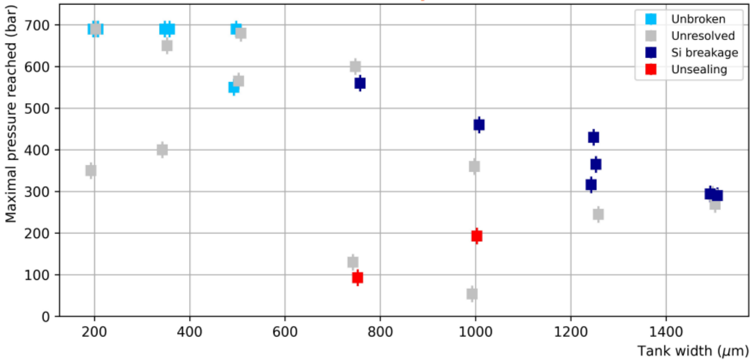
⇒ Focus on thermocompression as

- It generally allows to reach higher maximal pressures
- It is a widespread technique available in most clean room facilities





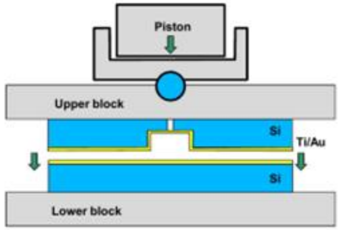
Maximum pressure limited by the adhesion force of the deposited BF33/SiO_2 layers

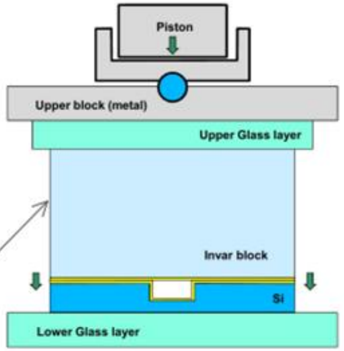


Maximum pressure limited by the silicon strength (except for a few outliers)

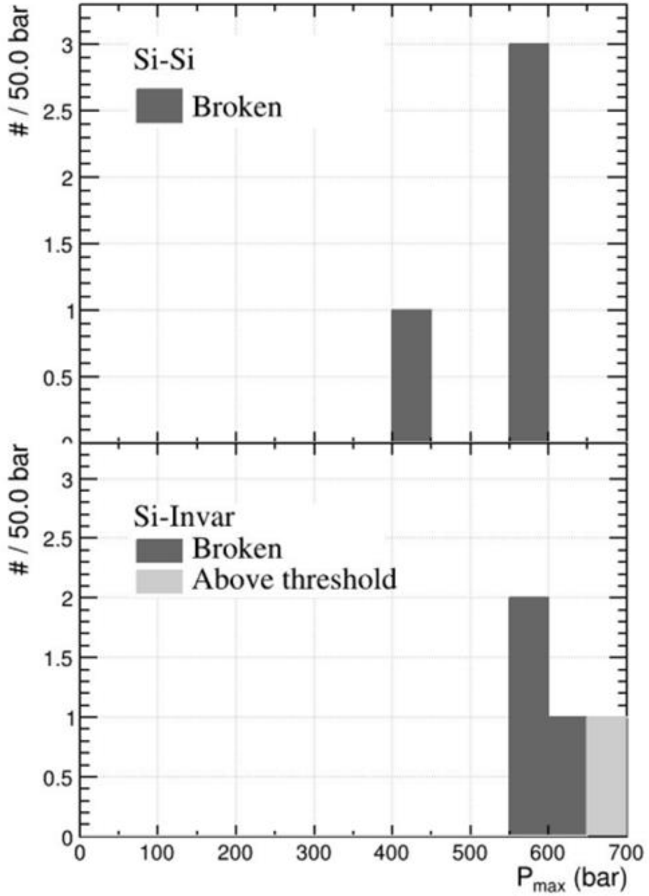
Microchannel cooling manufacturing via thermocompression

- Towards the bonding of a connector using thermocompression process:
  - Investigate chip level bonding replacing the bonder with a mechanical press at atmospheric pressure outside the clean room
- Two configurations tested:
  - -Si/Si bonding (for reference)
  - -Si/Invar
  - → Both types can sustain high pressure
  - → Proof of concept validated!





Polished block of Invar mimicking a connector



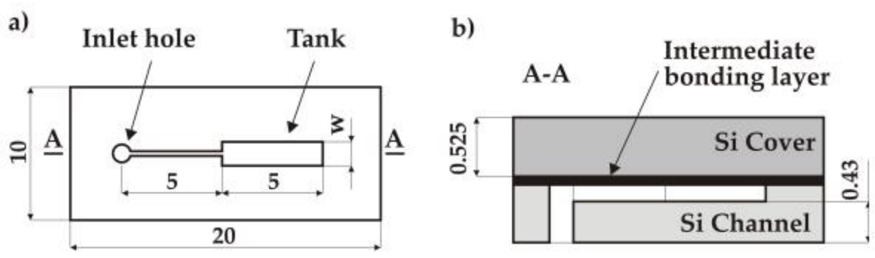
Microchannel cooling manufacturing via thermocompression

- Replace the mechanical press with an hyperbar chamber
  - Allow to reach very high pressure
  - ≥ 400 bar in chamber
  - Force applied in bonder limited to 40kN
  - (i.e. 5.1MPa for 4” wafer, 2.3MPa for 6” wafer)
  - Pressure more uniform
  - Less stress applied on wafer
  - Bonding at room temperature
  - Can adapt various geometries
- Test wafer bonding with fixed width pressure test structures (w=850µm)

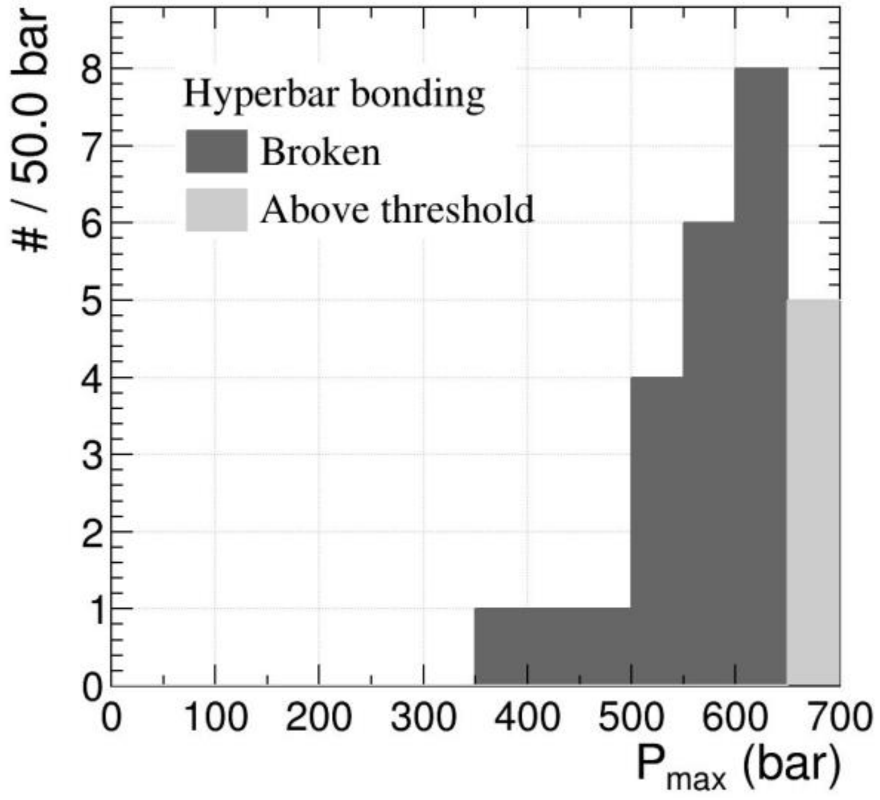
⇒ All samples sustained very high pressure

⇒ All breakage occurred in the silicon (i.e. bonding has held)

⇒ Proof of concept validated !



w=850 µm



Microchannel cooling manufacturing via thermocompression

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE
CPPM

R&D to develop low-cost micro-channel production process is being pursued at CPPM

Currently focusing on the bonding process, very appealing technique identified:
– "Hyperbar" bonding with thin intermediate Au layers
– Can be used to bond wafer
– Bonding of connector in hyperbar chamber being investigated

Goal is a functional prototype in the coming years

Part of a global R&T effort in CNRS/IN2P3, shared among 3 French laboratories and including developments on boiling flow modelling and testing.

Conclusion

- Microchannel cooling and active interconnection developments (CNM, DESY, IFIC)
  - Aiming to bring more functionalities to the cooling plate
    - Redistribution layer could be an interesting solution for ASICs with through-silicon vias
  - CMOS compatible process to integrate the cooling to the sensor

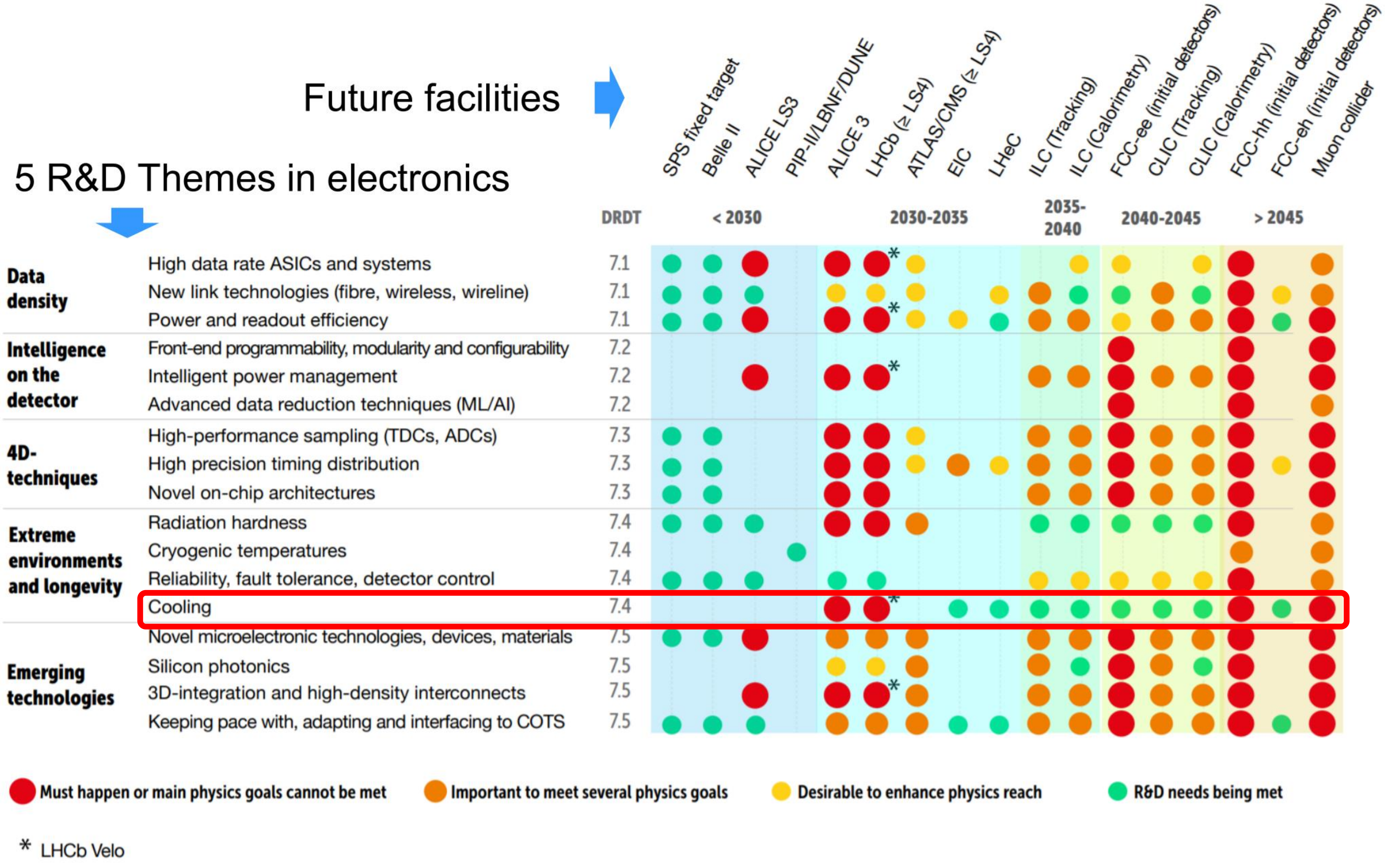
- Microchannel cooling manufacturing via thermocompression (CPPM)
  - Main motivation to reduce the manufacturing cost
    - Very promising results “hyperbar” chamber (resistance to high pressure)
  - Techniques developed can be also explored for integration (chips and connecturization)

- Ceramics
  - It has also the potential to include electronic features
  - Fully validated initial prototypes in the coming years to high pressure, leak tightness and cooling performance in the following years
  - LHCb VELO Upgrade 2 as benchmark requirements (High pressure, CO_2 evaporative cooling)

Backup slides

Future facilities

5 R&D Themes in electronics



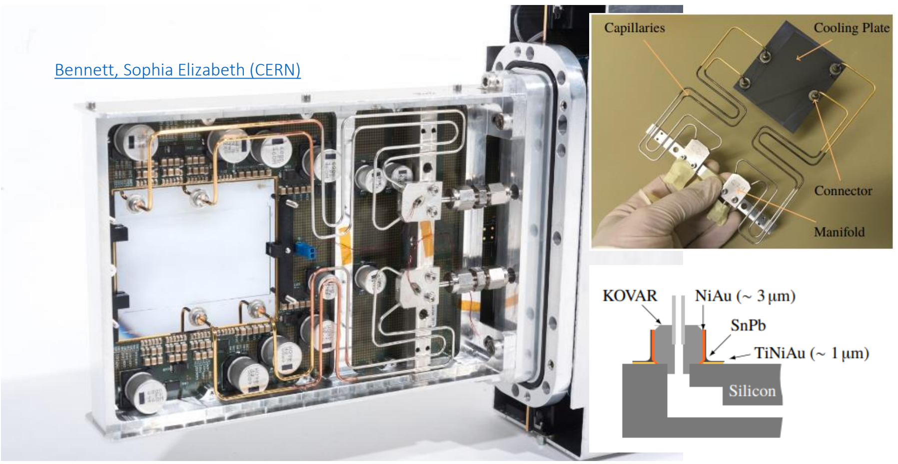
Cooling

- Vacuum
- Operating Temperature
- Material Budget
- Power density
- Thermal figure of merit
- Integration
- Area/Cost

NA62 GTK

JINST **14** P07010

Bennett, Sophia Elizabeth (CERN)

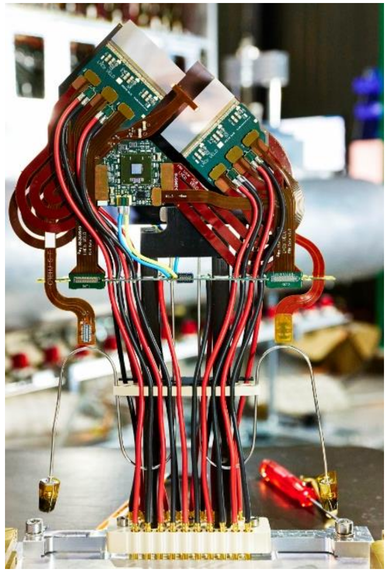


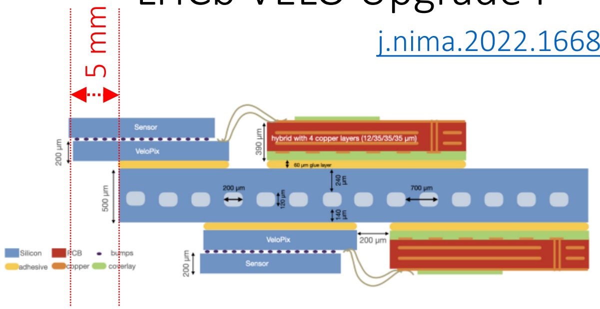
0.5% X_0, 200 × 70 μm^2 micro-channels, C6F14 liquid coolant, vacuum, 0.32 W/cm2 in the pixel matrix, < 5C

LHCb VELO Upgrade I

Brice, Maximilien; Ordan, Julien Marius (CERN)

j.nima.2022.166874

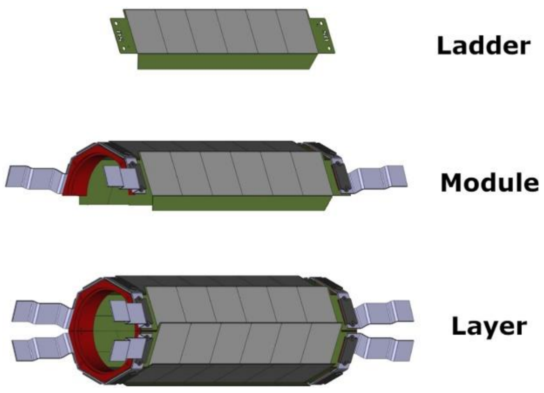




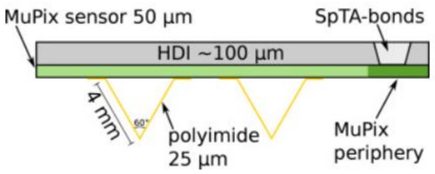
0.4-0.9% X_0 (innermost region)
ASIC/Sensor overhangs by 5 mm,
Micro-channels 120x200 μm^2,
CO2 bi-phase, 1W/cm^2, Sensor < $-20°C$,
vacuum

Mu3e

SciPost Phys. Proc. 5, 020 (2021)

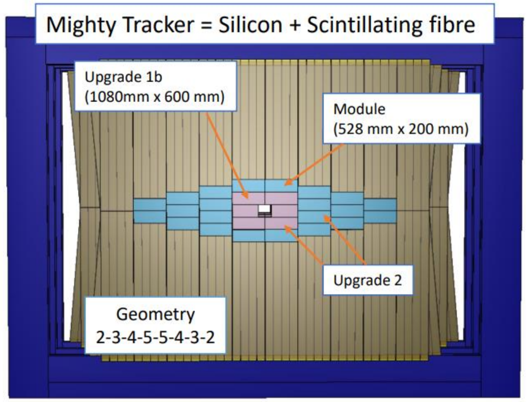


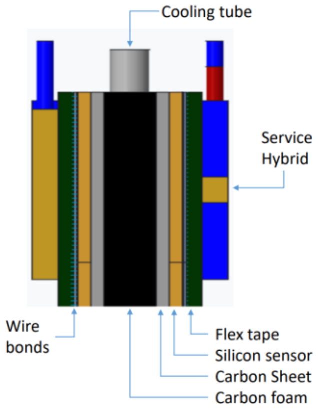
0.1% X_0, Helium gas cooling, $0.4 W/cm^2$, Temperature < $70°C$



LHCb Mighty Tracker (2032)

FTDR





$18 m^2$, 1-2% X_0, Kapton tubes, Liquid cooling (?), $0.3 W/cm^2$, Temperature $\leq 0°C$