DRD 7.5a: DAQOverflow

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On behalf of the DAQOverflow project contributors

Second DRD7 workshop, CERN

DRD 7.5a

Introduction

Strategic Vision

Project Aim

Timeframe

Example study

Contributors

Organisation

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September 26, 2023

Introduction

CPU, GPU, FPGA, and ASICs
Tradeoffs

CPU   GPU   FPGA   ASIC

Flexibility
Efficiency

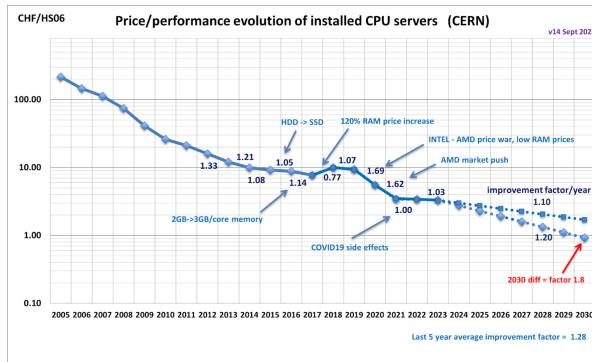Cost per unit
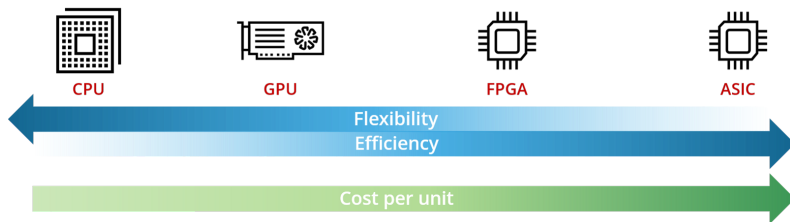
- ▶ The DRD 7.5 remit includes 'keeping pace with COTs technologies'
- ▶ DAQ evolution in recent years has become increasingly COTs based where possible
  - ▶ Economy of scale, standardisation and upgrade/maintenance benefits

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Innovative/Strategic vision

- ▶ However, choosing to go COTs comes with caveats:
  - ▶ We're (usually) not the target market
  - ▶ It takes time and effort to develop for general purpose technologies
  - ▶ Technology evolution is fast and hard to predict
  - ▶ Choosing the right technology for a given task needs extensive R&D.
- ▶ This is compounded further by dilution of expertise
  - ▶ Every experiment has a few experts in a few TDAQ workflows
  - ▶ Every experiment has a few experts in a few different COTs technologies
  - ▶ These people may not always be the same.

Introducing DAQOverflow

▶ This project aims to:
  ▶ Benchmark common TDAQ algorithms/workflows on existing and new architectures as they become available
  ▶ Develop optimised 'reference' implementations of these algorithms/workflows
  ▶ Maintain a community-led repository of these implementations and their benchmarks
▶ Think `Stack Overflow` for TDAQ development
▶ In doing so, we will serve as an up-to-date repository of information and expertise for TDAQ implementations that the community can use in decision making and design of future experiments

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Planning/Timeframe

- Year 1:
    - Define project structure (Institute PIs + Chair)
    - Regular meetings to determine Figures of Merit (power, efficiency, cost), initial reference implementations for benchmarking, and representative hardware platforms.
    - Initial studies to commence
- Year 2
    - Develop and host a searchable repository for firmware, software and documentation of best-practice implementations
    - expand as performance gains are realised from reference implementations and encourage community input
- Year 3+
    - Revisit reference implementations and benchmarks as new tech comes to market
- Regular meetings rotated through contributing institutes to present progress and comparitive benchmarks

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7.5a's first study: Zero-suppression for the Mu2e DAQ

MANCHESTER
1824
The University of Manchester

DRD 7.5a

Introduction
Strategic Vision
Project Aim
Timeframe
Example study
Contributors
Organisation

▶ Mu2e is an intensity frontier experiment at Fermilab

▶ High-rate Stopping target Monitor reads out a signal amplitude every 3ns with a throughput of 5.3 Gbits/sec. This data needs zero suppressed before further processing.

▶ University of Manchester MPhys students working in the Particle Physics DAQ testbed will develop HLS+VHDL (FPGA), CUDA (GPU) and multithreaded C++ (x86) implementations.

▶ Aim is to determine which implementations are highest throughput and lowest cost.

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DRD 7.5a

Introduction
Strategic Vision
Project Aim
Timeframe
Example study
Contributors
Organisation

- ▶ Several interested groups signed the LoI:
    - ▶ Univ. of Bristol: IPU expertise.
    - ▶ Spain (ICTEA /U. Oviedo IP; IFIC-CSIC/U. Valencia.; CIEMAT (Madrid))
    - ▶ Universite de Geneve
    - ▶ University of Manchester
    - ▶ Josef-Stefan Institute (JSI) Ljubljana
- ▶ Resources and funding under discussion in most cases:
    - ▶ Resources are COTs and readily available in current technology generations in many cases. Do not expect significant expenditure on equipment in 7.5a.
- ▶ Survey commitments still being incorporated- will reach out shortly. Latecomers are welcome.

Organisation

DRD 7.5a

Introduction

Strategic Vision

Project Aim

Timeframe

Example study

Contributors

Organisation

▶ Currently Niko and Conor are guiding the process

▶ Expect committed institutes to nominate a Project Chair at the first meetings

▶ Would expect a fixed-term to allow rotation among participating institutes

▶ Resources + Personpower to be discussed once chair appointed.

▶ Committed and interested institutes should make sure they are on the `ECFA-DRD7-WG7_5-Contributors@cern.ch` or `ECFA-DRD7-WG7_5-Observers@cern.ch` mailing lists

▶ We will arrange a dedicated list for this project shortly.