DRD 7.6a – Common Access to Imaging Technologies

DRD7.6

Strategic Goal

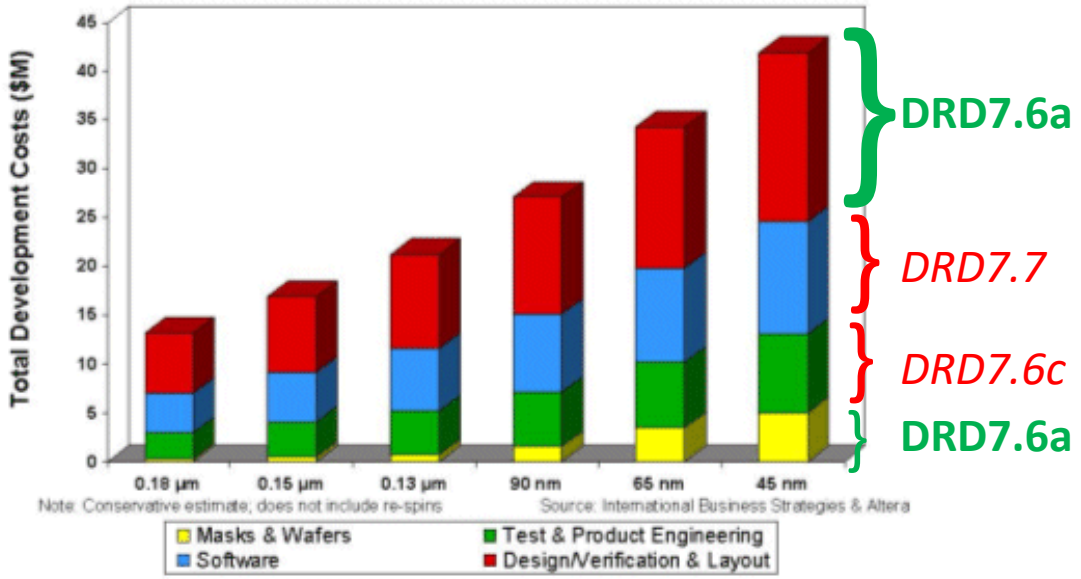
- Provide efficient and affordable access to imaging technologies
- Share and reduce development costs & time
- Requires concentration of resources

Performance Targets

- Shared PDKs, IPs and access to runs
- Chip submissions and test results

Supported Technologies

- TPSCO 65nm (this talk)
- Tower Semiconductor 180nm (this talk)
- LFoundry 110nm (Manuel's talk)



https://www.design-reuse.com/articles/12360/fpgas-and-structured-asics-low-risk-soc-for-the-masses.html

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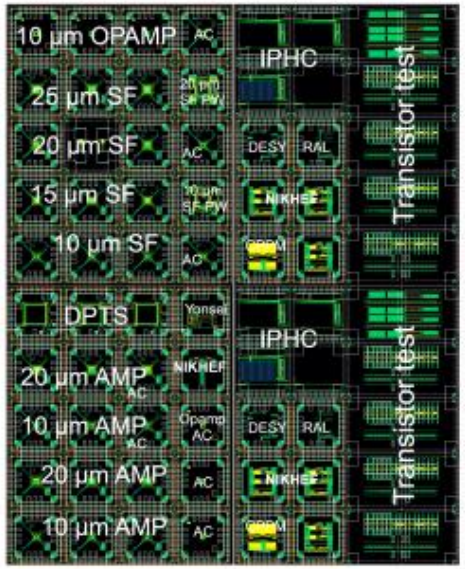
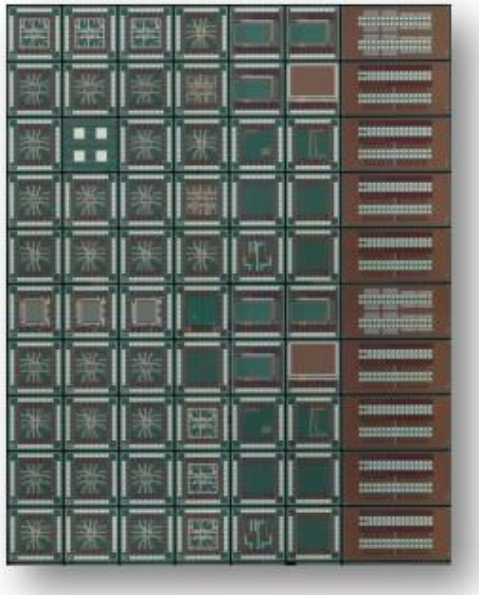
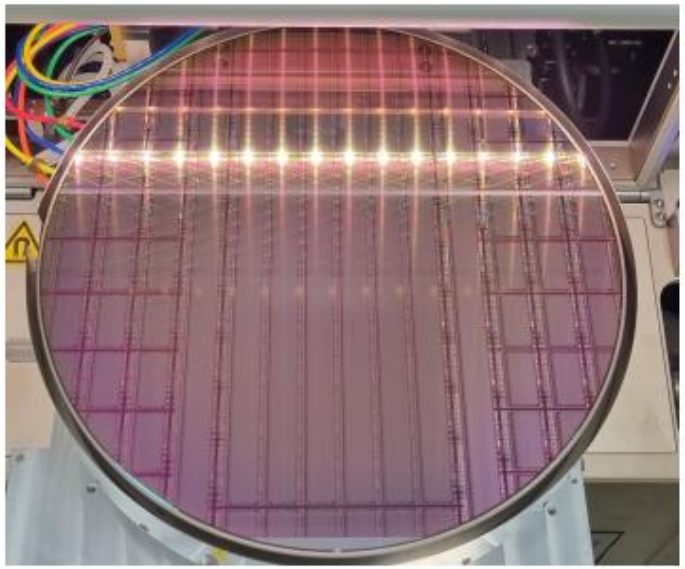
TPSCo 65nm

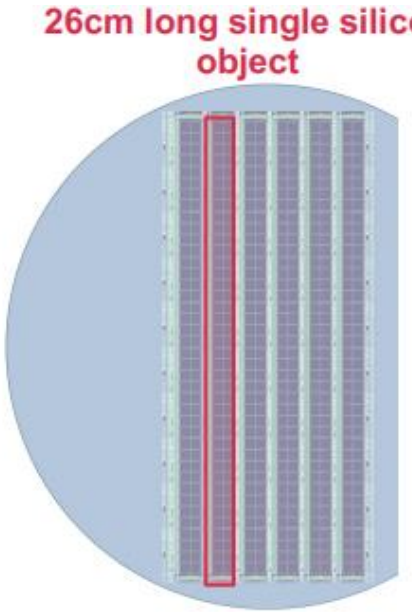
- Currently in use for ALICE ITS3 and EP R&D WP1.2
- Joint runs already carried out – MLR1, ER1
- CERN, IPHC, CPPM, INFN, NIKHEF, STFC, SLAC, DESY, SLAC, Yonsei…





MLR1 (December 2020): 1.5 x 1.5 mm^2 test chips





ER1 (December 2022): stitching

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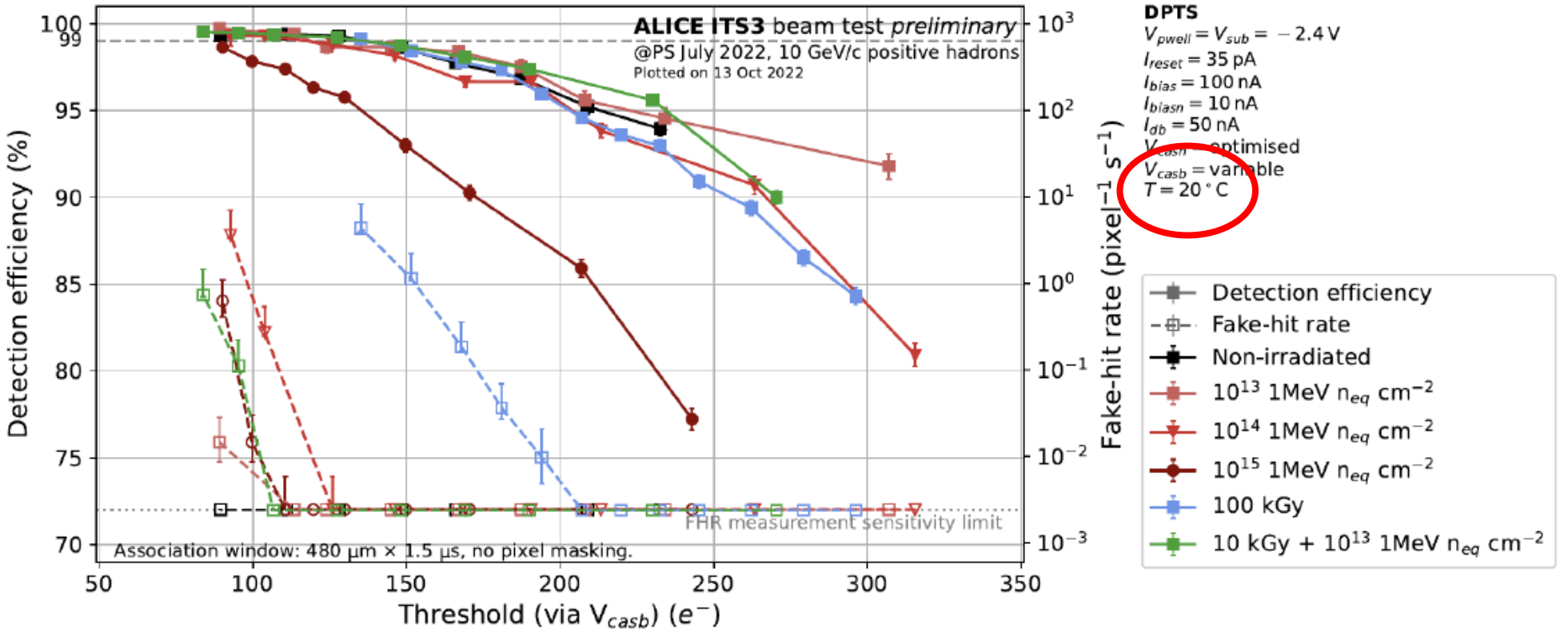
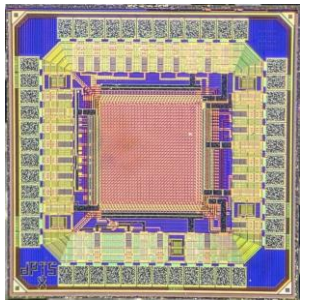
doi: 10.1016/j.nima.2023.168589

TPSCo 65nm : qualified for HEP



DPTS



15 x 15 µm^2 pixel

- Fully efficient after 10^{15} 1MeV n_{eq} cm^{-2}… at room temperature
- Transistor total ionizing dose tolerance doi: 10.1088/1748-0221/18/02/C02036 and SEU in line with other 65 nm technologies
- Many features not yet explored (wafer stacking, special imaging devices…)

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TPSCo 65 nm

- CERN engages to do the support and interface to the foundry
- Common runs foreseen in Q4 2025, Q2 2027, Q4 2028 with financial support at 50 % (excluding wafer stacking)
- Custom DRC rules, more automated reticle assembly and sign-off
- Some IPs already developed, including digital library for DFM.
- More are needed, with preparation for shared use

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Tower Semiconductor 180nm

- >10 years of experience in the community
- Used for:
  - ALPIDE in ALICE ITS2 (10m^2), taking data in the experiment
  - for STREAM, Belle II, GSI…
- CERN has been interface to the foundry and carried out the support so far:
  - intends to concentrate on TPSCo 65 nm
  - discussions underway with IPHC and foundry for support
- Custom DRC rules
- Several IPs developed, need preparation for shared use
- Common runs to be scheduled, could be foreseen in 2025, 2026 and 2028.

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Access

Institute 1

Institute 2

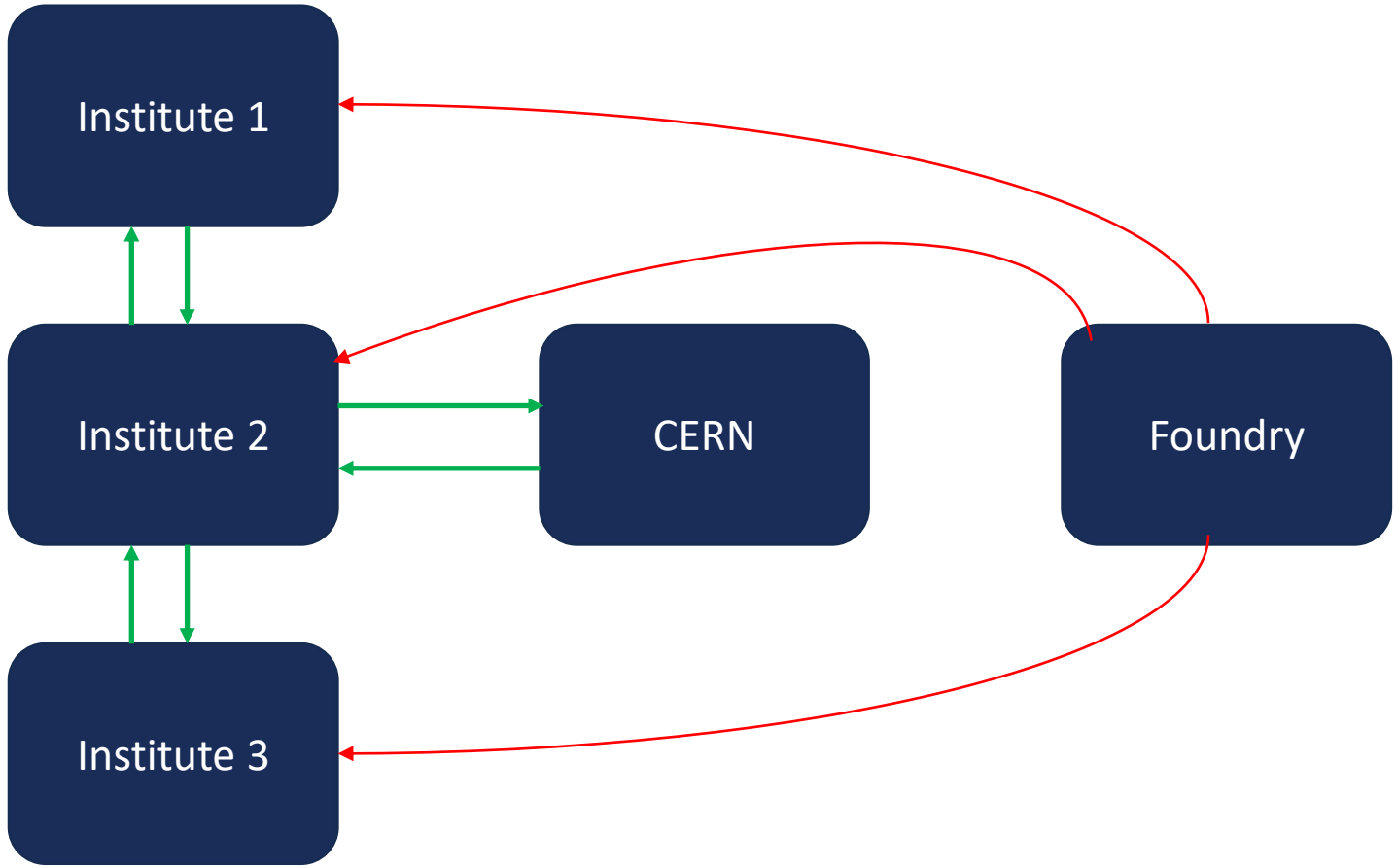
Institute 3

CERN

Foundry

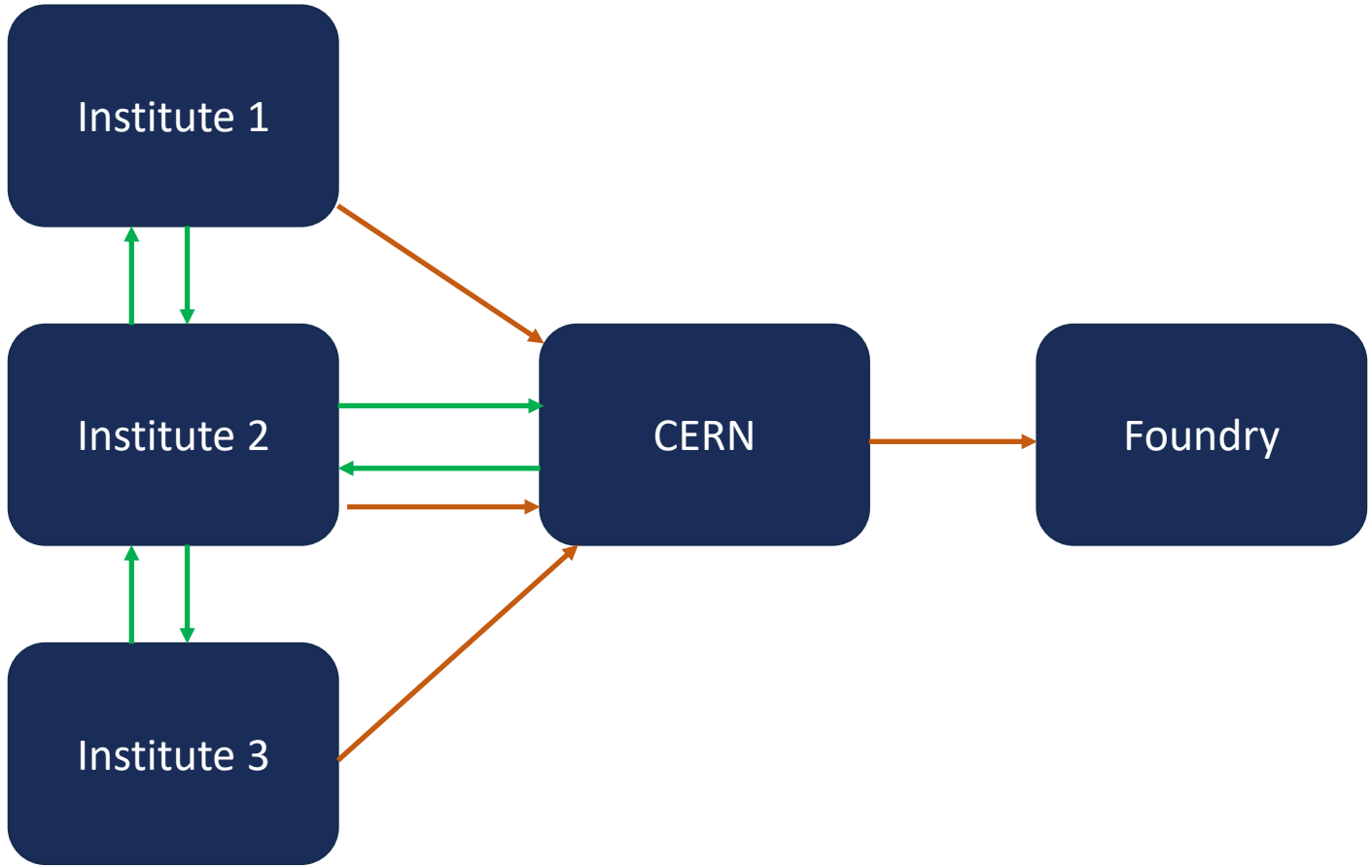
Access

1. Sign NDA (and Cadence Design Share Agreement if applicable). Permits:
   - Sharing of Designs
   - Access to PDK



Access

1. Sign NDA (and Cadence Design Share Agreement if applicable). Permits:
   - Sharing of Designs/Experience
   - Access to PDK
2. Institutes submit to CERN
3. CERN assembles and submits GDSII



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Resources

Technology	Current Resources		Requested Resources	
	FTE/year	Recurrent/year (€)	FTE/year	Recurrent/year (€)
TPSCo 65	8	250k	8	250k + stacking
Tower 180	0.5	20k	4	150k
LF11is	See Manuel's Presentation			

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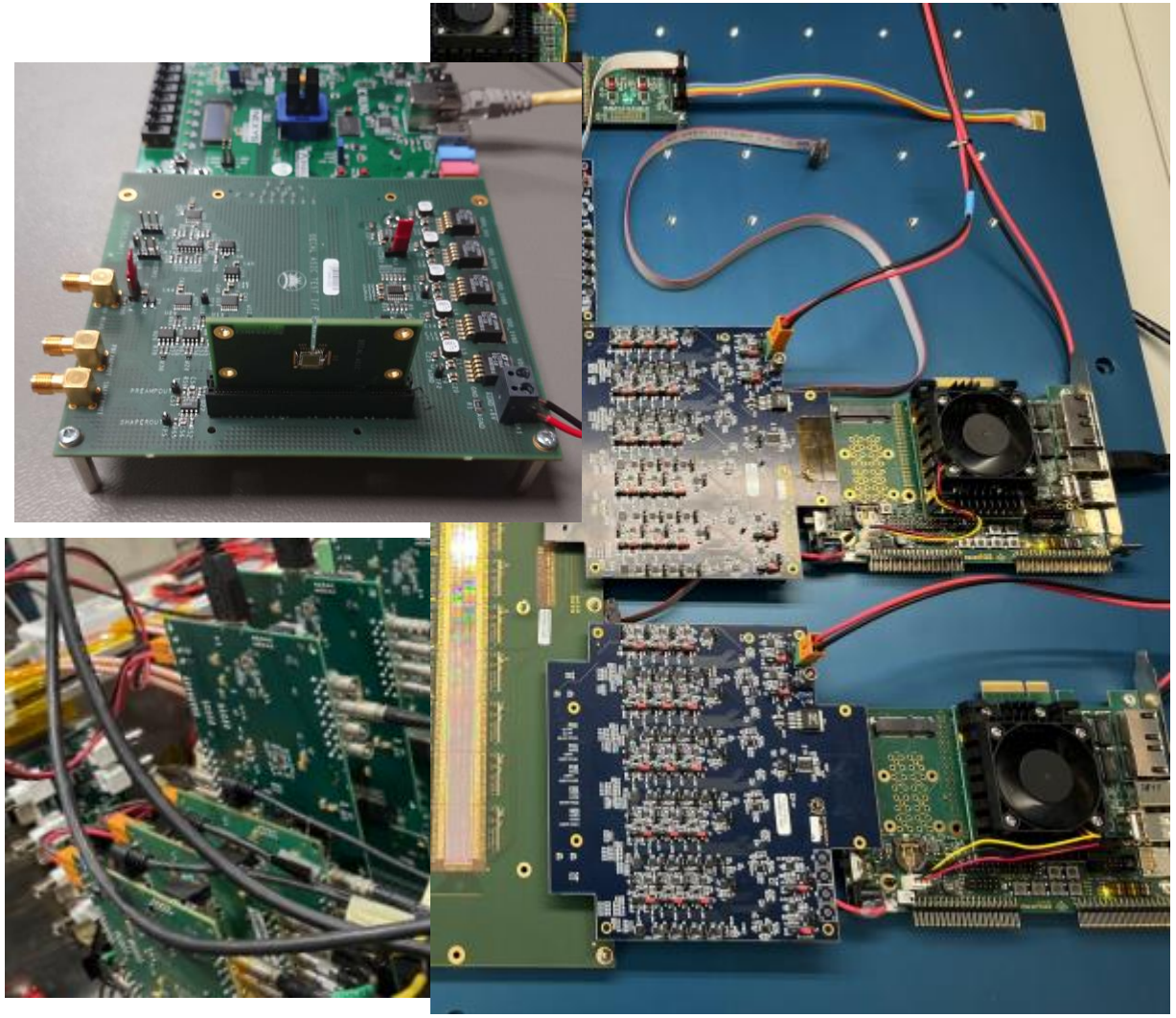
Shared Standardized Test Systems

- Desire to reduce duplication and development time of many test systems
- Render their support manageable (at present usually not sustainable)
- Standardise on chip interfaces
- Originally proposed as DRD7.6c
- Much interest, but no driving institute came forward
- If interested please get in touch – could include in future DRD7 calls



Questions?