Fachhochschule
Dortmund
University of Applied Sciences and Arts

Radiation Hard embedded FPGA – Programmable Logic Array IP

2nd DRD7 Workshop CERN

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Motivation

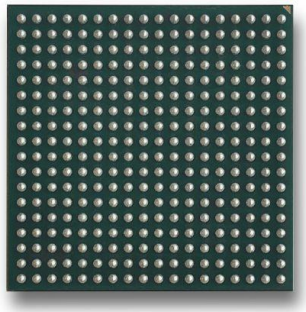
- State of the art chip-design methodology in HEP is based on hardwired non-programmable logic
  - Advantage
    - optimized hardware for specific application case
    - High resource efficiency in terms of power and area consumption
  - Disadvantage
    - no flexibility
    - bug fixes require costly design iteration
    - reuse of chips in different projects and applications difficult
- Embedded FPGA / Programmable Logic Array IP
  - allow reprogramming/reconfiguration of logic for bugfixes and project adaption

Collaboration Partners & Ressources

- Imperial College London, Andrew Rose
  - 1 FTE, 1 MPW ASIC production
- FH Dortmund, Michael Karagounis
  - 0.5 FTE 2024-2027, 1 Mini-Asic MPW production
    - BMBF (applied, evaluation is still pending)
  - 0.5 FTE 2024-2025, 2 Mini-ASIC MPW production

FHDO FPGA Development Background

- Collaborating with Cologne Chip AG in design and characterization of the Gatemate FPGA
  - Design is supported by EU (IPCEI) Important Projects of Common European Interest



Parameter	Detail
Logic Cells	20,480 CPE correspond to * 20,480 8-Input-LUT trees or * 40,960 4-Input-LUT trees with * 40,960 FF/Latches
Block RAM	Total 1,280 Kb 20Kb blocks: 64 40Kb blocks: 32
PLLs	4
SerDes 5 Gb/s	1
I/Os	single-ended: 162 differential: 81 1.2V to 2.5V

  - SRAM based FPGA in Globalfoundries 28 nm CMOS

- radiation characterization in cooperation with CERN, Salvaore Danzeca & Rudy Ferraro
- design and implementation of innovative architectures in TSMC 7 nm

Plans

- FHDO
  - Study OpenFPGA and/or FABulous framework
  - XML-to-Prototype Flow
    - FPGA architecture is described in XML
    - Backend flow creates “production ready” layouts
  - FABulous offers partial reconfiguration
  - Add radiation hardening features
    - Error Detection & Correction in the Configuration Memory
    - Scrubbing
    - Reconfiguration
- Imperial
  - Support either Logic Array IP from industrial partner or develop own IP
  - Develop software & infrastructure for synthesis and mapping of user-code

Status

- Project has been put on hold by steering committee
- Call for participation of additional interested institutes