Common Access to Selected Imaging Technologies and IP Blocks

LFoundry LF11is

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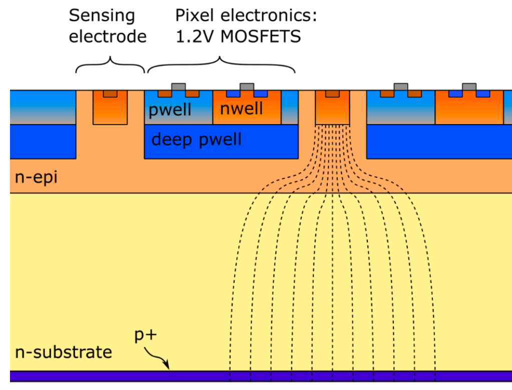
LFoundry LF11is 110nm technology features

- automotive-grade CMOS Image Sensor node
- 1.2V core and 3.3V IO devices
- 6 Aluminum BEOL stack and MiM capacitors
- MPW runs, MLM (Multi Layer Mask) and Full maskset SPW runs with a pilot lot starting 25 wafers
- 1D and 2D stitching options
- use of custom high-resistivity substrates on FSI and/or BSI process flows, including hence the possibility to use a dedicated maskset for backside lithography on thick substrates.

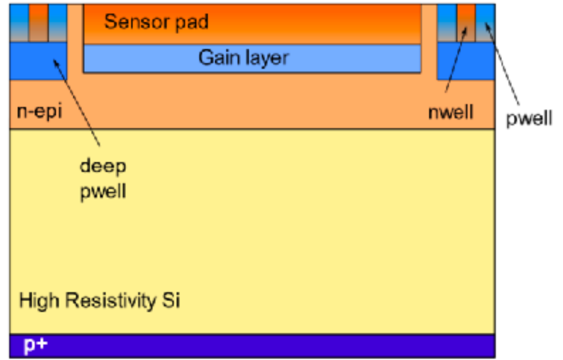
LFoundry LF11is 110nm FD-MAPS Technology

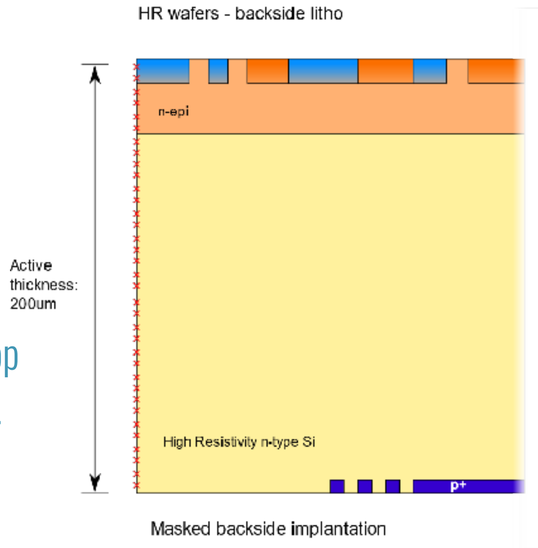
- Sensor technology developed by INFN and LFoundry
- Extensively used in the framework of the INFN project ARCADIA
- Several INFN groups involved on ongoing and future activities employing the LF11is FDMAPS technology, working on sensor technology, CMOS IP design and chip integration, data acquisition systems and characterisation: Torino, Trento, Padova, Milano, Bologna, Perugia, Pavia and Pisa. The ARCADIA budget of ≈ 1.5 MCHF covered so far the cost of 3 full-maskset engineering runs (ER) and hardware for DAQ systems.
- Joint runs (INFN, PSI) so far on – ARCADIA ER-1, ER-2, ER-3 (50 wafers), ER-4 (12 wafers to be started)

ARCADIA LF11is Sensor Concepts and post-processing

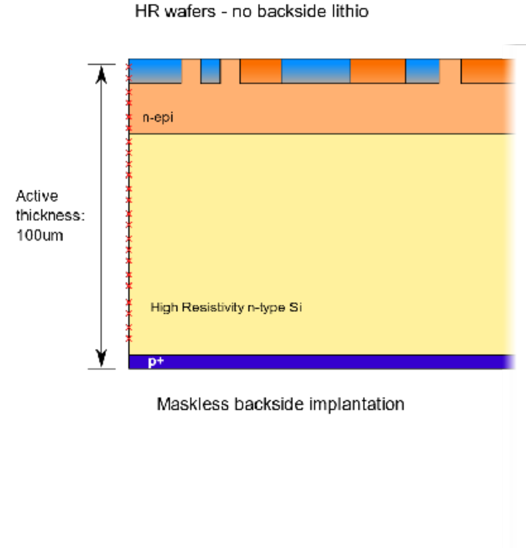


- n-type high resistivity active region + n-epi layer (reduces punch-through current between p+ and deep pwells)
- sensing electrodes can be biased at low voltage (< 1V)
- BSI Reverse-biased junction: depletion grows from back to top
- Option: Fully Depleted PAD sensors with avalanche gain layer

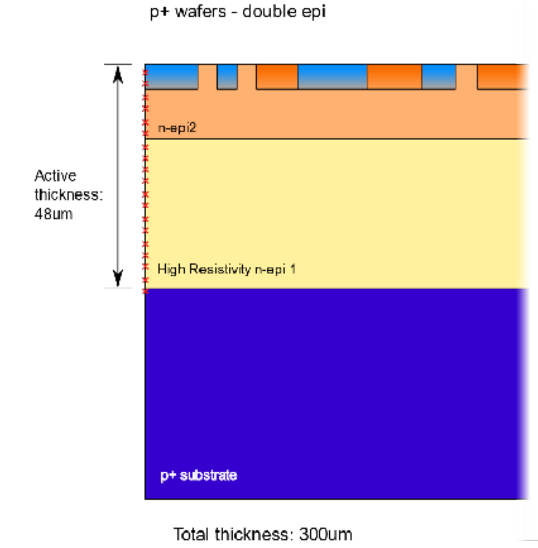




- thinning, lithography, backside p+ implantation and laser annealing, insulator and metal deposition to create backside guardring structures



- thinning, backside p+ implantation and laser annealing, no patterning on backside

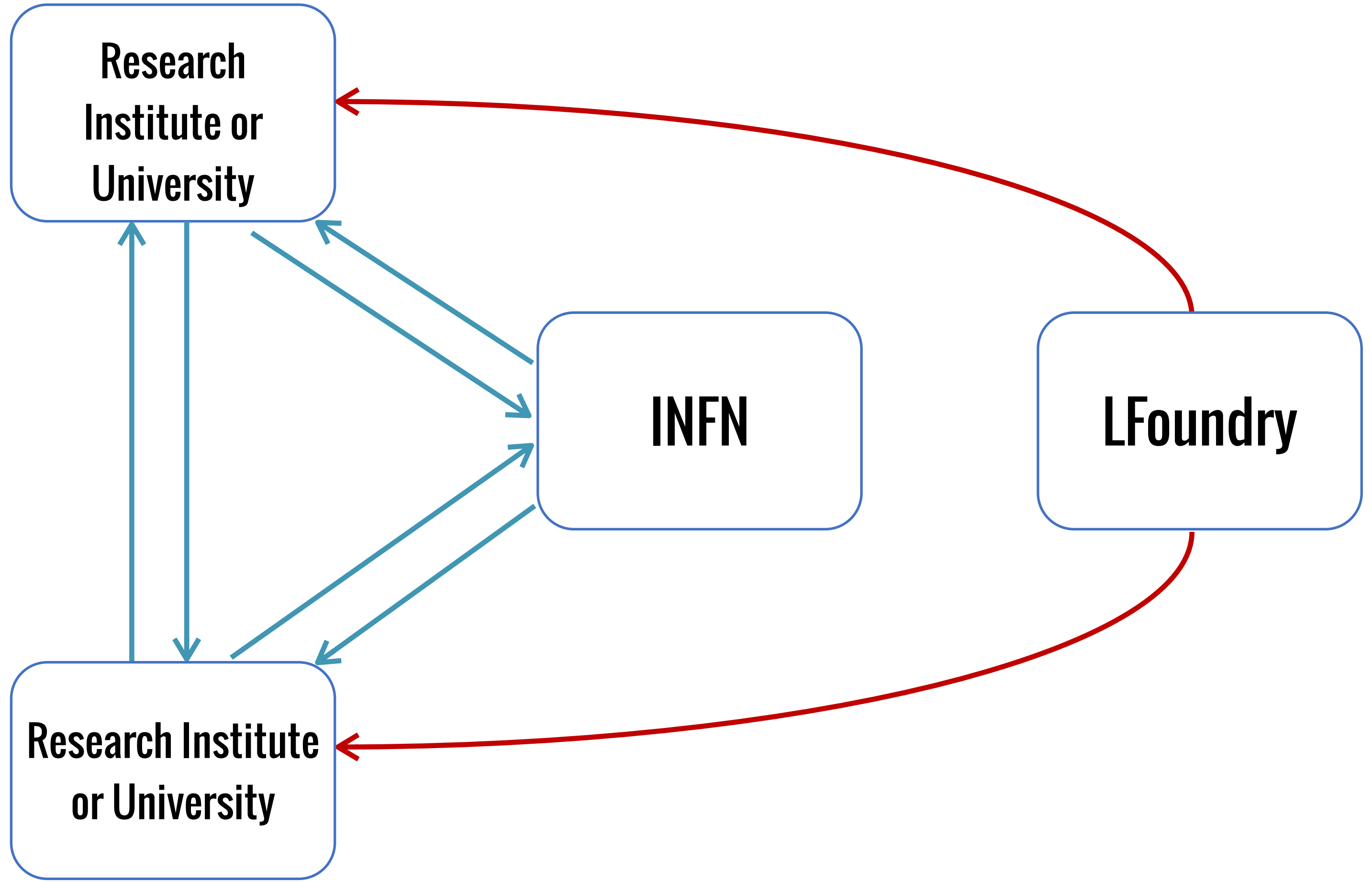


- thinning down to 100μm total thickness on a p+ starting substrate, active thickness below 50μm

Setup Access

1. Contact LFoundry for NDA and access to CMOS LF11is technology:
   - Sharing of Designs
   - Access to (i)PDK

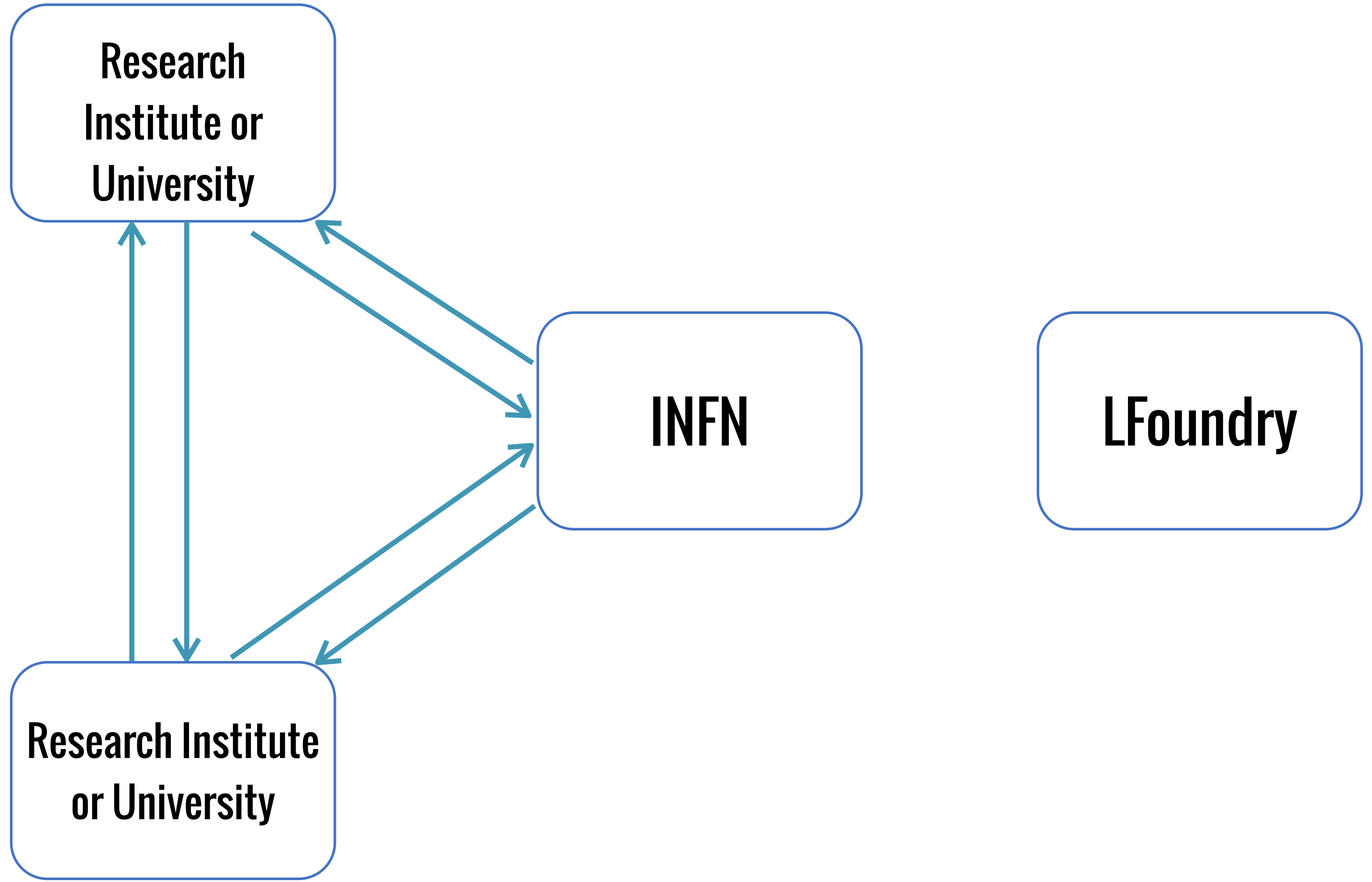
- the design group will be provided by LFoundry with regular access to the CMOS LF11is (i)PDK for the implementation of proprietary architecture and FDMAPS designs.



Sensor specifications

2. The design team and INFN discuss requirements (sensor properties, particle energy, …) and specifications for the physical implementation (pixel floorplan and sensor geometry);

3. INFN generates a library of signal samples for the chosen sensor properties and a dummy layout for the sensor.

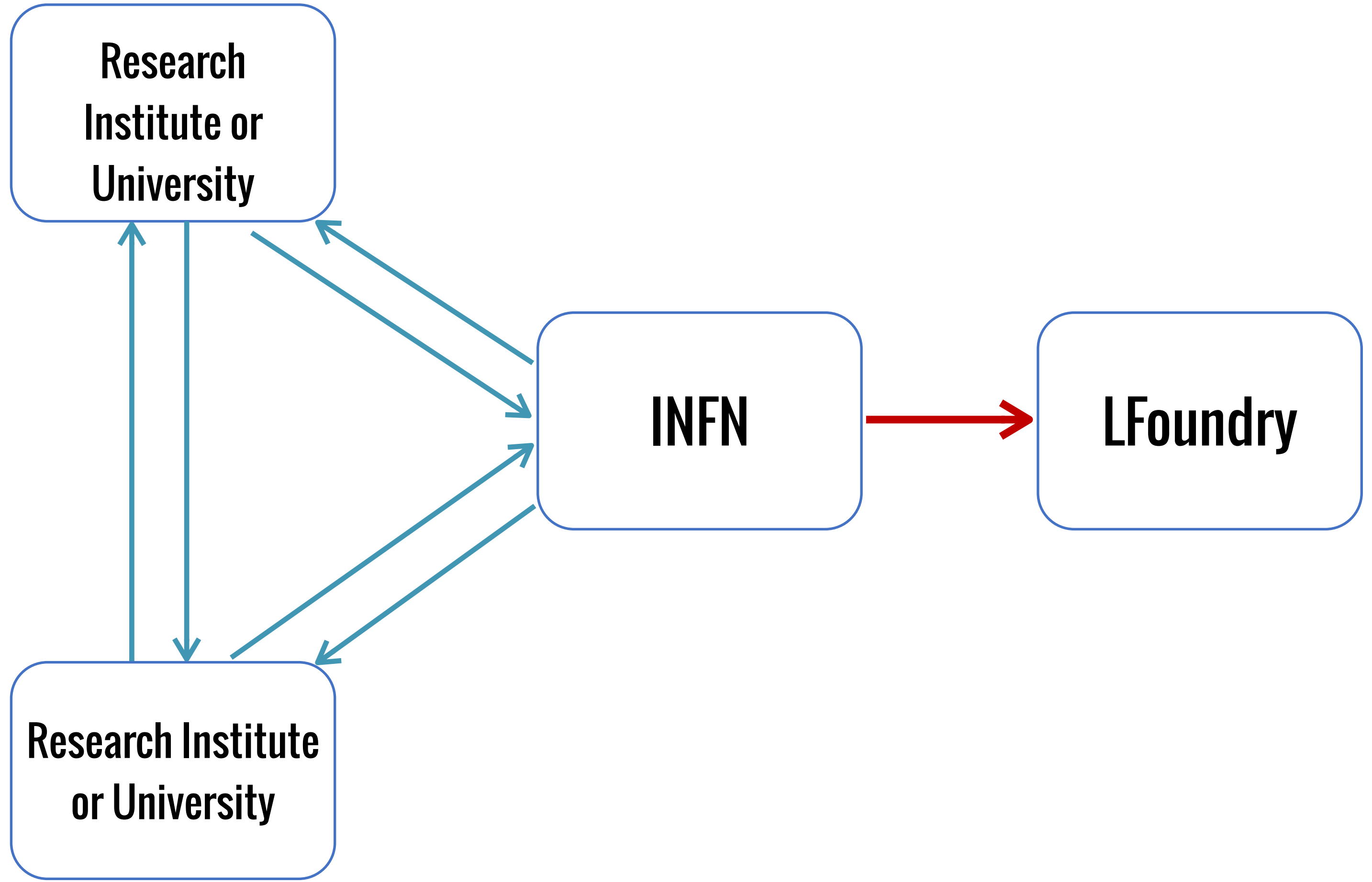


Design and Tapein

4. INFN assists the design team during the design phase, receives a chip floorplan and creates a booking number for the preparation of the reticle floorplan at LFoundry;

5. the final gds2 is sent to INFN for the preparation of the tapeout;

6. INFN handles the integration of the final sensor geometry (FSI and/or BSI), final DRC of the design database.

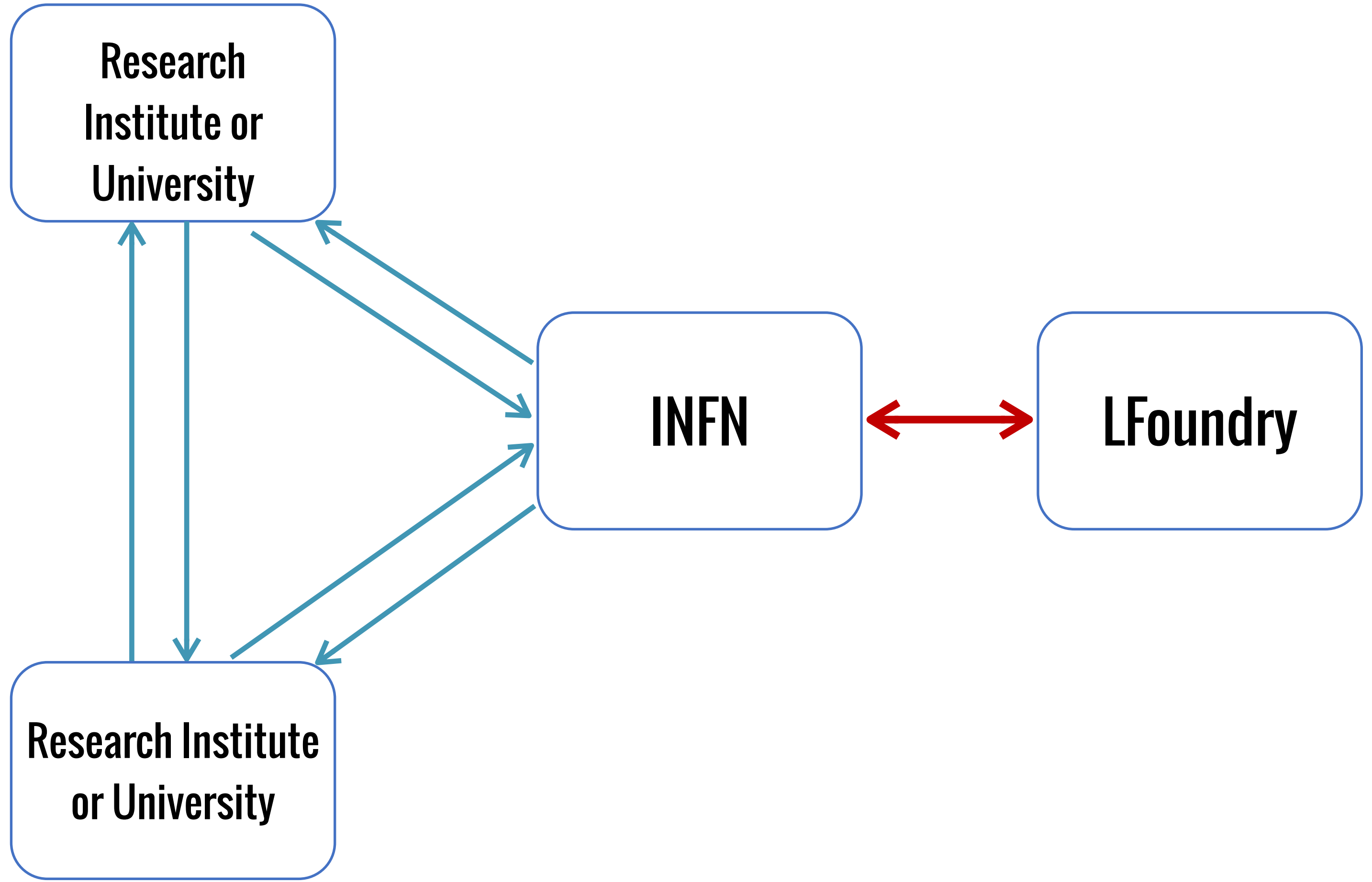


Tapeout and production

1. INFN sends individual final booking numbers to LFoundry for tapeout;

2. post-OPC modifications, if needed, are asked by INFN to the design team;

3. after fab out, INFN receives the wafer lot and coordinates backend services, shipping individual dice to the design teams or full wafers, upon agreement between the participants to the production run.

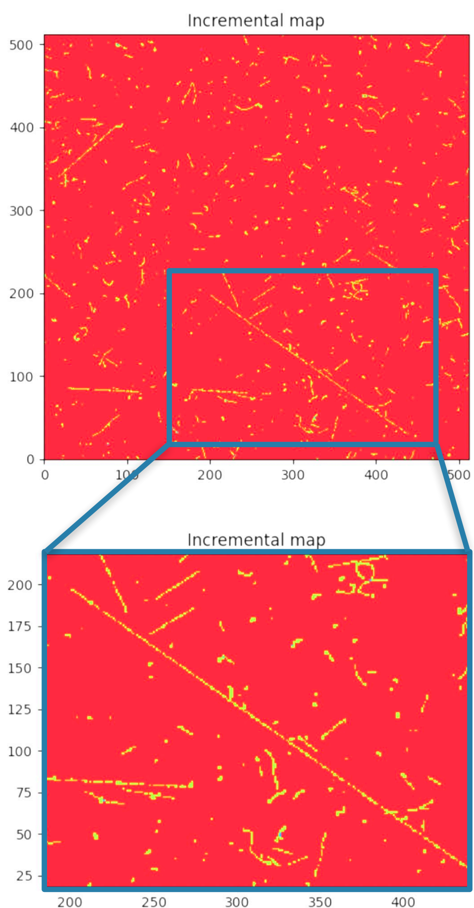


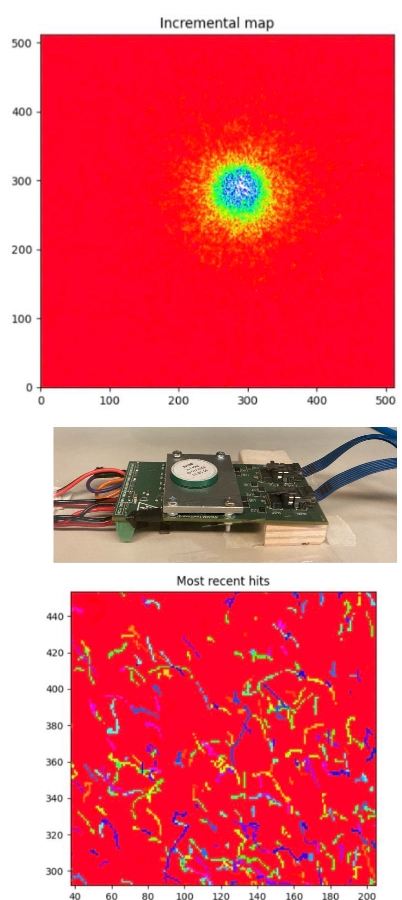
Common Access and Support for joint LF11is production runs

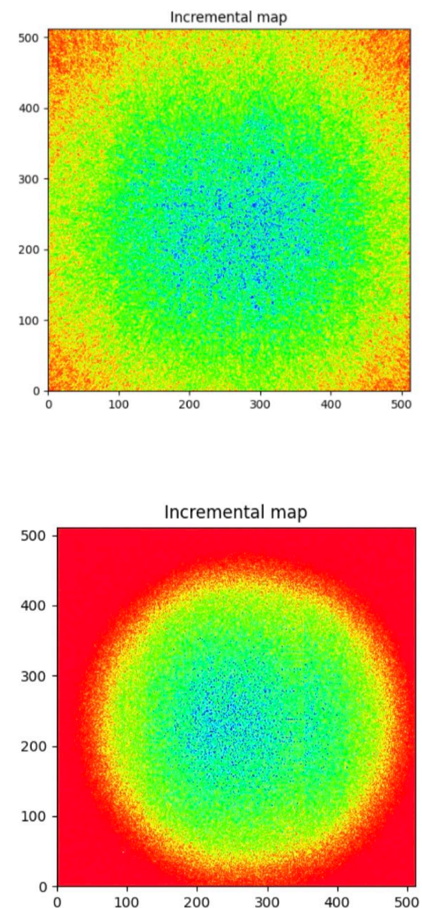
- Possibility to explore multiple wafer splits: n-epi thickness, n-type or p-type starting substrate, substrate resistivity, FSI or BSI process on different wafer thicknesses, use of a gain layer for the implementation of monolithic CMOS LGADs.
- INFN and LFoundry agree on the terms to allow for the participation of third-party design groups to joint LF11is production runs, enabling straightforward and low-risk ramp-up of the R&D on FDMAPS using LF11is technology for new design teams.
- Silicon-proven IP available (Serialisers, c-LVDS Transceivers, bandgap/LDO, SPI, DAC/ADCs).
- Funding secured for 2 SPW runs in early 2025 and 2026, a third common run could be scheduled and supported.

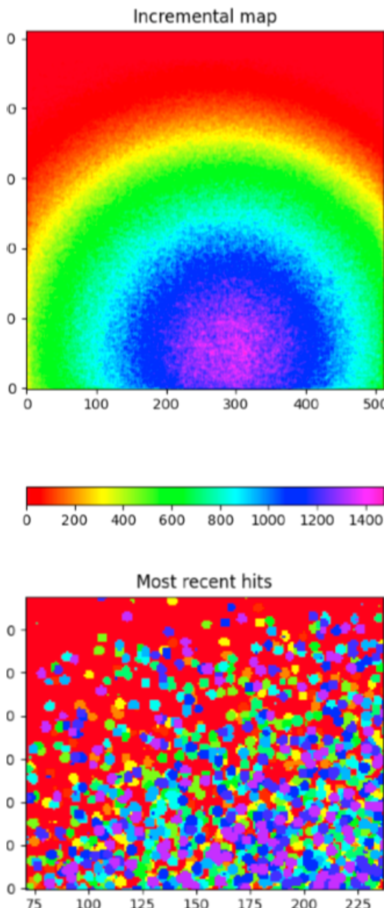
Thank you for your time!

DRD7.6 – Complex Imaging ASICs and Technologies









- Pixel size 25 µm x 25 µm, Matrix core 512 x 512
- Triggerless data-driven readout, clockless matrix
- Full-chip power density (measured) 10 mW/cm^2