HSF Reconstruction and Software Trigger Working Group

Towards Zero-Waste Computing with Performance Engineering

A Practical Example from Track Reconstruction

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Introduction – Clustering

- $\cdot\,$ Pixel detectors give deposition per pixel
- One particle may activate many pixels
- But no **cluster information** (let alone particle information) can be recorded
- Computing clusters is one of the first steps in reconstruction



Graphic by Uchendu Nwachukwu

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Introduction - Connected Component Labelling

- In graph theory and computer vision, known as connected component labelling (CCL)
 - You might recognise its greatest hit: the Microsoft Paint Fill tool
- Usually applied to **graph** or **dense image** data
- Vast body of knowledge on algorithms across all sorts of devices



- CCL problems in **HEP** are interesting because they are...
 - Extremely sparse (~2% N.Z.)
 - Across disjoint images (~2000 in ATLAS ID)
- Sparse problems are **less common** and there is **less work on algorithm design**
- **SparseCCL** was developed for HEP applications at CERN and Sorbonne University by A. Hennequin et al. (doi:10.1109/DASIP48288.2019.9049184)

Flavour	Positioning	Connection	
Dense	Implicit	Implicit	
Sparse	Explicit	Implicit	
Graph	N.A.	Explicit	

- SparseCCL runs sequentially over an image
 - We'll assume that SparseCCL is efficient
- How can we now run this efficiently on multi-core systems?
 - In other words: where is the parallelism?

SparseCCL: Connected Components Labeling and Analysis for sparse images

Arthur Hennequin^{1,2}, Ben Couturier², Vladimir V, Gligorov³, Lionel Lacassagne¹

LIPS. Sotherne Université, CNRS, Paris, France ²CERN, Switzerland ³LPNHE Sochoone Université Paris Diderot Sochoone Paris Cité CNRS/IN7P3 Paris France email: other hennemin@lin6 fr. lionel hemosarre@lin6 fr

Abstract-Connected components labeling and analysis for to be inefficient. The dense structure is replaced by various dense images have been extensively studied on a wide range flavourn of lists that hold the non-zero value and specialized of architectures. Some applications, like particles detectors in High Energy Physics, need to analyse many small and sparse images at high throughput. Because they process all pixels of the image, classic algorithms for dense images are inefficient on the same phenomenon happens: even if CCA algorithms are the many, taken address this individual in a new yory fast they are individual to closer and label matrices of sparse data. We address this methodency by introducing a new very last, they are inefficient to algorithm specifically designed for sparse images. We show that hits with a density around 0.5% we can further improve this snarse alregisting by specializing it for the data input format, avoiding a decoding step and promultiple uisels at once. A benchmark on Intel and AMD CPUs shows that the absorbing is from $\times 1.6$ to $\times 2.5$ faster on sporte I. INTRODUCTION

In computer vision. Connected Component labeline (CCL)

is a common and wide spread algorithm. Its purpose is to assign a unique label to each group of connected pixels. These

used for higher level tasks, like tracking, motion detection or

optical character recognition. First instances of this algorithm

the real impact positions

and FPGAs [13].

Connected Component Analysis (CCA).

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or dedicated algorithms are designed to process these data efficiently. In the case of tracking hits on detectors' sensors

The Section II presents some classic connected components labeling algorithms. Section III introduces a new algorithm for connected components labeling of sparse images and its specialization for the pattern recognition of CERN's LHCb experiment. Finally, in Section IV, we evaluate this new algorithm and compare it to state-of-the-art.

II. CLASSIC ALCORITING FOR DENSE IMAGES

In this section, we present three classes of connected groups of pixels, called Connected Components (CC), are then components labeling algorithms

A. One component of a time

were proposed by pioneers like Rosenfeld [20] or Haralick [8]. In this first class of algorithm, we rencess one connected In High Energy Physics (HEP), CCL is used for tracking component at a time. The image is scanned one time and, matricles by labeling hits on the detectory sensors to estruct. For every foreground nised ecountered a traversal of the connected communent is done to lobel all the nixels. This alreerithm A CCL alregister by itself, only prevides the association of and its variants are often called thead 60 or semetimes cool 60. pixels, this is why it is followed by an analysis algorithm. The The traversal can be done using a stack in depth-first order or purpose of the analysis is to compute features of each CC, like a more, in breadth-feat order, Irrelementations of alcorithms the bounding how or the first statistical moments in order to of this class are found in [21] and [1]. This abarithm can be commute the center of arasity. If naive algorithm perform the optimized by only adding, on top of the stack, the branching labeling first and then the analysis, the optimized algorithms pixels - ie, the pixels that have more than one non-visited do the analysis during the labeling. These algorithms are called neighbour - and directly processing the others. Doing so. we avoid a store and a load for these pixels. If the image Most of CCL algorithms used to be sequential ones, is sparse and if we have a list of pixel coordinates, we can developed on single-core processors [9] [4]. Recently, new directly start at known pixel positions avoiding the grad of parallel algorithms were developed for multi-core processors many background nisels. However, this does not meyere the [16] [7], SIMD processors [22] [14] [10], GPUs [18] [11] test of every pixel on the contour of the connected component and it adds the cost of removing pixels from the list. An implementation of this algorithm specialized for the LHCb These algorithms are very efficient for natural images but experiment is described in [3] not for very low density images (very few pixels set to one).

B. Denative algorithms

The case considered here is similar to matrix alarbes. The accord class was introduced by Maralick DI. Each nixed When a matrix has very few non-zero value the closeled is initialized with a unione temporary label then this label dense structure and the classical dense algorithms turn out is propagated to the pixel's neighbors using local minimum

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 - In other words: where is the parallelism?
- We have parallelism **between images (modules)**...
- and between events!

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Zero Waste Computing – SparseCCL for GPU

- Now, how can we do clustering on graphics programming units (GPUs)?
- Get a summer / technical / doctoral student to implement SparseCCL in CUDA or HIP!



Zero Waste Computing – SparseCCL for GPU

- Now, how can we do clustering on graphics programming units (GPUs)?
- Get a summer / technical / doctoral student to implement SparseCCL in CUDA or HIP!
- $\cdot\,$ It turns out this would be a doomed effort
- $\cdot\,$ But we know this before we write any code
 - Analyse the properties of the software...
 - ...as well as the hardware...
 - ...and predict how they would interact!



Performance engineering gives us the tools to reduce waste of energy, compute time, *and* human resources

- GPGPUs are designed to execute **similar tasks** in a **massively parallel** fashion
- This is achieved by sharing a small amount of control between a large amount of compute
- This makes individual "cores" less independent: lock-step execution!
- Beware NVIDIA marketing!



Differences in hardware require us to think differently about efficiency and zero-waste!

CPUs have...

- Complex pipelines & many ports
- Very large global memories
- Complex cache hierarchies; etc.

GPUs have...

- Large numbers of dependent "cores"
- Very-high-speed shared memories
- Coalesced load-store logic; etc.

...so we must think (more) about...

- Instruction-level parallelism
- Coarse task-level parallelism
- Temporal data locality; etc.

- Thread imbalance & divergence
- Fine task-level parallelism
- Data access strides; etc.

SparseCCL for GPU – Introduction

- How do we expose parallelism in **SparseCCL** for **GPUs**?
- Recall the design of GPUs: many **small** cores that share control



SparseCCL for GPU – Introduction

- How do we expose parallelism in **SparseCCL** for **GPUs**?
- Recall the design of GPUs: many **small** cores that share control
- Roughly two options: map each module onto one **thread**...
- \cdot ...or onto one thread group



SparseCCL for GPU - Per-Thread

- Mapping **each module to one thread** feels natural
- ...similar to how we parallelised for CPU!



SparseCCL for GPU - Per-Thread

- Mapping **each module to one thread** feels natural
- ...similar to how we parallelised for CPU!
- But modules have different hit counts!
- This leads to **imbalance**: threads waiting (but still consuming power)
- Turns out we can also understand this behaviour through statistical **models**!



SparseCCL for GPU – Per-Group

- We can also map one module onto a group of threads
- This is a powerful technique known as thread refinement (opp. coarsening)

 $\overrightarrow{t_1}$ $\overrightarrow{t_2}$ $\overrightarrow{t_3}$ $\overrightarrow{t_4}$ $\overrightarrow{t_5}$ $\overrightarrow{t_6}$ $\overrightarrow{t_7}$ $\overrightarrow{t_8}$ $\overrightarrow{t_9}$ $\overrightarrow{t_{10}}$ $\overrightarrow{t_{11}}$ $\overrightarrow{t_{12}}$ $\overrightarrow{t_{13}}$ $\overrightarrow{t_{14}}$ $\overrightarrow{t_{15}}$ t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10} t_{11} t_{12} t_{13} t_{14} t_{15} wo t_0 t_1 t_2 t_3 t7 t8 t9 t10 t11 t12 t13 t14 t15 ts

SparseCCL for GPU – Per-Group

- We can also map one module onto a group of threads
- This is a powerful technique known as thread refinement (opp. coarsening)
- Does it actually help us here? Need to parallelise work over 32/64 threads
- Puts us in the **exact same problem as on CPU**: SparseCCL is sequential!

 $\widehat{t_2}$ $\widehat{t_3}$ $\widehat{t_4}$ $\widehat{t_5}$ $\widehat{t_6}$ $\widehat{t_7}$ $\widehat{t_8}$ $\widehat{t_9}$ $\widehat{t_{10}}$ $\widehat{t_{11}}$ $\widehat{t_{12}}$ $\widehat{t_{13}}$ $\widehat{t_{14}}$ $\widehat{t_{15}}$ t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 to t10 t11 t12 t13 t14 t15 wo ti to ts to t10 t11 t12 t13 t14 t15

- To recap: we have **abstractly examined** two implementations:
 - Thread-per-module mapping suffers from huge imbalance
 - Group-per-module mapping suffers from **insufficient parallelism**
- Both implementations would be **wasteful**: **slow and power-inefficient**
- Implementing these kernels would take dozens of **person-hours**
- Performance engineering **from step one** saves us from wasting resources: *predictive power*

- Performance engineering also allows us to **define requirements** which helps us to **find or design solutions**
- Prescriptive power!
- In this case, requirement for shared memory, massive parallelism, and support for sparseness

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- We eventually settled on a graph algorithm: FastSV
- **Reduction** of sparse problem to a graph problem
 - Motivated by cost modelling
- Optimised for GPU execution using shared memory, occupancy optimisation, thread coarsening, load balancing, etc.

FastSV: A Distributed-Memory Connected Component Algorithm with Fast Convergence				
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- Our solution perform up to **twice as well** as on an equivalent CPU
- **Descriptive tools** can now tell us what is still bottlenecking our code
 - In this case: NVIDIA Nsight Compute
- Approximately **50%** utilisation of resources (=50% waste!)

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- GPU Speed Of Light Throughput			
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SM: Inst Executed Pipe Uniform [1;]			

- It remains to be seen if we will reach the **speed of light** for this kernel
- Important to posit requirements and goals in context (Amdahl's law)
- To improve, we **need** to apply **models**, **analyses**, and **techniques** from the PE domain!

Compute (SM) Throughput [%]	45.98	
Memory Throughput [%]	36.22	
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Issued Warp Per Scheduler	0.53	
No Eligible [%] 47.12 One or More Eligible [%] 52.88		
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- **Performance engineering** gives us a **toolbox** to **predict** performance, **prescribe** optimisation, and **describe behaviour**
- Many non-functional metrics:
 - Running time: more science in less time
 - Power usage: more science with reduced environmental impact
 - Monetary cost: more travel budget
 - · Implementation time: more human resources to do science
- Requires us to think carefully and from the beginning about software and hardware