The Norwegian ALICE Program - Instrumentation

Jørgen Lien (USN)
on behalf of ALICE Norway,
NorCC 2024 Workshop

UNIVERSITAS OSLOENSIS MDCCCXI

UNIVERSITAS BERGENSIS

Høgskulen
på Vestlandet

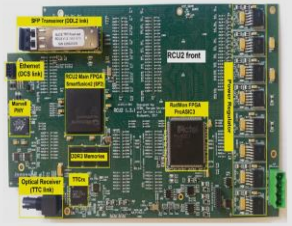
Universitetet
i Sørøst-Norge

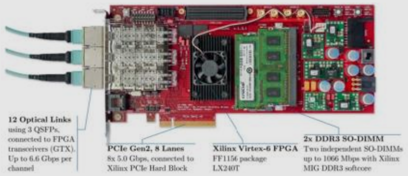
2010-2012 2015-2018 2022-2025 2029-2032 2035-2037

Run 1 | LS1 | Run 2 | LS2 | Run 3 | LS3 | Run 4 | LS4 | Run 5 | LS5 | Run 6

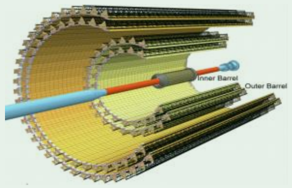
ALICE 1 | phase I upg | ALICE 2 | Phase IIb Upg | ALICE 3

PHOS
TPC RCU & RCU2
HLT

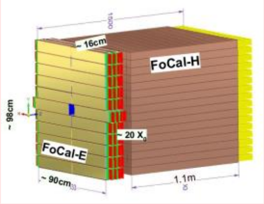




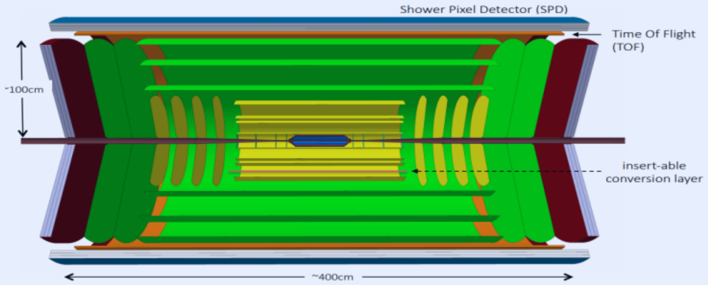
ITS2
TPC



FOCAL
ITS3

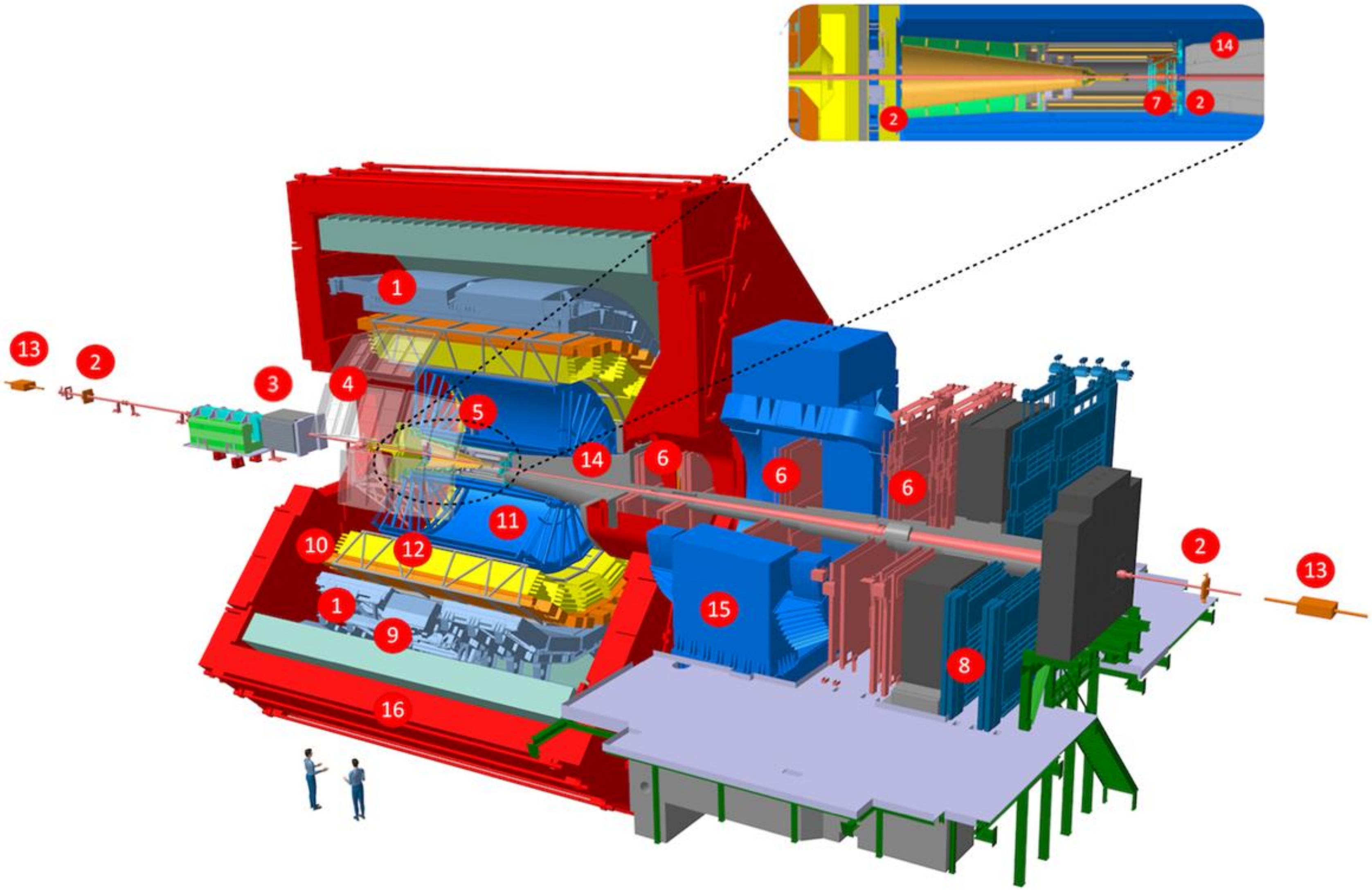


ALICE3



Future Run4

2029 → 2030 → 2031 → 2032



1 **EMCAL |** Electromagnetic Calorimeter

2 **FIT |** Fast Interaction Trigger

3 **FoCal |** Forward Calorimeter
(in front of compensator magnet)

4 **HMPID|** High Momentum Particle Identification Detector

5 **ITS|** Inner Tracking System

6 **MCH|** Muon Tracking Chambers

7 **MFT|** Muon Forward Tracker

8 **MID|** Muon Identifier

9 **PHOS/CPV|** Photon Spectrometer

10 **TOF|** Time Of Flight

11 **TPC|** Time Projection Chamber

12 **TRD|** Transition Radiation Detector

13 **ZDC|** Zero Degree Calorimeter

14 **Absorber**

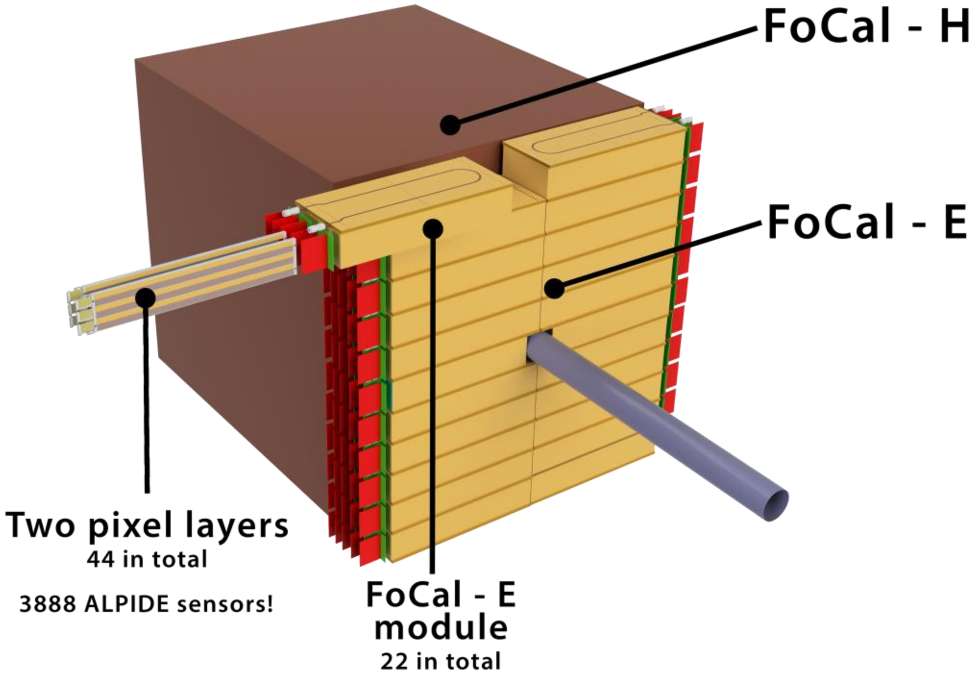
15 **Dipole Magnet**

16 **L3 Magnet**

Forward Calorimeter

Aim:

Exploring non-linear QCD in regime of saturated gluons at low Bjorken-x and constrain nPDFs



Method:

Forward Calorimeter 7m from the interaction point in ALICE

Electromagnetic Calorimeter
Highly granular Si-W layers

- **18** Si pads layers
  lower granularity
- **2** MAPS pixels layers
  higher granularity

Hadronic
Scintillating fibers embedded in Cu tubes
~7t of tubes and 200km of fiber

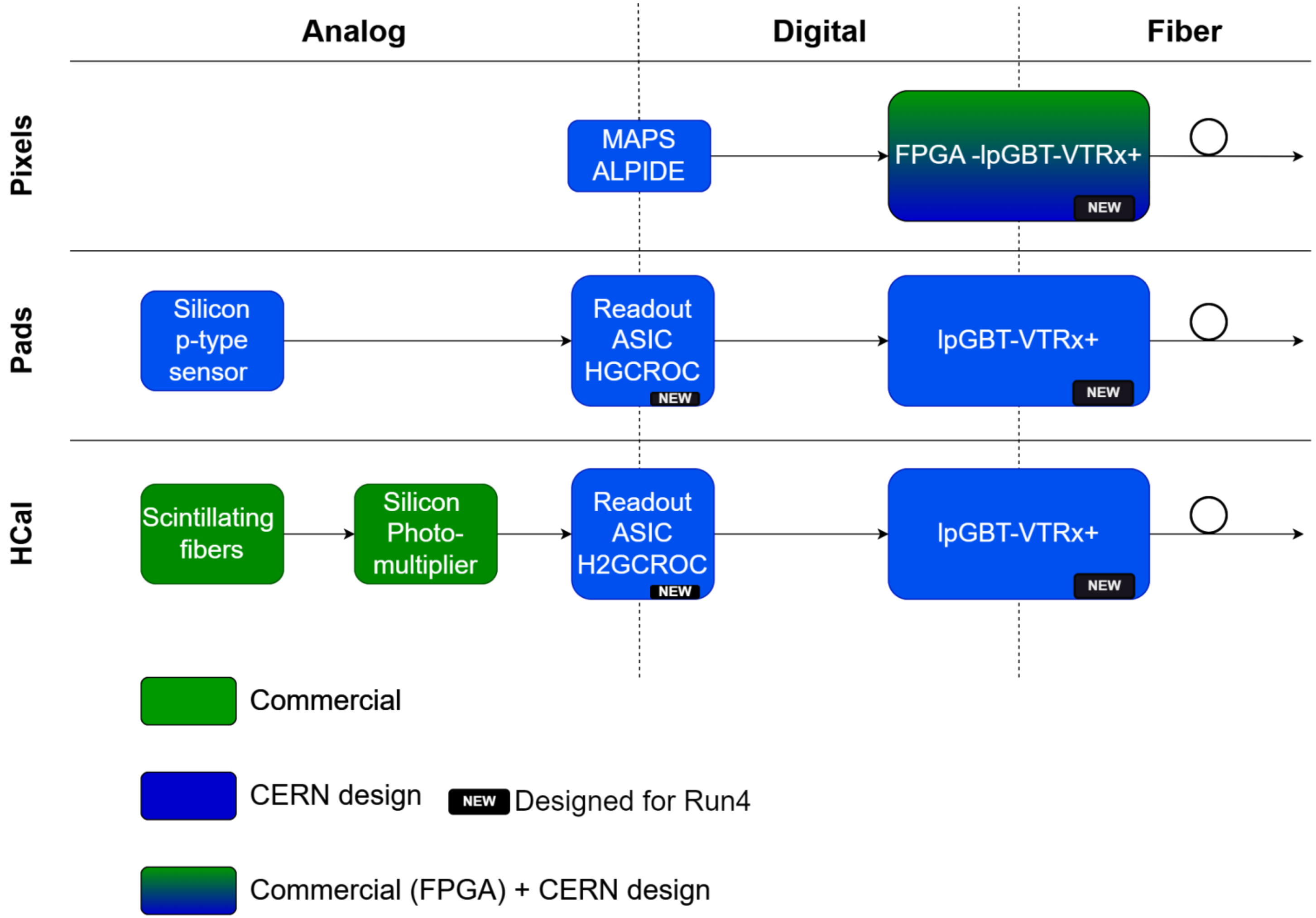
FoCal slides by Tea Bodova

Forward Calorimeter – frontend and readout

3888 ALPIDES in 2 layers

1944 pads in 18 layers

~10 000 channels



Analog | Digital | Fiber

Pixels: MAPS ALPIDE → FPGA -lpGBT-VTRx+ (NEW) → ○ →

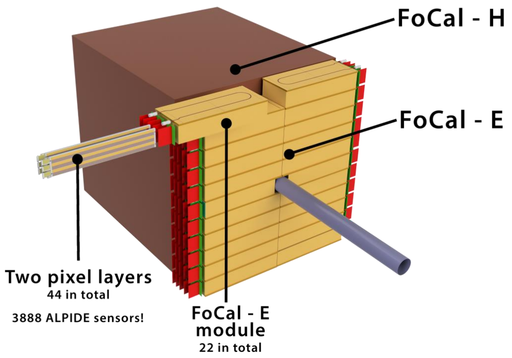
Pads: Silicon p-type sensor → Readout ASIC HGCROC (NEW) → lpGBT-VTRx+ (NEW) → ○ →

HCal: Scintillating fibers → Silicon Photo-multiplier → Readout ASIC H2GCROC (NEW) → lpGBT-VTRx+ (NEW) → ○ →

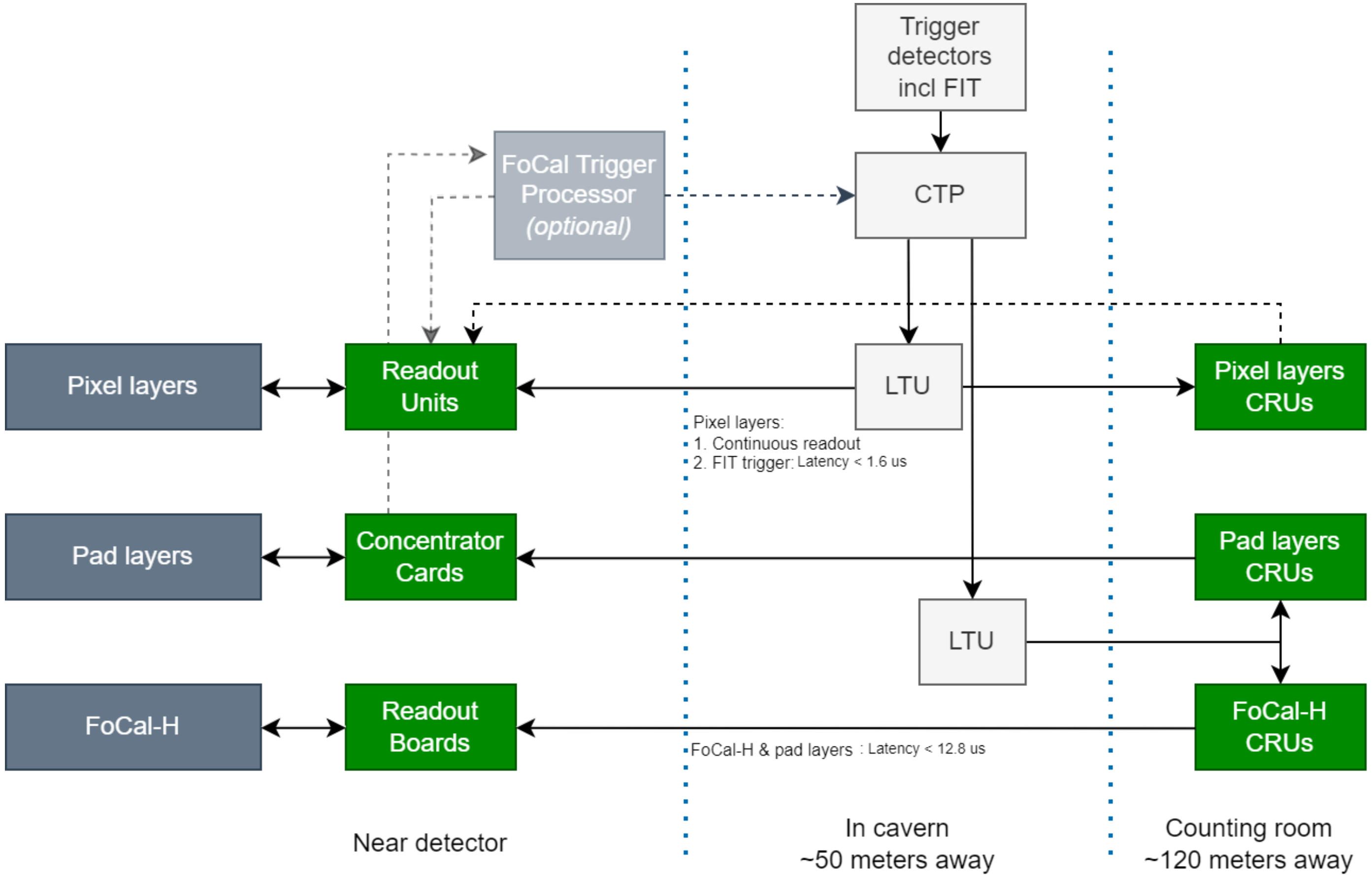
🟩 Commercial

🟦 CERN design   NEW Designed for Run4

▨ Commercial (FPGA) + CERN design



Forward Calorimeter – system level



Trigger detectors incl FIT

FoCal Trigger Processor *(optional)*

CTP

Pixel layers

Readout Units

LTU

Pixel layers CRUs

Pixel layers:
1. Continuous readout
2. FIT trigger: Latency < 1.6 us

Pad layers

Concentrator Cards

Pad layers CRUs

LTU

FoCal-H

Readout Boards

FoCal-H CRUs

FoCal-H & pad layers : Latency < 12.8 us

Near detector

In cavern
~50 meters away

Counting room
~120 meters away

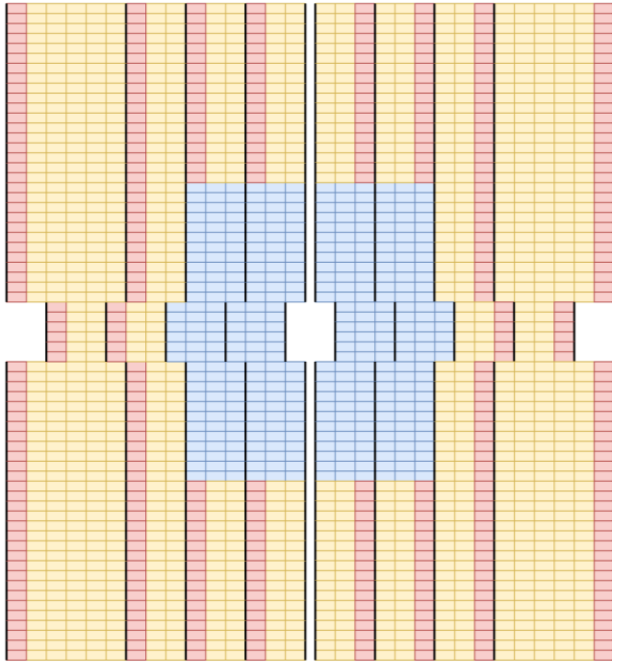
Readout Unit = FPGA + lpGBT + VTRX+
(+ bPOL48V on separate Power Boards)

Concentrator Cards = HGCROC + lpGBT + VTRX+
(+ bPOL48V)

Readout Boards = HGCROC + lpGBT + VTRX+
(+ bPOL48V)

Forward Calorimeter – pixels – FEE layers

One full pixel layer

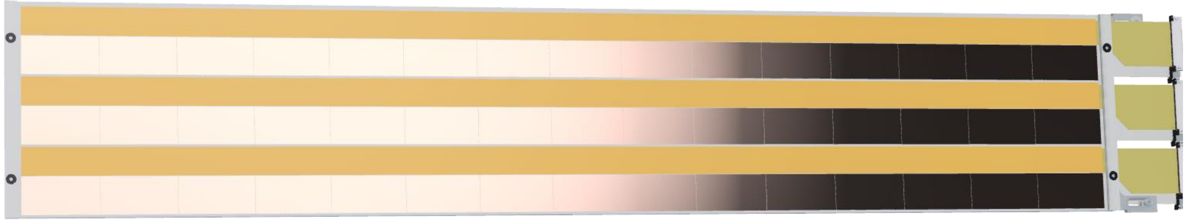


Note: Pixels layer is not to scale

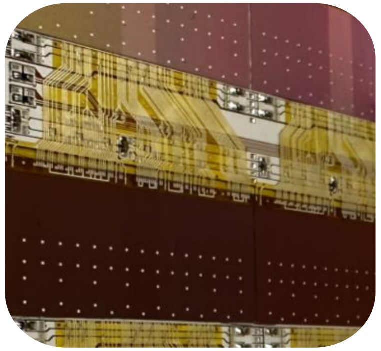
ALPIDE modes:

- 🟦 Inner Barrel
- 🟥 Outer Barrel Master
- 🟨 Outer Barrel Slave

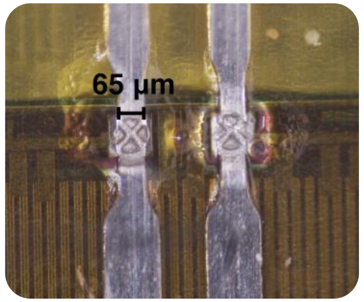
One full pixel module-layer



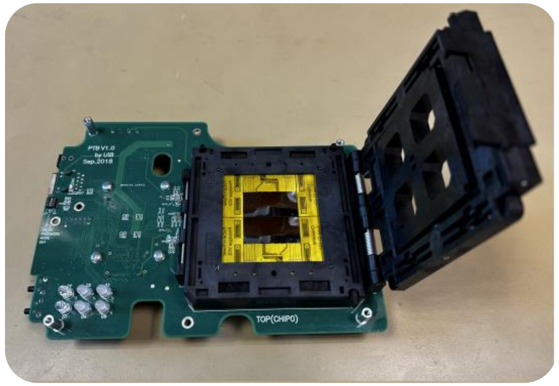
Bonded and assembled ALPIDE



SpTAB joints

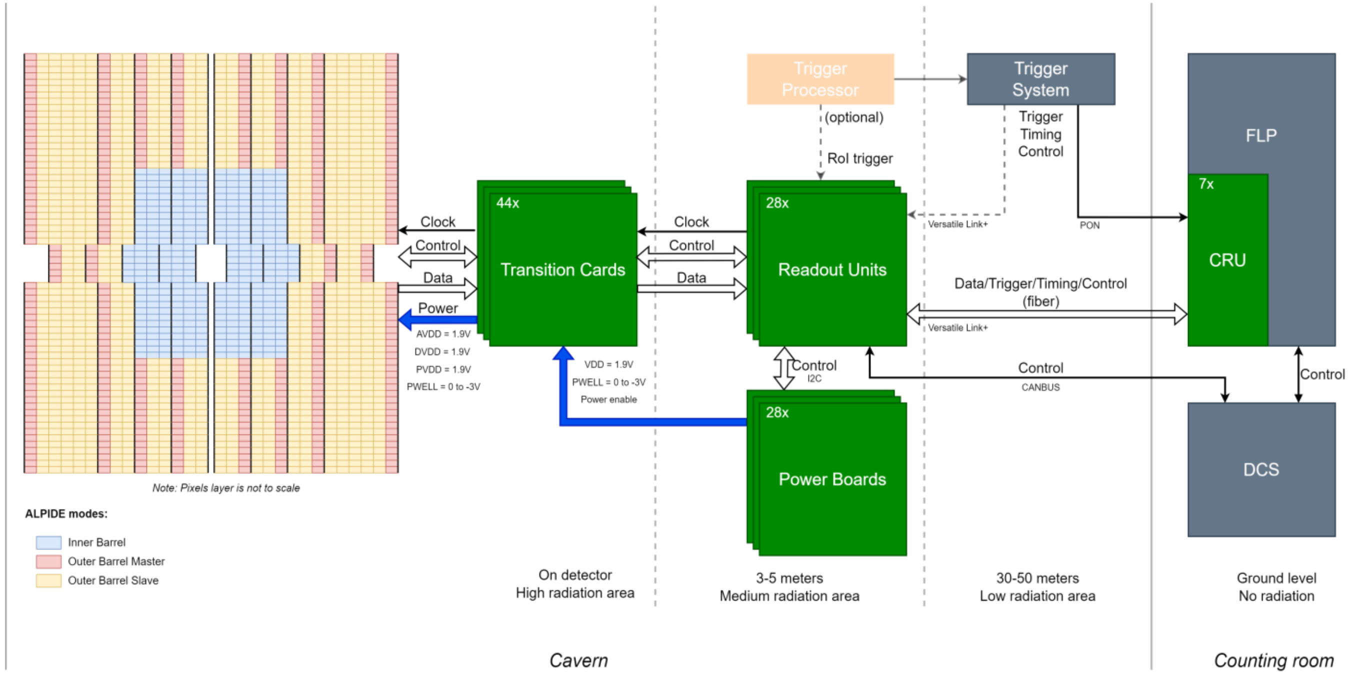


Production Test Box



ALPIDEs (both Inner and Outer Barrel modes!) ultrasonically welded by the **SpTAB** technique (Single-point Tape Automated Bonding) to aluminium-polyimide dielectrics into long multi-chip strings.

Forward Calorimeter – pixels – readout



<u>Readout architecture</u> based on current ITS2.
Main differences:
10Gbps transceiver - **lpGBT** instead of GBTx
10Gbps optical link - **VL+** instead of VL
Bigger main FPGA - **KU085** instead of KU060
New auxiliary FPGA - **IGLOO2** instead of ProASIC3
New flash for reprogramming
Handles Inner & Outer Barrel modes simultaneously
Expected data throughput ~**18 Gbps**

<u>Radiation mitigation</u> techniques for SEUs remain the same - **TMR and scrubbing**

<u>Power distribution</u>
Radiation hardened DCDC **bPOL48V** on the Power Board.

LDOs on the detector (on Transition Card) to compensate for voltage drop and provide stable power to ALPIDEs.

Forward Calorimeter – ALICE Norway

Shared responsibility in FoCal

Pixel layers – Bergen, USN
Pixel readout – Bergen
Integration – Bergen
O2 – Oslo
Simulations – Oslo, HVL

Forward Calorimeter – Bergen

Pixel layers

- ✓ 9-chip prototype test and verification
- ✓ 15-chip prototype design
- ☐ 15-chip prototype production, test and verification (Q4 2024)
- ☐ Testing station for production (Q4 2024 – hardware already produced, software and firmware update ongoing)

Pixel readout

- ✓ Readout Unit conceptual design
- ✓ Power Board conceptual design
- ☐ PCB designs – schematics and layout (Q1 2025)
- ☐ PCB production and assembly (Q2 2025)
- ☐ First iteration of test firmware for Readout Unit (Q2 2025)
- ☐ First iteration of test software for Readout Unit (Q2 2025)

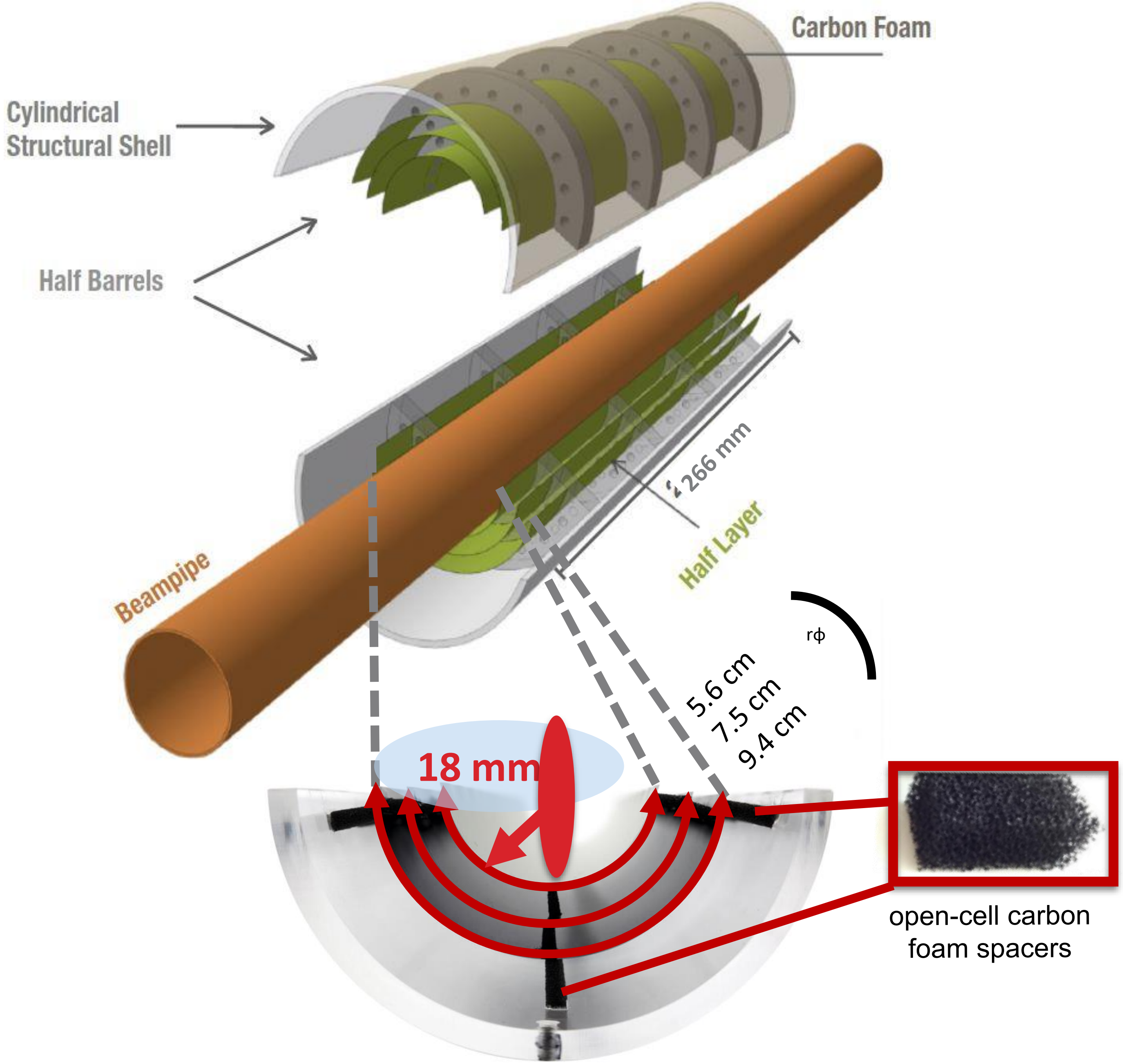
General

- ☐ Full pixel layer and readout chain and power distribution for verification (Q1 2026)
- ☐ Finished mass production of pixel layer, readout chain and power distribution (Q4 2026)

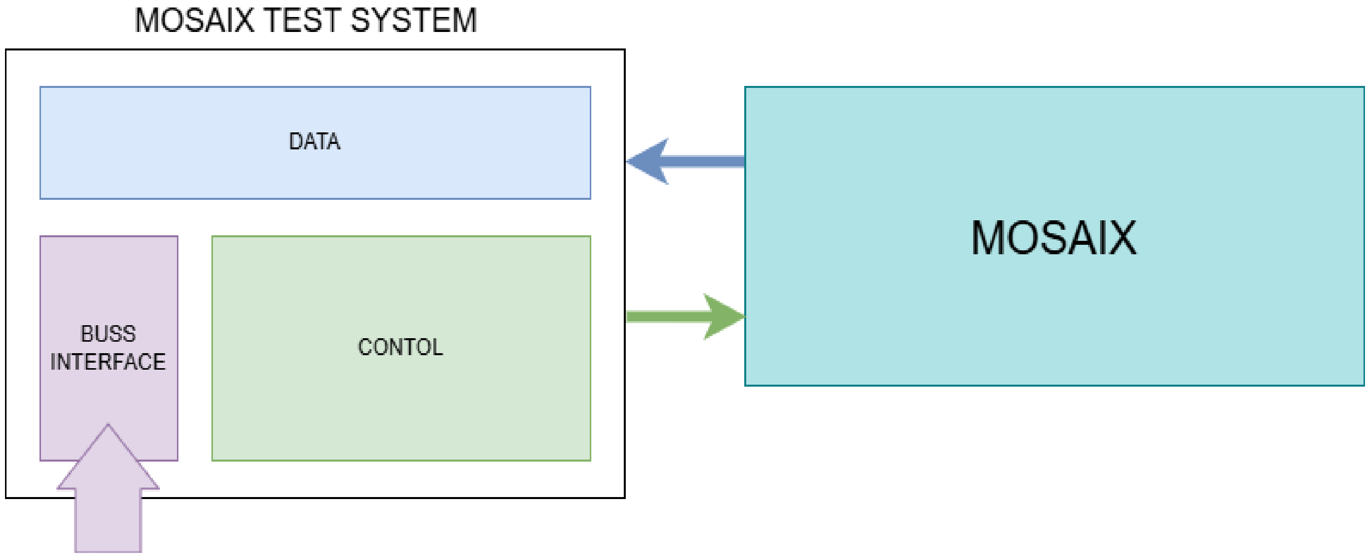
Inner Tracking System 3 (ITS3)

- Detector Overview
  - Wafer-scale sensor ASICs
  - Fabricated with stitching
  - All electrical signals and power routed on-chip
  - Ultra-thin and bendable: 50 µm
  - 266 mm (Z) x variable width* (rϕ)
  - CMOS MAPS
    - 65 nm technology
  - Open-cell carbon foam spacers

- Key benefits
  - Extremely lightweight
    - Material budget: 0.35% X_0 => 0.05% X_0
  - Uniformly distributed material
  - Closer to interaction point
    - Beam pipe radius: 18.2 mm => 16 mm
    - Radial position: 24 mm => 18 mm



MOSAIX Test System


MOSAIX TEST SYSTEM

DATA

BUSS INTERFACE

CONTOL

MOSAIX

Purpose:

- Testing of MOSAIX chips out of fabrication
    - Planning to receive prototype in February-March
- Testing of all functionality and configurations

How:

- FPGA SoC solution
- DATA Processing module (IpGBT interface)
- Contol and Slow-Control module
- IPBuss interface to modules

Test system tested by MOSAIX model:

- Why: Testing the test system
- How: Emulating data input to the TRU (Top Readout Unit) in FW

ALICE detector technology activities at UiO

Emilie H. Solheim, PhD student (2021–2025): FoCal
Detector performance analysis
(MC simulations, test beam)

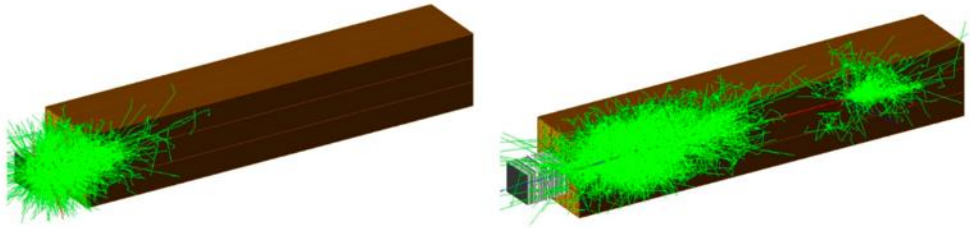


Figure 9. Geant4 simulation of the FoCal-E and FoCal-H (second version) prototype detectors for a shower created by a 100 GeV electron (left) and pion (right). The incident particle, which enters the detector from the left, is not shown.

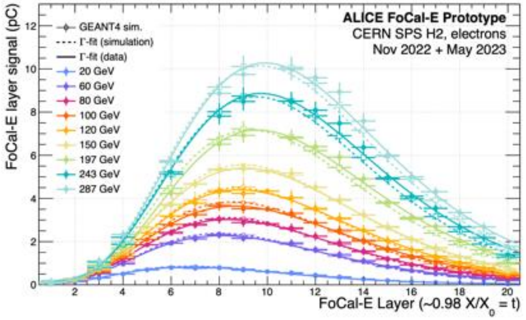


Figure 26. Longitudinal shower profiles for 20–300 GeV electrons compared to Geant4 simulations and fitted with a Γ-distribution.

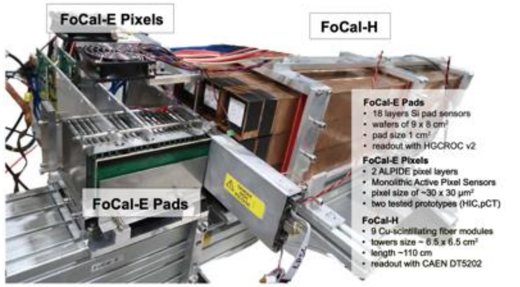
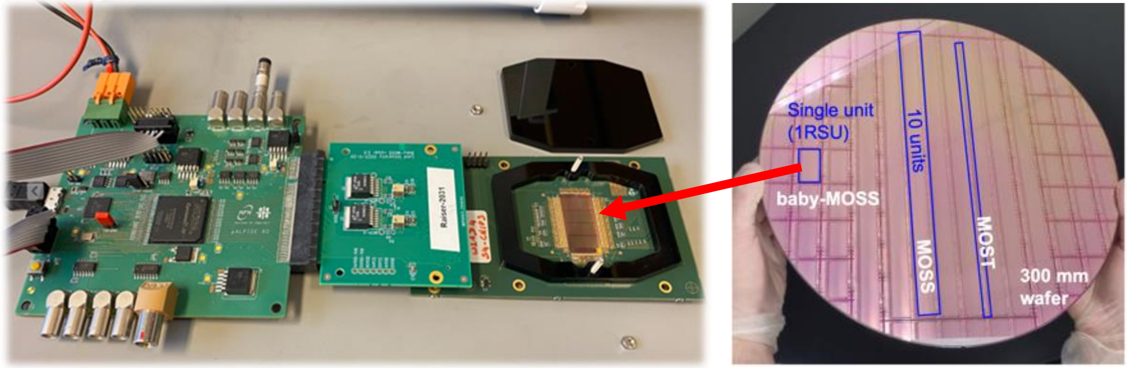


Figure 11. Picture of the full FoCal test beam setup used during the fall 2022 and 2023 campaigns. The FoCal-E consisted out of 18 pad layers, and 2 pixel layers (shown are pCT-based layers but also HIC-based layers were used). The second prototype for FoCal-H was used.

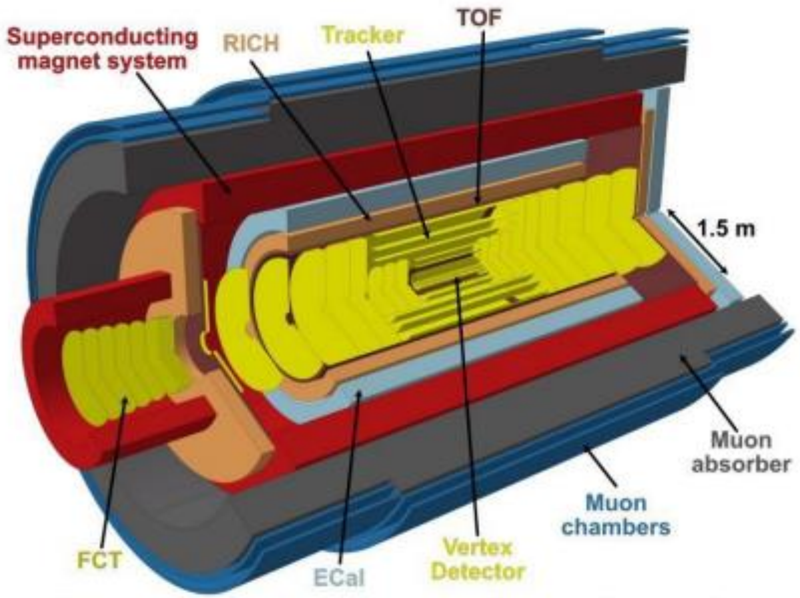
2024 JINST 19 P07006: https://doi.org/10.1088/1748-0221/19/07/P07006

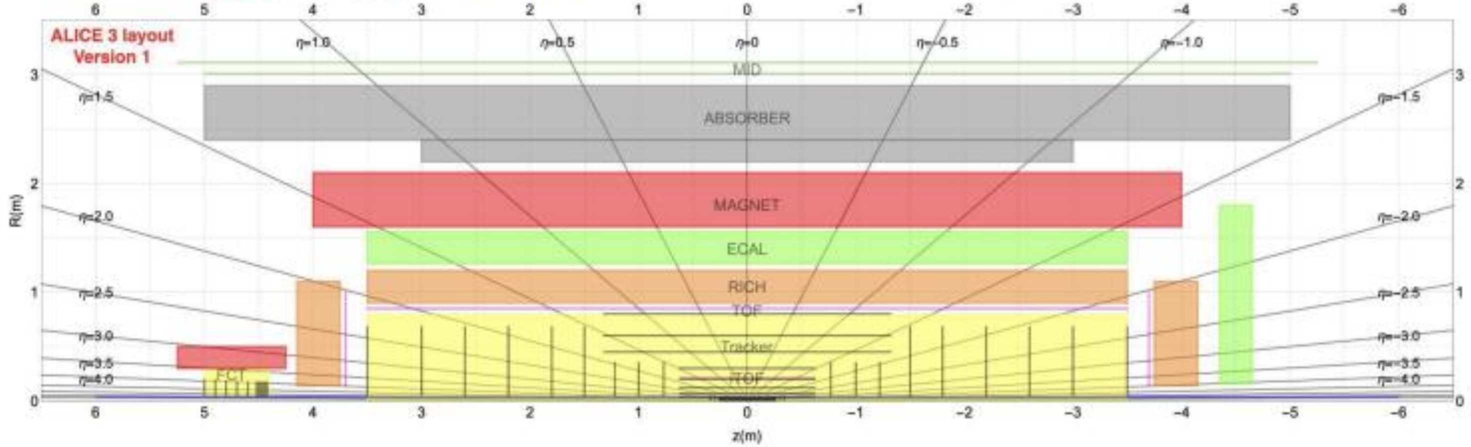
Christina Tsolanta, PhD student (2023-2026): ITS3
Characterization & test beam analysis of MAPS (baby-MOSS)



baby-MOSS setup @UiO

ALICE 3





Next generation **compact experiment for LHC Run 5** and beyond

- **60 m^2** low-mass **all-silicon tracker** fully made of MAPS
- **Retractable vertex detector** for unprecedented pointing resolution
- **Large acceptance:** $-4 < \eta < 4$
- Excellent PID capabilities thanks to TOF and RICH detectors
- Superconducting magnet system
- Continuous readout and online data processing to access rare signals
- Target interaction rates x2 in Pb-Pb and x50 in pp (24 MHz) wrt Run 3 & 4

- **LOI** approved in 2022
- **Scoping Document** in preparation
- Specific **R&D starting up**

ALICE 3 sensor specification estimates https://arxiv.org/pdf/2211.02491.pdf

LOI estimates, 24 MHz pp collision rate, $1/r^2$ – scaling					Hit Rate		Bandwidth					
	Layer	Radius (cm)	Surface (m2)	Pixels (1e6)	Hit Rate (1e6/cm^2/s)	Hit Rate (1e9/layer/s)	Hits (Gbit/s)	Noise (Gbit/s)	Total (Gbit/s)	Power (W)	NIEL (1 MeV n_eq/cm^2)	TID (Mrad)
Vertex Detector	0	0.5	0.016	160	94	17	274	1	275	13	9,00E+15	288
	1	1.2	0.038	380	16	7.3	117	2.4	119	32	1,60E+15	50
	2	2.5	0.079	790	3.8	3.6	57	5	62	66	3,60E+14	12
Middle Layers	3	3.8	0.29	120	1.7	1.8	28	0.7	79	175	1,60E+14	5
	4	7	0.55	220	0.48	1.2	18	1.4	43	131	4,60E+13	1.5
	5	12	0.94	370	0.16	0.8	13	2.4	27	224	1,60E+13	0.5
	6	20	1.6	620	0.058	0.6	9.9	4	19	374	5,60E+12	0.2
Outer Tracker	7	30	2.3	930	0.026	0.5	7.9	6	16	561	2,50E+12	0.08
	8	45	7.5	3000	0.012	0.6	9.6	19.1	33	1792	1,10E+12	0.04
	9	60	10	4.00E+03	6.50E-03	0.5	8.2	25.5	36	2389	6,30E+11	0.02
	10	80	13.3	5.30E+03	3.70E-03	0.4	6.8	34	42	3185	3,50E+11	0.01

	Vertex Detector	Middle Layers	Outer Tracker	ITS3	ITS2
Pixel size (µm^2)	*O(10 x 10)*	*O(50 x 50)*	*O(50 x 50)*	*O(20 x 20)*	*O(30 x 30)*
Position resolution (µm)	2.5	10	10	5	5
Time resolution (ns RMS)	100	100	100	100* / O(1000)	O(1000)
in-pixel rate (/ pixel / s)	100	100	100		
Fake-hit rate (/ pixel / event)	<1e-7	<1e-7	<1e-7	<1e-7	<< 1e-6
Power consumption (mW / cm^2)	70	20	20	20**	47 / 35***

F. Reidt et al.

Need significant improvement in:

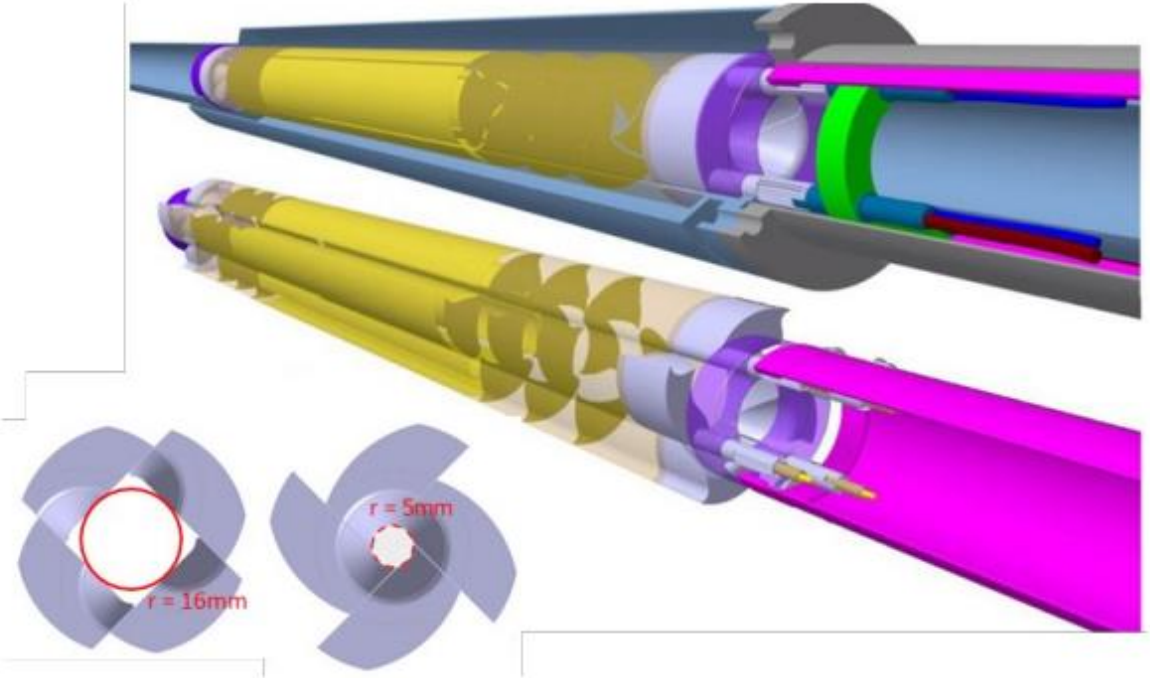
- Power-performance ratio, not only in front end, but also on and off chip data transmission, and architecture
- Radiation tolerance for inner layers

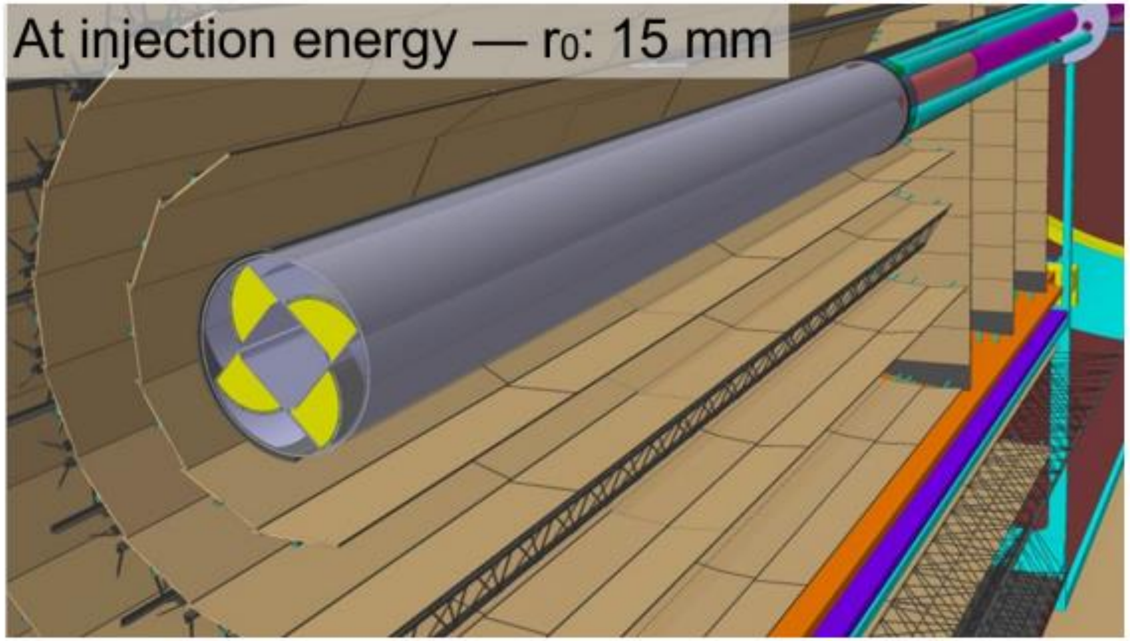
=> Observing convergence in sensor development targets, mostly common in the short term for different HEP applications, with longer term incremental R&D (L. Musa https://indico.cern.ch/event/994685/contributions/4181740/attachments/2193327/3707745/MUSA_ECFA_IS_2021FEB.pdf) see also D. Contardo

ALICE 3 Vertex Detector

3 barrel layers of ultra-thin, curved, wafer-scale MAPS

- Retractable structure inside the beam pipe secondary vacuum
- First detection layer at **5 mm from the interaction point**
- Completed by 2 x 3 end-cap disks for high |η| coverage




At injection energy — r_0: 15 mm

ALICE 3 Vertex Detector

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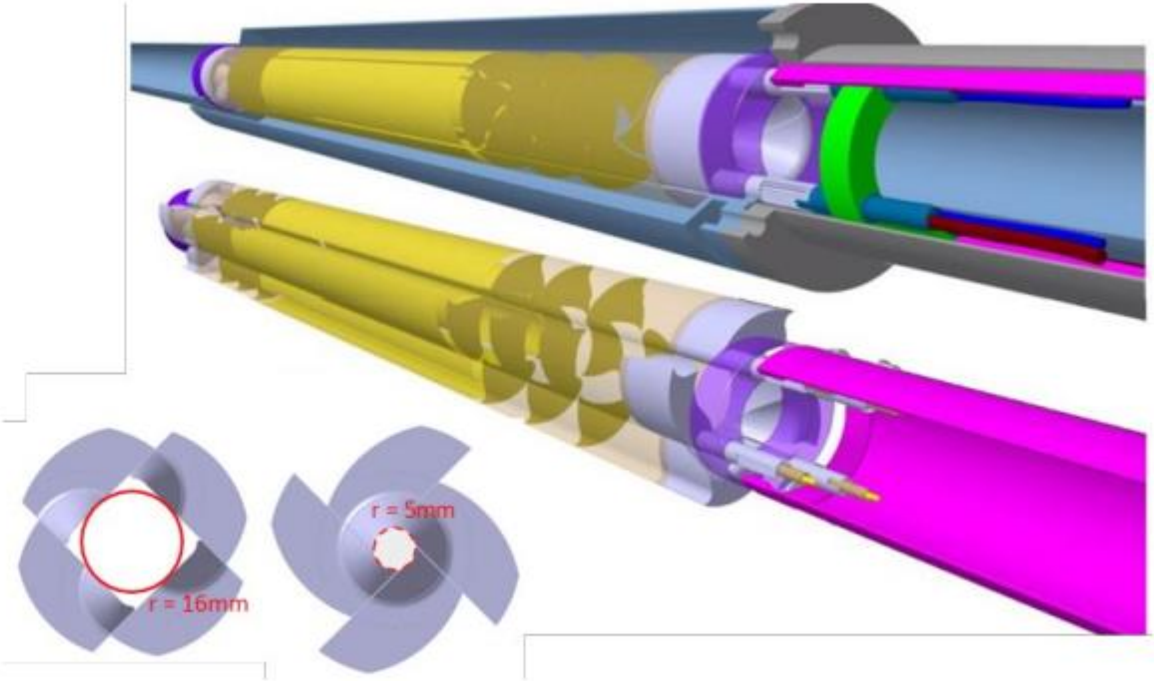

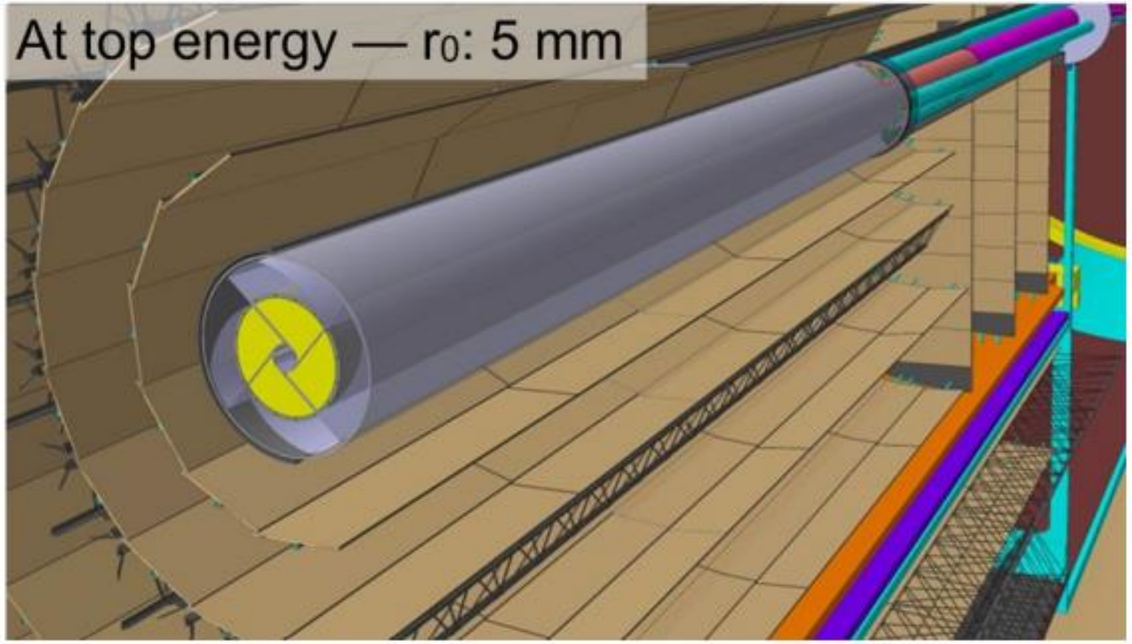

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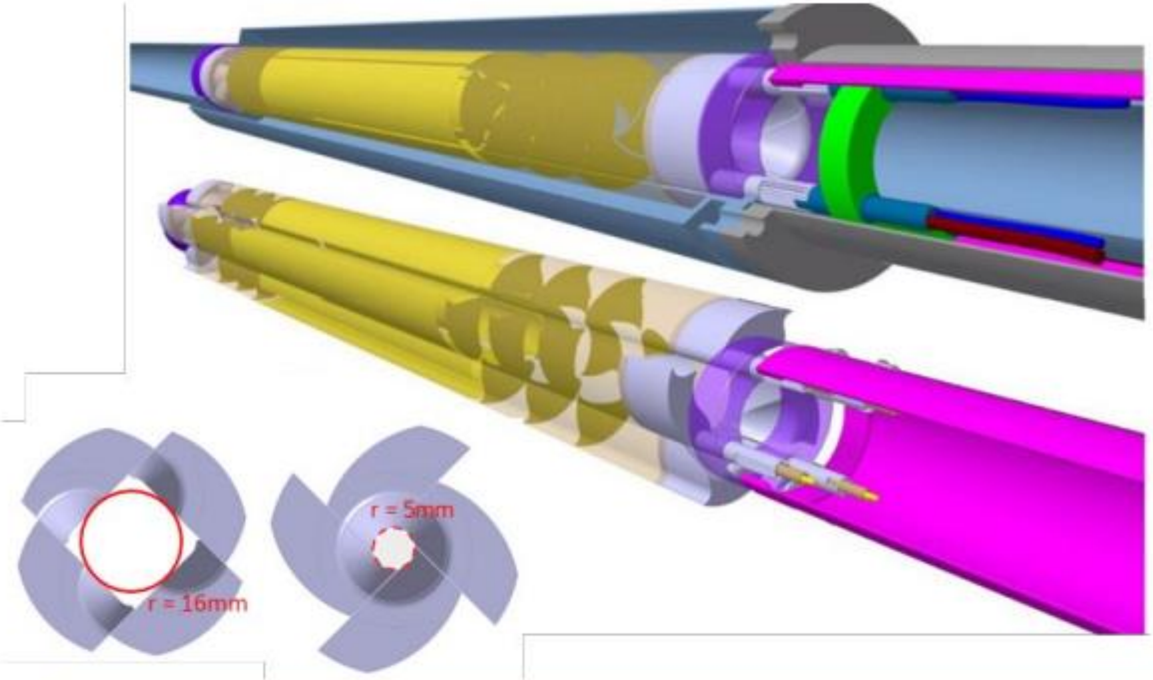
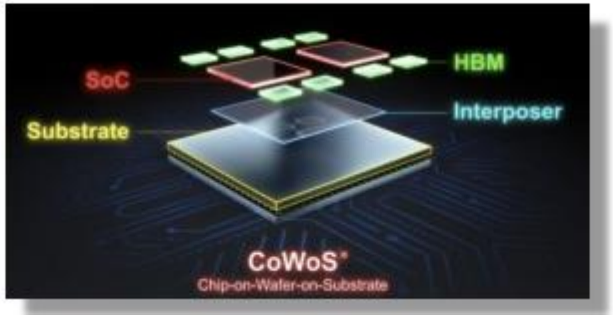


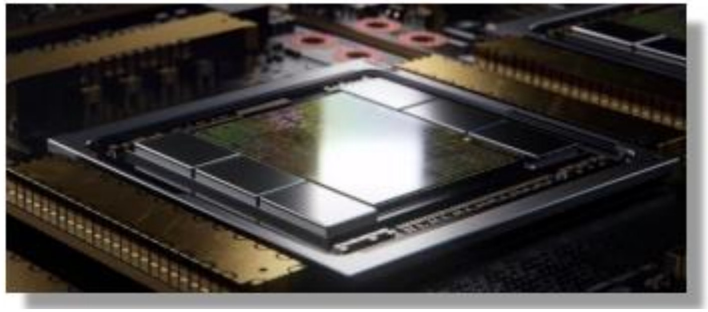
- Unprecedented **spatial resolution: 2.5 μm**
- Extremely low **material budget: 0.1%** X_0/layer
- **Hit rate: up to 94 MHz cm^{-2}**
- **Main R&D challenges:**
  - Radiation hardness
    - **10^{16} 1MeV n_{eq} cm^{-2} + 300 Mrad** *(LOI values)*
  - In-vacuum mechanics and cooling
  - **10 μm pixel pitch**
  - Data and power distribution

FCC Week 2024 - giacomo.contin@ts.infn.it

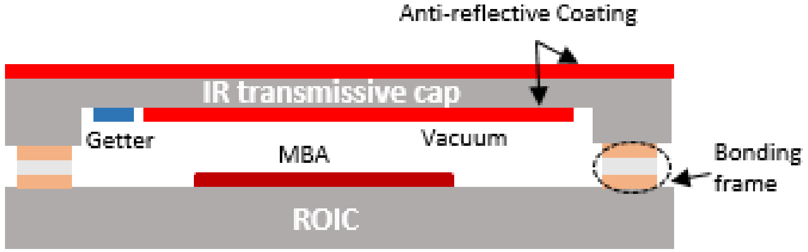
- ALICE3 (and ITS3):
  - Die to die, and die to wafer connections connecting the analog pixels to power distribution , DC-DC converters, digital processing layers and ….
  - Organized as DRD (Detector R&D)
    - DRD 3-WG7 – Experiment oriented. Sensor interconnection techniques
    - DRD 7.2b – Integration of RISC-V System-On-Chip and/or FPGA on detector
    - DRD 7.6b – Development of fundamental integration technologies (2D, 2.5D and 3D)
  - USN capabilities (see next 4 slides)

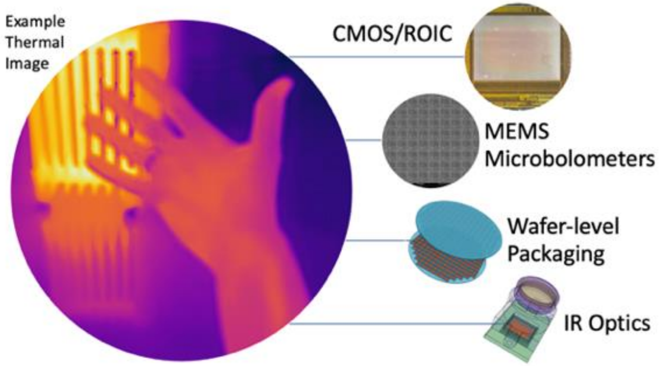


Powering AI

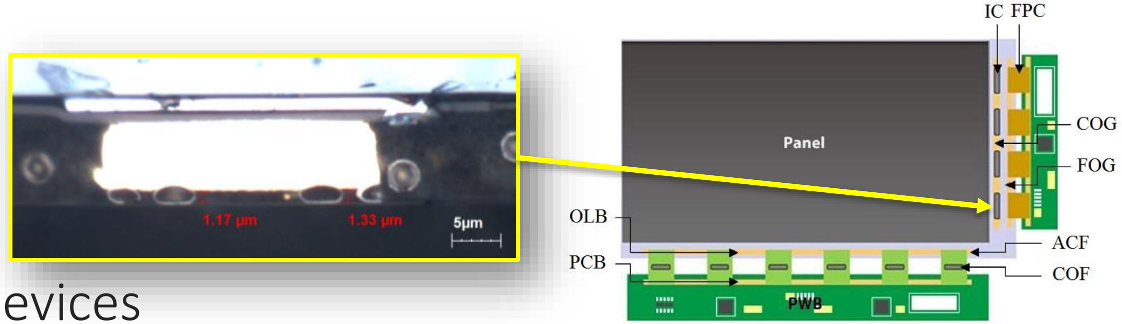


Packaging technology @USN

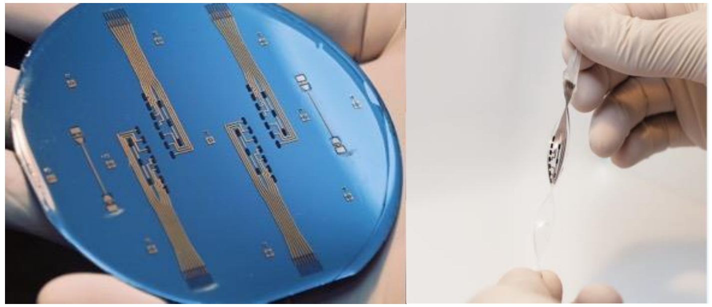




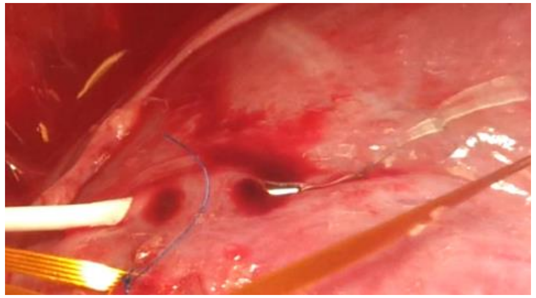
- Encapsulation of MEMS sensors
- Interconnection technologies for MEMS and electronics



- System-integration and encapsulation for medical devices



Bioelectronic interfaces



Sensor implanted in the heart muscle

- Packaging technologies for demanding applications

University of South-Eastern Norway

Packaging slides by Hoang Vu Nguyen, USN

Bonding technology example:
SLID (intermetallic bonding)

Interconnection and die-attach for high temperatures

- Processing at 250–300 °C
- Bond solid to 500–700 °C

Thin-layer bonding (~10 µm)

- Hermetic sealing
- MEMS microbolometers
- Getter activation possible

Fine-pitch possible (few µm)

2.5D–3D integration compatible

Low-temperature SLID (In–Bi alloys and similar)

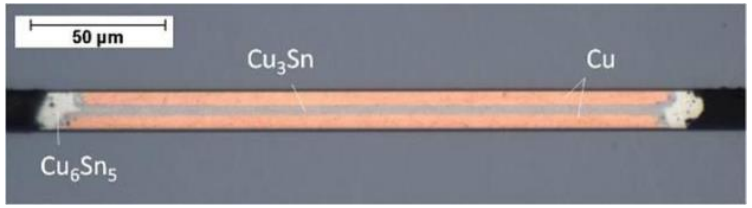
- Processing at 90–120 °C
- Bond solid to 271 °C or higher

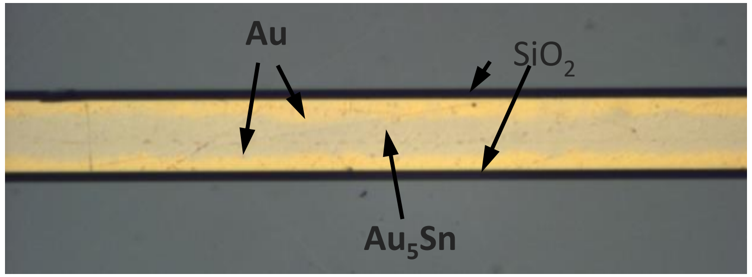
Where are we now:

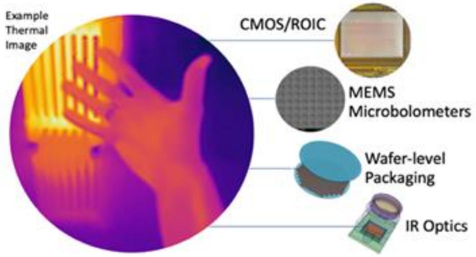
- Cu–Sn: Hermetic sealing for IR cameras
- Au–Sn:
  - Power electronics
  - Down-hole (oil well) instrumentation
  - Compatible with thermal cycling of CTE mismatched die/ substrate
  - Lamination of ultrasound transducers
- Ni–Sn: Potential for extreme high-temperature stability
- Au–Ge: Thermoelectric generators
- Au–In: Demonstrated high-temperature stability
- In–Bi based:
  - Extreme low-temperature bonding
  - Compatible with ultrasound transducers lamination
- Wafer-level and die-level implementation

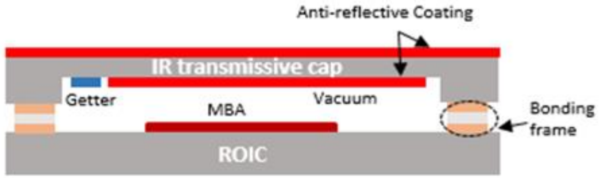
Way forward:

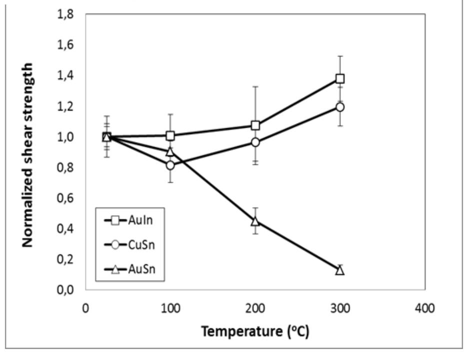
- Further work on industrial implementation
- Low-temperature SLID
  - Process optimalization and fundamental understanding
  - New material systems (Cu–Sn–Bi and others)











Interconnection Technologies based on Metal-coated Polymer Spheres

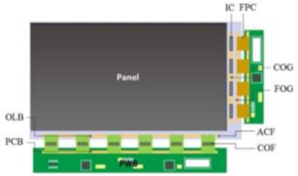
Motivation

Electrical interconnections for demanding applications

Improved mechanical reliability Fine-pitch capability

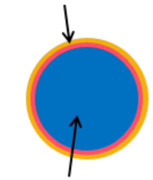
Mechanical vibration and mechanical shock

Bending and dynamic mechanical loading

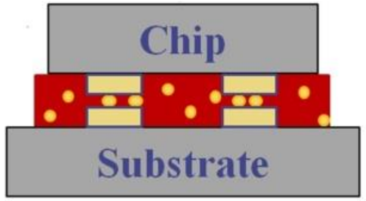


Technologies

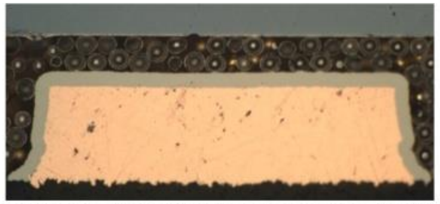
Interconnections based on MPS



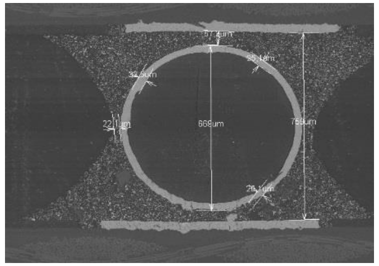
Metal-coated Polymer Sphere (MPS)



Anisotropic Conductive Adhesive (ACA) joint using MPS as conductive fillers

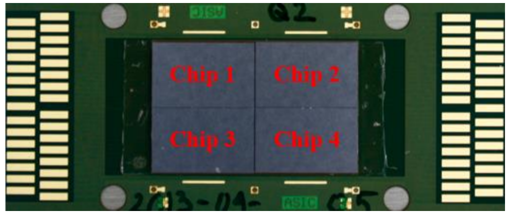


Isotropic Conductive Adhesive (ICA) joint using MPS as conductive fillers

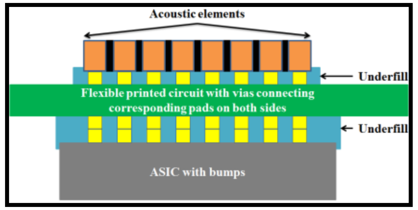


MPS to replace BGA solder balls, or even completely replace solders

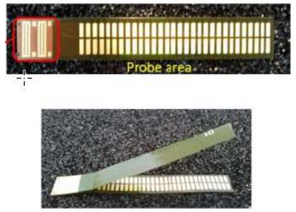
University of South-Eastern Norway



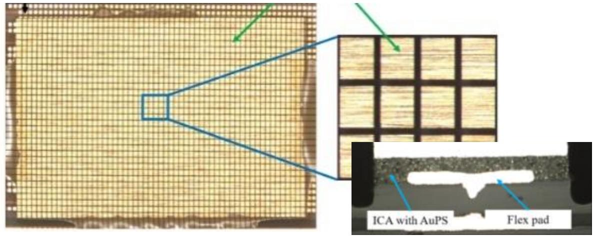
Bonding multiple chips with high-density interconnects to a substrate using ACA



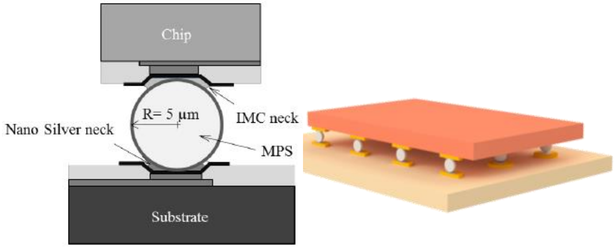
Double-sided assembly using ACA



Flex-to-flex using ACA



Assembly for thousands of ultrasonic transducer elements using ACA, ICA



Interconnect based on a single MPS

Where are we now:

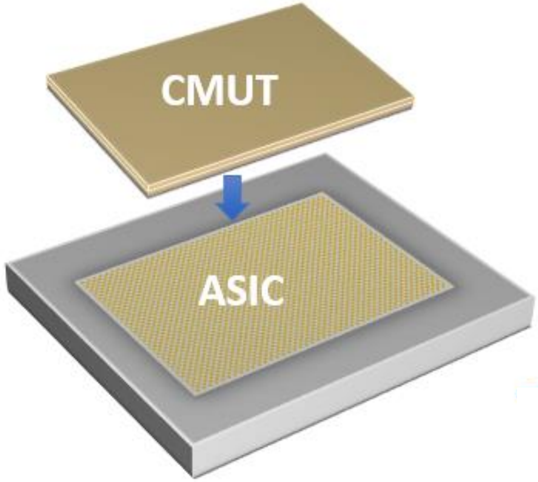
- ☐ Demonstrate interconnects with improved ductility, reduced induced tress, improved impact strength, and hance mechanical reliability
- ☐ Know-how: high-density interconnects; fine-pitch (<200 µm) to ultra fine-pitch capability (< 100 µm); bonding dies from a few mm^2 to >100 mm^2, from 700 µm to 50 µm thickness
- ☐ Applications: medical ultrasound probes, electronics in ammunition, display

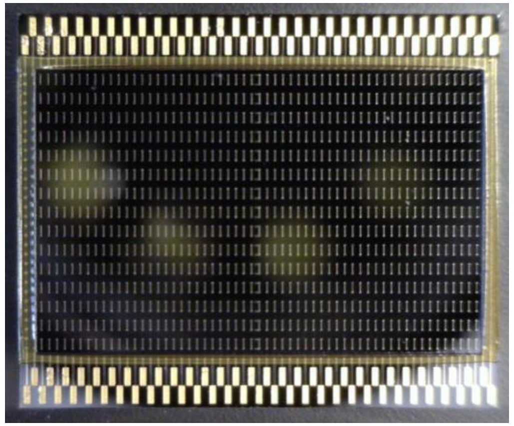
Way forward:

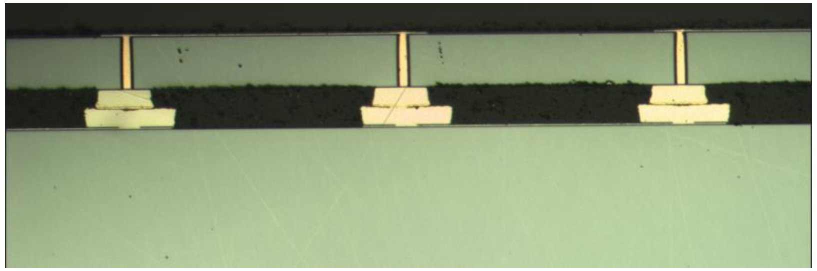
- ☐ Further work on industrial implementation
- ☐ Demonstrate feasibility of the technologies in new applications
- ☐ Solutions for low-temperature, low-pressure, ultra-fine pitch interconnections

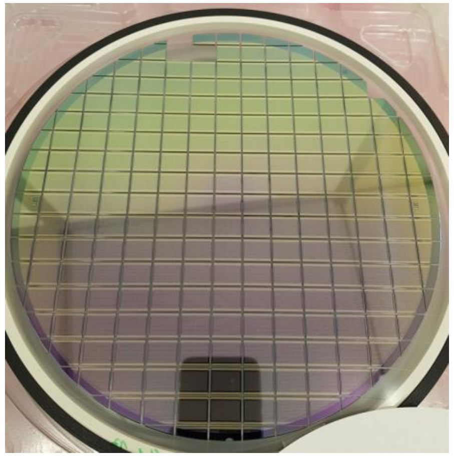
Towards Heterogeneous Integration

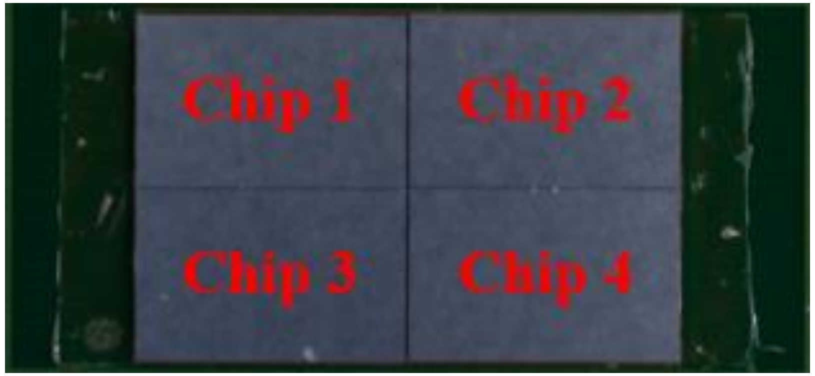
- MEMS-on-CMOS
- Chiplets integration
- 2.5D–3D integration
- Assembly of small-sized, large-sized, ultrathin dies
- Chip-scale package, chip-to-wafer, wafer-level integration

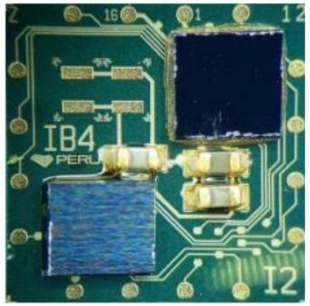












ALICE Upgrades and FCC-ee common challenges

- The ALICE silicon upgrades planned for LHC LS3 and LS4 and the FCC-ee vertex and tracker detectors are targeting similar performance

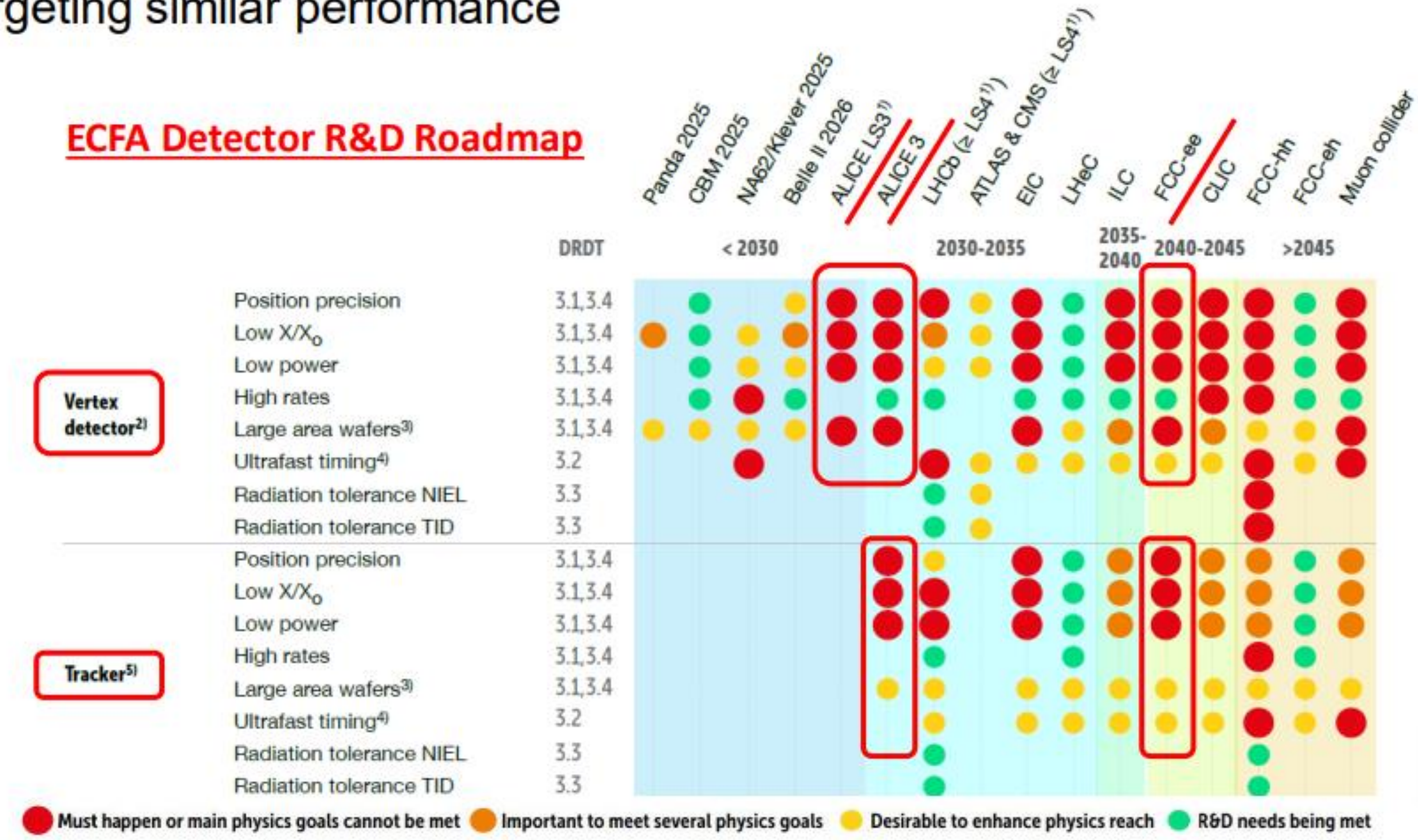
Target performance	ITS3	ALICE 3	FCC-ee
Position precision	5 μm	2.5 μm	3 μm
X/X_0 per layer	0.09% *(average)* 0.07% *(most of active region)*	0.1 %	0.3 %
Power consumption	40 mW/cm^2 *(active region)*	20 mW/cm^2	50 mW/cm^2
NIEL	10^{13} 1MeV n_{eq} /cm^2	10^{16} 1MeV n_{eq} /cm^2 *(LOI, *)*	$\sim 6 \times 10^{12} n_{eq}$/year
TID	1 Mrad	300 Mrad *(LOI , *)*	~3.4 Mrad/year
Maximum hit rate	$<$ 10 MHz/cm^2	94 MHz/cm^2	400 MHz/cm^2 *(*)*

** = being revised*

ALICE Upgrades and FCC-ee common challenges

- The ALICE silicon upgrades planned for LHC LS3 and LS4 and the FCC-ee vertex and tracker detectors are targeting similar performance

Can the R&D for ITS3 and ALICE 3 serve as a stepping stone for FCC-ee vertex and tracker detectors?



ECFA Detector R&D Roadmap

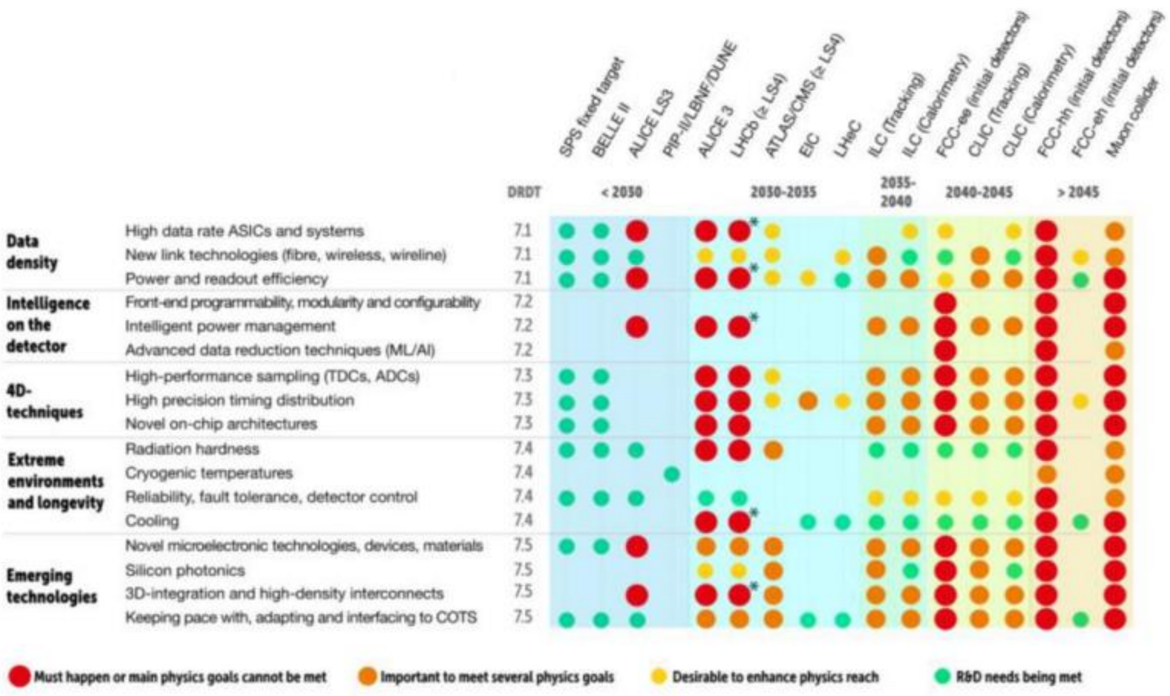
			< 2030					2030-2035					2035-2040	2040-2045		>2045		
		DRDT	Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3[1]	ALICE 3	LHCb (≥ LS4[1])	ATLAS & CMS (≥ LS4[1])	EIC	LHeC	ILC	FCC-ee	CLIC	FCC-hh	FCC-eh	Muon collider
Vertex detector[2]	Position precision	3.1,3.4		🟢		🟡	🔴	🔴	🔴	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low X/X_0	3.1,3.4	🟠	🟢	🟡	🟠	🔴	🔴	🟠	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low power	3.1,3.4		🟢	🟡	🟡	🔴	🔴	🟡	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	High rates	3.1,3.4		🟢	🔴	🟢		🟢	🟢		🟢	🟢	🟢	🟢	🔴	🔴	🟢	🟢
	Large area wafers[3]	3.1,3.4	🟡	🟡	🟡	🟡	🔴	🔴			🔴	🟡	🟠	🔴	🟠	🟡	🟡	🔴
	Ultrafast timing[4]	3.2			🔴				🔴	🟡	🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢	🟡						🔴		
	Radiation tolerance TID	3.3							🟢	🟡						🔴		
Tracker[5]	Position precision	3.1,3.4						🔴	🟡		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low X/X_0	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low power	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	High rates	3.1,3.4							🟢			🟢				🔴	🟢	
	Large area wafers[3]	3.1,3.4						🟡	🟡		🟡	🟡	🟡	🟡	🟡	🟡	🟡	🟡
	Ultrafast timing[4]	3.2							🟡		🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢							🟢		
	Radiation tolerance TID	3.3							🟢							🟢		

🔴 Must happen or main physics goals cannot be met 🟠 Important to meet several physics goals 🟡 Desirable to enhance physics reach 🟢 R&D needs being met

From Roadmap to DRD7

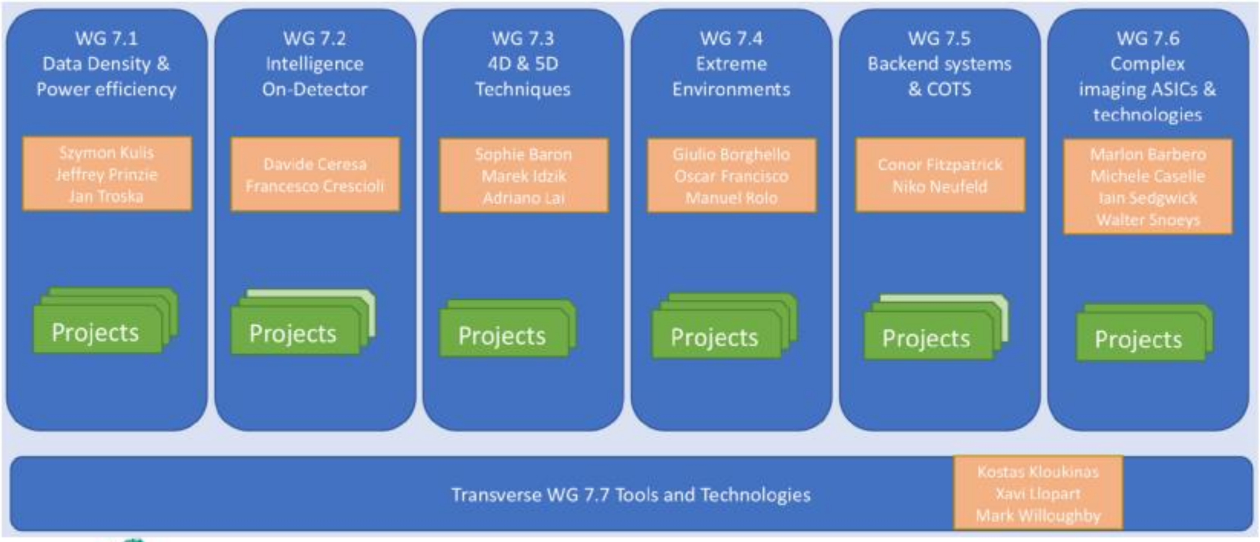
DRDTs to WPs and Projects

- Seen a rich and interesting R&D program that addresses all *Detector R&D Themes* identified in the ECFA Detector R&D Roadmap



		DRDT	< 2030				2030-2035					2035-2040		2040-2045			> 2045		
			SPS fixed target	BELLE II	ALICE LS3	PIP-II/LBNF/DUNE	ALICE 3	LHCb (≥ LS4)	ATLAS/CMS (≥ LS4)	EIC	LHeC	ILC (Tracking)	ILC (Calorimetry)	FCC-ee (initial detectors)	CLIC (Tracking)	CLIC (Calorimetry)	FCC-hh (initial detectors)	FCC-eh (initial detectors)	Muon collider
Data density	High data rate ASICs and systems	7.1	🟢	🟢	🔴		🔴	🔴*	🟡				🟡	🟡		🟡	🔴		🟠
	New link technologies (fibre, wireless, wireline)	7.1	🟢	🟢	🟢		🟡	🟡	🟡		🟡	🟠	🟢	🟢	🟠	🟢	🔴	🟡	🟠
	Power and readout efficiency	7.1	🟢	🟢	🔴		🔴	🔴*	🟡	🟡	🟢	🟠	🟠	🟡	🟠	🟠	🔴	🟢	🔴
Intelligence on the detector	Front-end programmability, modularity and configurability	7.2												🔴			🔴		🔴
	Intelligent power management	7.2			🔴		🔴	🔴*				🟠	🟠	🔴	🟠	🟠	🔴		🔴
	Advanced data reduction techniques (ML/AI)	7.2												🔴			🔴		🟠
4D-techniques	High-performance sampling (TDCs, ADCs)	7.3	🟢	🟢			🔴	🔴	🟡			🟠	🟠	🔴	🟠	🟠	🔴		🔴
	High precision timing distribution	7.3	🟢	🟢			🔴	🔴	🟡	🟠	🟡	🟠	🟠	🔴	🟠	🟠	🔴	🟡	🔴
	Novel on-chip architectures	7.3	🟢	🟢			🔴	🔴				🟠	🟠	🔴	🟠	🟠	🔴		🔴
Extreme environments and longevity	Radiation hardness	7.4	🟢	🟢	🟢		🔴	🔴	🟠			🟢	🟢	🟢	🟢	🟢	🔴		🟠
	Cryogenic temperatures	7.4				🟢											🟠		🟠
	Reliability, fault tolerance, detector control	7.4	🟢	🟢	🟢		🟢	🟢				🟡	🟡	🟡	🟡	🟡	🔴		🟠
	Cooling	7.4					🔴	🔴*		🟢	🟢	🟢	🟢	🟢	🟢	🟢	🔴	🟢	🔴
Emerging technologies	Novel microelectronic technologies, devices, materials	7.5	🟢	🟢	🔴		🟠	🟠	🟠			🟠	🟠	🔴	🟠	🟠	🔴		🔴
	Silicon photonics	7.5					🟡	🟡	🟠			🟠	🟢	🔴	🟠	🟢	🔴		🔴
	3D-integration and high-density interconnects	7.5			🔴		🔴	🔴*	🟠			🟠	🟠	🔴	🟠	🟠	🔴		🔴
	Keeping pace with, adapting and interfacing to COTS	7.5	🟢	🟢	🟢		🟠	🟠	🟠	🟢	🟢	🟠	🟠	🔴	🟠	🟠	🔴	🟢	🔴

🔴 **Must happen or main physics goals cannot be met** 🟠 **Important to meet several physics goals** 🟡 **Desirable to enhance physics reach** 🟢 **R&D needs being met**



WG 7.1
Data Density &
Power efficiency
Szymon Kulis
Jeffrey Prinzie
Jan Troska
Projects

WG 7.2
Intelligence
On-Detector
Davide Ceresa
Francesco Crescioli
Projects

WG 7.3
4D & 5D
Techniques
Sophie Baron
Marek Idzik
Adriano Lai
Projects

WG 7.4
Extreme
Environments
Giulio Borghello
Oscar Francisco
Manuel Rolo
Projects

WG 7.5
Backend systems
& COTS
Conor Fitzpatrick
Niko Neufeld
Projects

WG 7.6
Complex
imaging ASICs &
technologies
Marlon Barbero
Michele Caselle
Iain Sedgwick
Walter Snoeys
Projects

Transverse WG 7.7 Tools and Technologies
Kostas Kloukinas
Xavi Llopart
Mark Willoughby

Summary

- ALICE Norway contributes to many aspects of the ALICE Collaboration programme, including core detector development, software and computing
- Strong involvement in the ongoing R&D for the LS3 upgrade:
  - FoCal
  - ITS3
- Aim at continuing working within ALICE beyond Run4 and be involved in the ALICE3 project
- Involved in DRDs

Backup

WorkPackages & Projects

High-Level Overview

WP7.1 Data density and power efficiency	**PROJECTS** **7.1a** Silicon Photonics transceiver development **7.1b** Powering next generation detector systems **7.1c** Wireless Data And Power Transmission (WADAPT)	More channels More bits Less power
WP7.2 Intelligence on the detector	* **7.2b** Radiation tolerant RISC-V SoC **7.2c** Virtual electronic system prototyping	Programmability, modularity, configurability System-level optimization
WP7.3 4D and 5D techniques	**7.3a** High performance TDC and ADC blocks at ultra-low power **7.3b1** Strategies for characterizing and calibrating sources impacting time measurements **7.3b2** Timing distribution techniques	High resolution in position, time and energy System-level optimization

- For each project: Milestones and deliverables defined - currently 2024 - 2026, with perspectives beyond for most projects
- Summary table for each project in the appendix of this presentation

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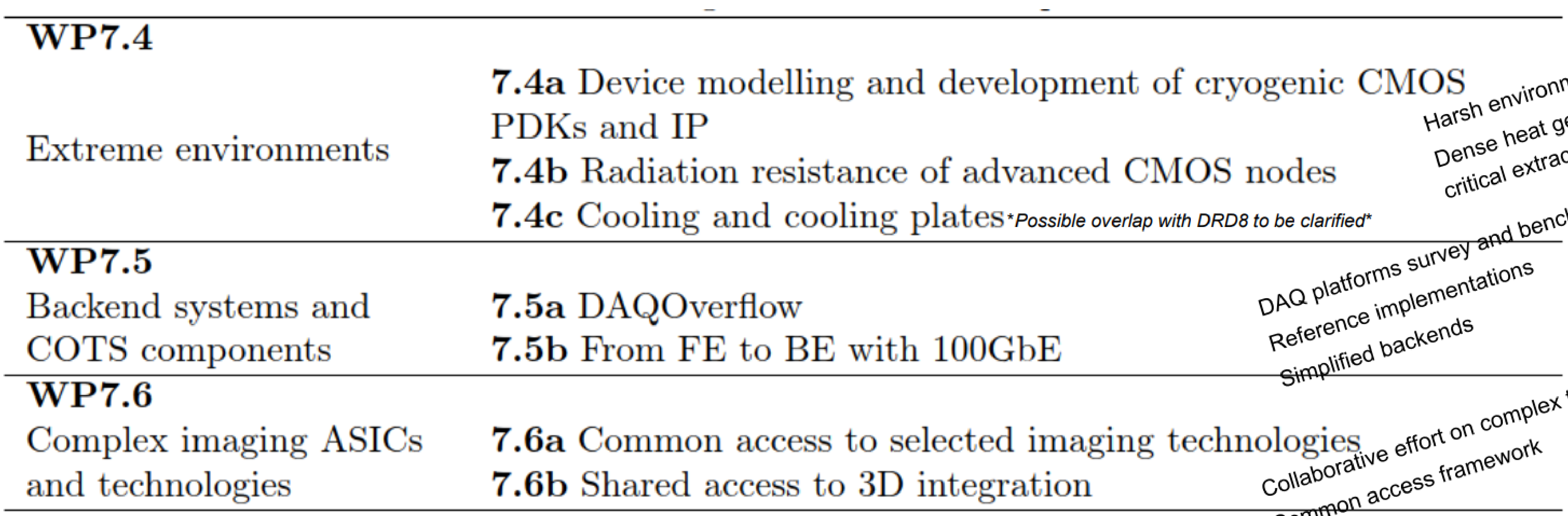
* Project 7.2a (e-FPGA) postponed, pending consolidation of resources

WorkPackages & Projects

High-Level Overview



WP7.4 Extreme environments	**7.4a** Device modelling and development of cryogenic CMOS PDKs and IP **7.4b** Radiation resistance of advanced CMOS nodes **7.4c** Cooling and cooling plates **Possible overlap with DRD8 to be clarified**
WP7.5 Backend systems and COTS components	**7.5a** DAQOverflow **7.5b** From FE to BE with 100GbE
WP7.6 Complex imaging ASICs and technologies	**7.6a** Common access to selected imaging technologies **7.6b** Shared access to 3D integration

Harsh environments
Dense heat generation and critical extraction

DAQ platforms survey and benchmarking
Reference implementations
Simplified backends

Collaborative effort on complex technologies
Common access framework
IP blocks

- For each project: Milestones and deliverables defined - currently 2024 - 2026, with perspectives beyond for most projects
- Summary table for each project in the appendix of this presentation