STATUS AND PLANS OF SRS READOUT ELECTRONICS FOR THE NEXT TPC

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The NEXT Collaboration

About NEXT (a Neutrino Experiment TPC)

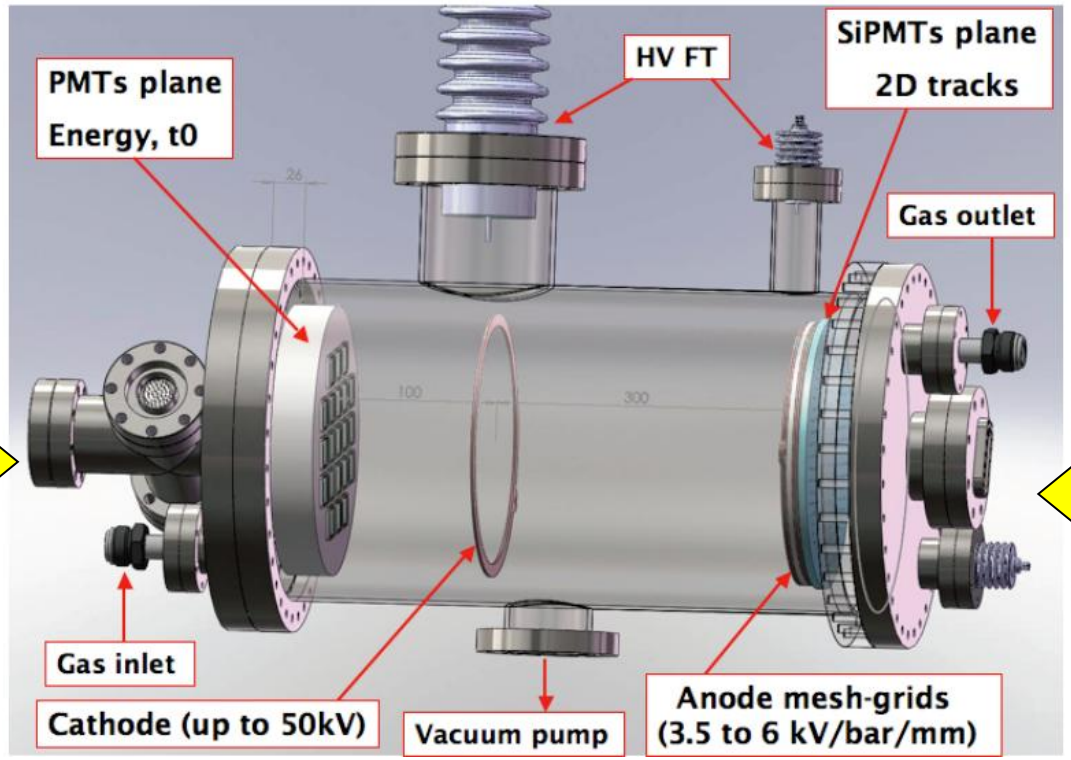
http://next.ific.uv.es/next/

- Double beta decay experiment
  - Funded and approved in 2008
  - To be operated in the Canfranc Undergroung Laboratory
  - Goal: build and operate a TPC filled with 100-kg HPGXe enriched with ^{136}Xe to measure its $\beta\beta0\nu$ decay
  - Gas-filled TPC allows high energy resolution with xenon gas and 3D track topology for background rejection
- The Collaboration
  - IFIC-Valencia, Univ. Politécnica de Valencia, IFAE-Barcelona, CIEMAT-Madrid
  - Univ. Zaragoza, Univ. Santiago de Compostela (Spain)
  - Univ. Coimbra, Univ. Aveiro (Portugal), Univ. Antonio Nariño (Colombia)
  - Lawrence Berkeley National Laboratory, Texas A&M University
  - JINR (Russia), Centre d'Études Nucléaires de Saclay (France)

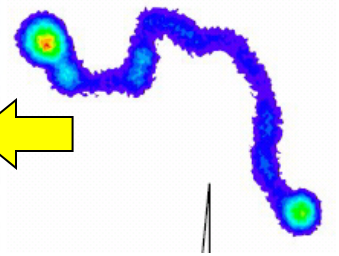
The NEXT-1 prototype (2011-2012)

- Non-radiopure, electroluminiscent TPC
  - Energy measured with a PMT plane behind the transparent cathode
  - t0 (primary scintillation) also measured with the same PMTs
  - Tracks reconstructed by a sensor array (such as SiPMs) behind the transparent grids of the anode

~38 PMT ch (E, t0)



248 SiPMs (tracking)



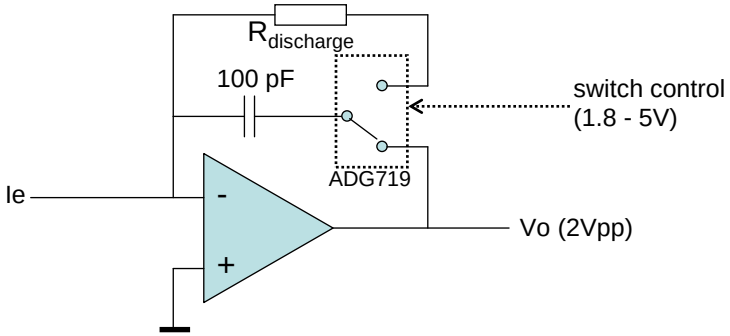
SiPM readout in NEXT-1

248 SiPMs in NEXT-1

But the solution must provide a path for 10^4 channels in the final TPC

The FE-SiPM front-end card for NEXT-1

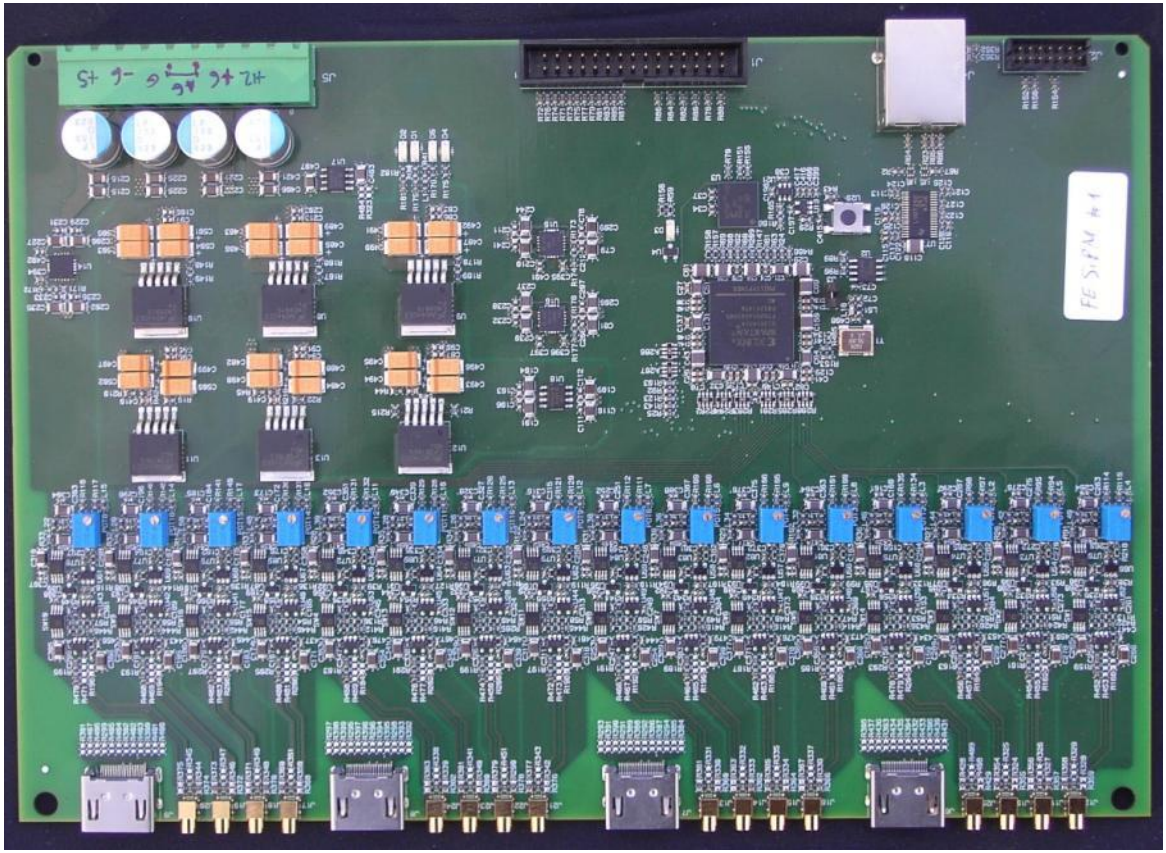
16ch three-stage analog path (I/V+integration+offset adj.) + 16x ADCs + data formatting + LVDS RJ-45 connection to FEC



- FPGA controlled gated integrator
- 1 us integration time

FPGA firmware is correct (ADC and integrator control, data formatting, timestamping, LVDS comm. with FEC,…)

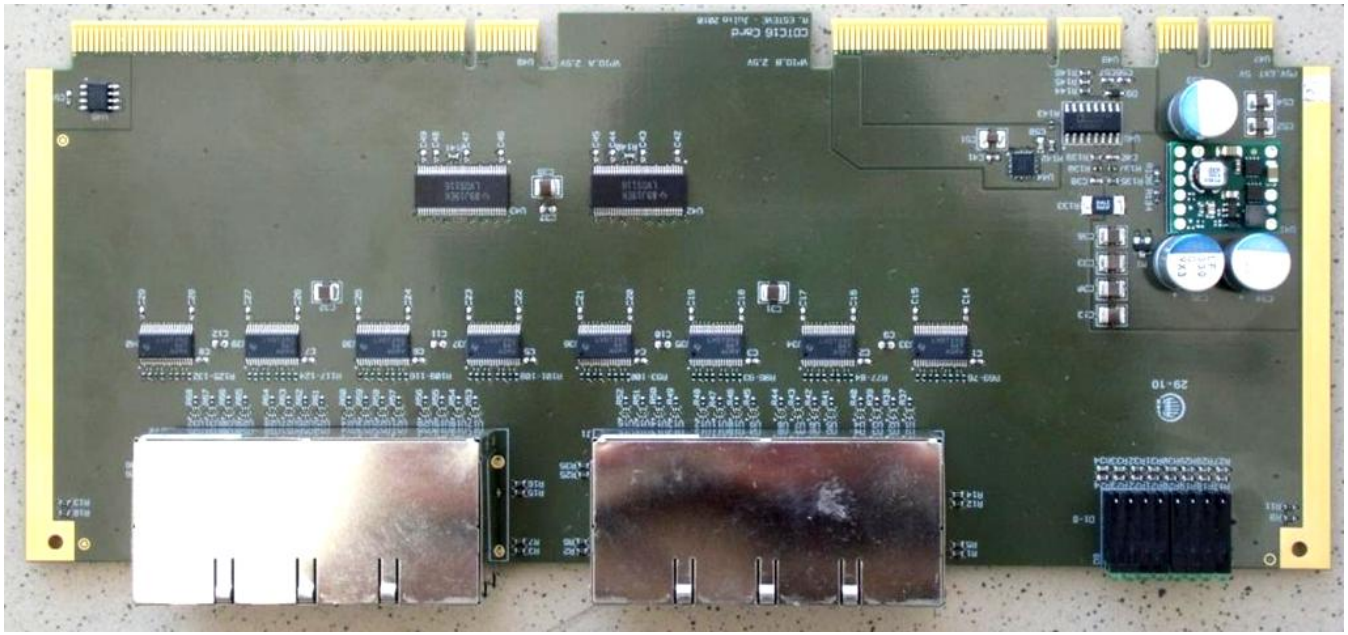
But: bad offset control, need to modify the analog path



Abstract submitted to NDIP 2011, Lyon

The LVDS I/O card for NEXT-1

- 16x quad-LVDS links over RJ-45 (SRS DTC concept)
- Tested 2 LVDS pairs upstream for data (independent for each link)
- 2 LVDS pairs downstream: clock + trigger/commands, common to all 16 links
- Downstream links tested at 100 Mb/s, upstream links at 200 Mb/s each



Dual use as (1) front-end interface and (2) trigger/command distribution to FECs !!!

Downstream LVDS buffers are limited in speed to 100 Mb/s (but this is ok for NEXT-1)

SiPM readout scheme in NEXT-1

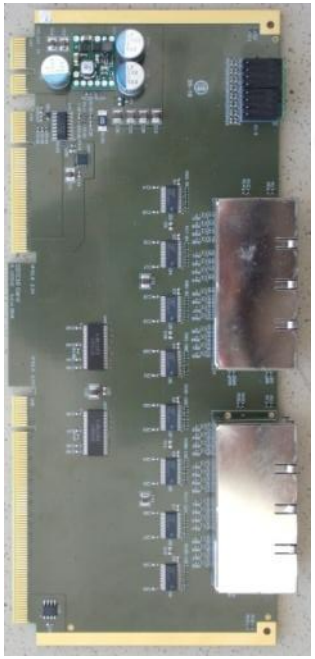
Tested
- Raw readout mode: (1) stores 96 ch/FEC, 384 us data in FPGA FEC, (2) sends event to DATE, (3) ready for a new trigger

In test
- Raw data mode with DDR2 memory: 128 ch/FEC, longer buffer, still dead time

Untested
- Zero-suppression mode: up to 256 ch/FEC, no dead time, continuous acquisition, DDR2 buffer

2x GbE

2x FECs



2x LVDS I/O cards

CAT6 cable

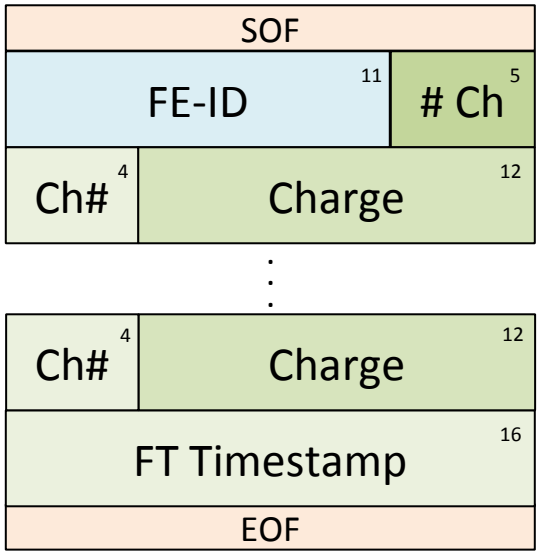
320Mb/s per FE board (raw data mode)

tbd Mb/s in zero-suppression mode

16x SiPM-FE boards

SiPM readout data formats on the RJ-45 link

Upstream data frame format (max. twenty 16-bit words, one frame each us)



→ Start of frame word

→ Unique FE card ID + Number of active channels

→ Channel ID (4bit) + channel ADC count (12bit)

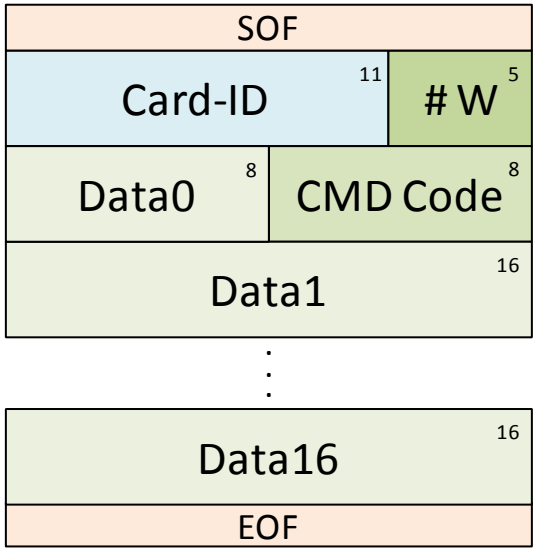
→ Timestamp + error flag

→ End of frame word

CRC to be added soon to the data formats

Downstream command frame

COMMANDS CODIFICATION				
CMD Code	**Command**	**Description**	**Address to**	**Source**
00h	ACQUISITION	Configuration, start/stop acquition	FEC/FE-SiPM	DATE/FEC TRG
01h	TRIGGER	Trigger command	FEC/FE-SiPM	FEC TRG
02h	WRITE REGISTER	Write configuration register	FEC/FE-SiPM	FEC
03h	READ REGISTER	Read configuration/status register	FEC/FE-SiPM	FEC
04h	STATUS	Status information (alarms, errors…)	FEC TRG	FEC
05h	SYNC	Synchronization command	FEC/FE-SiPM	FEC TRG



PMT readout in NEXT-1

Up to 38 PMT channels in NEXT-1

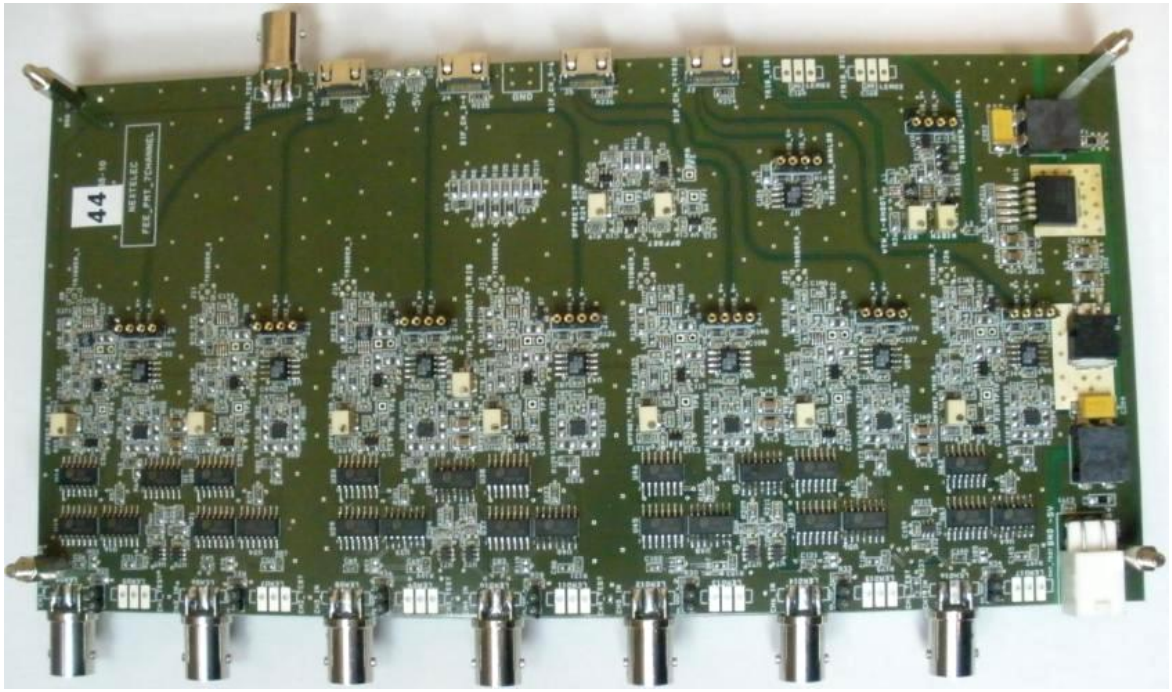
But the solution must provide a path for ~200 channels in the final TPC

The FE-PMT front-end card for NEXT-1

7-ch analog paths (amp+shaping) + analog sum (trigger) + 8 ch HDMI output to CERN ADC card

The card needs a re-design as it is not working properly.

In the meantime, COTS amplifiers + ADC modules + NIM trigger logic + custom adapters (LEMO to HDMI) are being used



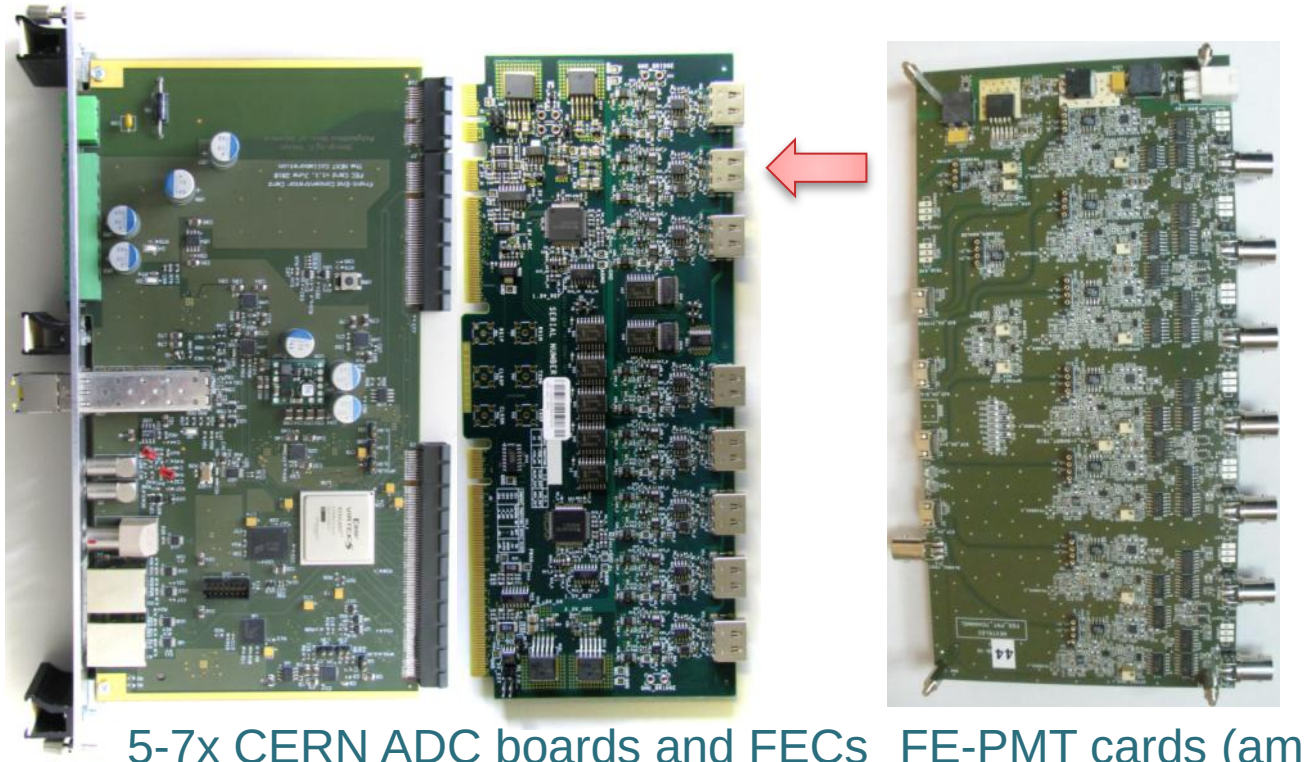
The old FE-PMT card (amp+shaping+analog sum)

PMT readout scheme in NEXT-1

Tested
- Raw readout mode: (1) stores 6 ch/FEC, 384 us data in FPGA FEC, (2) sends event to DATE, (3) ready for a new trigger

In test
- Raw data mode with DDR2 memory: 8 ch/FEC, longer buffer, still dead time

Untested
- Zero-suppression mode: no dead time, continuous acquisition, DDR2 buffer



5-7x GbE

38x PMT ch

5-7x CERN ADC boards and FECs FE-PMT cards (amp+shaping)

Trigger in NEXT-1

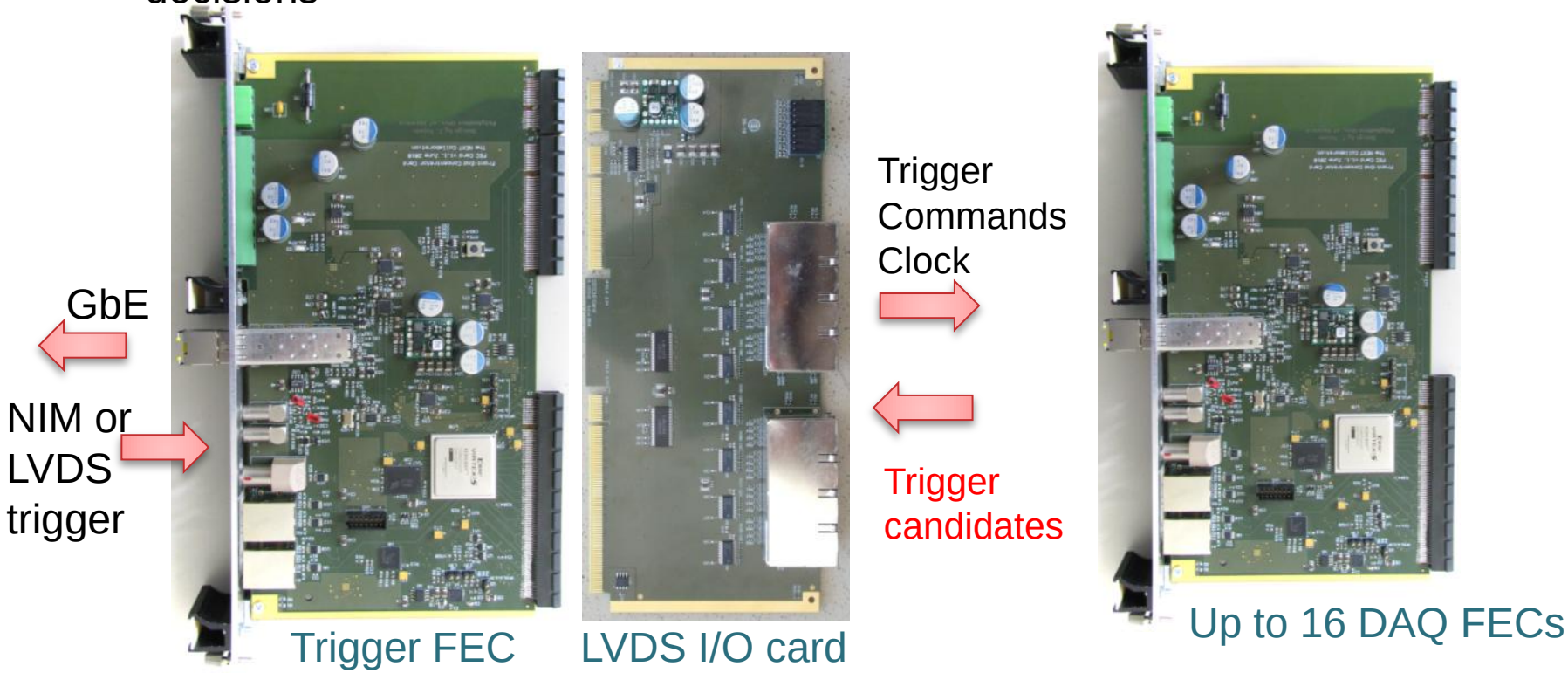
Trigger in NEXT-1

Tested

- External trigger mode: NIM or LVDS input to the trigger FEC is distributed to the DAQ FECs via RJ-45 links using a star topology

Untested

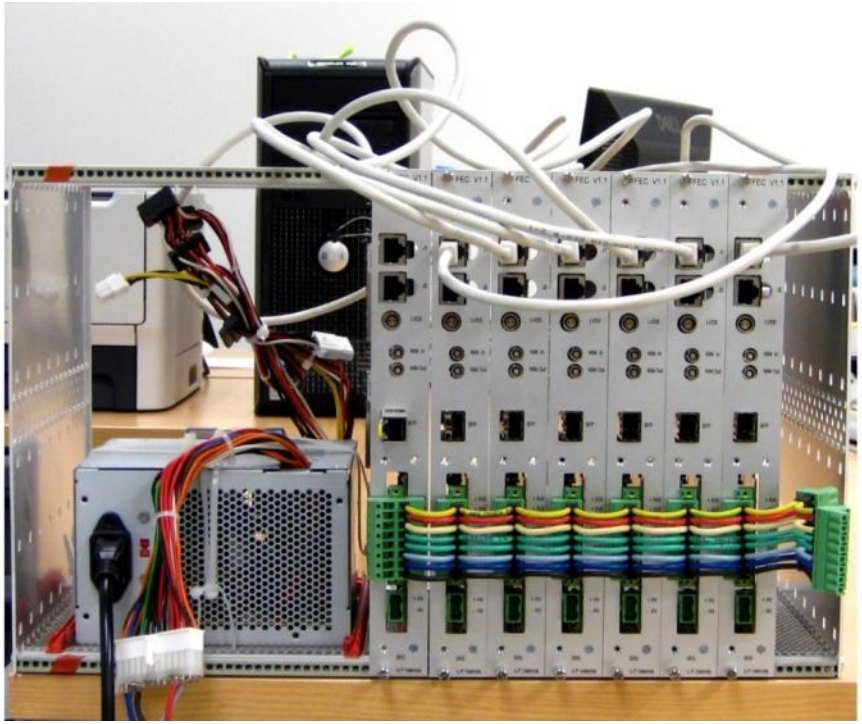
- Self-triggered: DAQ FECs send trigger candidates to the trigger FEC over the RJ-45 link. Trigger FEC runs a trigger algorithm and distributes trigger decisions



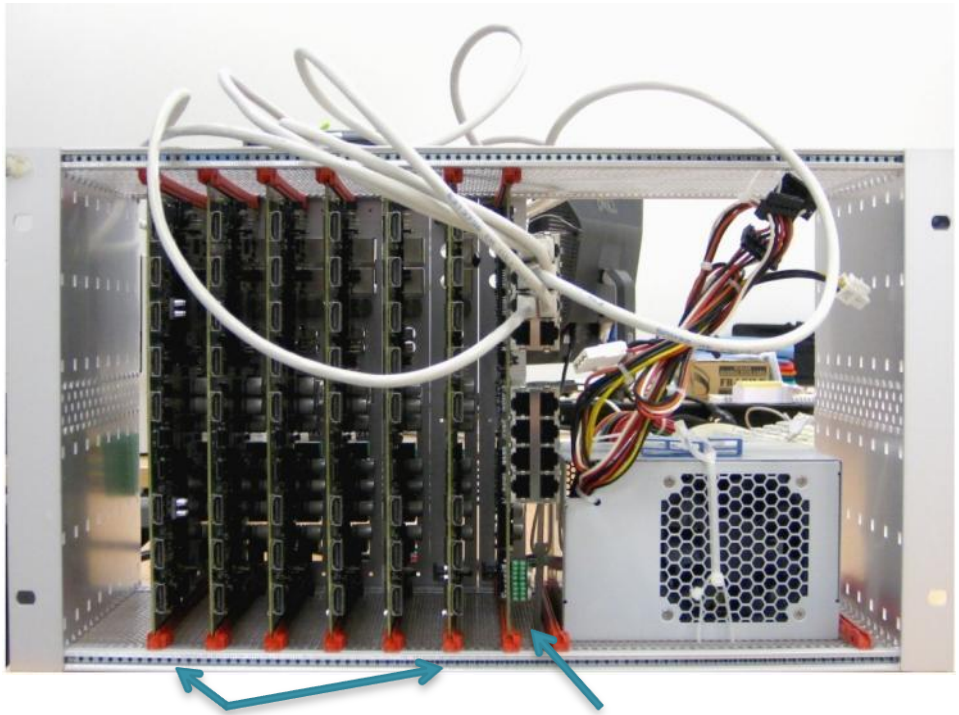
PMT readout test setup for NEXT-1

Tested Clock, trigger and commands sent from Trigger FEC to DAQ FECs
Trigger FEC communicates with a PC via GbE

Front view



Rear view



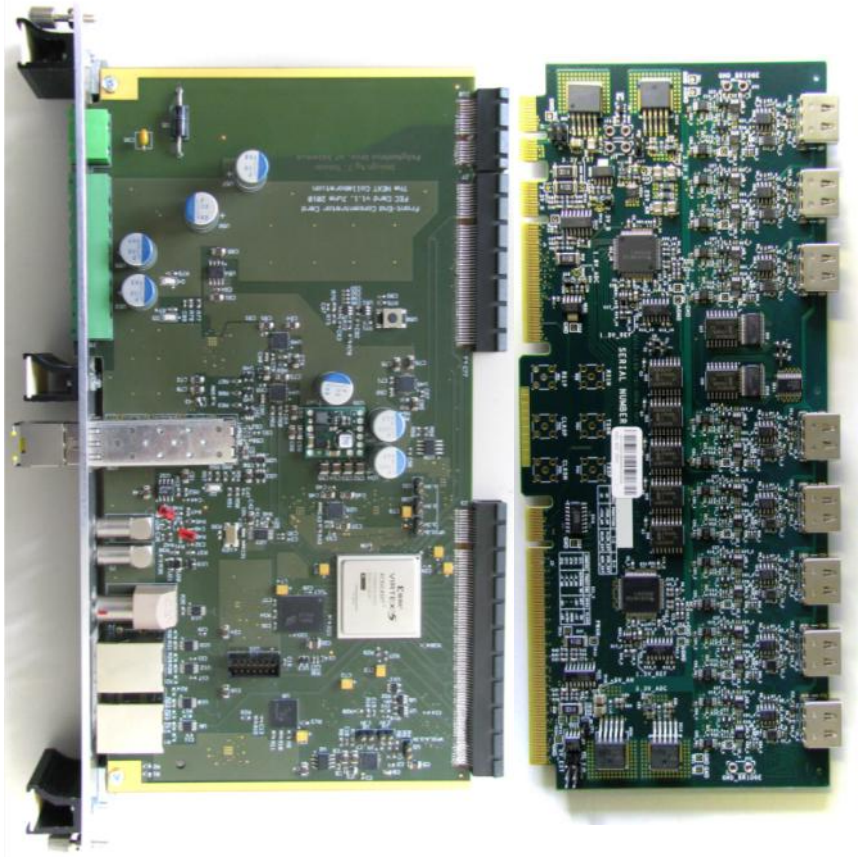
Solutions for PMT readout, SiPM readout, slow controls and trigger beyond NEXT-1

Counting on the comingVirtex-6 FECs

(higher throughput, buffer, speed, logic and resources than current Virtex-5 FECs)

PMT readout for ~200 PMTs

The existing solution (FE-PMT + CERN ADC + FEC) could be used, as it requires less than 20 card sets

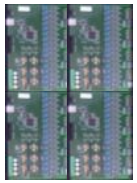


New Amp+shaping cards

SiPM readout for 10^4 SiPMs

• The existing solution (FE-SiPMs + LVDS I/O + FEC) cannot be used (requires 625 card sets!)

• **Preferrer solution**:



  • Integrate 4xFE-SiPM cards in an ASIC (64ch)
  • Integrate ~160 ASICs inside the TPC
  • Use ~160 bidirectional optical links to communicate with the DAQ
  • DAQ:
    • Upgrade LVDS I/O card to Nx optical I/O card + Mx FECs?
    • Use SRUs with Nx optical links?

• **Backup solution**:
  • Design new FE-SiPM for 64 channels, optical output

Trigger solution

- Overall number of FECs: 20 FECs for PMTs + 40 FECs for SiPMs ??
- **2-3x SRUs would make great trigger modules!!**

Slow controls solution

- **Use one of the available SFP+ transceivers for slow controls over GbE**

RD-51 related activities in 2011

RD-51 related activities in 2011

- Hardware
  - FECv6 design (jointly with CERN-PH-AID)
    - LX130T/195T/240T FPGA
    - DDR3 SODIMM buffer
    - Up to 4x SFP+ transceivers allows GbE slow controls and higher data throughput
- Firmware
  - DDR2/DDR3 buffer interface for FEC (Virtex-5,-6) and SRU (Virtex-6)
  - DTC link code for FEC and SRU
  - Port GbE and Texas ADC interfaces (ADC card) to Virtex-6

Summary

NEXT-1 readout electronics well advanced.

Still, some firmware development and debugging to be done.

Need to modify PMT and SiPM front-end modules.

We have a clear roadmap to the final NEXT readout scheme.