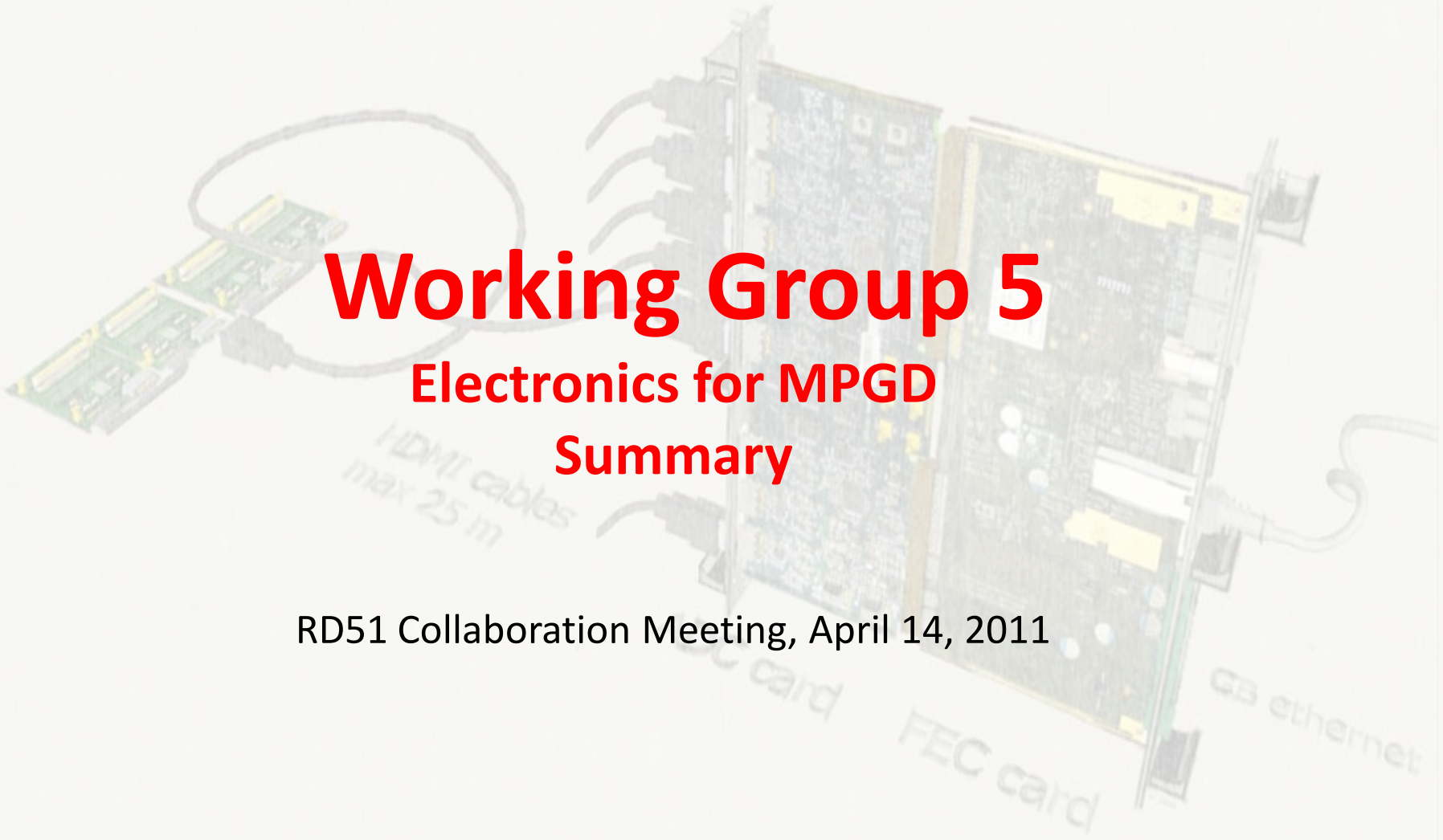


Working Group 5

Electronics for MPGD

Summary

RD51 Collaboration Meeting, April 14, 2011

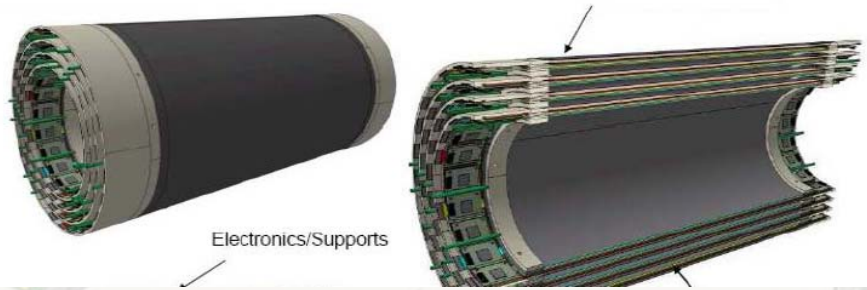
16 Talks !

- Test of readout plane production of the Inner Tracker in KLOE
- Status of the Nikhef miniHV Unit
- Signal processing requirements for the Muon Phase 1 Upgrade
- Status of APV based electronics for JLab tracker
- Some results with SRS readout and DAQ tests with THGEM
- First experience with small system SRS characterization
- Status and plans of SRS readout electronics for NEXT TPC
- Status of SRS readout electronics for resistive strip Micromegas
- Status of the medium-sized SRS readout electronics with DATE and AMORE for Muon Tomography using GEMs
- Data reduction and feature extraction firmware for SRS
- Status of the Timepix readout
- Status of the Labview readout of APV hybrid via SRS
- Status of the Scalable Detector Control (SDC)
- CMS Upgrade and synergy with RD51
- Status of SRS/SDC hardware and firmware, SRS demo
- SRS systems: where will/should we go from here

A. Ranieri on behalf of IT Kloe2 Group

The cylindrical GEM IT detector for KLOE2 experiment @LNF

Inner Tracker Layout - CGem 4 Layers design



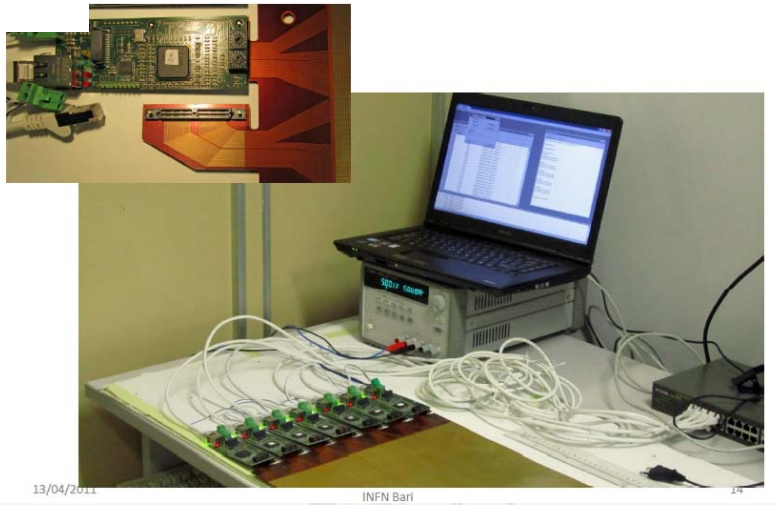
High resolution TDC system test design

The system has been designed:

1. To check lines connectivity (continuity)
2. To discover possible shorts

The system is based on a *delay chain* implemented inside FPGA-CLB measuring the propagation time of the reflected signal injected onto a microstrip.

Readout plane test system



Fred Hartjes, NIKHEF

Prices, availability

- 5 miniHVs are operational
  - Only for Nikhef use
- 20 miniHVs in preparation
  - Expected to be finished mid May 2011
  - Partly for Nikhef use
  - Price not yet fixed, but ~ € 1200 + 19% VAT (Europe)
- 10 modified power supply units in development (connected to line ground)
  - Expected to be finished July 2011
  - Price not yet fixed, but ~ € 400 + 19% VAT (Europe)
- In addition a CAN interface is needed (National Instruments or KVASER)

Send me an email if you're interested

F.Hartjes@nikhef.nl

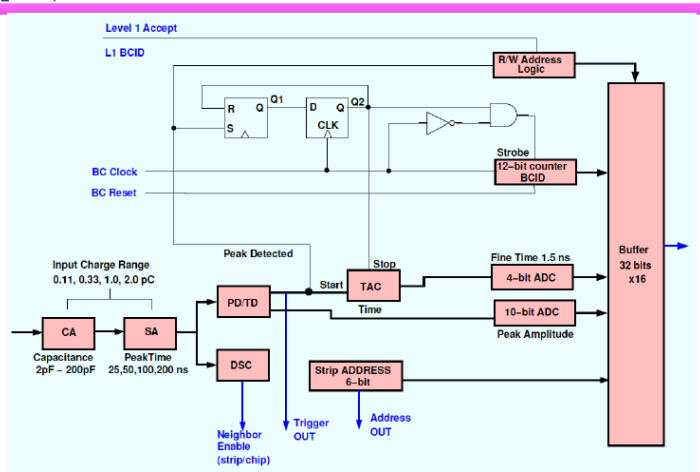
Will be exchanged by grounded AC power connection

Electronics,for Phase 1 Muon Upgrade

- An effort was launched late last Summer do develop a system that:
  - Can be used by either mMegas or TGC detectors (most likely technologies)
  - Utilizes a peak detector and time stamp concept developed at BNL for several applications including a GEM-based TPC with similar signal processing requirements
  - This concept results in a data driven system with automatic zero supression
  - Simultaneous read/write with built-in Derandomizing Buffers
- Further design parameters
  - Able to provide Trigger Primitives for on-detector track segm
  - Built-in ADC

- 1 mrad with a lever arm of ~0.5 m requires spatial resolution ~ 0.5 mm
- Trigger must be deadtimeless
- Pipeline @ 40 MHz
- Total time available 37 BC (includes 16 BC transit time to counting room)

Block Diagram of the IC being designed



Paolo Musico , INFN Genova

Status of APV based electronics for JLab tracker

Second prototype

Used in November 2010 DESY test beam.

Well usable. No big modifications.

Introduced HDMI connectors.

Added delay line for CK phase tuning.

Still only raw data processing.

Two boards fabricated.

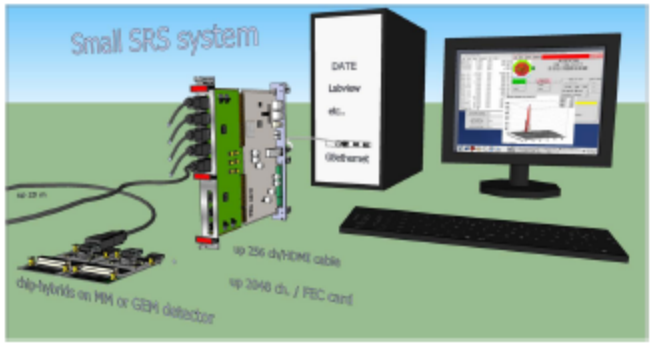
Electronic Noise < 1 LSB (RMS).

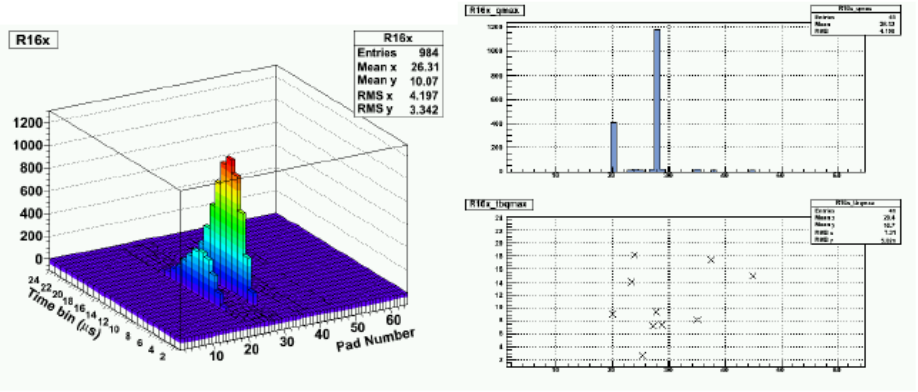
RD51 front-end compatible with HDMI-A.

Now used for development.

Some results with SRS readout and DAQ tests with THGEM

Hugo Natal da Luz et al.





- Each event can be visualized separately,
- Charge shared between pads 20 and 28 (adjacent ones).

- Although still in a developing stage, fits THGEM requirements very well;
- Provides very useful amount of information;
- **Very important:** no damage, even when operating at severe spark regime.

Francisco Garcia , HIP

Characterization of Small Scalable Readout System at HIP

Small Scalable Readout System

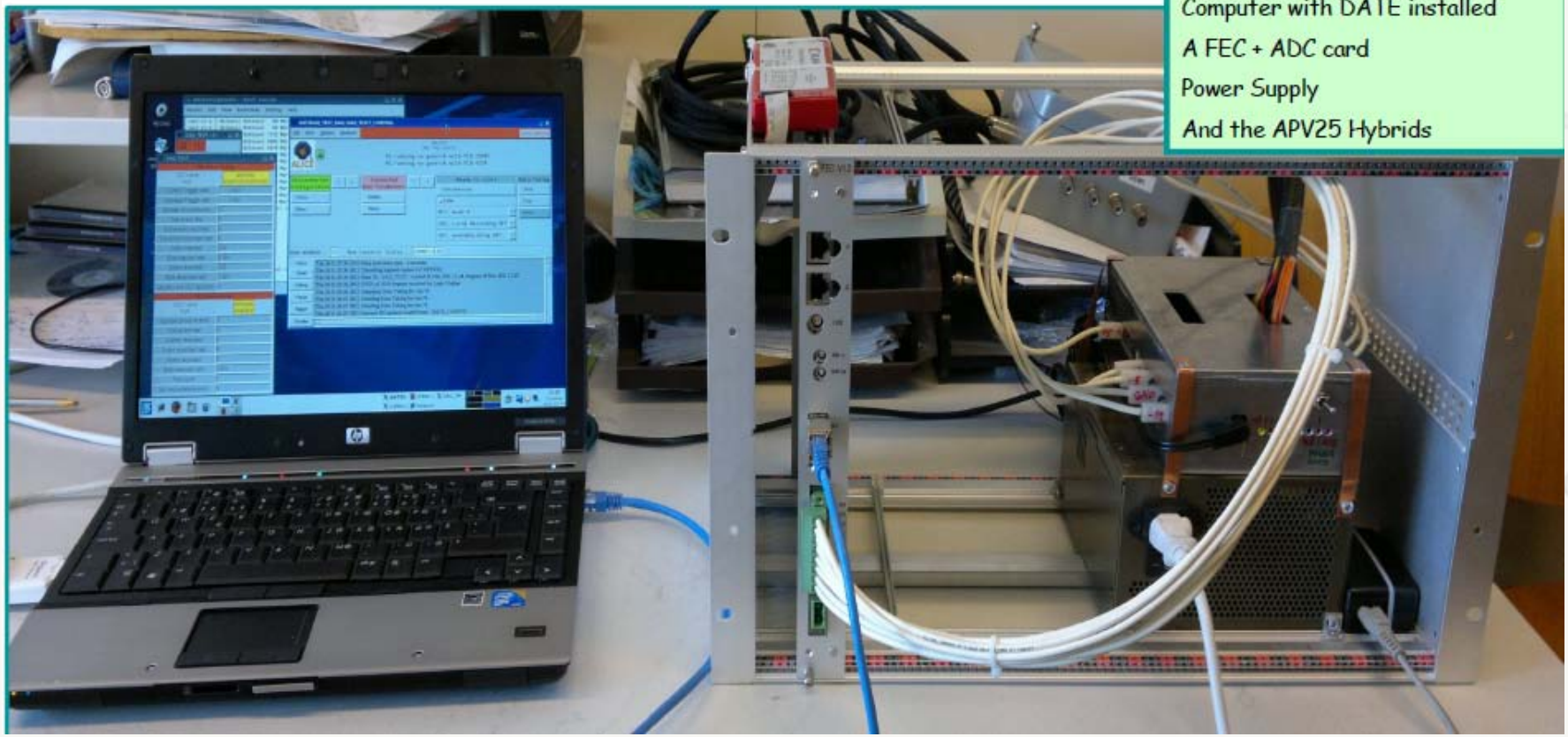
The system consists of:

Computer with DATE installed

A FEC + ADC card

Power Supply

And the APV25 Hybrids



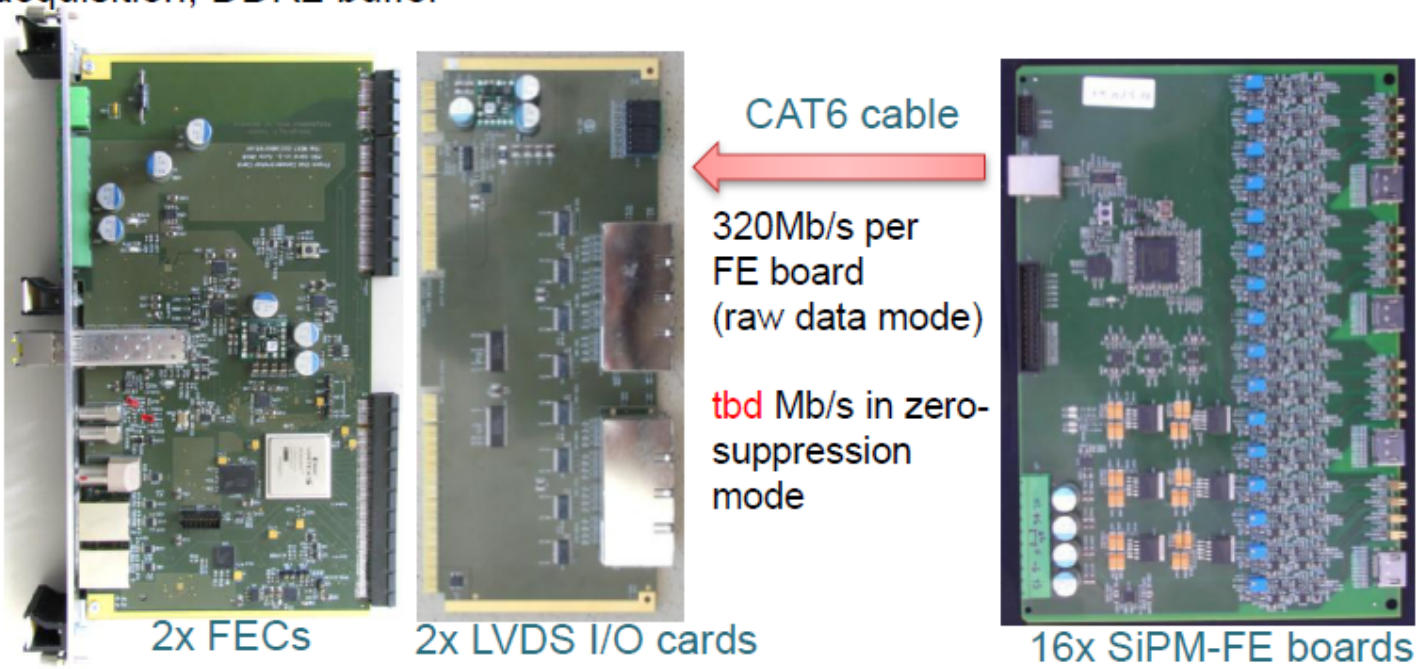
Jose Toledo, UPV Valencia

SiPM readout scheme in NEXT-1

Tested
- Raw readout mode: (1) stores 96 ch/FEC, 384 us data in FPGA FEC, (2) sends event to DATE, (3) ready for a new trigger

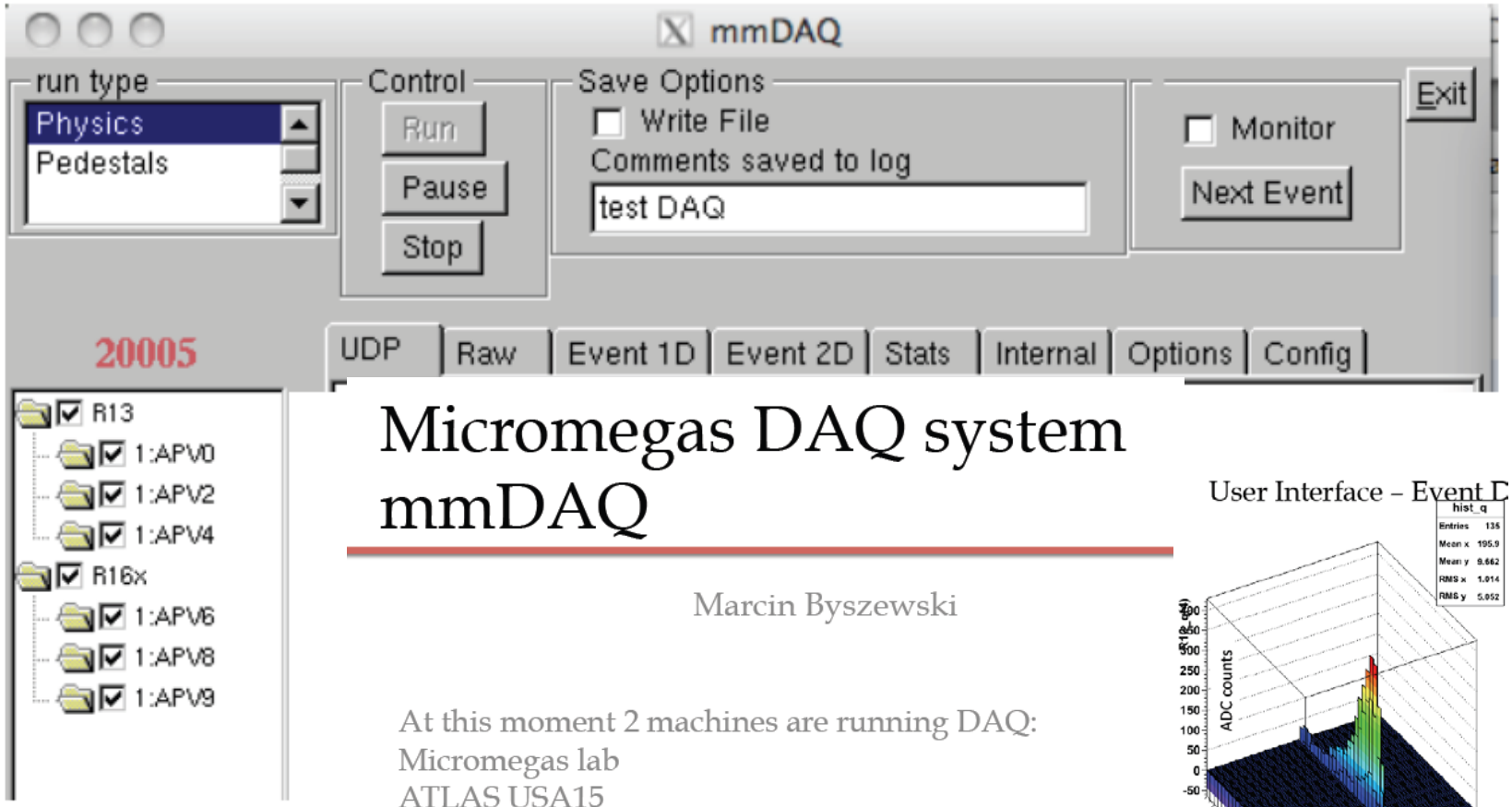
In test
- Raw data mode with DDR2 memory: 128 ch/FEC, longer buffer, still dead time

Untested
- Zero-suppression mode: up to 256 ch/FEC, no dead time, continuous acquisition, DDR2 buffer



Marcin Byszewski, ATLAS CERN

User Interface – Run Control



Micromegas DAQ system mmDAQ

Marcin Byszewski

At this moment 2 machines are running DAQ:
Micromegas lab
ATLAS USA15

Current Configurati

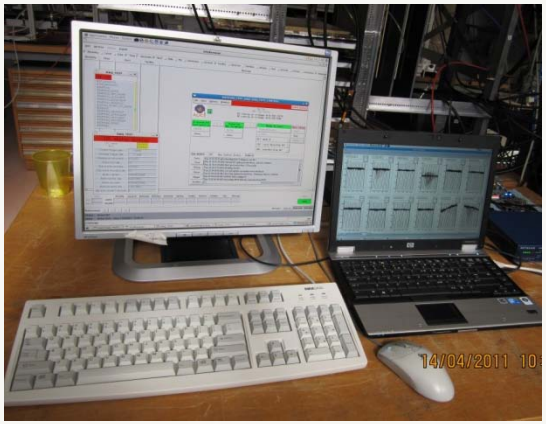
Medium-size SRS Electronics for Muon Tomography

Kondo Gnanvo, FIT Florida

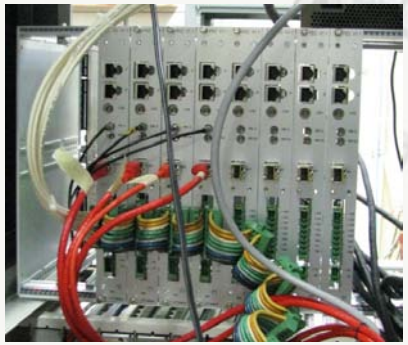
Trigger PMT

GEM test setup

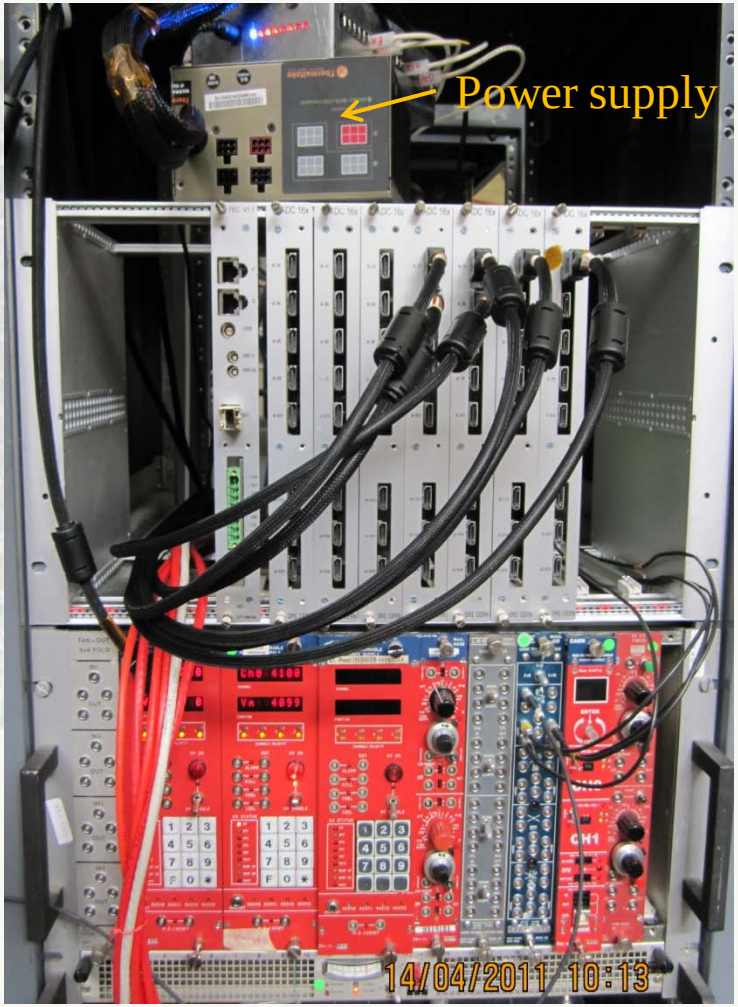
Network switch



DATE and AMORE PC



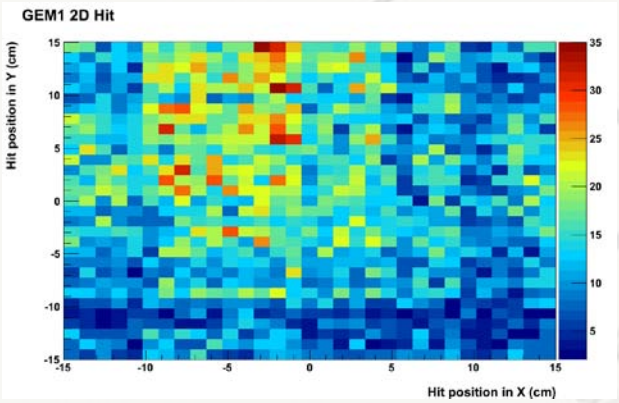
Back side of SRS FEC interface



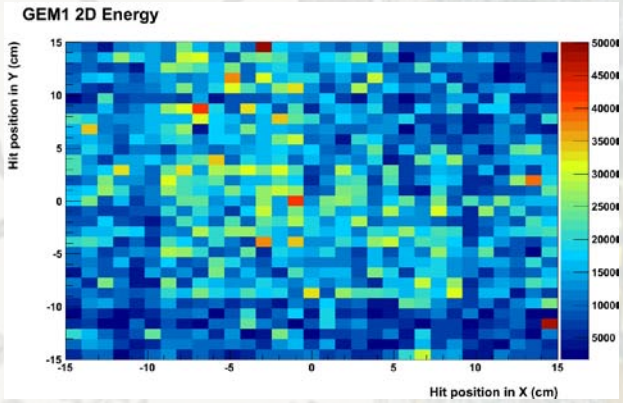
Front side of SRS: C-Cards interface HV supply for the GEMs

Preliminary results: Test of GEM1

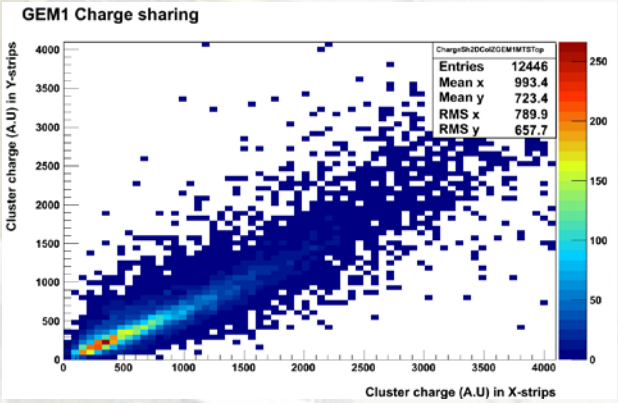
2D hit distribution



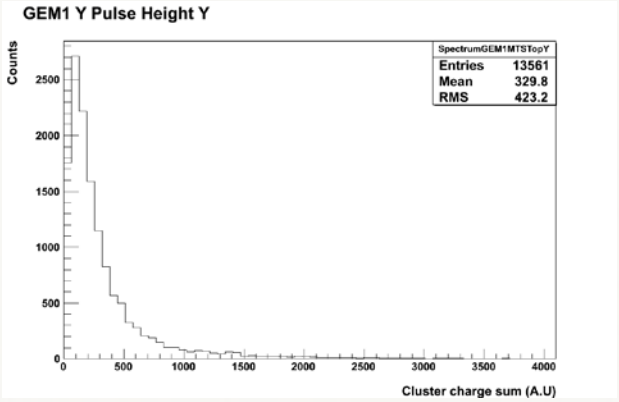
2D charge distribution



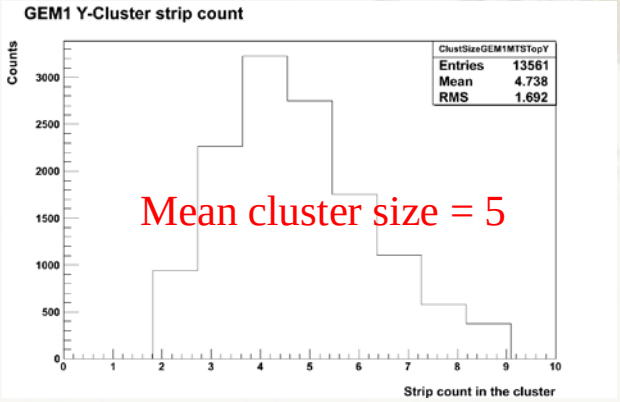
X/Y charge sharing



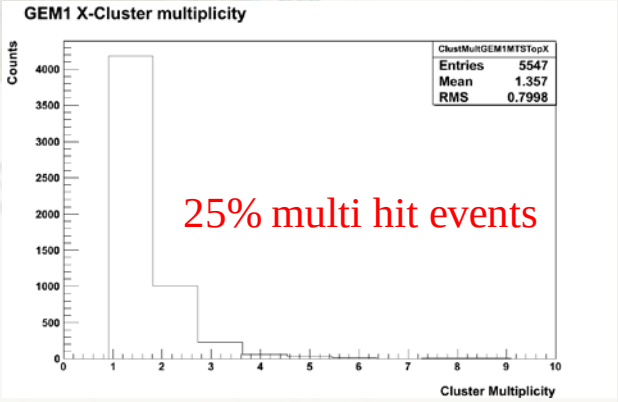
MIP spectrum



Cluster size distribution

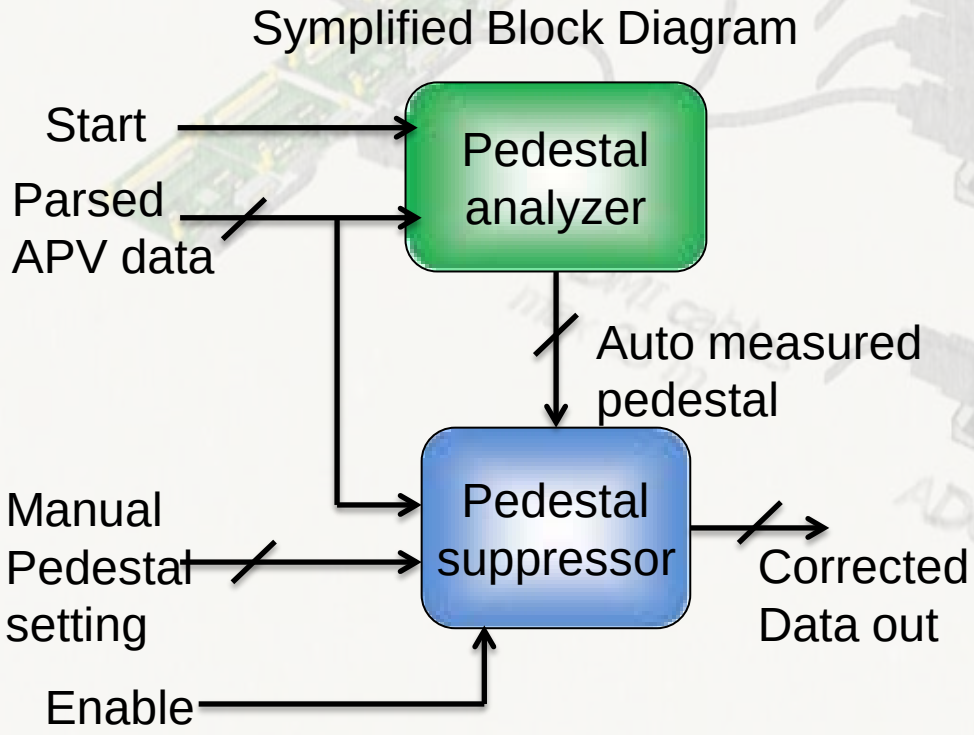


Cluster multiplicity



Alberto Aloisio on behalf of Raffaele Giordano, INFN Napoli

Pedestal Measurer & Remover



- Two pedestal setting mode
  - Automatic: acquire the pedestal from the stream (parsed APV data)
  - Manual setting of the pedestal via a dedicated port
- Enable/Disable pedestal removal
- Fully pipelined

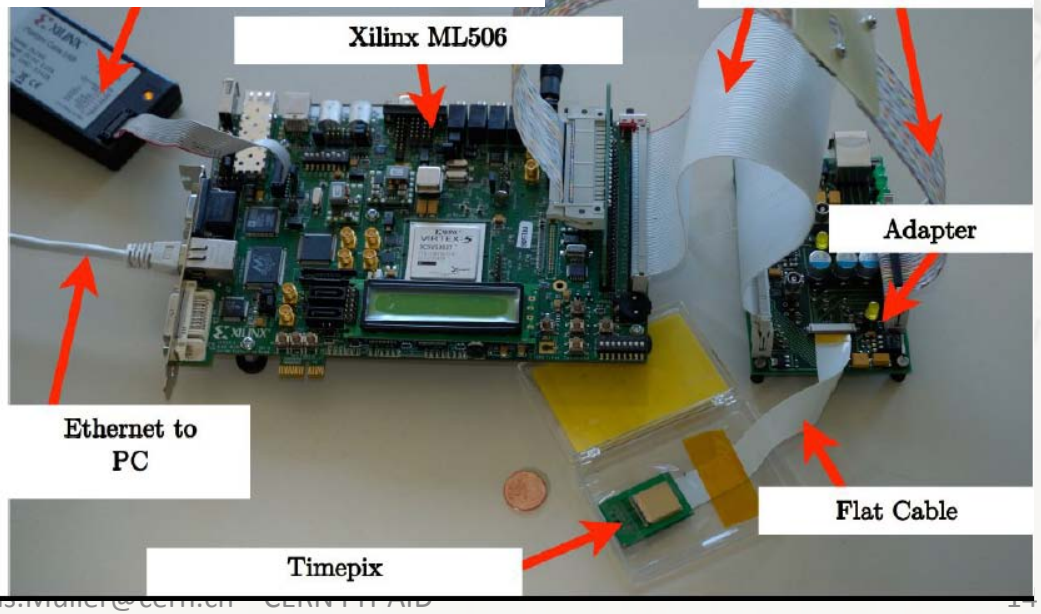
Michael Lupberger, Uni Bonn

New readout system

- Goals:
  - ultimately read out ~100 chips
    → large area detector (e.g. full TPC endplate module)
  - modular system → use SRS (RD51)
  - ethernet based
  - use Virtex6 FPGA
  - zero suppression
  - triggerable, integrate with slow control & calibration
  - Timepix2 compatibility in view

Readout chip: The Timepix chip

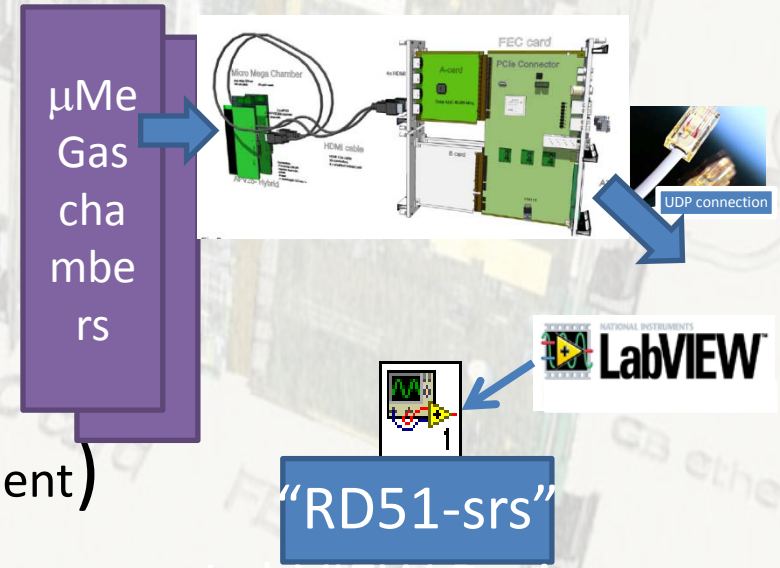
Properties
- 1,4 x 1,4 cm² active surface
- 256 x 256 pixel matrix
- CMOS 250 nm technology, IBM
- 55 x 55 µm² per pixel
- amplifier/shaper (t_{rise} ~150 ns)
- 14 bits count clock cycles
  → Pixel pit when/how long
- clock up to 100 MHz in every pixel
- lower threshold
- noise level ~ 500 e-



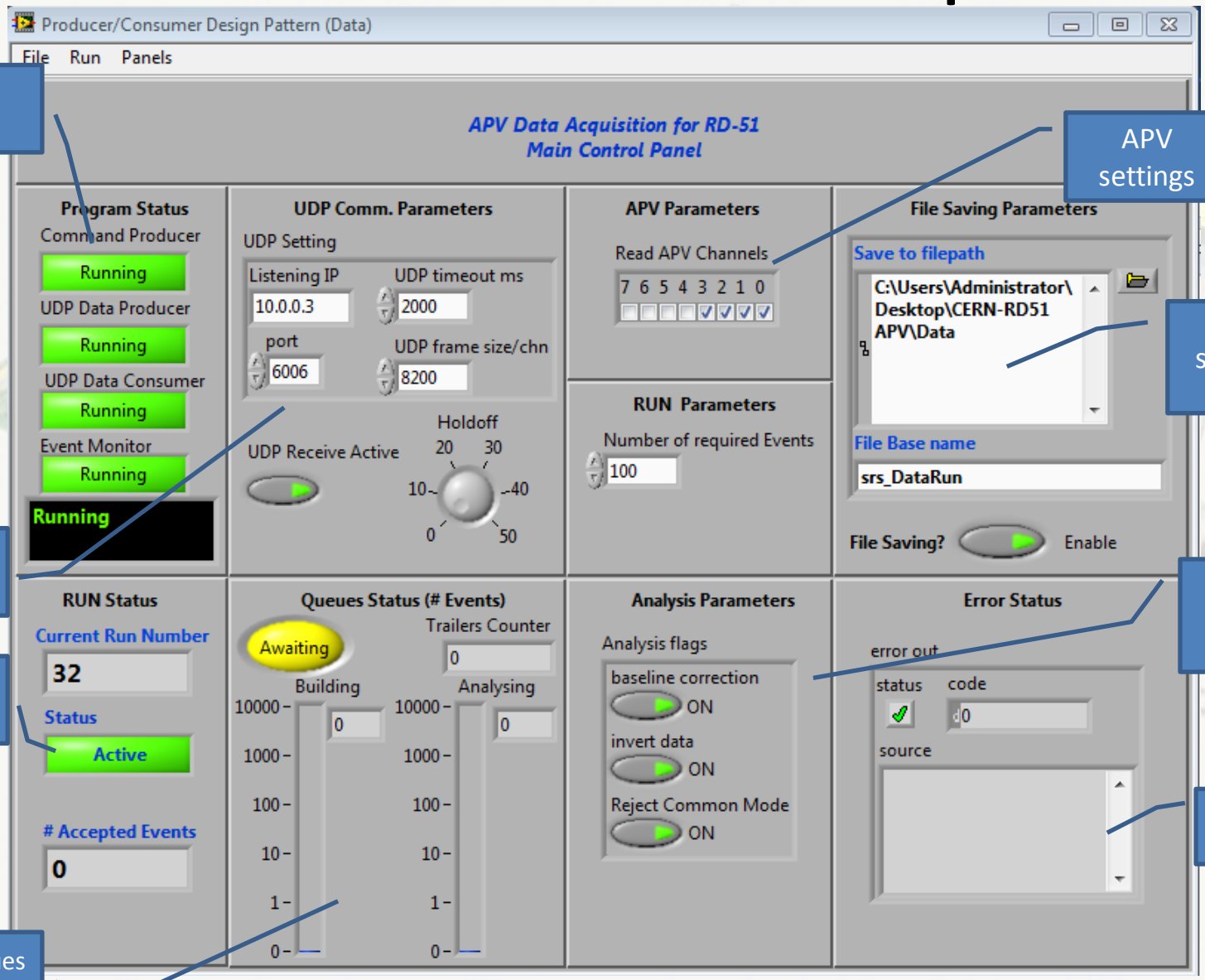
Riccardo de Asmundis
INFN Napoli
[Certified LabVIEW Developer]

LabVIEW RD51-srs

- ~30 modules developed (VIs)
- GUI (Graphical User Interface)
- Monitors for data flow
- RUN handling
- File saving
- Data quality monitor (under development)



Labview Main control panel



Running Processes control

APV settings

Data Files saving paths & Naming

UDP Parameters

Online analysis parameters

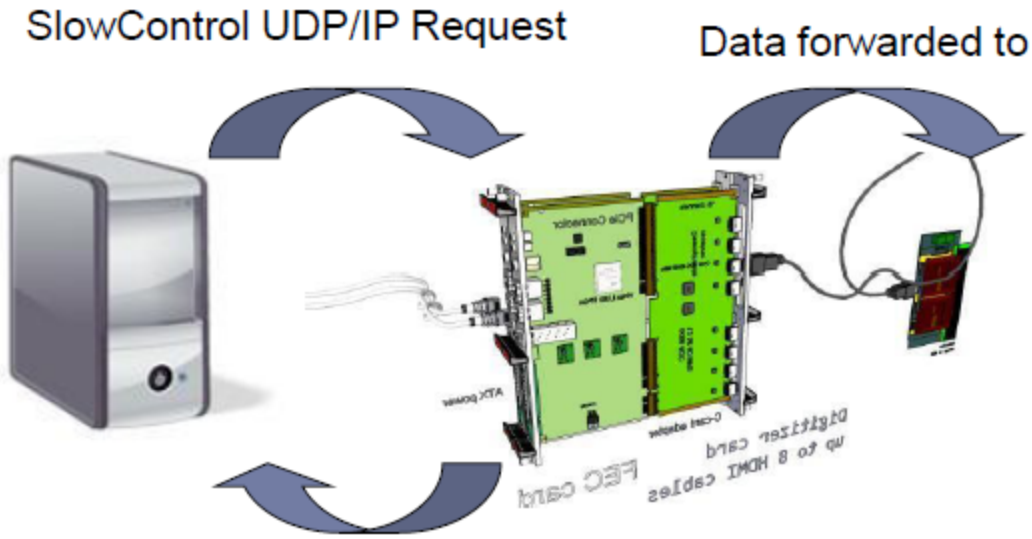
RUN status control

Error status

Internal queues occupacy

Sorin Martoiu, RD51 CERN

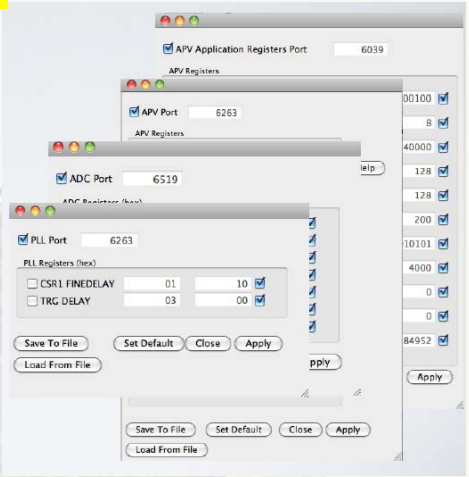
SlowControl over Ethernet



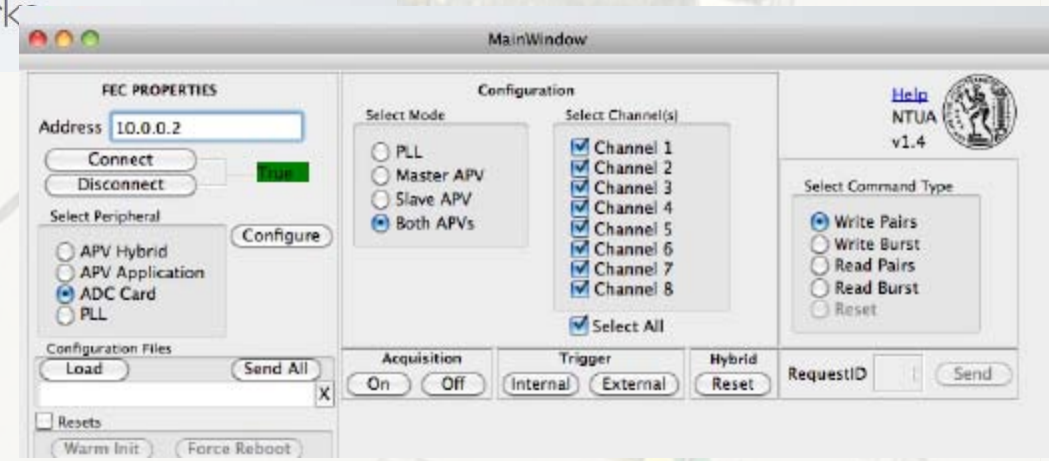
George Iakovidis, Konstantinos Karakostas, NTU Athens

What About SDC ?

- SDC is replacing the existing readout electronics control done until now through USB interfaces.
- Get rid of USB restriction which was a bottleneck for ATLAS Micromegas installation.
- Developed within Qt and C++ framework



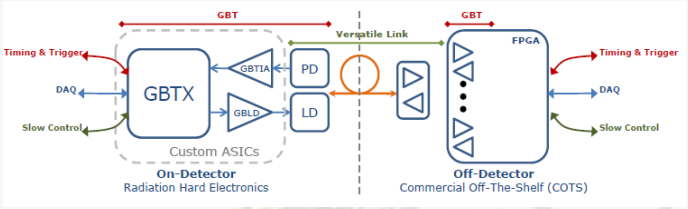
- Version **1.4.1** Ready and Stable
- Implemented Log files on Request
- Broadcast mode
- IP Range Initialisation
- Implement forthcoming chips eg BNL chip
- Error handling mechanism improvement



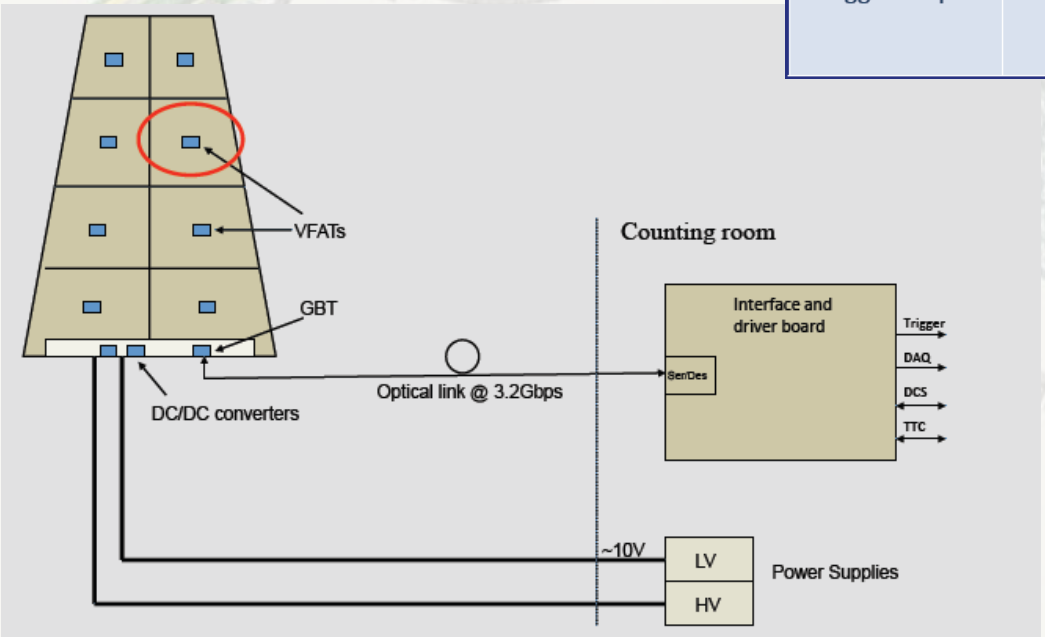
Public Twiki page for SDC

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/SDC

Paul Aspell, CERN



	Analog Memories	Binary	DSP
Examples	APV PACE	VFAT Pixels	Saltro GdSP
Age	Development some years ago. (LHC)	Now (LHC & SLHC)	Future (SLHC ?) (ILC/Clic)
Threshold	no	analog	digital
Common mode subtraction	offline	no	Yes (GdSP), on-line
Trigger output	no	yes	Yes (lower noise, longer latency)



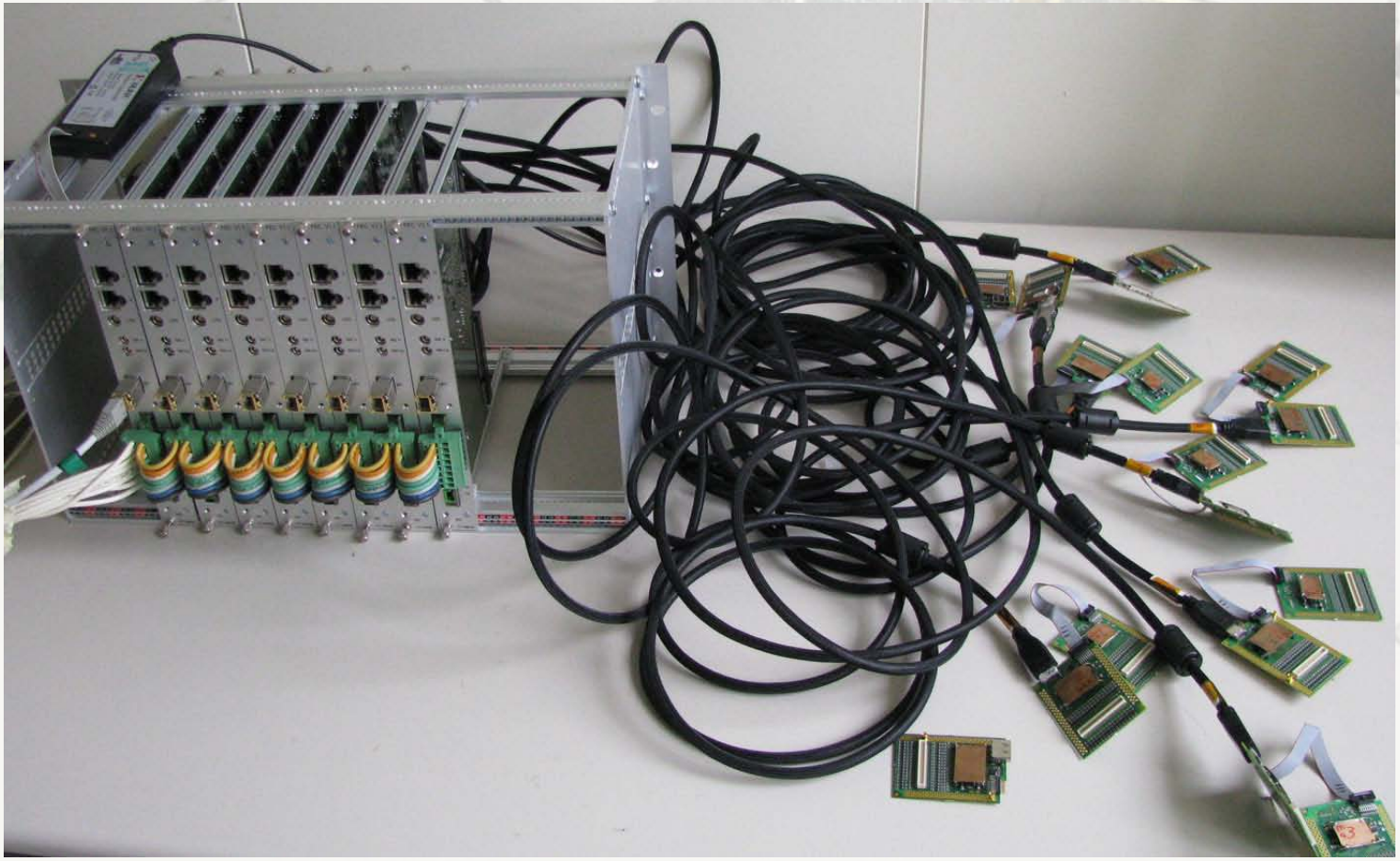
Very early days but
The big picture is taking shape:

Large GEM detectors
Front-end ASIC ideas : VFAT3/GDSP ?
Chip power and signal routing on the GEM.
GEM design as a stand alone electronic module.
Use generic R&D existing in CERN for the upgrades such as :
DC/DC powering
GBT and Versatile link optical communication and readout.

Hans Muller, CERN

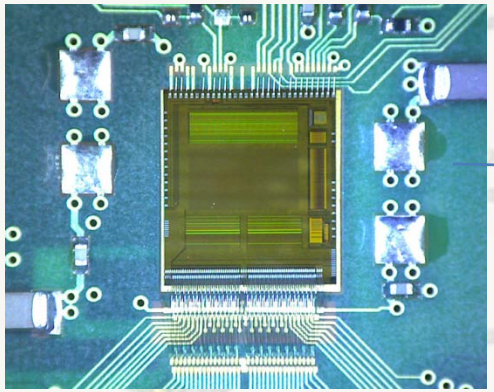
Medium-sized system (FIT)

8 FECs for 16 k APV channels



Frontend hybrids

so far all based on APV25 chip



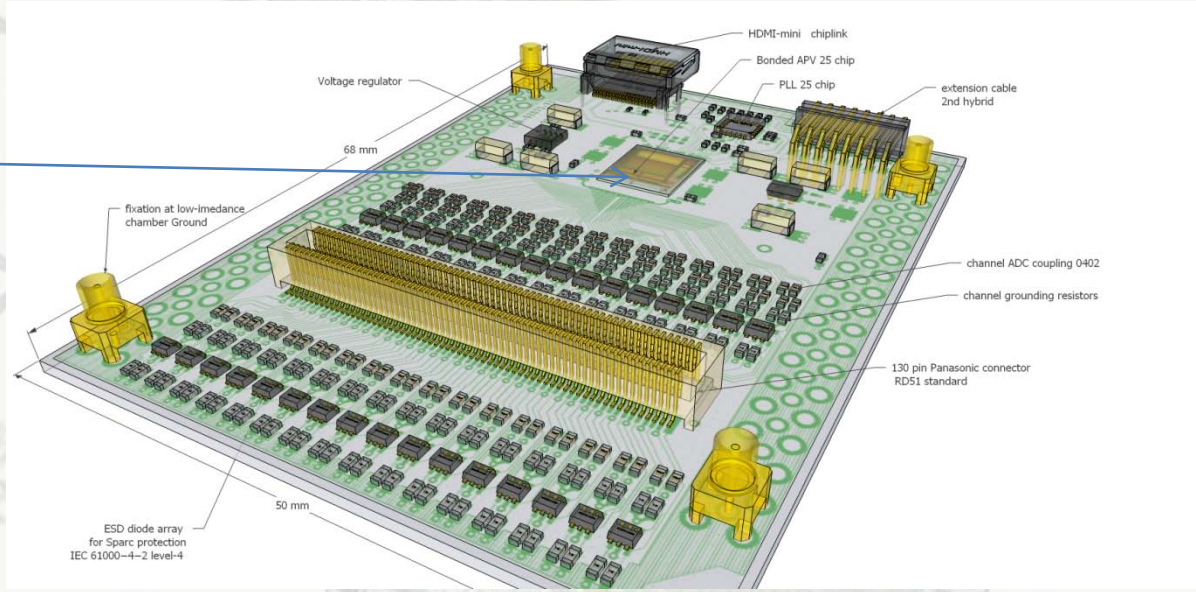
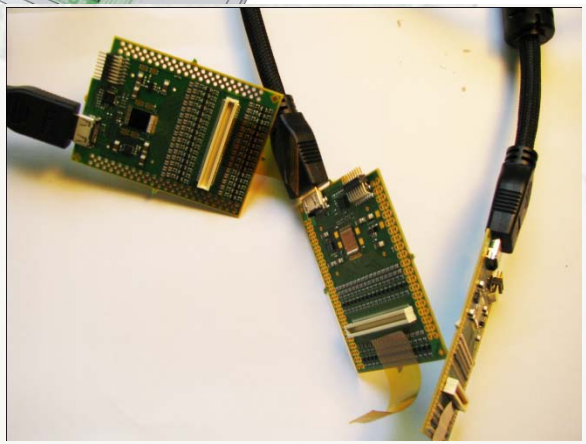
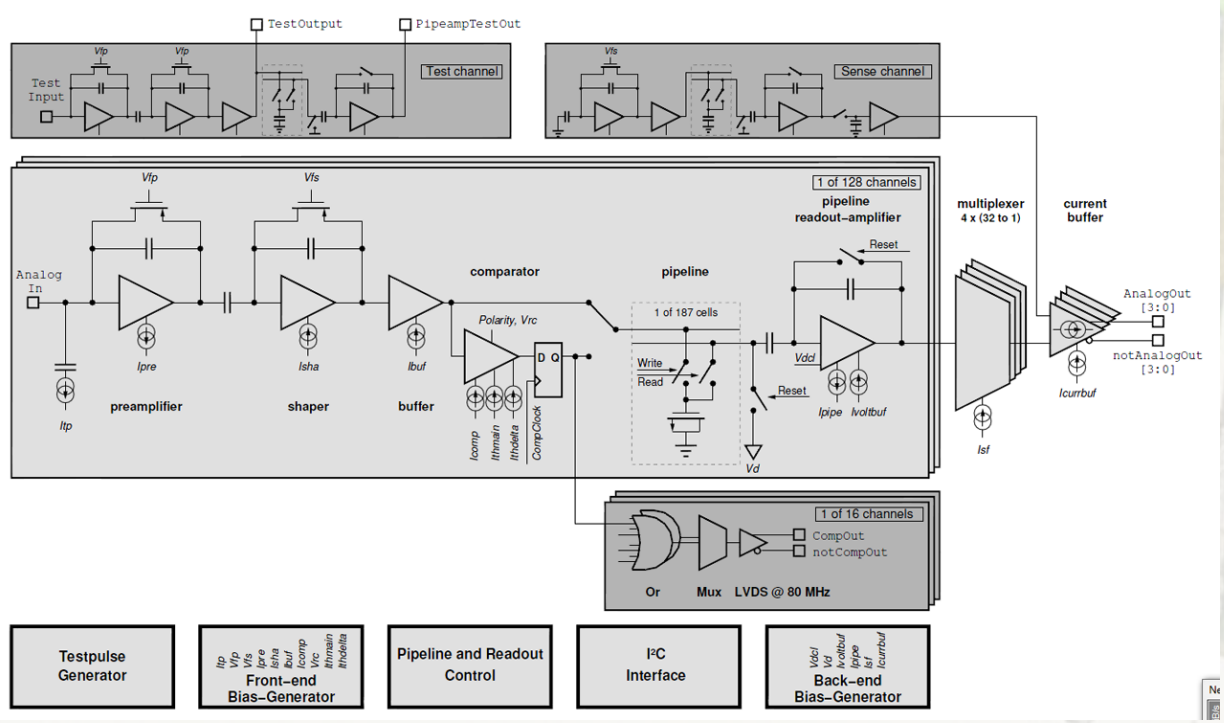


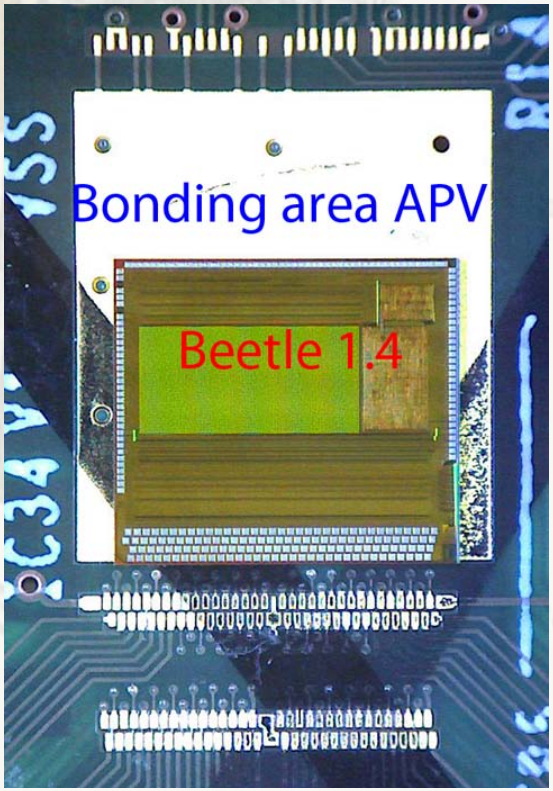
Photo of wire-bonded APV on RD51 hybrid Version 3



Version 1 proto: 5 working ones
Version 2 users: 11
Version 3 systems: 15 (CERN: Rui + bonding service)
292 (ELTOS + Hybrid SA)
under production this week

Beetle hybrid for SRS





Lorne Levinson, WIS

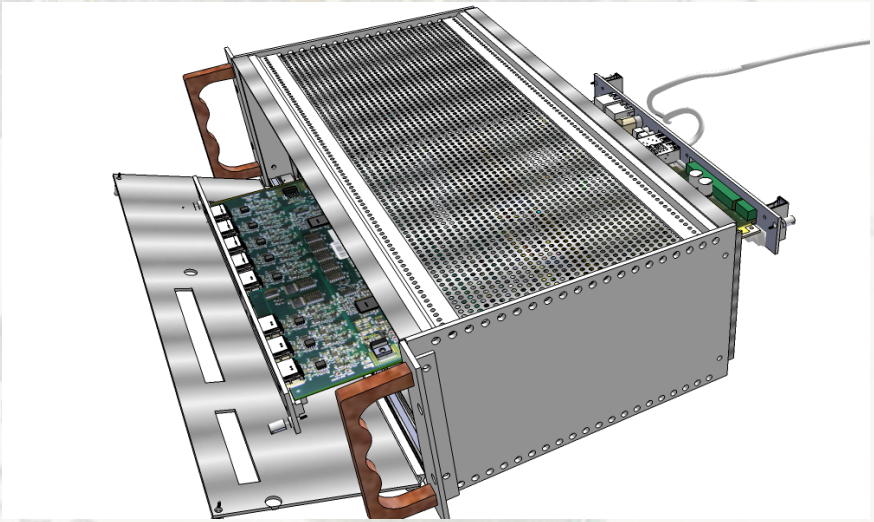
Beetle Carrier for SRS – II

Status

- Like AVP carrier, this board requires direct bonding from the chip pads to the PCB.
- PCB traces and vias are smaller than most PCB houses can do.
- Layout is almost complete.
- Fabrication by same companies as for the AVP carrier
- First version: trigger CPLD is not rad hard, perhaps rad tol to 100krad
- Expect PCB to be sent for fabrication in 2-4 weeks
- Please tell how many boards you would like.

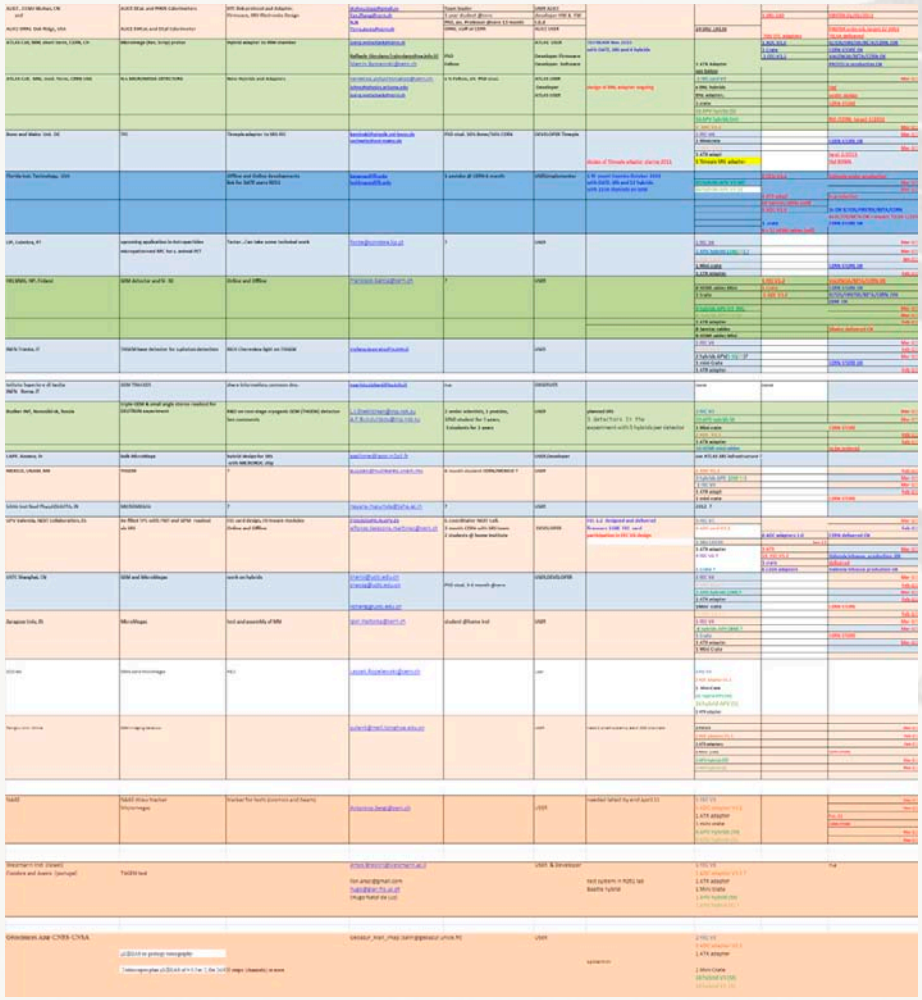
Eurocrate vs Minicrate

Eurocrate 6U: up to 14 positions, power not included



Minicrate 3U , max 2 positions, power included

Registered SRS Users



CERN experiments

- ATLAS CSC upgrade Micromegas
- ALICE EMCaL , SRU-based readout backend
- NA62 Straw tracker

Other HEP experiments

- NEXT Collaboration, dual Beta decay, SiPM, PM
- BUDKER, INP, Deuteron, triple-GEM

Applications with Cosmic Tomography

- FIT Florida, homeland security, GEMs
- Geoscienes Azur CRNS- Waterquality, MMegas

R&D with MPGD's (small systems)

- Weizmann Inst. Sci., THGEM tests
- Tsinghua Univ, GEM Imaging
- Bonn/Mainz Univ, Timepix readout
- Helsinki HIP, GEM detector
- LIP Coimbra, micropatten RPC, for PET
- INFN Trieste, THGEM photon detection
- MEXICO UNAM, THGEM
- SAHA Kolkotta, Micromegas
- USTC Shanghai, GEM and MicroMegas
- Zaragoza Univ, GEM and MicroMegas
- CE Saclay, Micromegas
- ..... some more non-confirmed