Timepix readout

A readout system for a pixelated TPC

Michael Lupberger

University of Bonn

RD51 7th annual meeting, 13th - 15th of April 2011 CERN

Titel

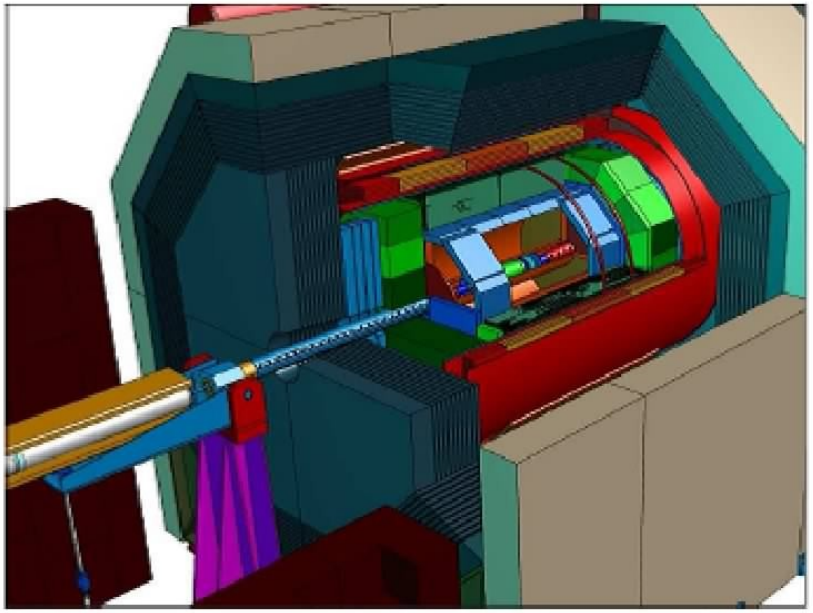
- Motivation
  - ILC detector
  - TPC tracking
  - Endplate concepts
- Timepix chip
- Readout system: status
- New readout system

universitätbonn

ILD

- International Linear Detector
  - constrains on momentum resolution: $\sigma_{1/p} \sim 5 \times 10^{-5}$/GeV/c
- Use Time Projection Chamber (TPC) as central tracker

Size	ø = 4.1 m L = 4,6 m
Momentum res	$\delta(1/p_t) \sim 10^{-4}$/GeV/c
σ_{point} in $r\Phi$	~100 µm
σ_{point} in rz	~ 0,5 mm
dE/dx res	< 4,5 %

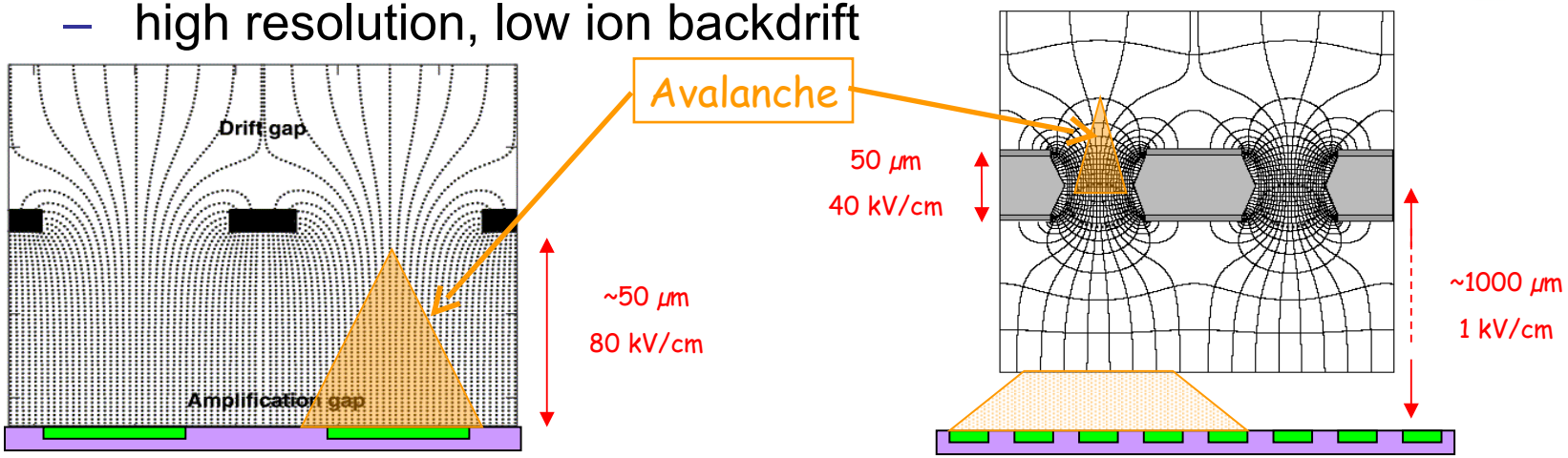


- For high point resolution
  → use micro pattern gaseous detectors

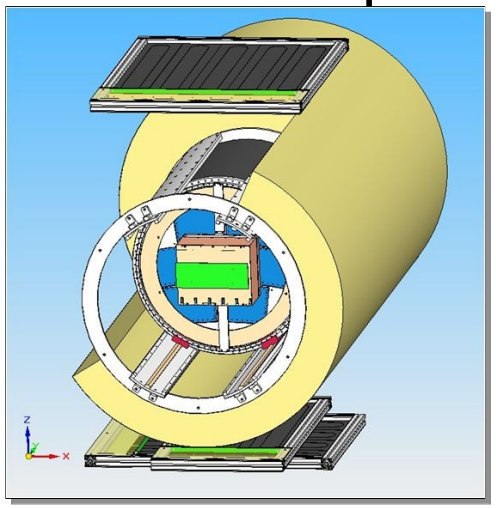
universitätbonn

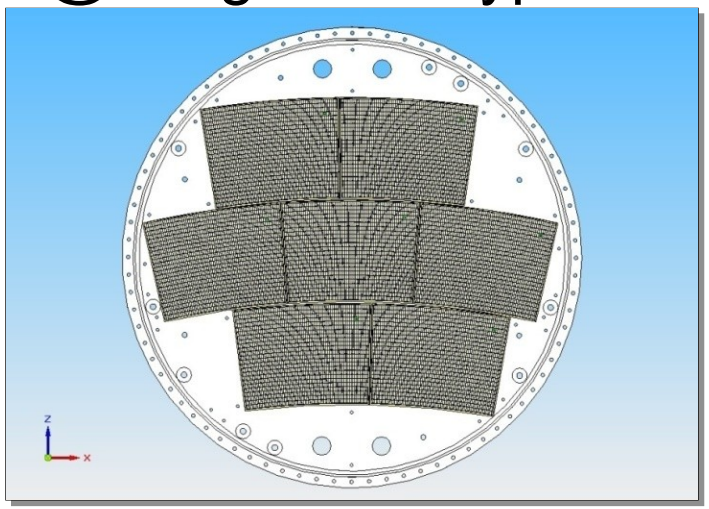
MPGDs

- Gas amplification process: Micromegas or GEM
  - high resolution, low ion backdrift



- Readout structure: Pads or pixel
- Different setups tested @ Large Prototype of LCTPC collab.

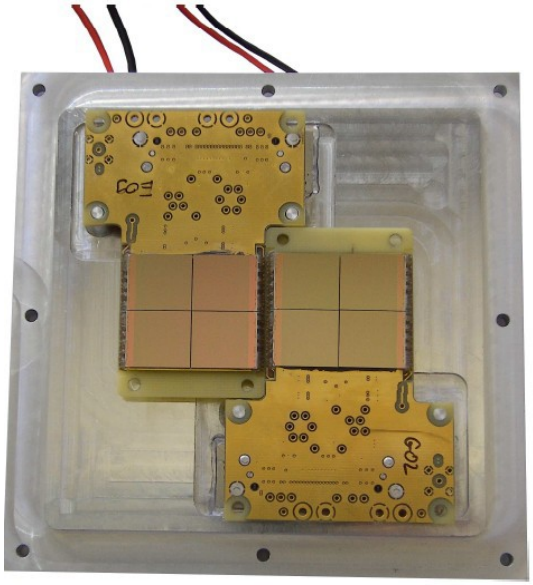




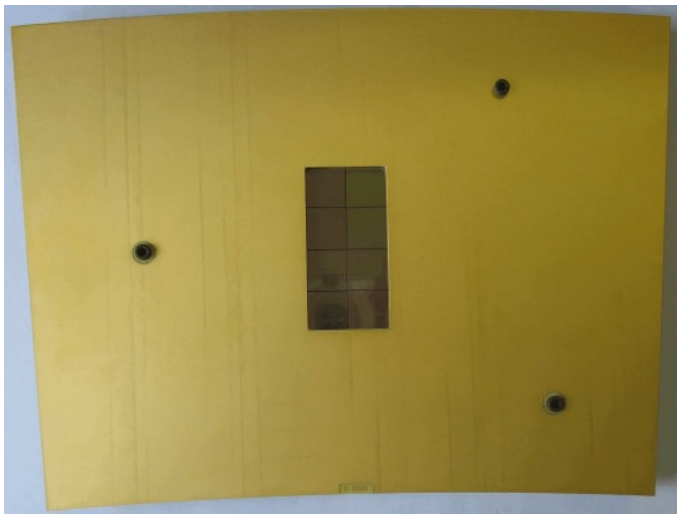
universitätbonn

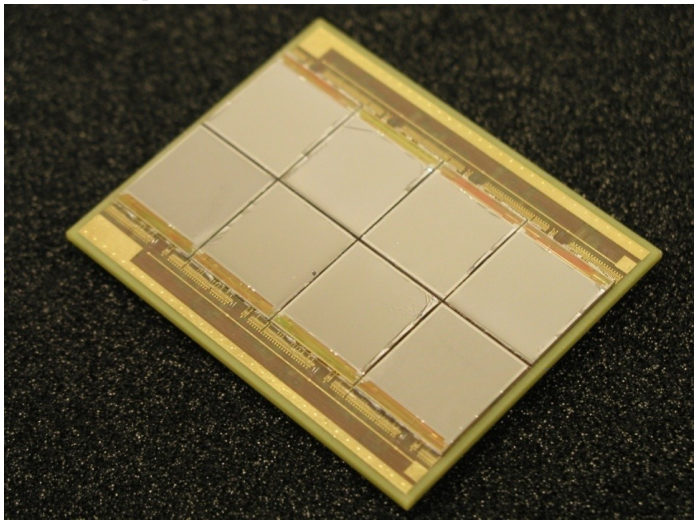
Pixelated endplate

- Until now: only few pixel chips for readout
- Bonn/NIKHEF: GEM + pixel



- CEA Saclay: Micromegas + pixel

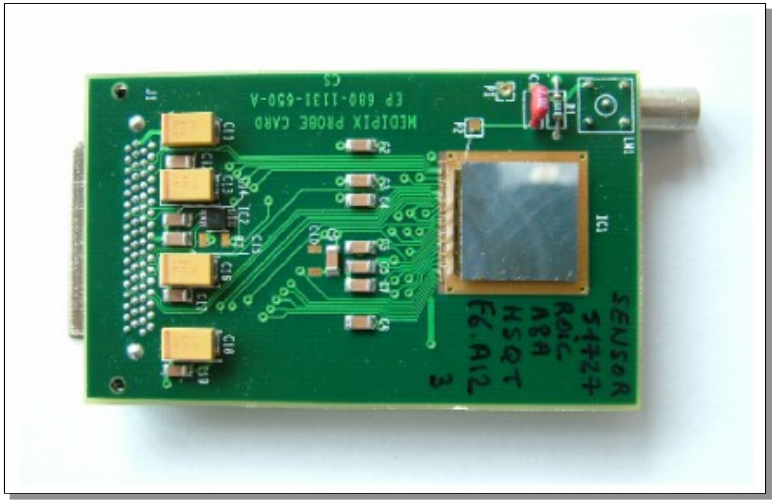




universitätbonn

Timepix chip

- Readout chip: The Timepix chip



- Properties
  - 1,4 x 1,4 cm² active surface
  - 256 x 256 pixel matrix
  - CMOS 250 nm technology, IBM
  - 55 x 55 µm² per pixel
  - amplifier/shaper (t_{rise} ~150 ns)
  - 14 bits count clock cycles
    → Pixel pit when/how long
  - clock up to 100 MHz in every pixel
  - lower threshold
  - noise level ~ 500 e-

universitätbonn

Timepix chip

- 4 different modi to operate

  – Medipix:

Pixel hit how often

  – Time-over-threshold:

Pixel hit how long

→ proportional to charge

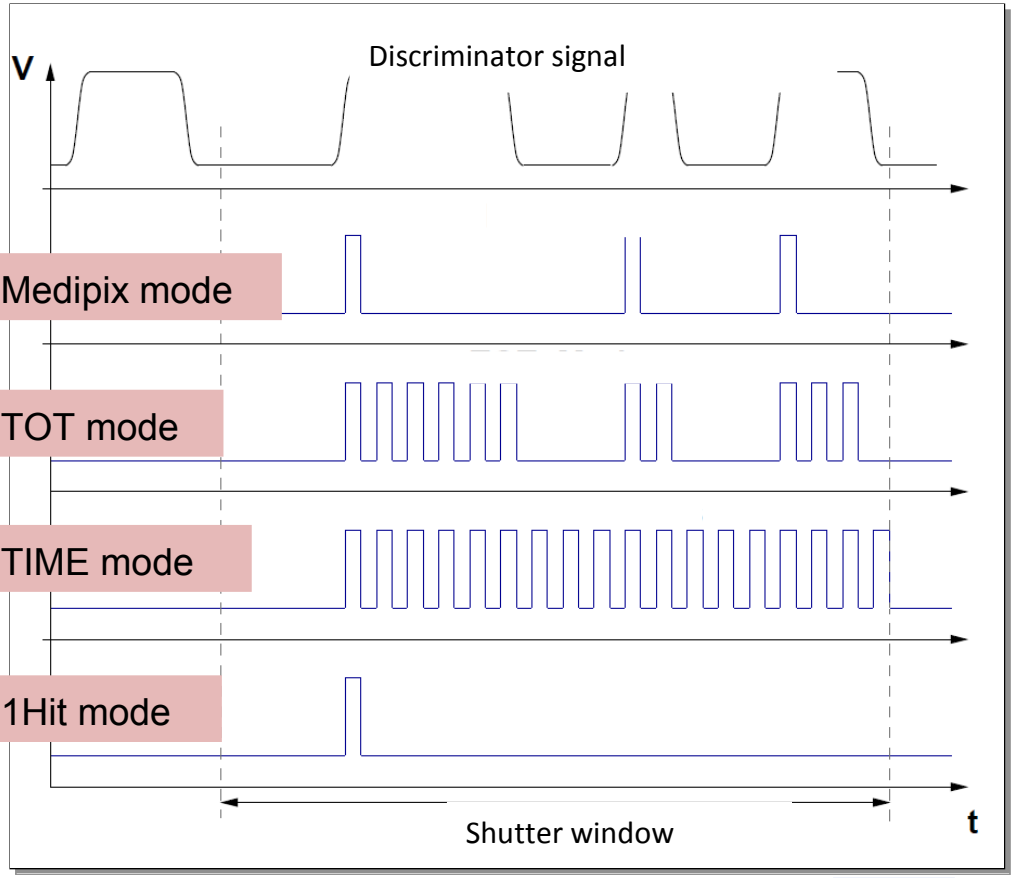
  – Time:

Pixel hit when

→ time of arrival

  – 1Hit:

Pixel hit in shutter window



universitätbonn

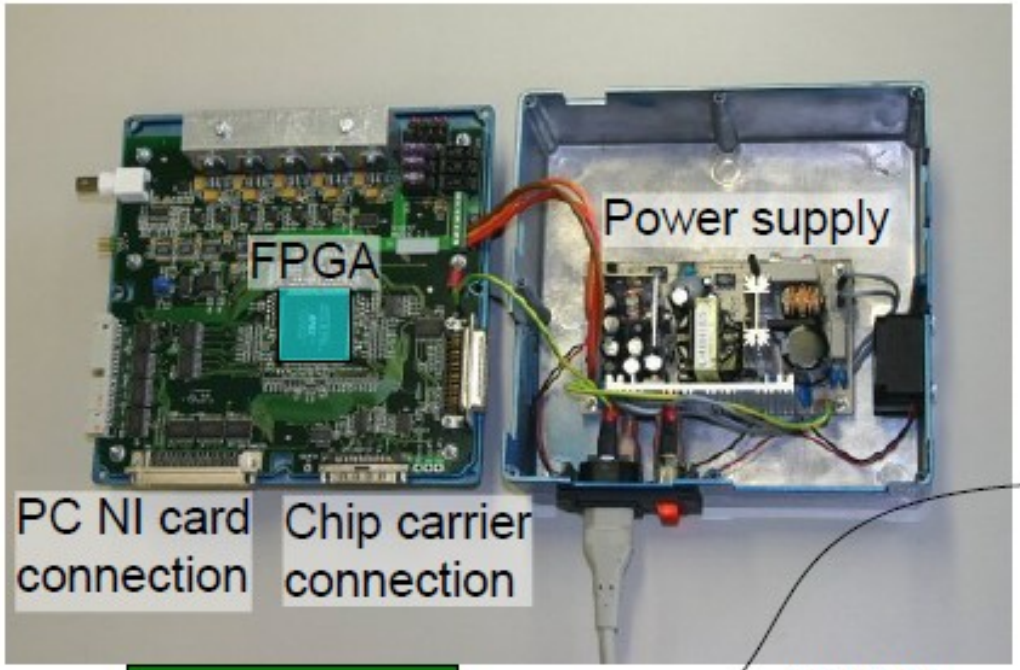
Readout system: status

- MUROS v2.1:
  - designed at NIKHEF for Medipix2 and Timepix chip readout (new FPGA code)
  - serial readout for at most 8 Timepix chips
  - VHDCI cable <3 m to Timepix carrier board
  - VHDCI cable to NI card in PC
  - Timepix readout: theo. < 50 frames/sec
    lowered by shutter length
  - adjustable readout frequency [<240MHz]
  - data acquisition on PC(Pixelman software)

http://www.nikhef.nl/pub/experiments/medipix/muros.html

universitätbonn

Readout status



- Problems with MUROS v2.1:
  - only limited availability, no production
  - NI card and driver out of date
  - at most 8 chips daisy chained

universitätbonn

New readout system

- Goals:
  - ultimately read out ~100 chips
    → large area detector (e.g. full TPC endplate module)
  - modular system → use SRS (RD51)
  - ethernet based
  - use Virtex6 FPGA
  - zero suppression
  - triggerable, integrate with slow control & calibration
  - Timepix2 compatibility in view

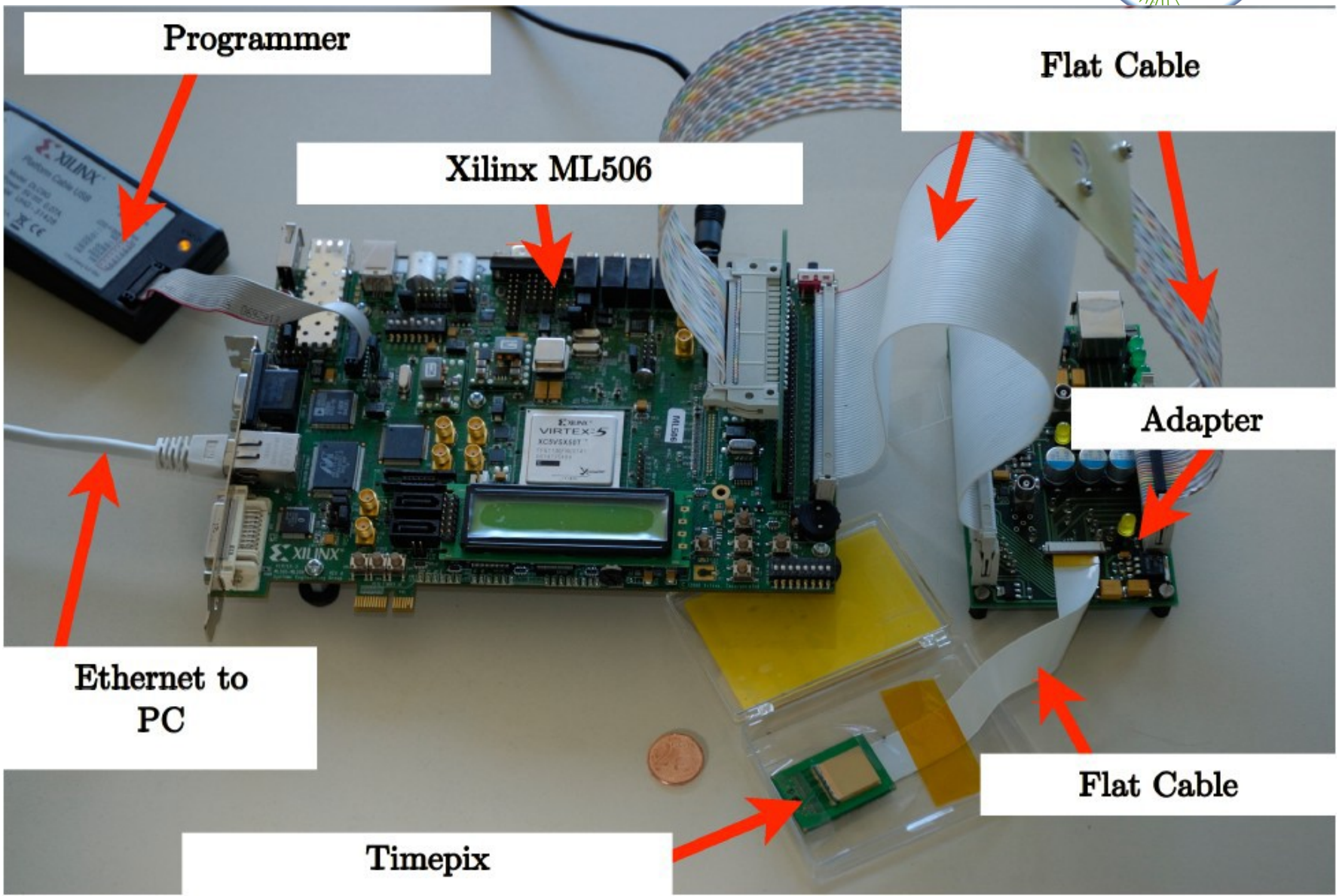
universitätbonn

First steps

- Single chip readout (Uni Mainz)
  - Timepix chip on FR4 carrier
    - LVDS link
  - Adapter board
    - trigger
    - test pulses
    - power supply
  - Xilinx ML506 evaluation board (Virtex5)
    - Timepix control
    - ethernet (UDP) communication
  - PC software
    - command prompt based
    - Timepix control
    - data acquisition

universitätbonn

Mainz readout system



FPGA

- On-chip Ethernet MAC
- On-board Gigabit Ethernet phy chip
  - 1000BASE-T
  - no embedded CPU
- Firmware
  - VHDL description
  - common clock for digitisation and data transfer, crystal based
  - serial/deserial interface to the Timepix bit-serial port
  - Timepix matrix data not buffered in FPGA
    → kept on Timepix while awaiting packet transmission
  - shutter with programmable delay and width
    - software control or
    - external trigger (TLU)
  - non-volatile storage of hardware description on CF card

universitätbonn

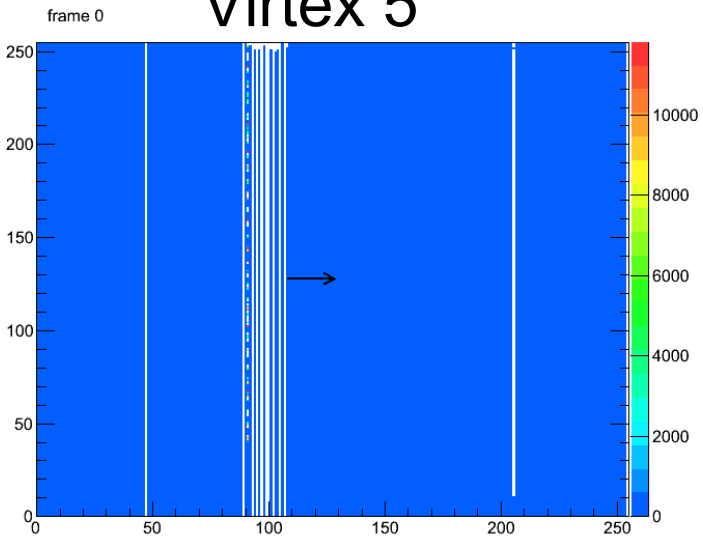
Bonn activities

- Setup of second Mainz system in Bonn
  - Xilinx ML506 board with Virtex5 FPGA
  - single Timepix readout
  - adapter board
- Re-target to Virtex6
  - Xilinx ML605 board with Virtex6 FPGA
  - firmware modifications to Virtex5 VHDL
    - new ethernet MAC
    - adapt to different clock and pin setup
    - implement Timepix control modules
    - solve timing problems
  - hardware modifications
    - new adapter board for cabling

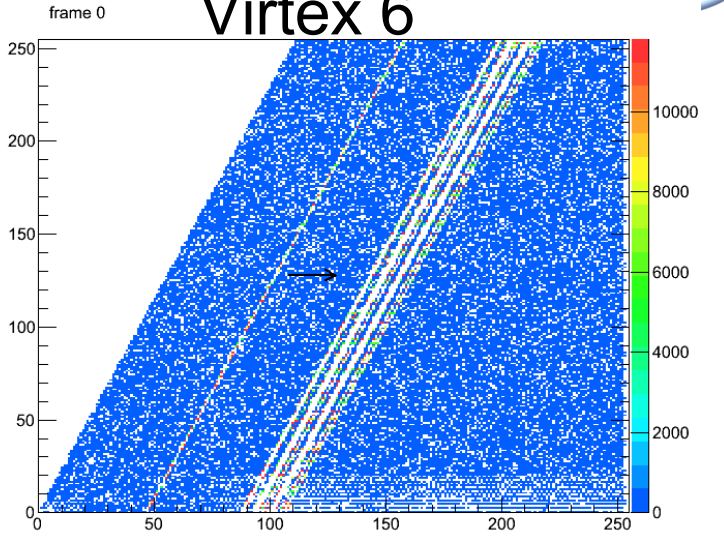
universitätbonn

TPC readout with V5/V6

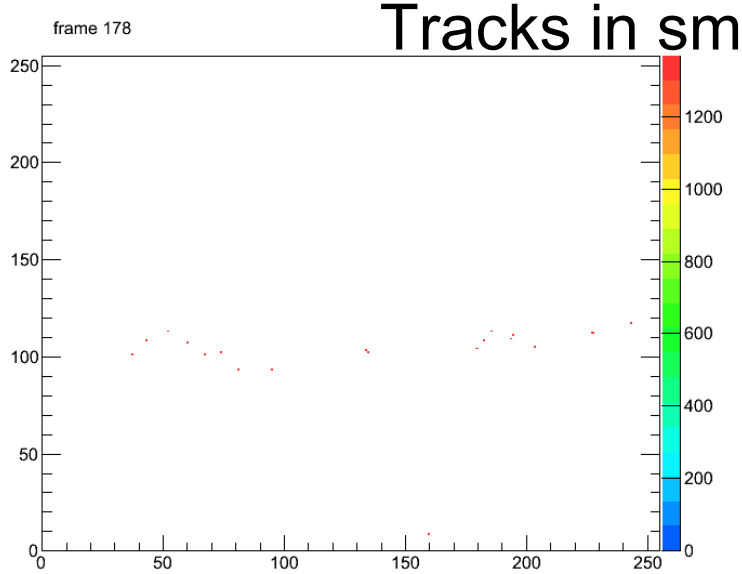
Virtex 5

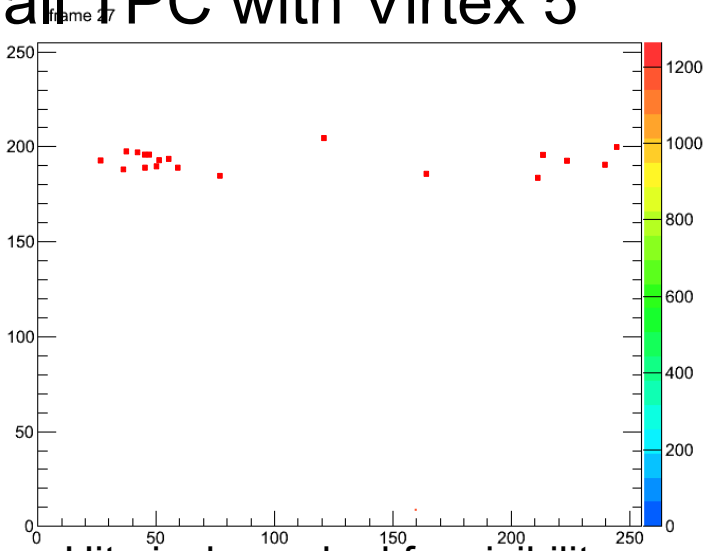


Virtex 6



Tracks in small TPC with Virtex 5





Hit pixels marked for visibility

universitätbonn

Way to go

- Use Modular system: Scalable Readout System SRS:
  - small set of modular components
  - performance at low cost
  - designed for scalability

  (e.g. 1 FEC for 8 chips x
  14 FEC/crate = 112 chips)
  - plugin-choice of frontend ASICs → to do

- Multi chip (first step: 4 or 8) readout with Virtex6 (Bonn)
- Or single chip readout with SRS
- Mechanics of box to house Readout card, including all connectors, supplies, switches and LEDs (Saclay)

universitätbonn

Summery

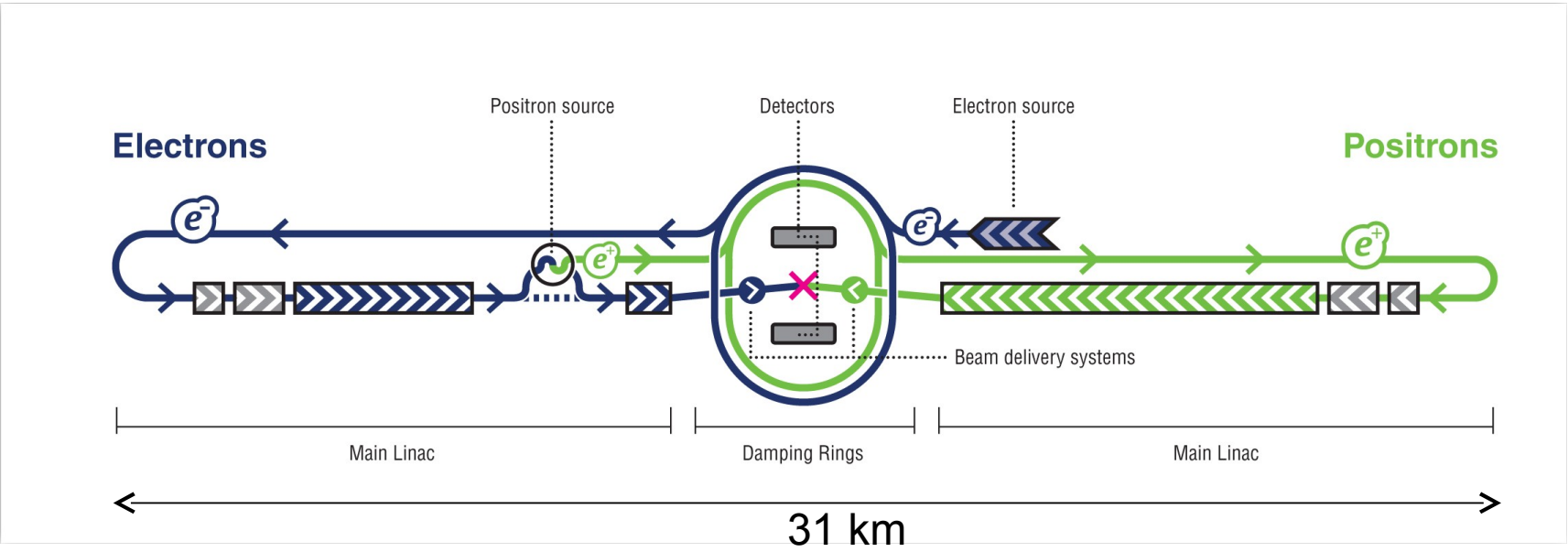
- Development of pixelated readout for a TPC
- Other field of interest: LHC upgrade:
  - pixelatex gaseous inner tracker layers (Gossip)
  - concept lately approved by ATLAS upgrade steering committee

- New readout system required
- Development of an FPGA based modular system using SRS
- Read out ~100 Timepix chips

universitätbonn

ILC

- International Linear Collider
  - one of the concepts for a future e^- e^+ collider
  - 0.5 TeV (1TeV) centre of mass energy
  - beam structure: 1 ms trains every 200 ms
  - one interaction point, 2 detectors (push-pull)



universitätbonn