The CMS high eta upgrade electronics

(Summary of the main points of the first MPGD high eta electronics meeting 7th April 2011)

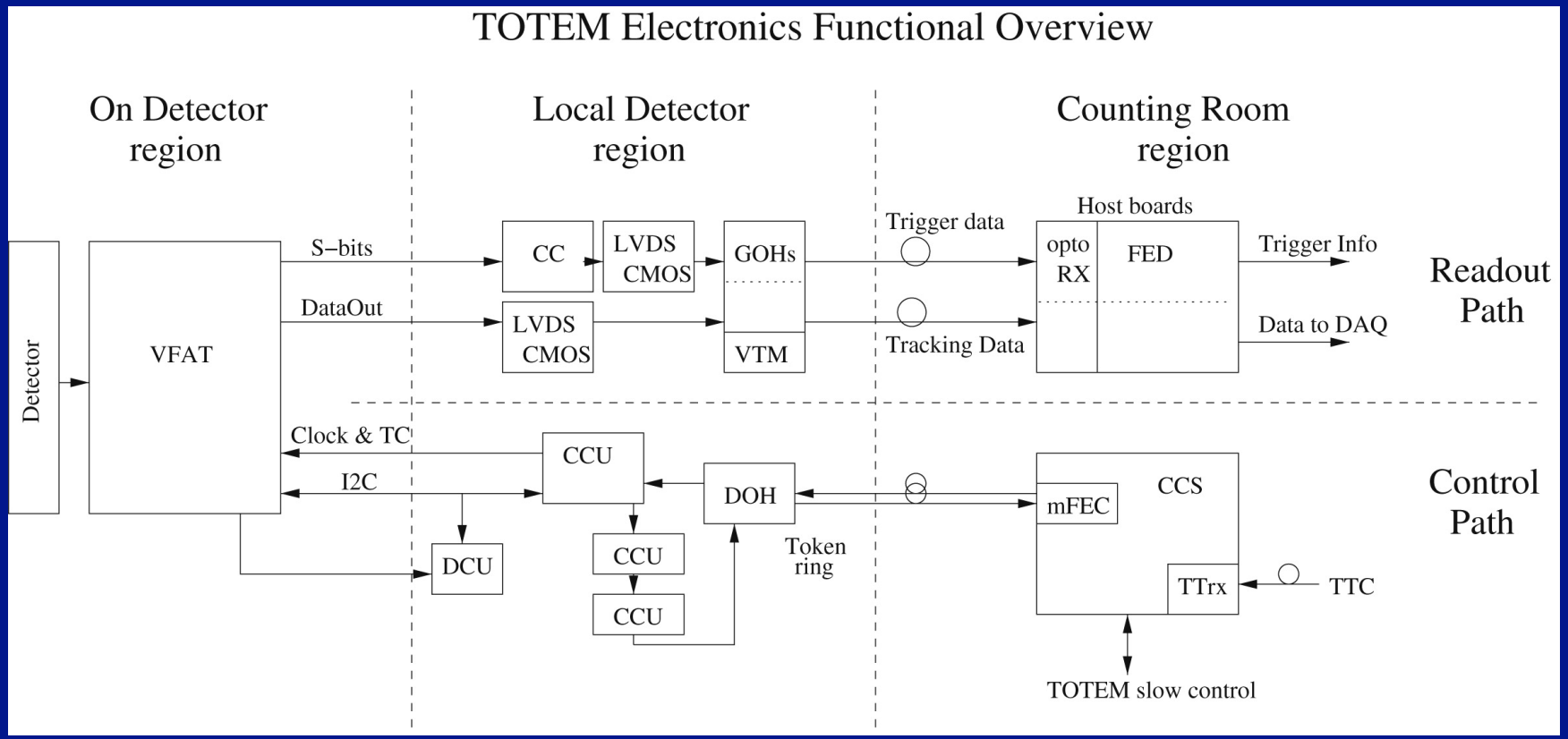
LHC to LHC-upgrade System Styles

Front-ends

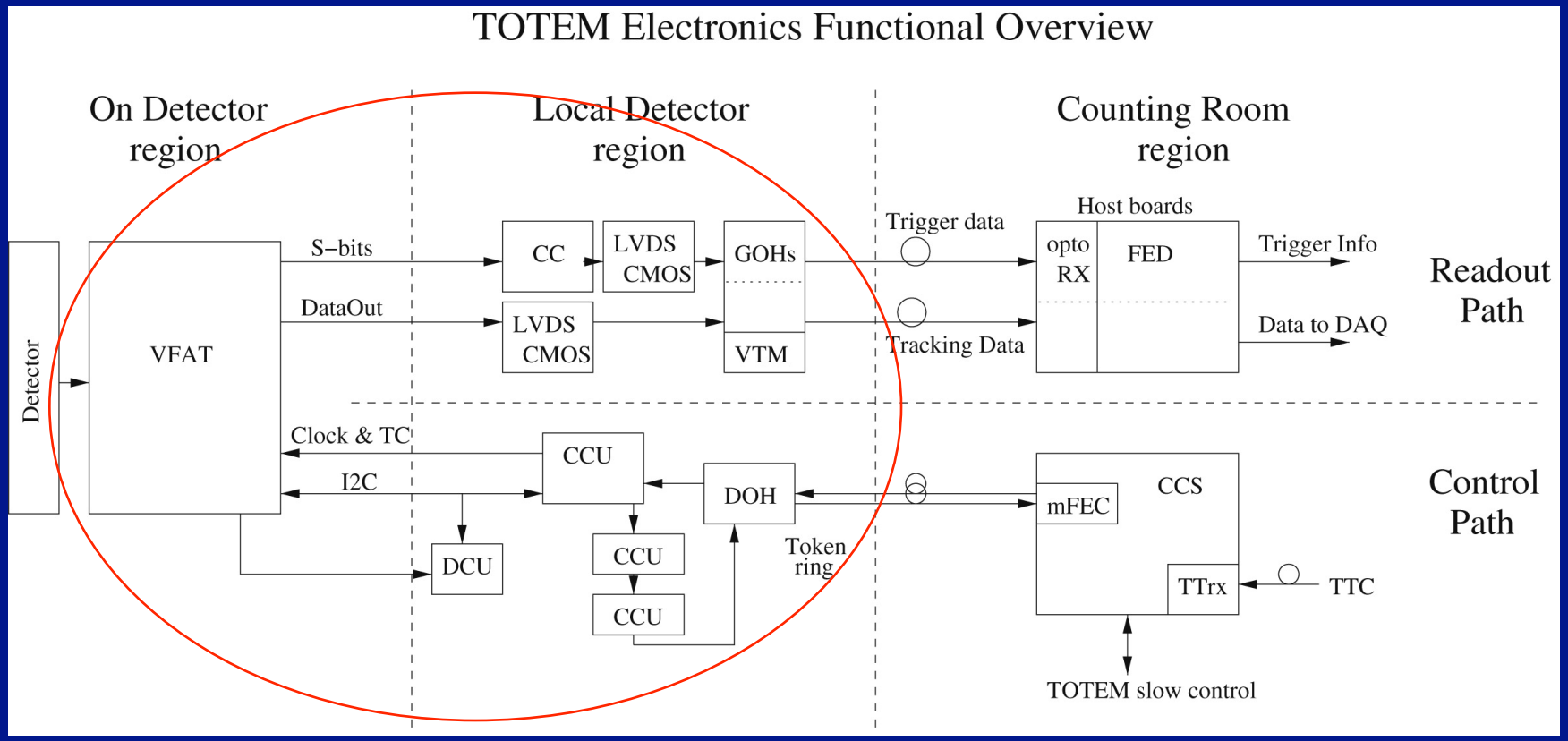
Powering

Data transmission

LHC style readout system – example TOTEM



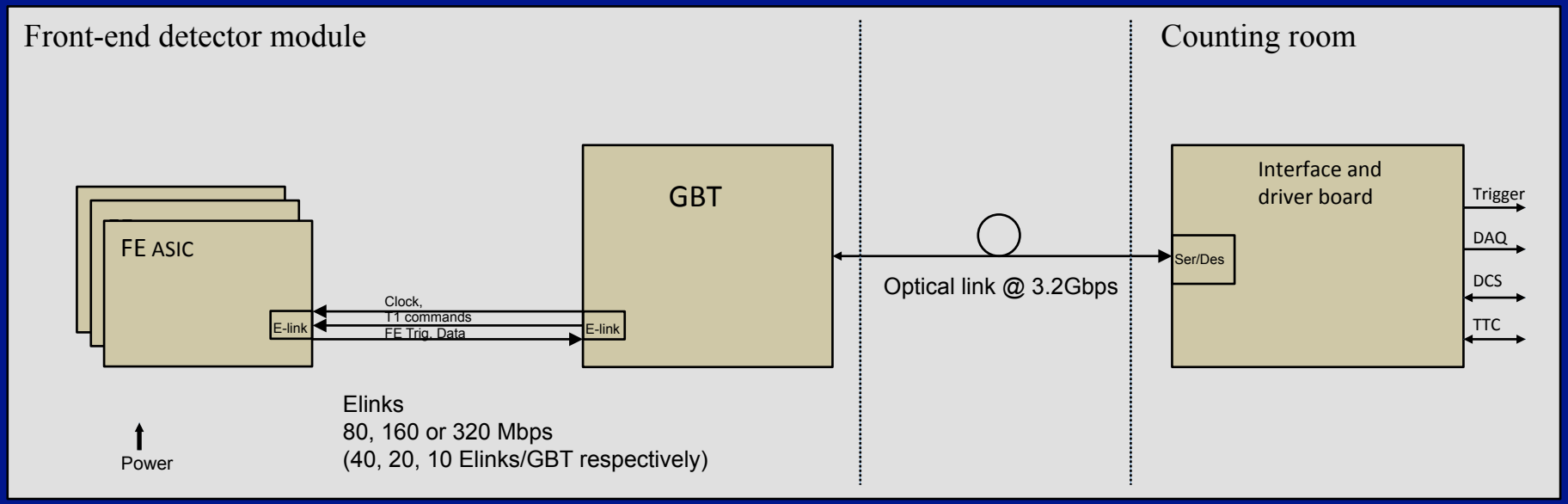
LHC style readout system – example TOTEM



Problem : LHC radiation hard custom components designed ~ 2003-2005.

Most of which face either obsolescence or are out of stock.

LHC-Upgrade style readout system

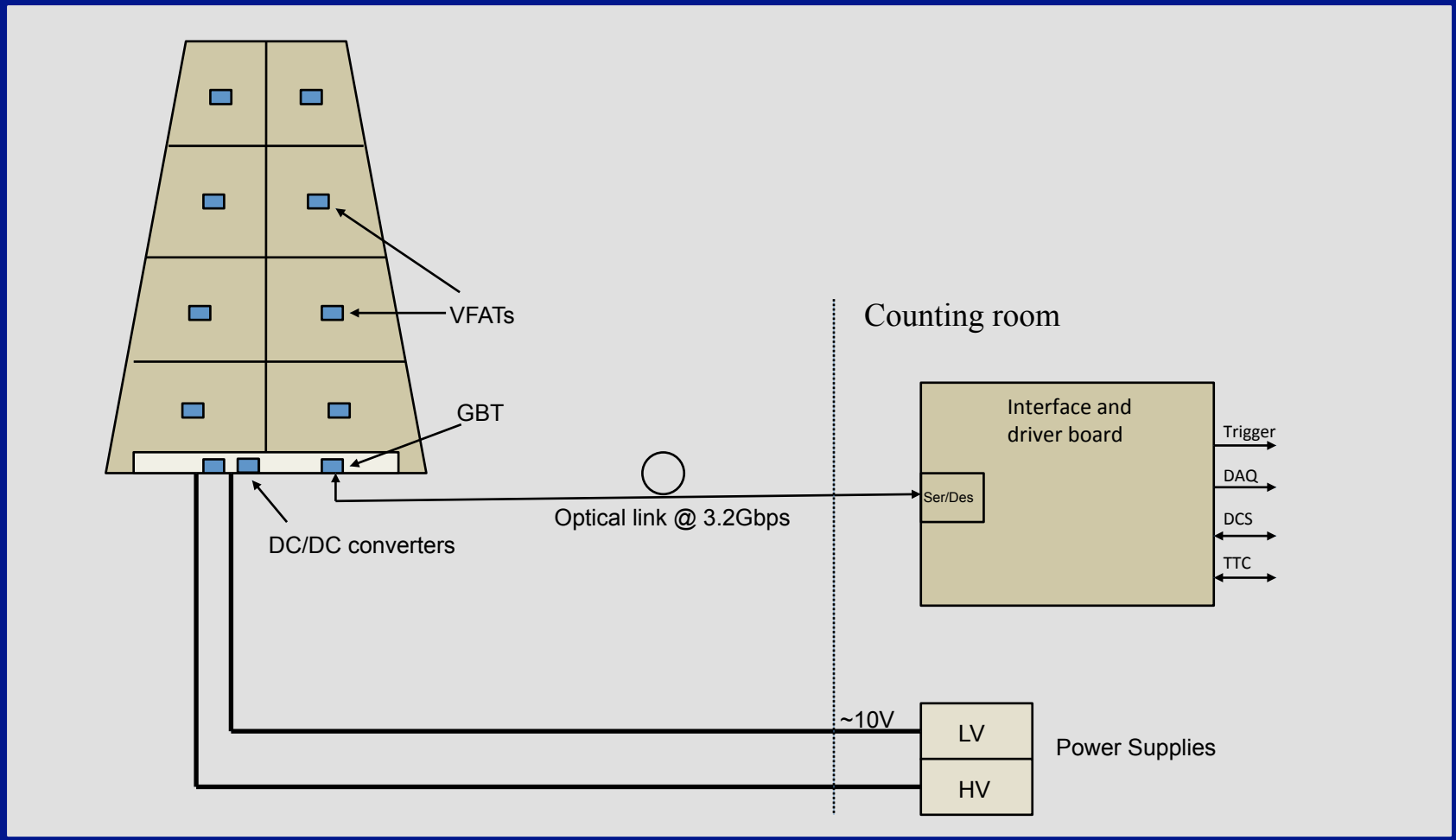


The GBT is currently foreseen for many LHC upgrades :
CMS tracker, HCAL, Atlas tracker, LHCb (all upgrades)

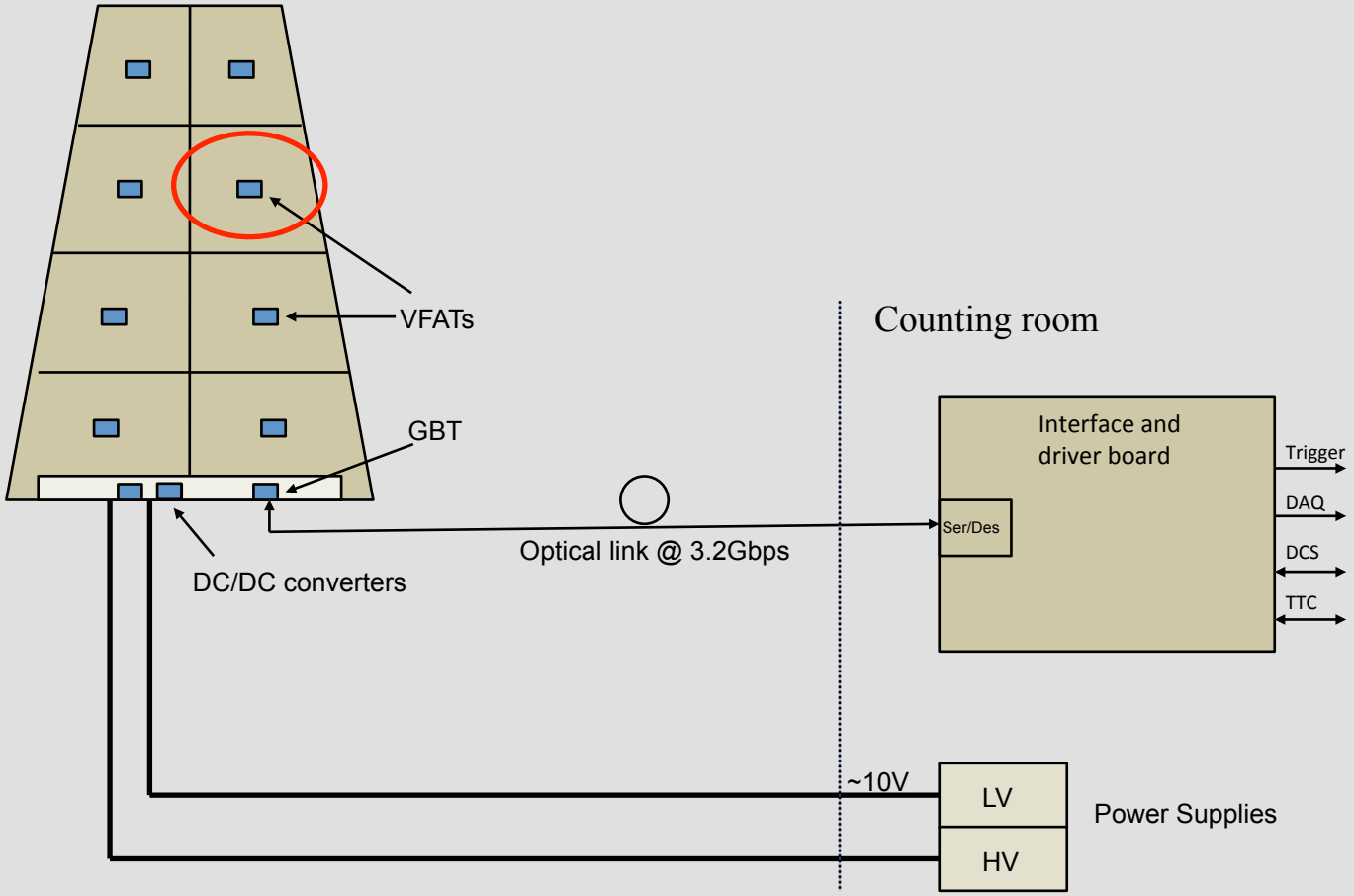
Generic projects in CERN for :

DC/DC Powering
GBT
Versatile Link

Basic system idea

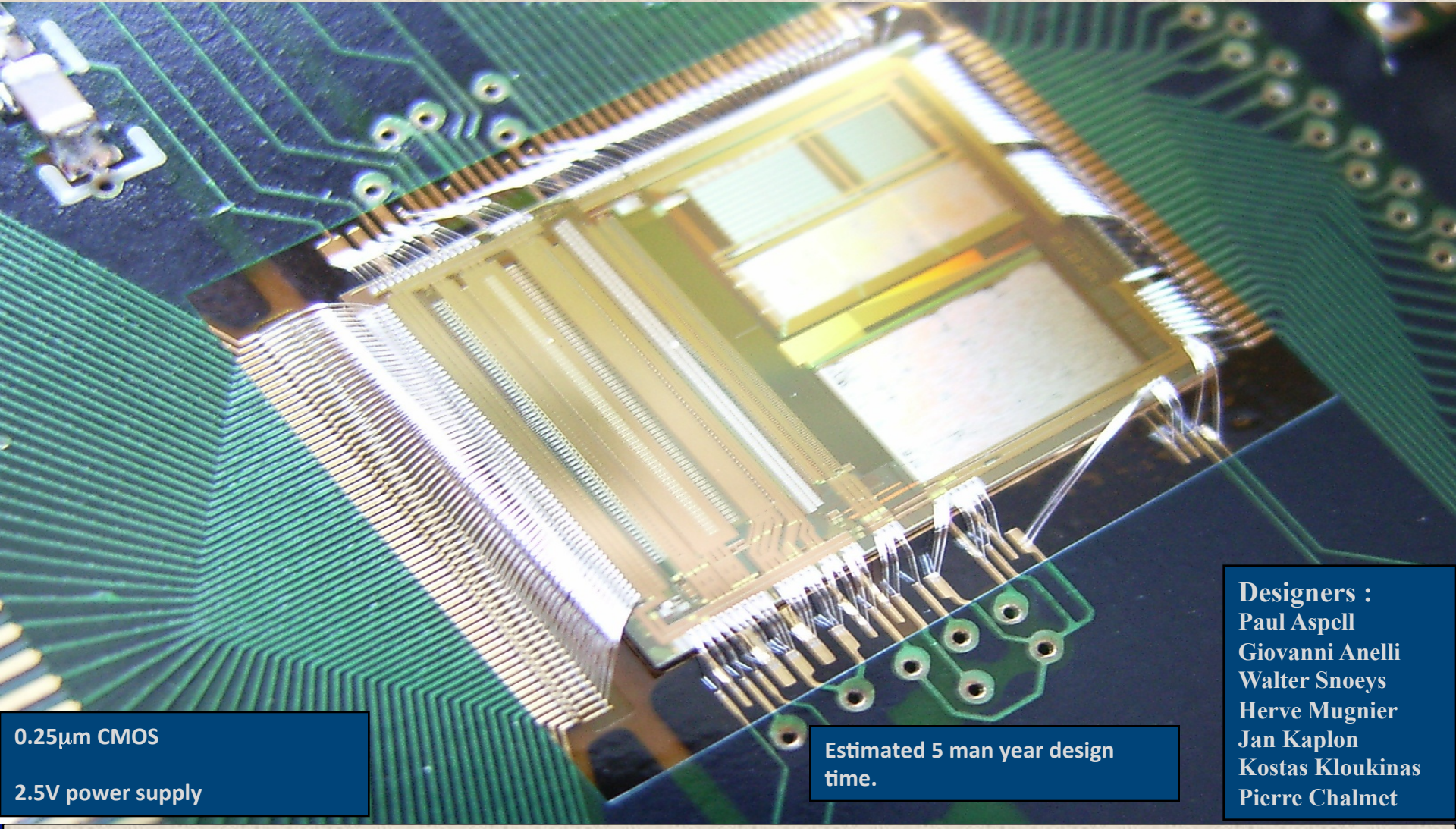


Front-ends


VFATs
GBT
DC/DC converters
Optical link @ 3.2Gbps
Counting room
Interface and
driver board
Ser/Des
Trigger
DAQ
DCS
TTC
~10V
LV
HV
Power Supplies

VFAT

A front-end "system on chip" providing fast trigger information and digitized data storage for the charge sensitive readout of multi-channel silicon and gas particle detectors.



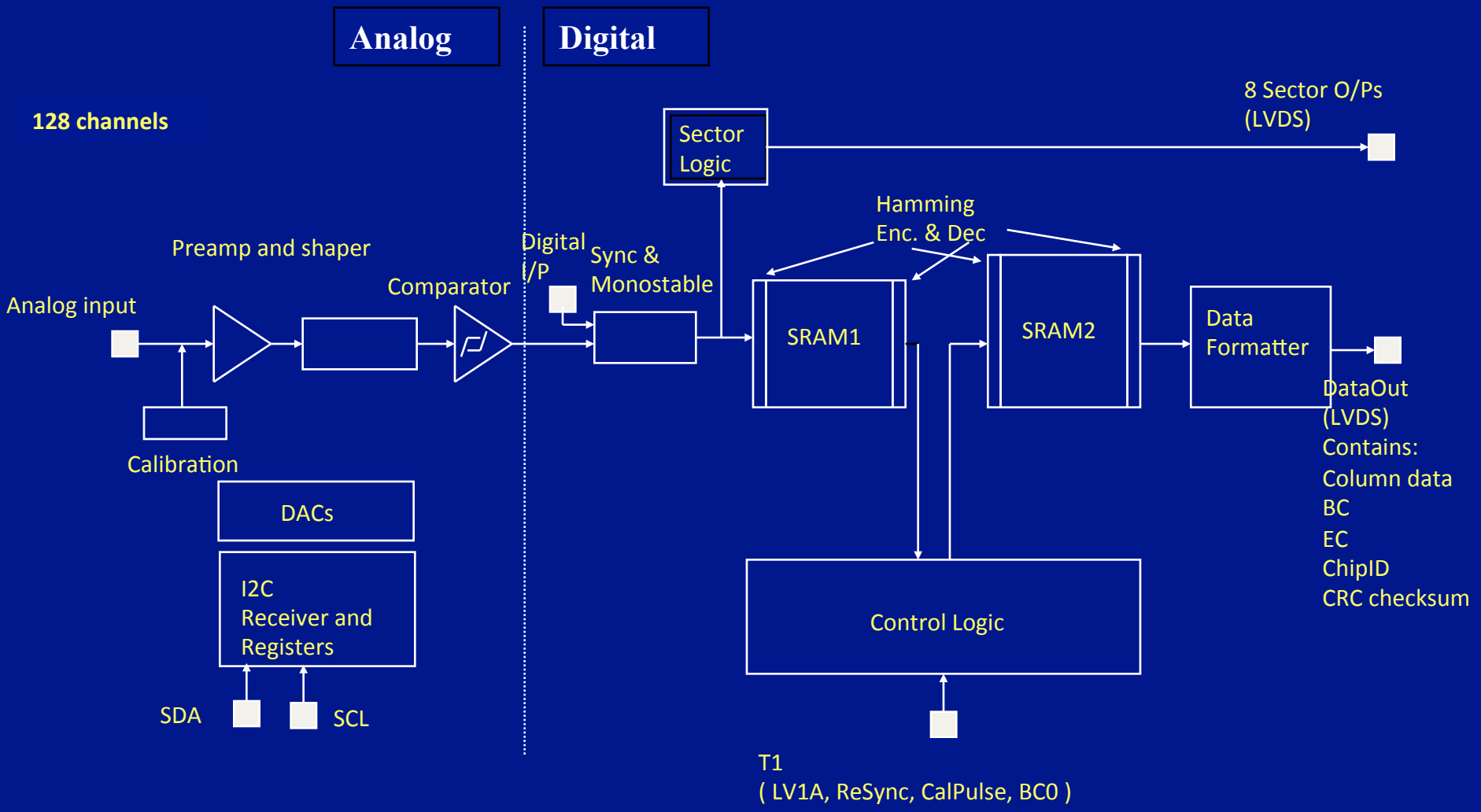
0.25μm CMOS

2.5V power supply

Estimated 5 man year design time.

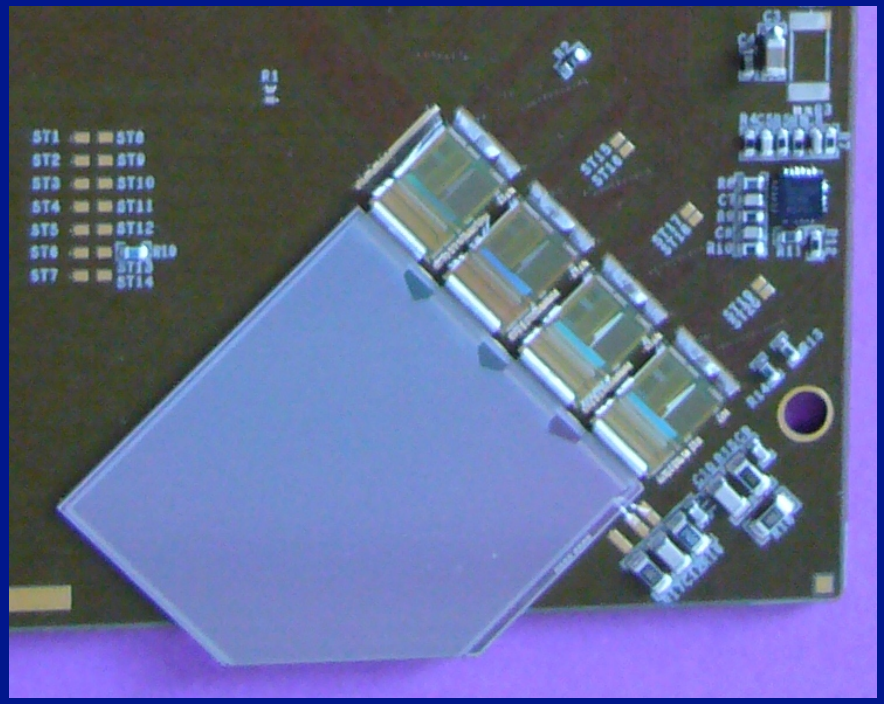
Designers :
Paul Aspell
Giovanni Anelli
Walter Snoeys
Herve Mugnier
Jan Kaplon
Kostas Kloukinas
Pierre Chalmet

VFAT2 Signal Flow

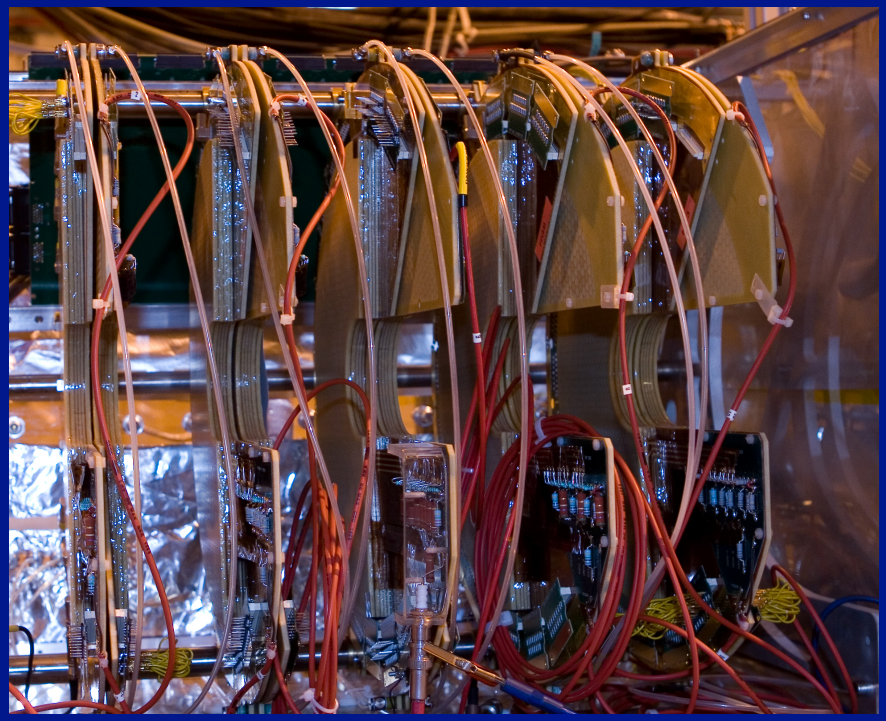


Used in TOTEM for RP silicon, T1 & T2 GEM detectors

Roman Pot – Silicon strips

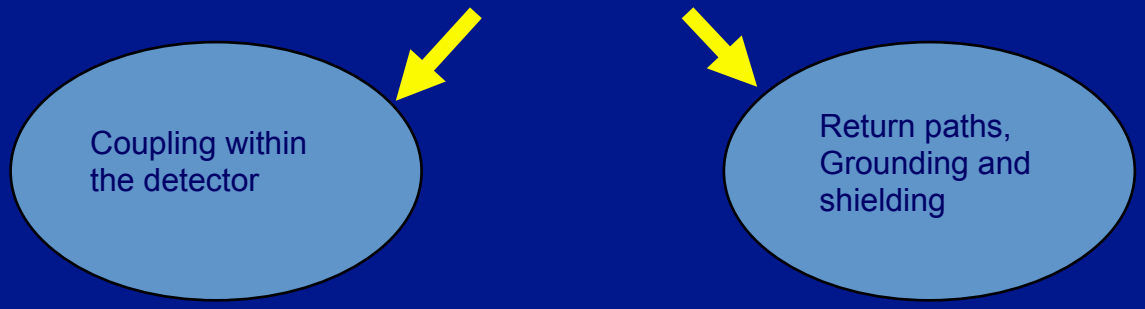


T2 GEMs



Common mode issues with GEMs

Measurements in Totem T2 and in the MPGD lab show the minimum threshold is different between detectors and higher than it should be. There appears to be a high level of common mode pickup.



Detailed studies on-going in these two areas both in the lab and via simulation.

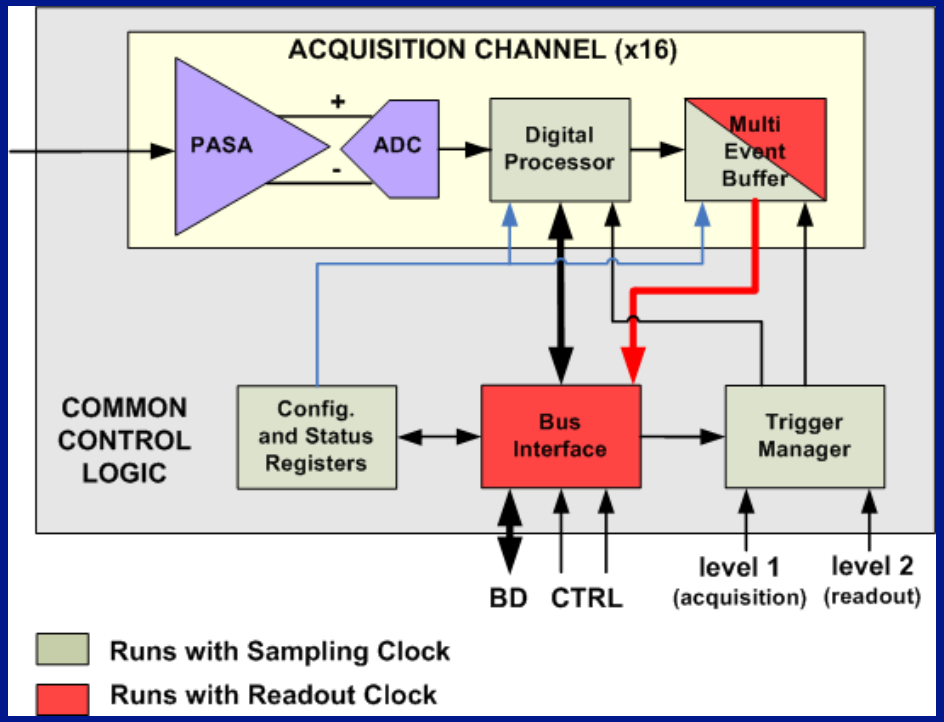
Aim : to arrive at proposals for improvements in :

Detector design	Grounding, return paths and shielding	Front-end design : VFAT3 GDSP	Readout

Front-end families

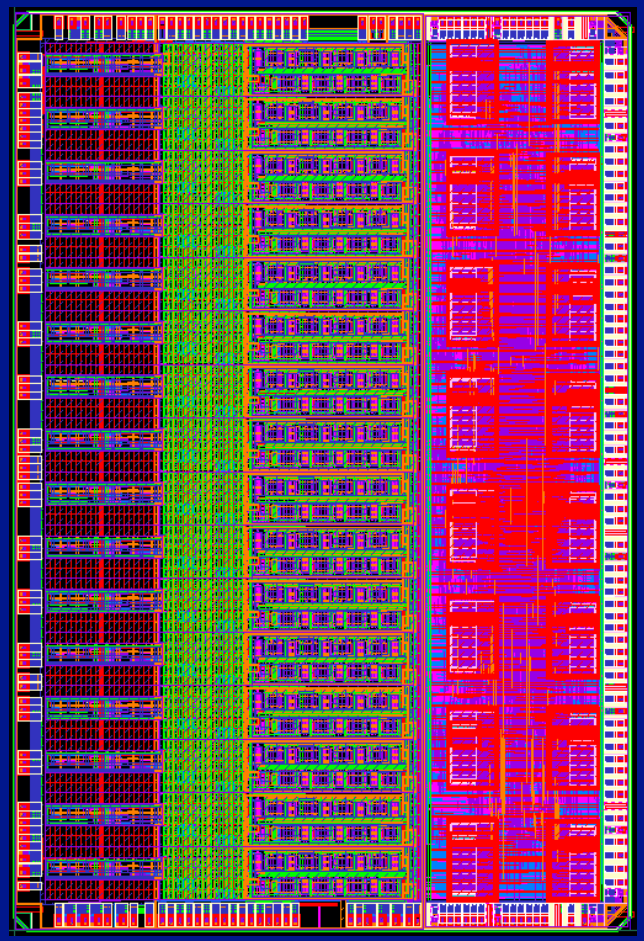
	Analog Memories	Binary	DSP
Examples	APV PACE	VFAT Pixels	Saltro GdSP
Age	Development some years ago. (LHC)	Now (LHC & SLHC)	Future (SLHC ?) (ILC/Clic)
Threshold	no	analog	digital
Common mode subtraction	offline	no	Yes (GdSP), on-line
Trigger output	no	yes	Yes (lower noise, longer latency)

SAltro16



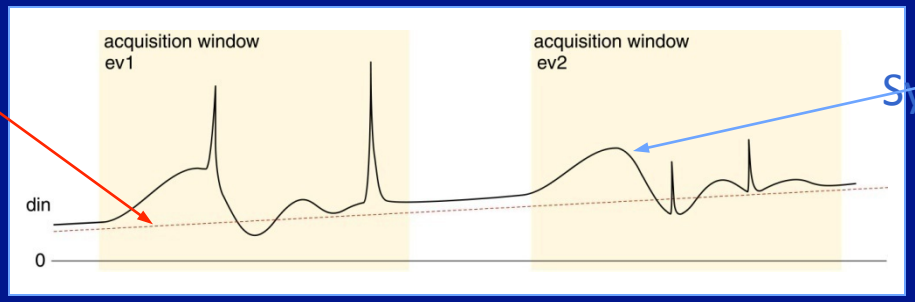
16 channel demonstrator chip designed in 2009-2010, recently received back from the foundry awaiting test.

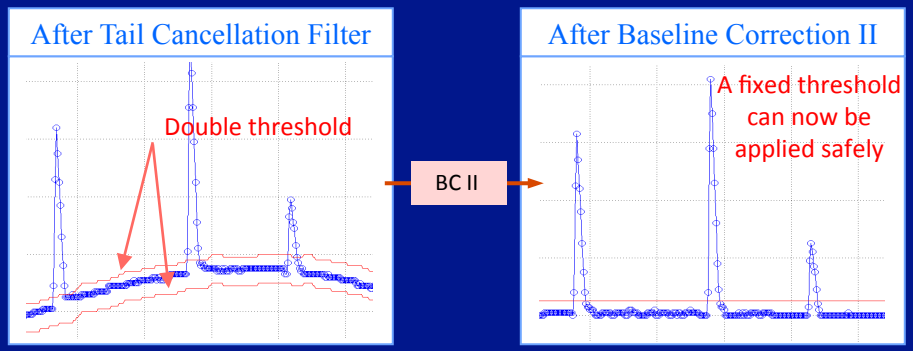
Technology : IBM 130nm CMOS



Luciano Musa …… S-Altro Specs. & Architecture
Paul Aspell …… Coordinator of design
Designers :
Massimiliano De Gaspari ……. Front-end + ADC
Hugo França-Santos ……... ADC core
Eduardo Garcia …… Data Processing & Control

Digital processing

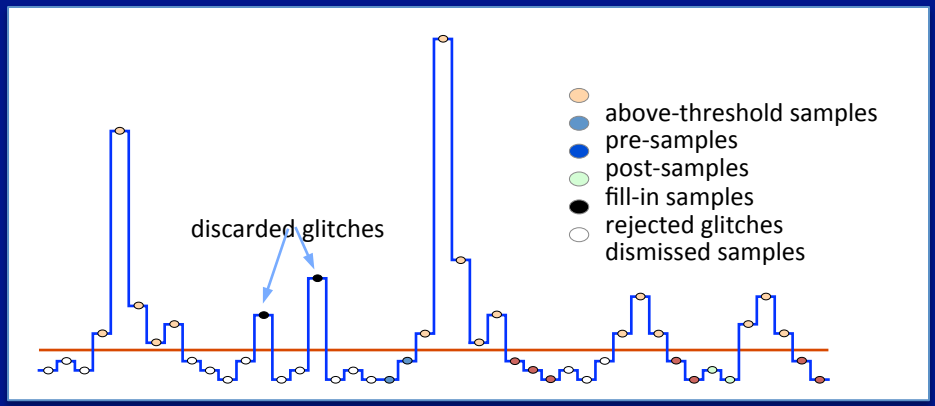




Corrects on-chip for :

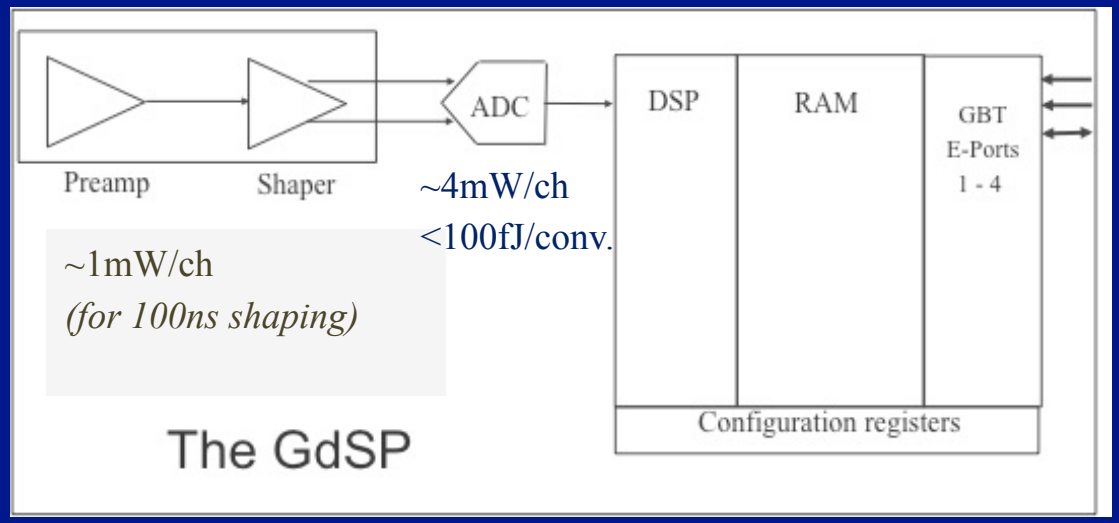
Systematic offsets,
Baseline movements
Ion tails
Removial of glitches

Zero-suppressed output



DP Design and simulations : Eduardo Garcia

The GDSP (a possibility)



Estimate for optimal future power (static)

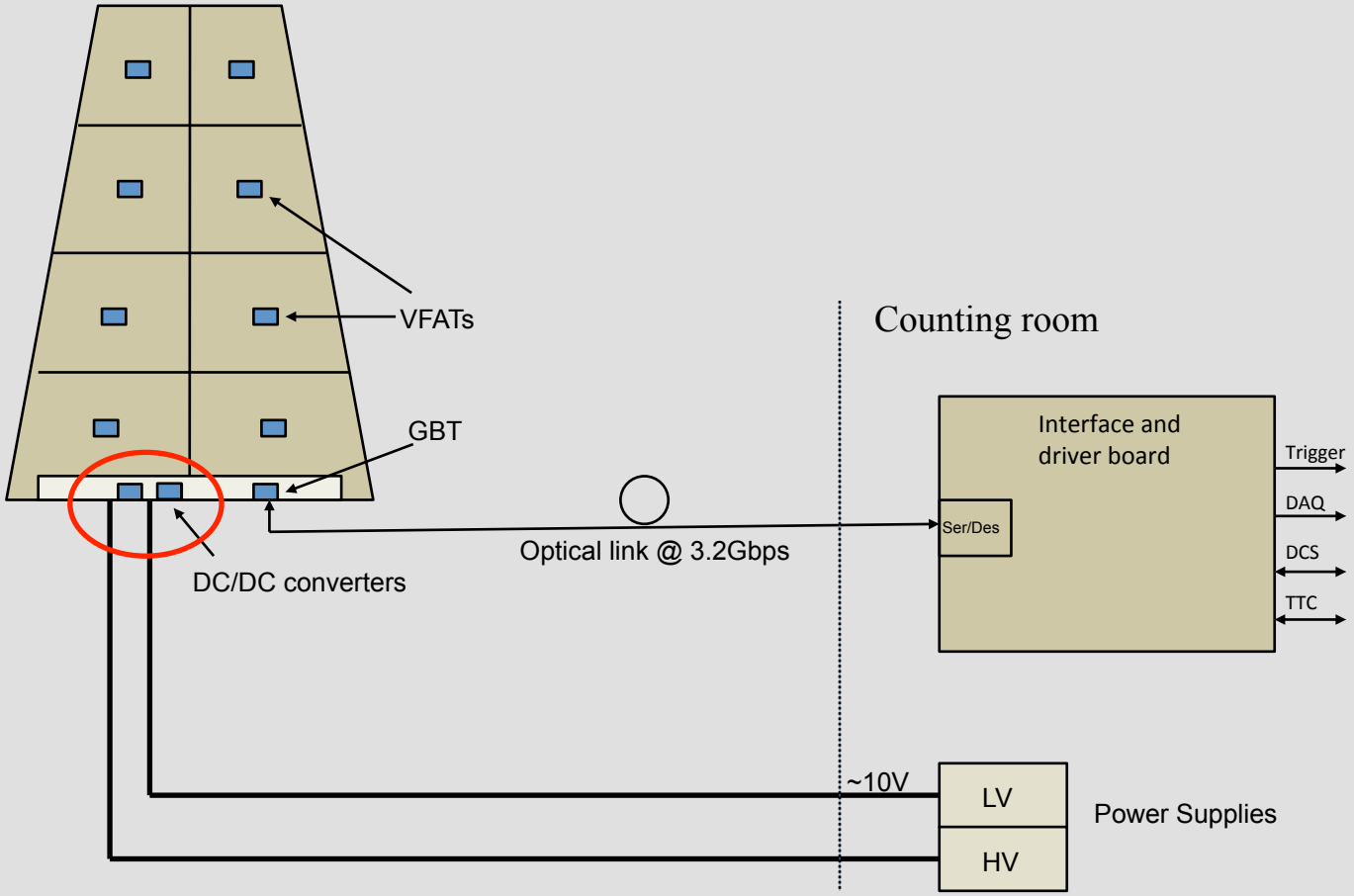
64 channels = Analog power ~ 320mW + Digital power ~ a few hundred mW.
Approx. ~500mW / chip.

128 channels = Analog power 640mW + Digital power ~ some hundreds mW.
Approx. ~900mW / chip.

Should be possible to get 7-8 mW/ch for everything on a 128 ch chip.

Power management & pulsing may then be applied to reduce power further.

Powering

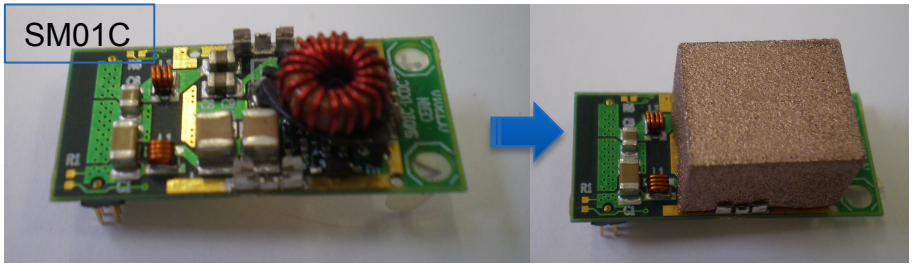

VFATs
GBT
DC/DC converters
Optical link @ 3.2Gbps
Counting room
Interface and
driver board
Ser/Des
Trigger
DAQ
DCS
TTC
~10V
LV
HV
Power Supplies

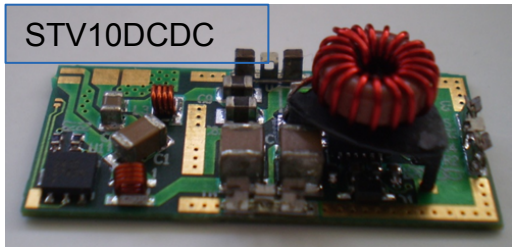
Radiation Hard DC-DC Converters Development at CERN

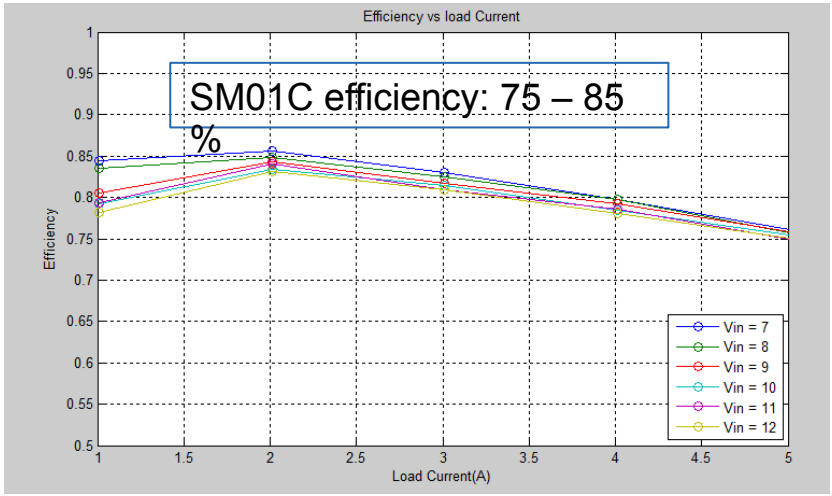
G. Blanchot, F. Faccio, S. Michelis

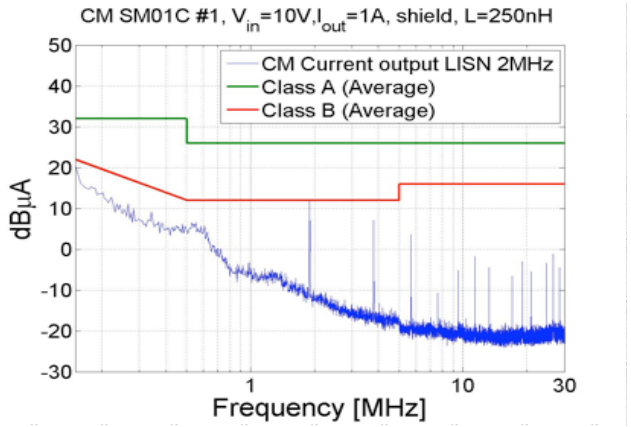
C. Fuentes, B. Allongue

- Some applications are still using ASICs that require more current than what AMIS2 can deliver.
  - SM01C based on LT3605, delivers up to 5A at 2.5V (can be tuned), replacement for AMIS2.
  - STV10 is identical to SM01C, but is intended to be bonded on staves (no connector).



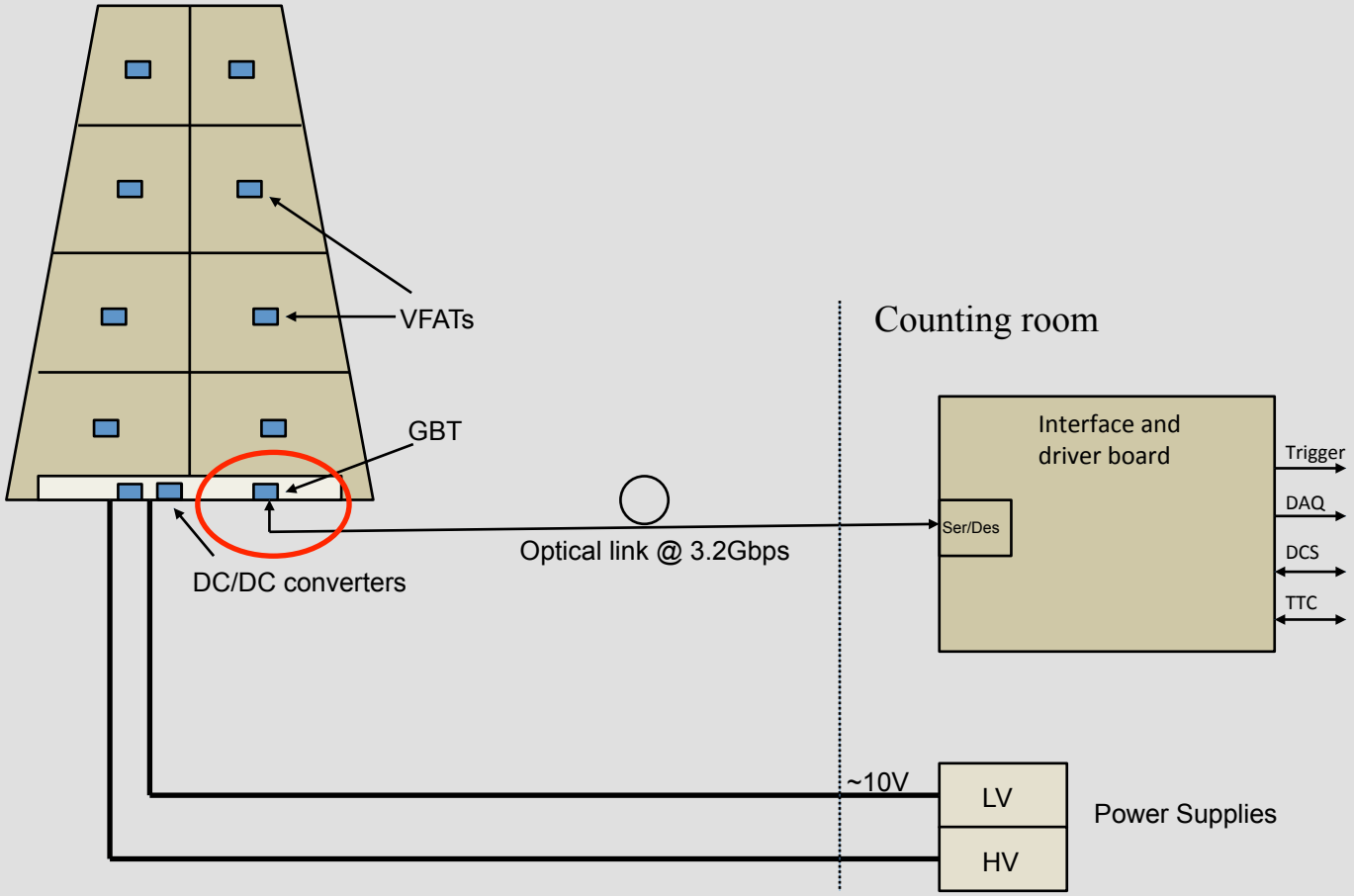






CM current < 0 dBuA above 7 MHz
DM current < -10 dBuA above 7 MHz

GBT


VFATs
GBT
DC/DC converters
Optical link @ 3.2Gbps
Counting room
Interface and
driver board
Ser/Des
Trigger
DAQ
DCS
TTC
~10V
LV
HV
Power Supplies

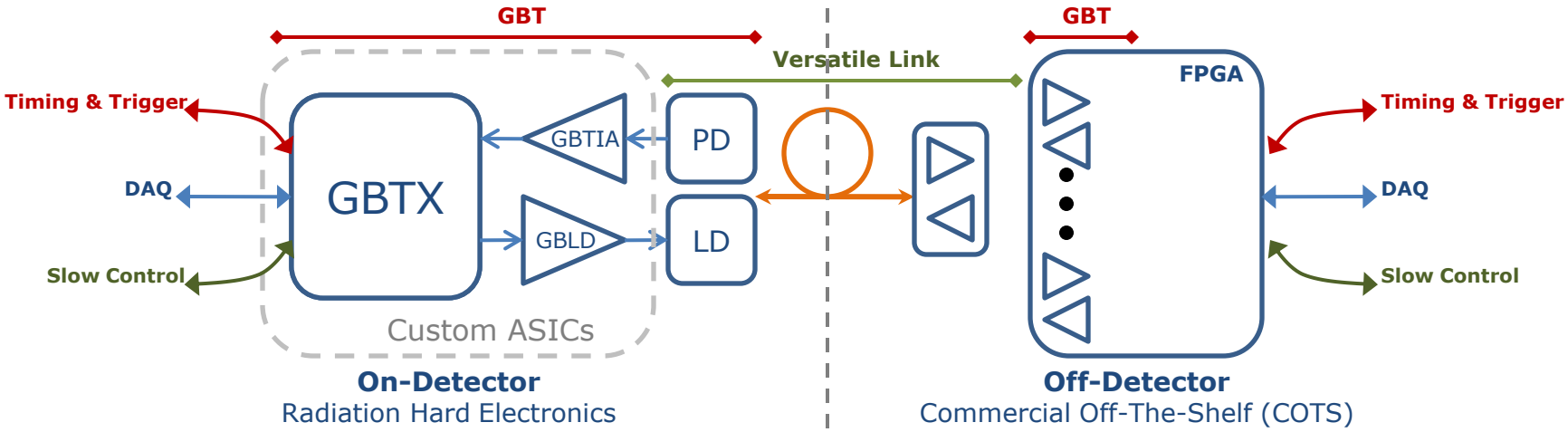
Radiation Hard Optical Link Architecture

Defined in the "DG White Paper"

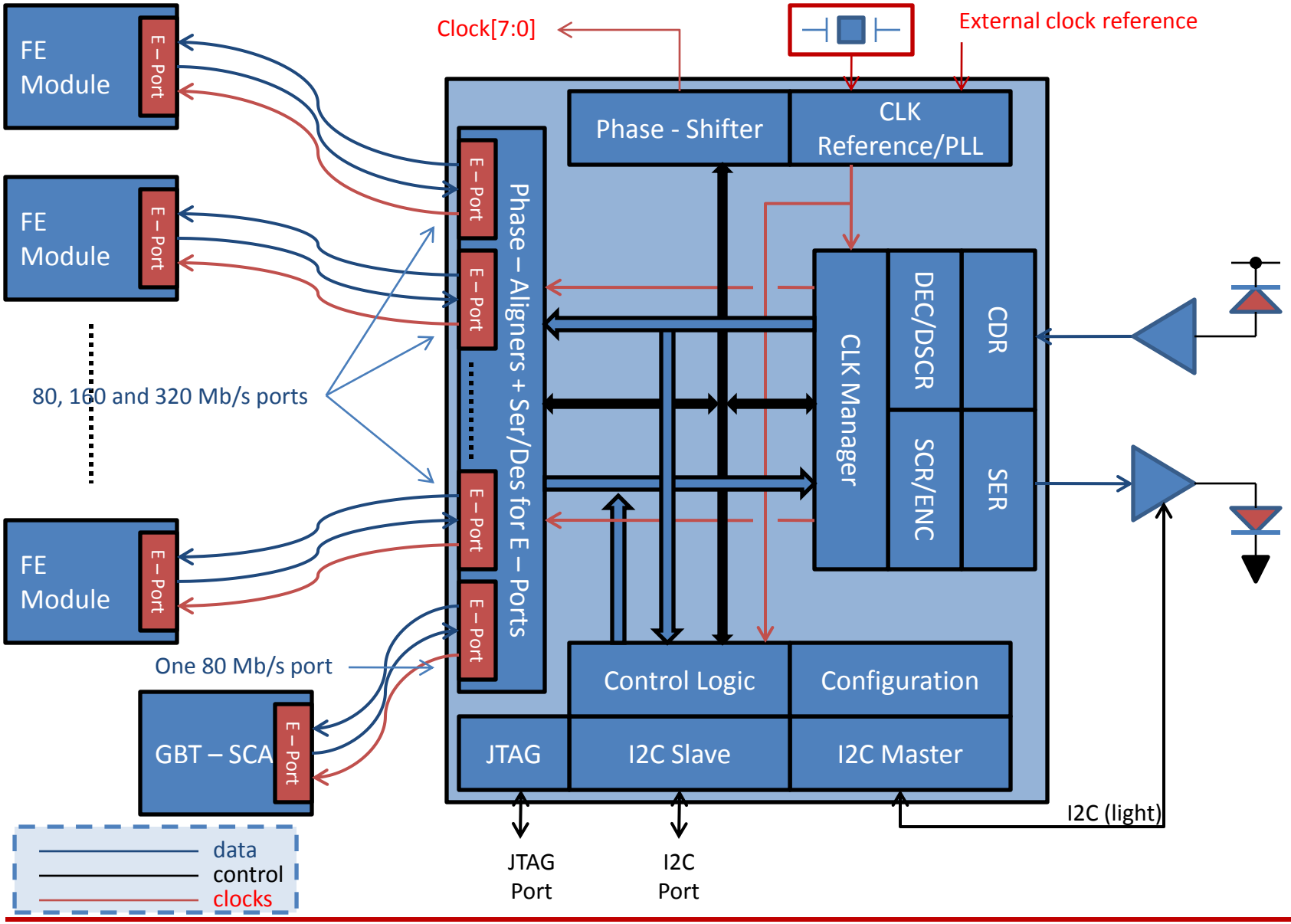
- "Work Package 3-1"
  - Objective:
    - Development of an high speed bidirectional radiation hard optical link
  - Deliverable:
    - Tested and qualified radiation hard optical link
  - Duration:
    - 4 years (2008 – 2011)

Radiation Hard Optical Link:

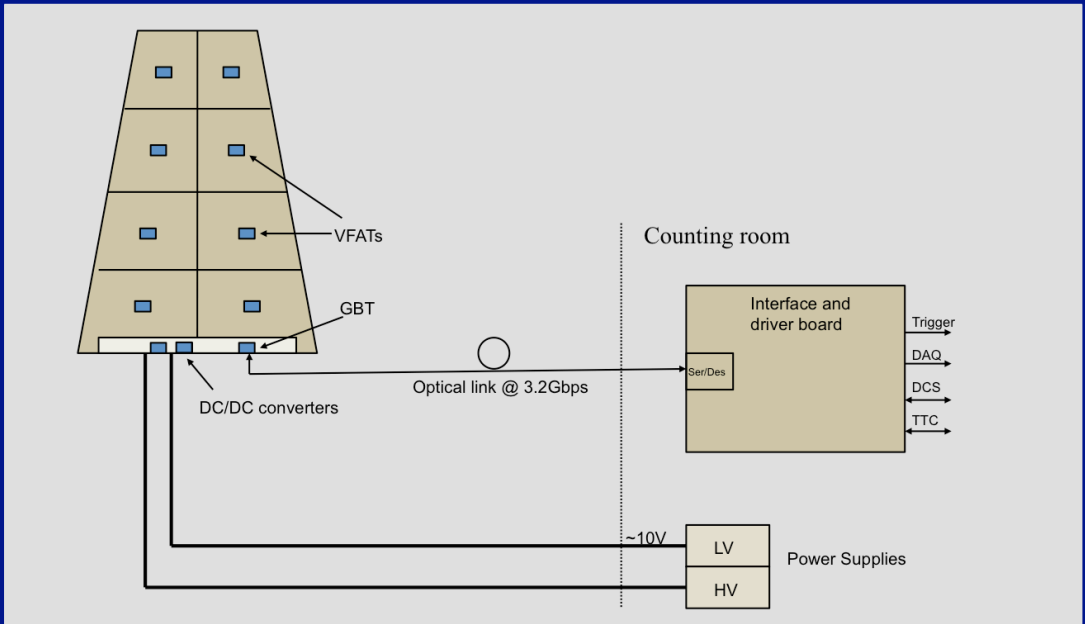
- Versatile link project:
  - Opto-electronics components
  - Radiation hardness
  - Functionality testing
- GBT project:
  - ASIC design
  - Verification
  - Radiation hardness
  - Functionality testing



GBTX Block Diagram



Summary



On-going work :

Lab: Investigation into common mode pickup :
tests with 10cmx10cm GEM detectors and VFAT2 readout.
Preparation for beam tests.

Office : Simulations of VFAT2 with GEM and System planning
VFAT3 design ideas.
GDSP design ideas.

Very early days but
The big picture is taking shape:

Large GEM detectors
Front-end ASIC ideas : VFAT3/GDSP ?
Chip power and signal routing on the GEM.
GEM design as a stand alone electronic module.
Use generic R&D existing in CERN for the upgrades such as :
DC/DC powering
GBT and Versatile link optical communication and readout.

Large GEM prototyping and design evolution to incorporate electronics.