Status of APV based electronics for JLab tracker

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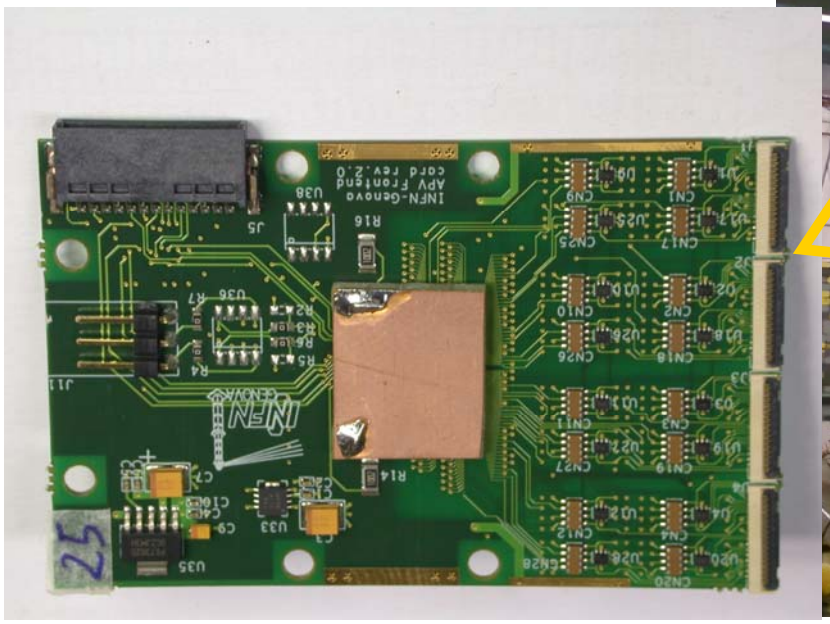
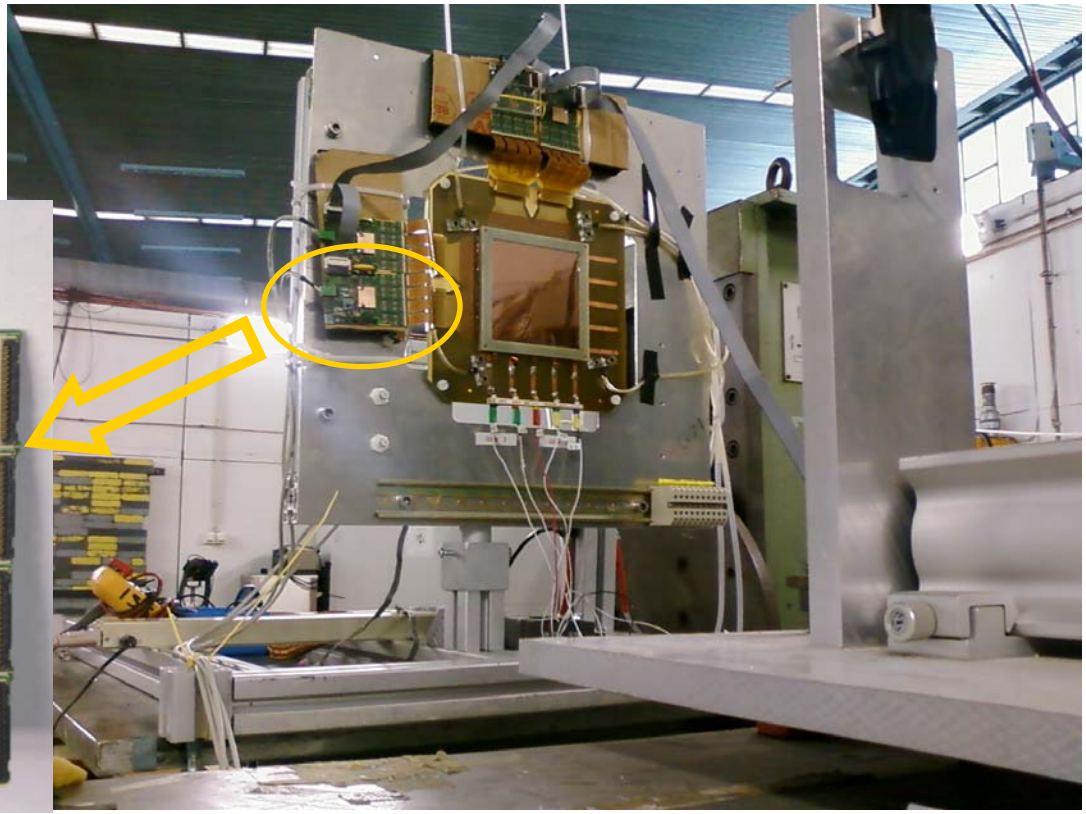
- Test Beam Setups
- Front-end APV card
- Multi Purpose Digitizer card

July 2010 DESY setup



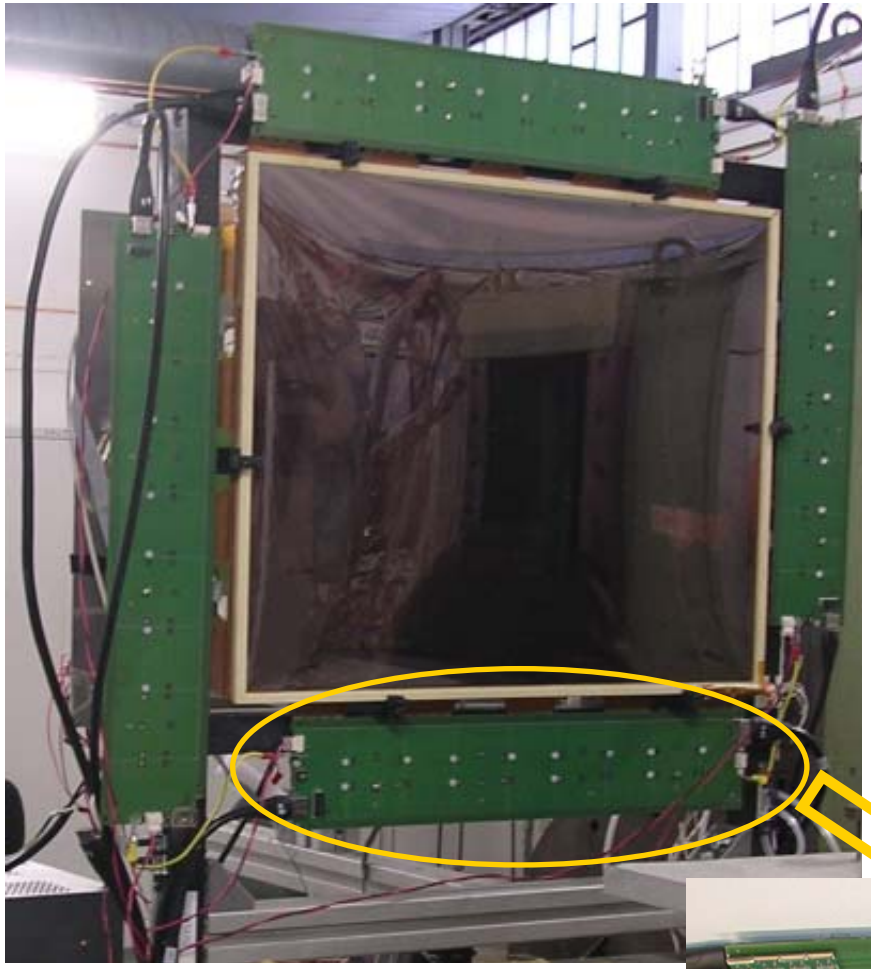


Small (10 x 10 cm^2) chamber

Only 4 APV cards + 1 ADC card (not shown)

Flat cable ribbon connection

November 2010 DESY setup



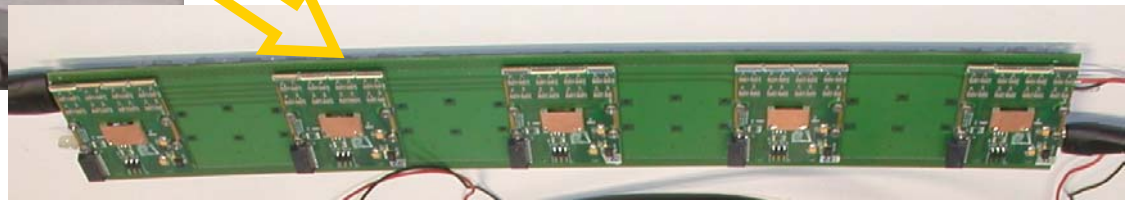
Big (50 x 40 cm^2) chamber

18 APV cards + 2 MPD cards

Backplane connections

HDMI cables

Additional small chamber added last days

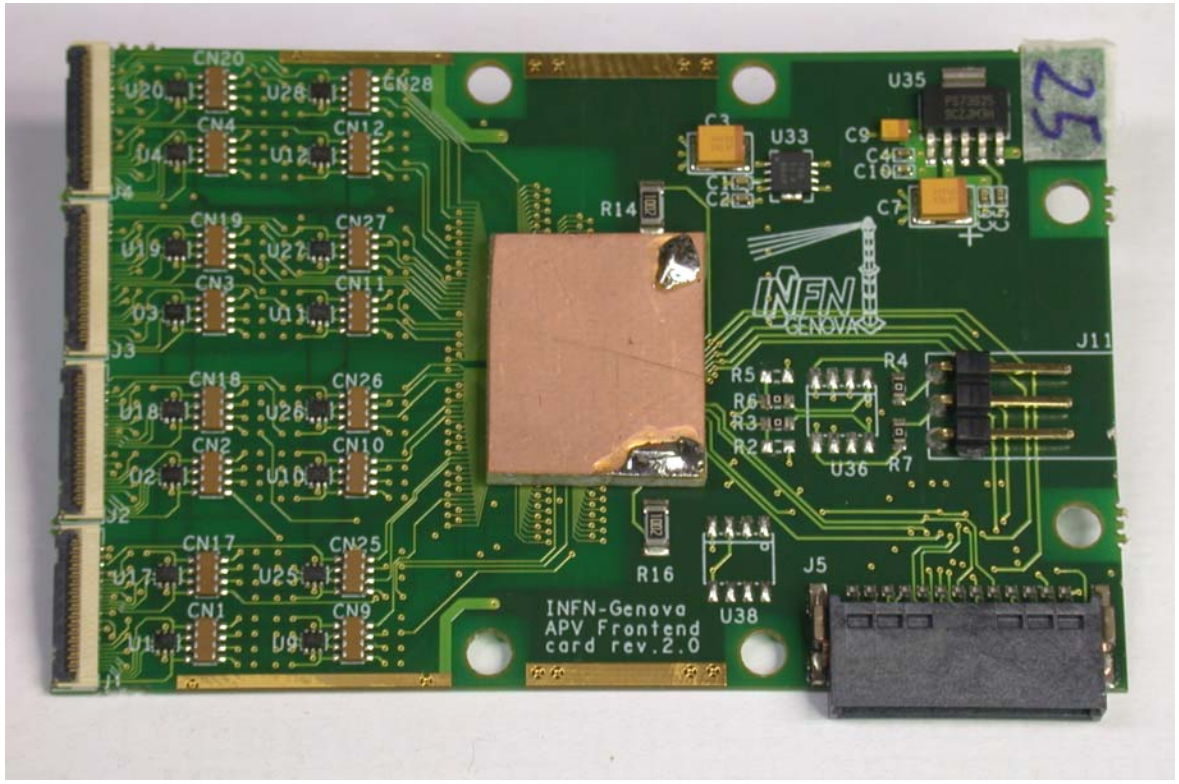


APV Card

NUP4114

APV25S1 (covered)

Power regulators



NO analog buffer

Optional °T & ID

FPC Connectors

C network

Old style connectors
(new style on back side)

APV Front End Card status

Prototypes are OK

In house APV wire bonding using 2 columns (fine pitch PCB)

Value of input C must be optimized for each chamber:

- small chamber: 10 - 15 pF
- big chamber: 200 - 400 pF

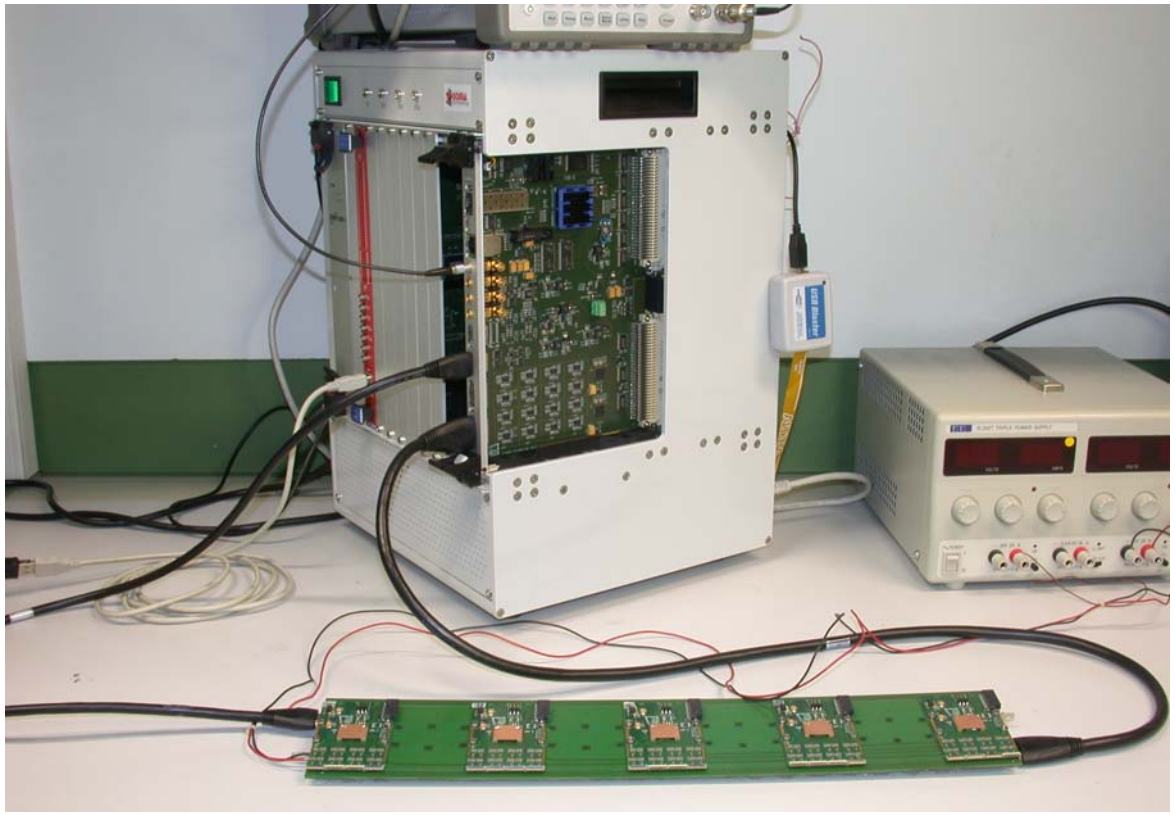
Are NUP4114 protections really needed?

Seems that APV has internal spark protection circuit

Setup optimization in progress (noise reduction)

Additional iteration of the PCB to move FPC connectors on the opposite side

Front End + Readout



Bench setup:

1 MPD in a 10 slots benchtop VME-VXS crate connected to

1 backplane equipped with

5 APV front-end cards

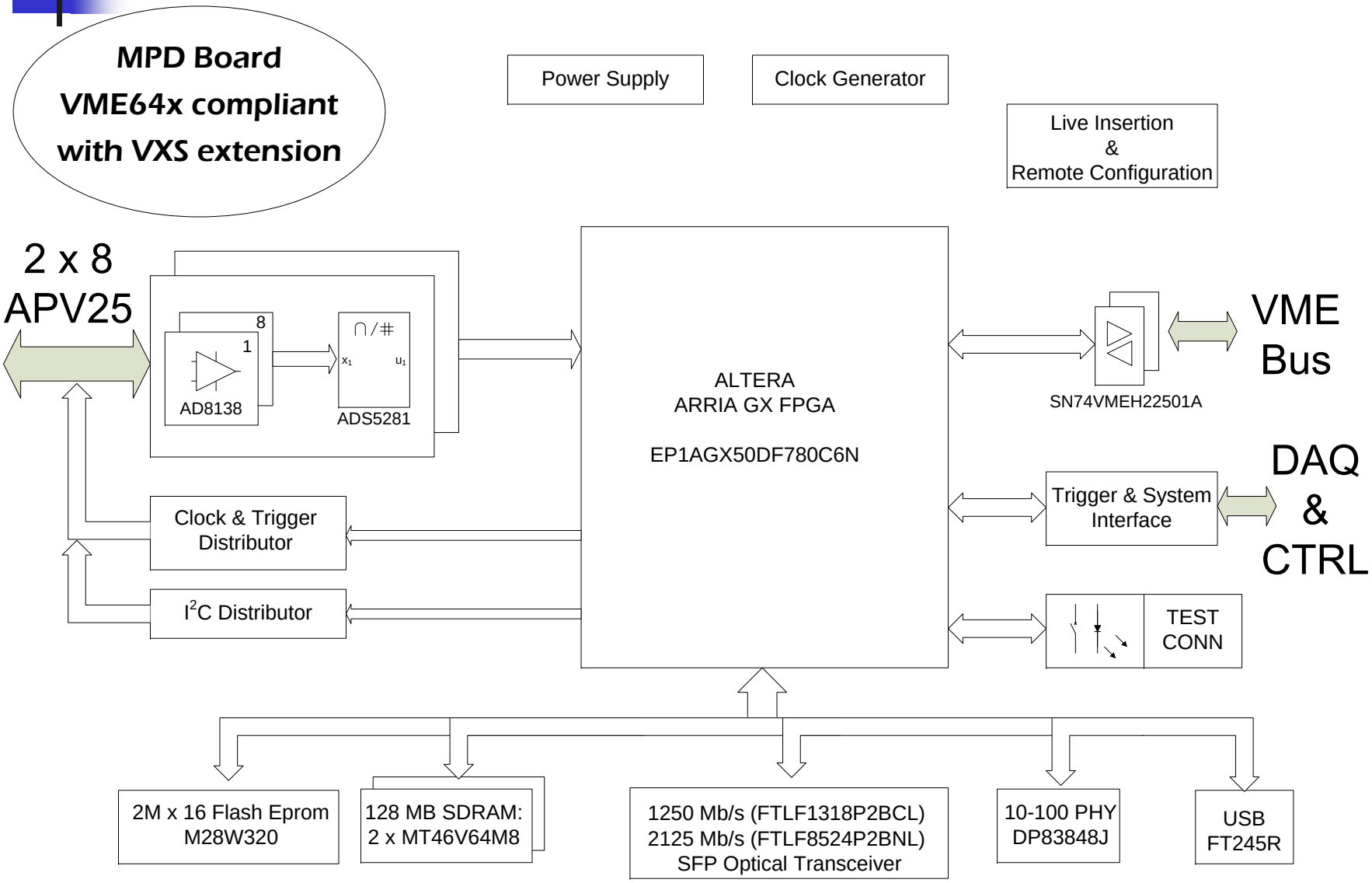
Pulser (for trigger) and LVPS

MPD Features

Main features:

- Digitization of 16 APVs (2048 channels)
- APV serial stream decoding
- Data reduction: baseline removal, zero suppression
- Big memory buffer, multi event
- Possibility to implement SOC:
  - Flash memory, Ethernet
- Remote logic reconfiguration, hot swappable
- Multiple access ports:
  - VME, optical, USB, Ethernet

MPD Block Diagram



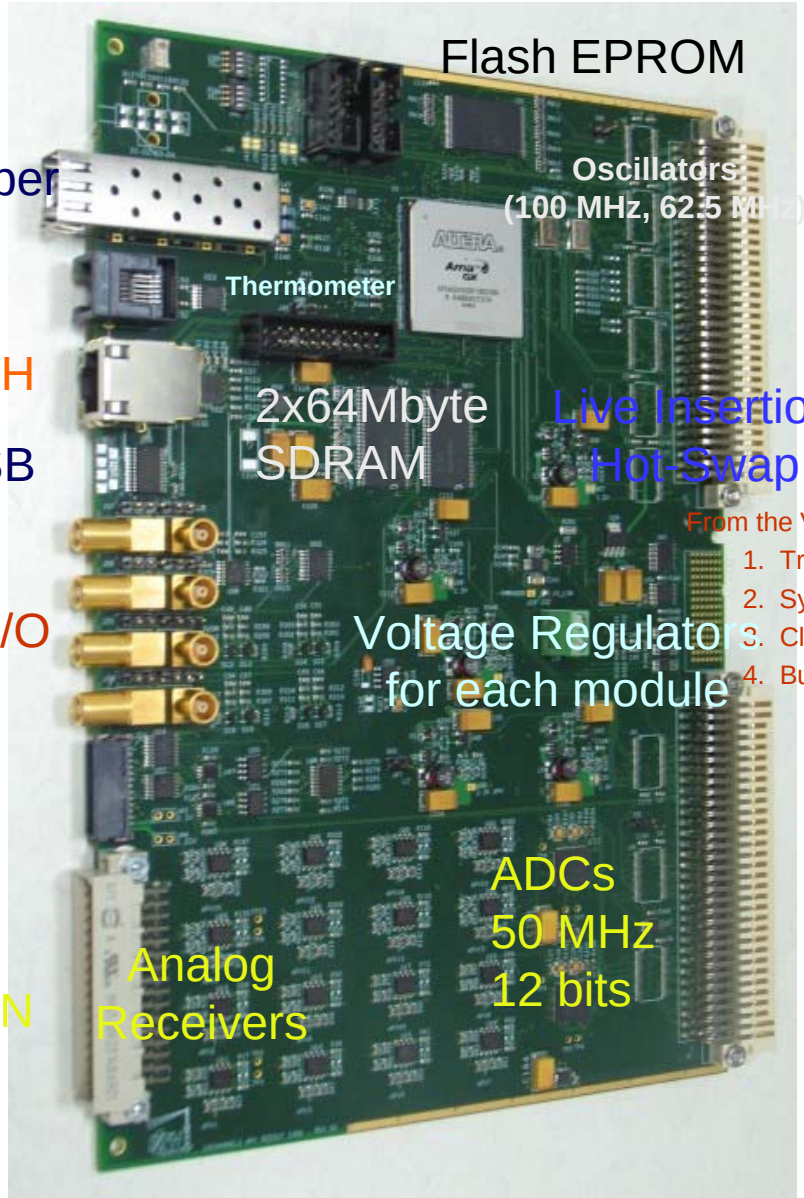
First prototype

Used in July 2010 DESY test beam.

A lot of wire modifications, mainly on power regulators.

Only raw data processing.

Two boards fabricated.



Second prototype

Used in November 2010 DESY test beam.

Well usable. No big modifications.

Introduced HDMI connectors.

Added delay line for CK phase tuning.

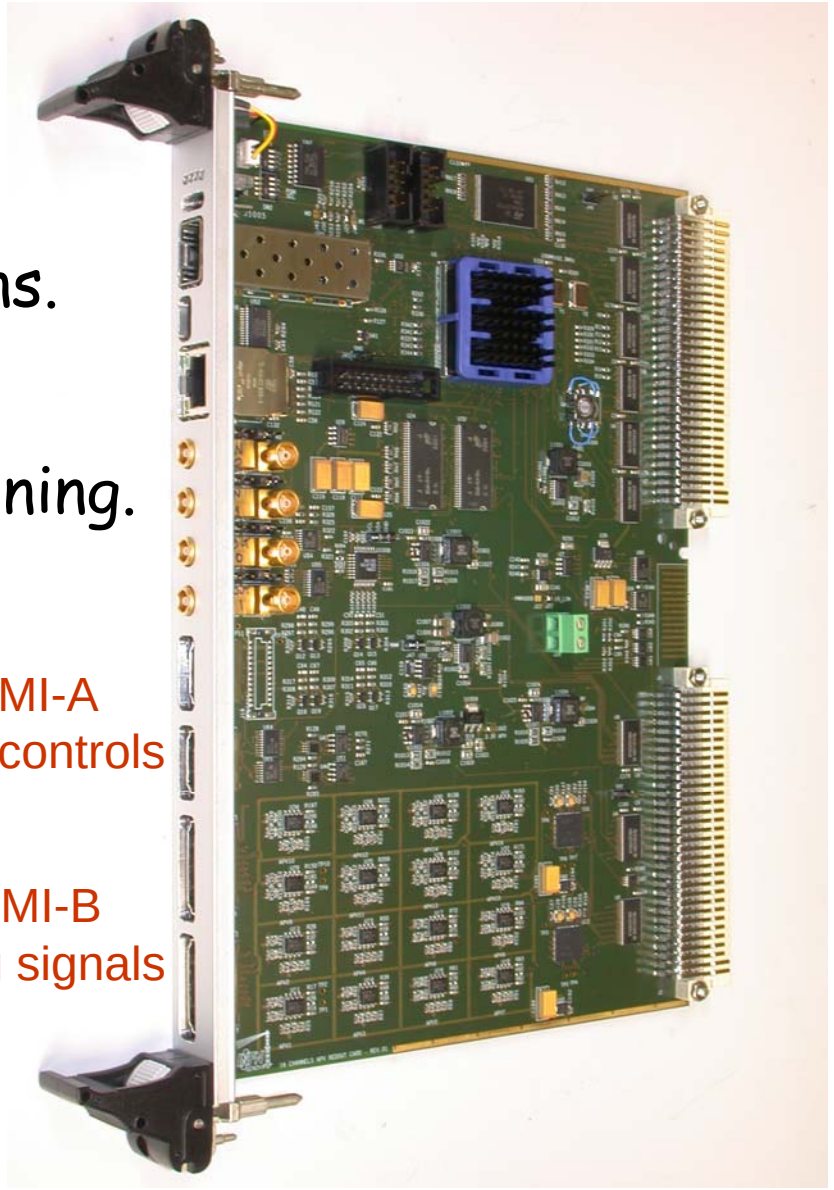
Still only raw data processing.

Two boards fabricated.

Electronic Noise < 1 LSB (RMS).

RD51 front-end compatible with HDMI-A.

Now used for development.



Third revision

Few HW modification (small bugs) and optimizations.

Implementation of other users requests.

Data processing development:

- Baseline calculation and removal (common mode noise)
- Pedestal subtraction
- Threshold cut
- Fragment building

Use of large data buffer (DDR SDRAM)

JLAB12 DAQ data format compatibility.

Submitted for fabrication last week.

Conclusions

The development of the system is in advanced phase.

Several groups asked to buy different pieces of the system: front-end, MPD, adapters...

All items are produced by Italian firm EES S.p.A.

Next steps:

- Release a complete and stable version with VME interface

Future development:

- Implement optical interface (connect to SIS1100e)
- Implement SOC with Ethernet interface