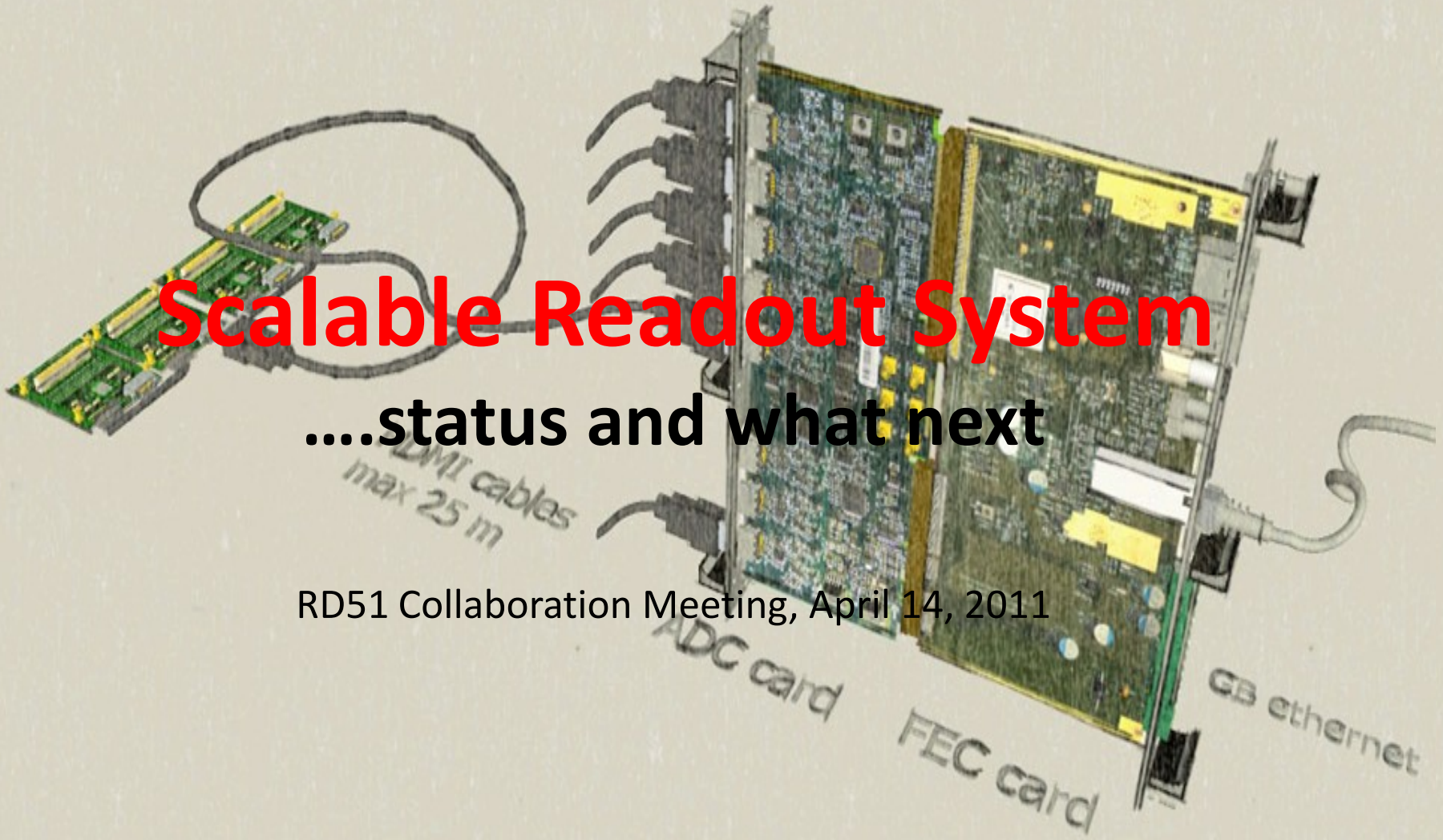
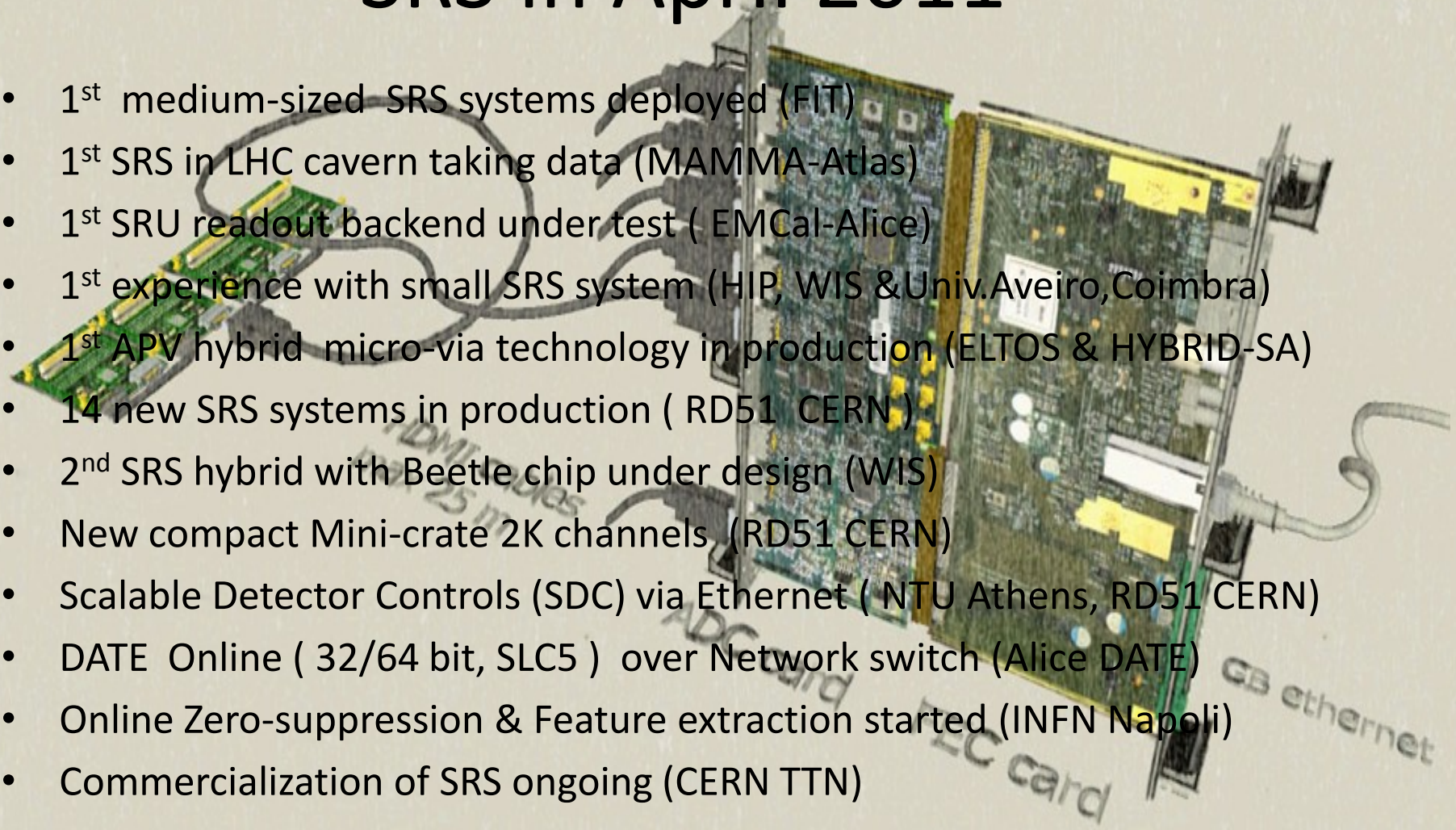


Scalable Readout System

….status and what next

RD51 Collaboration Meeting, April 14, 2011

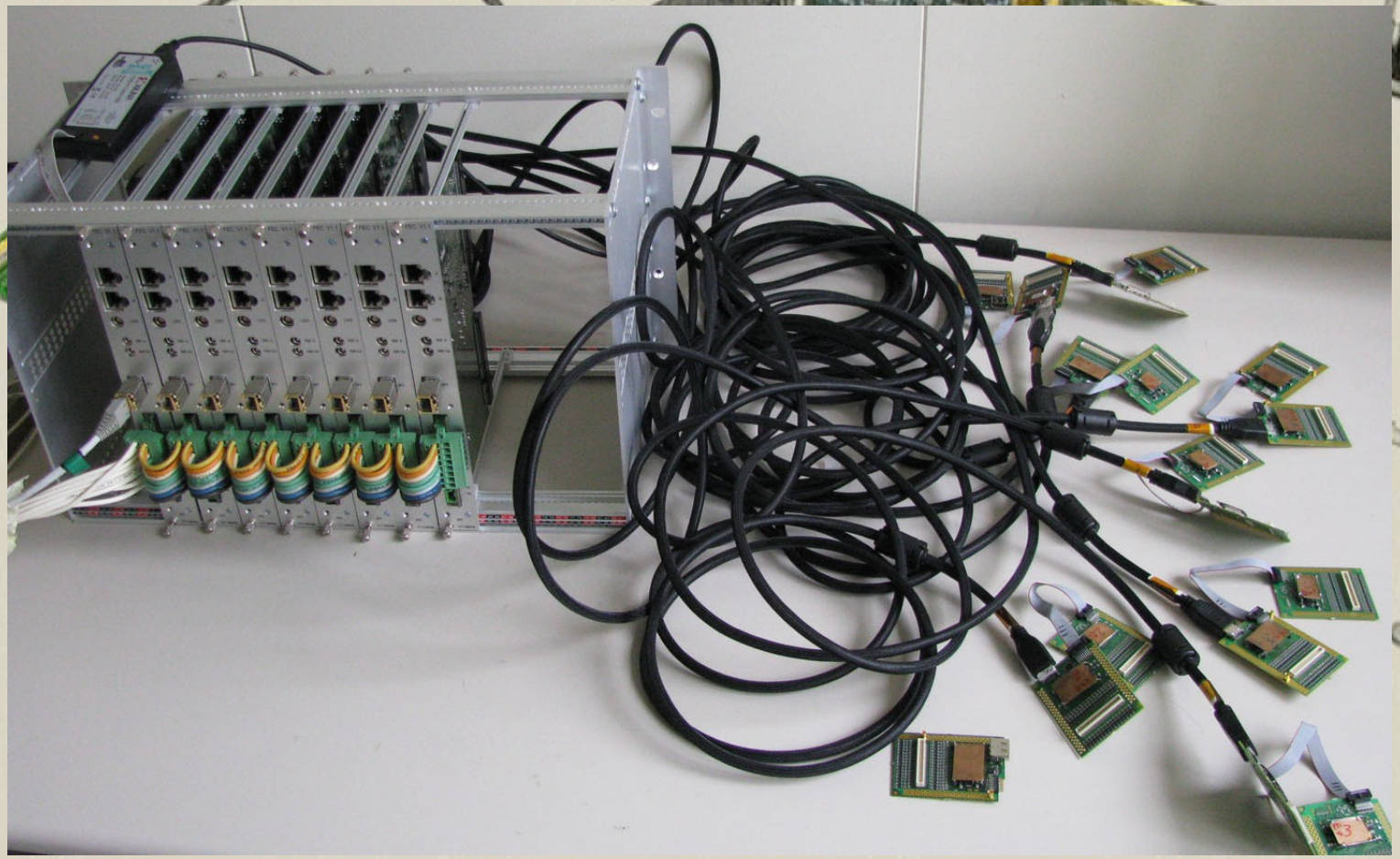
SRS in April 2011



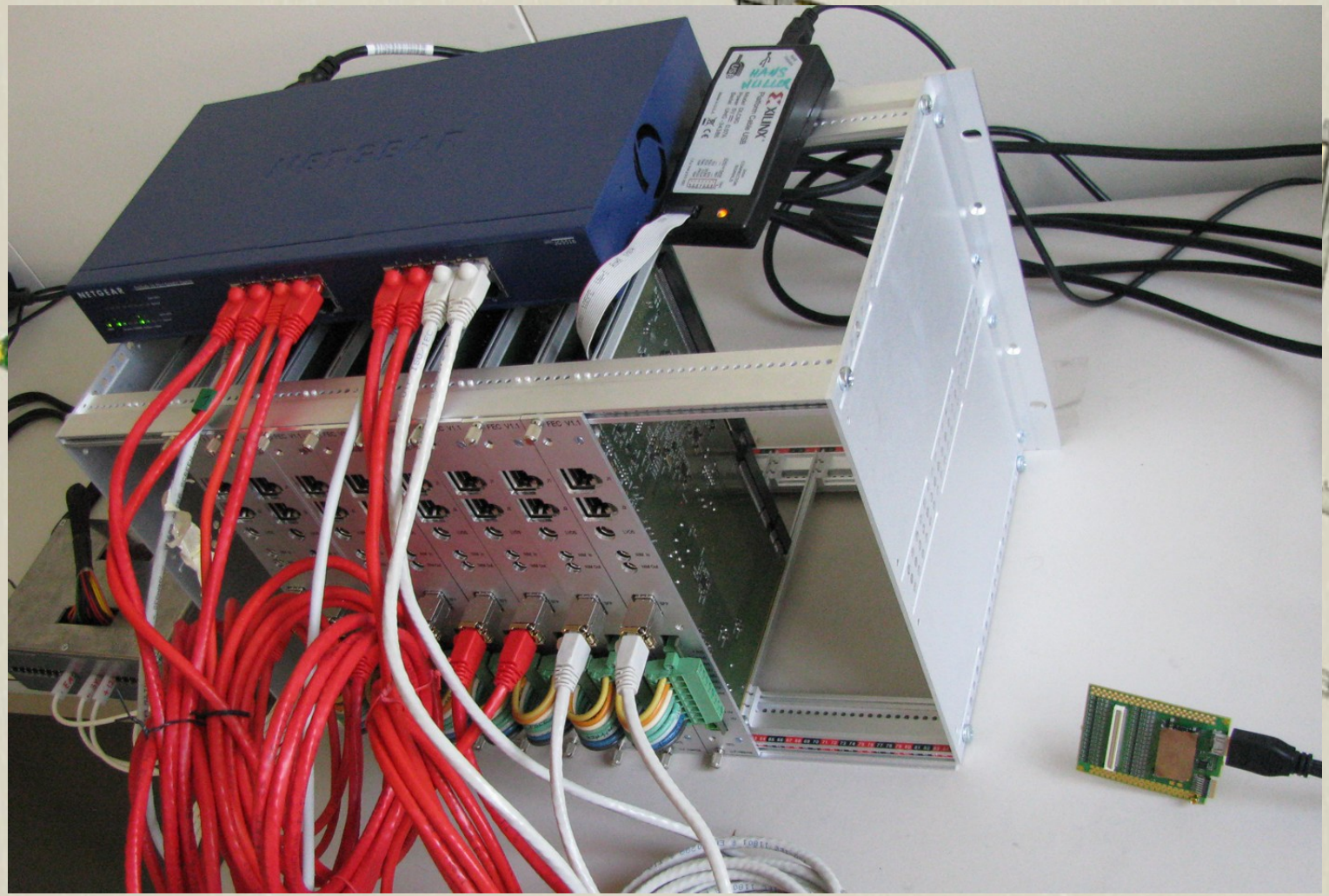
- 1st medium-sized SRS systems deployed (FIT)
- 1st SRS in LHC cavern taking data (MAMMA-Atlas)
- 1st SRU readout backend under test (EMCal-Alice)
- 1st experience with small SRS system (HIP, WIS &Univ.Aveiro,Coimbra)
- 1st APV hybrid micro-via technology in production (ELTOS & HYBRID-SA)
- 14 new SRS systems in production (RD51 CERN)
- 2nd SRS hybrid with Beetle chip under design (WIS)
- New compact Mini-crate 2K channels (RD51 CERN)
- Scalable Detector Controls (SDC) via Ethernet (NTU Athens, RD51 CERN)
- DATE Online (32/64 bit, SLC5) over Network switch (Alice DATE)
- Online Zero-suppression & Feature extraction started (INFN Napoli)
- Commercialization of SRS ongoing (CERN TTN)

Medium-sized system (FIT)

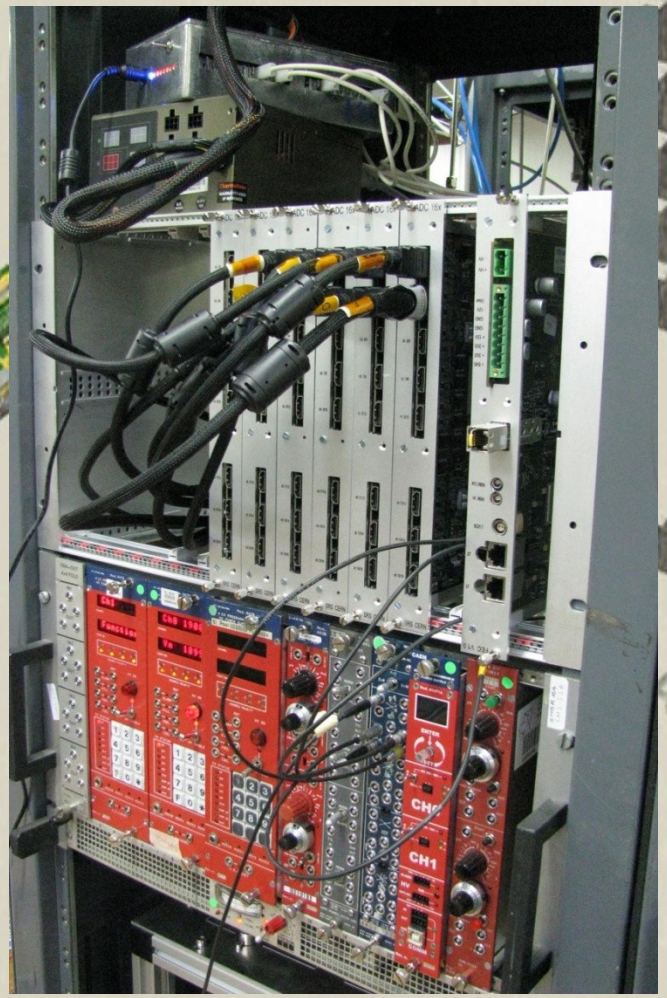
8 FECs for 16 k APV channels

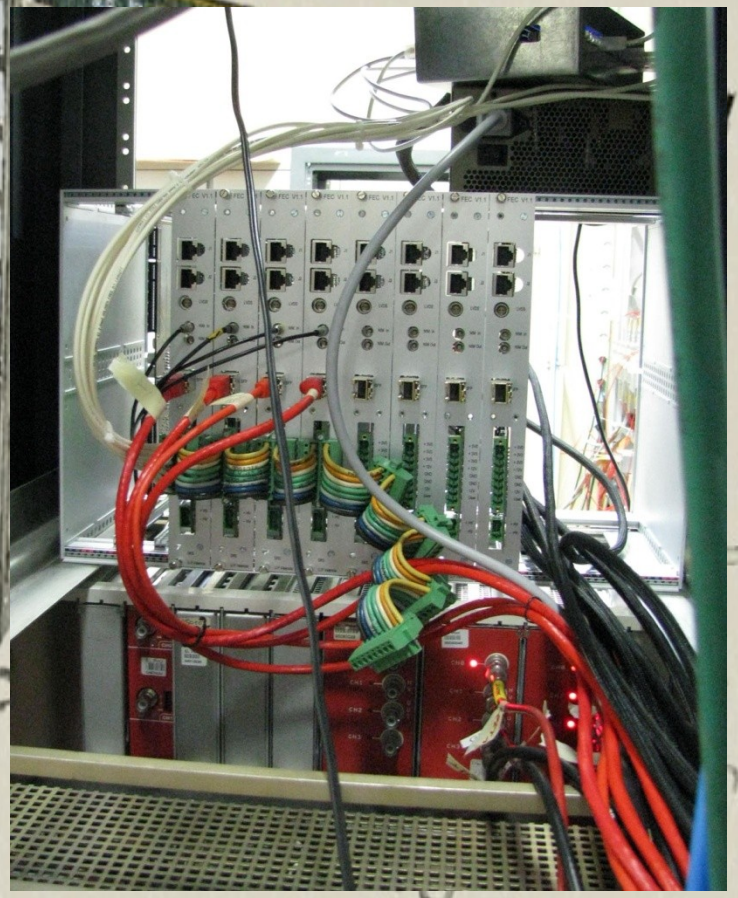


Online(DATE) via 8xGbE Switch

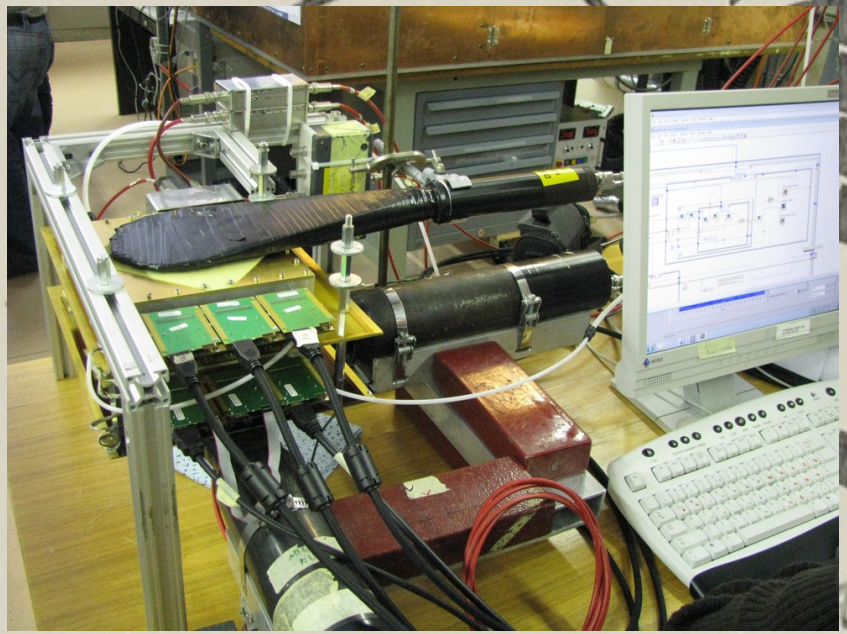


GEM readout in GDD lab





ATLAS MicroMega



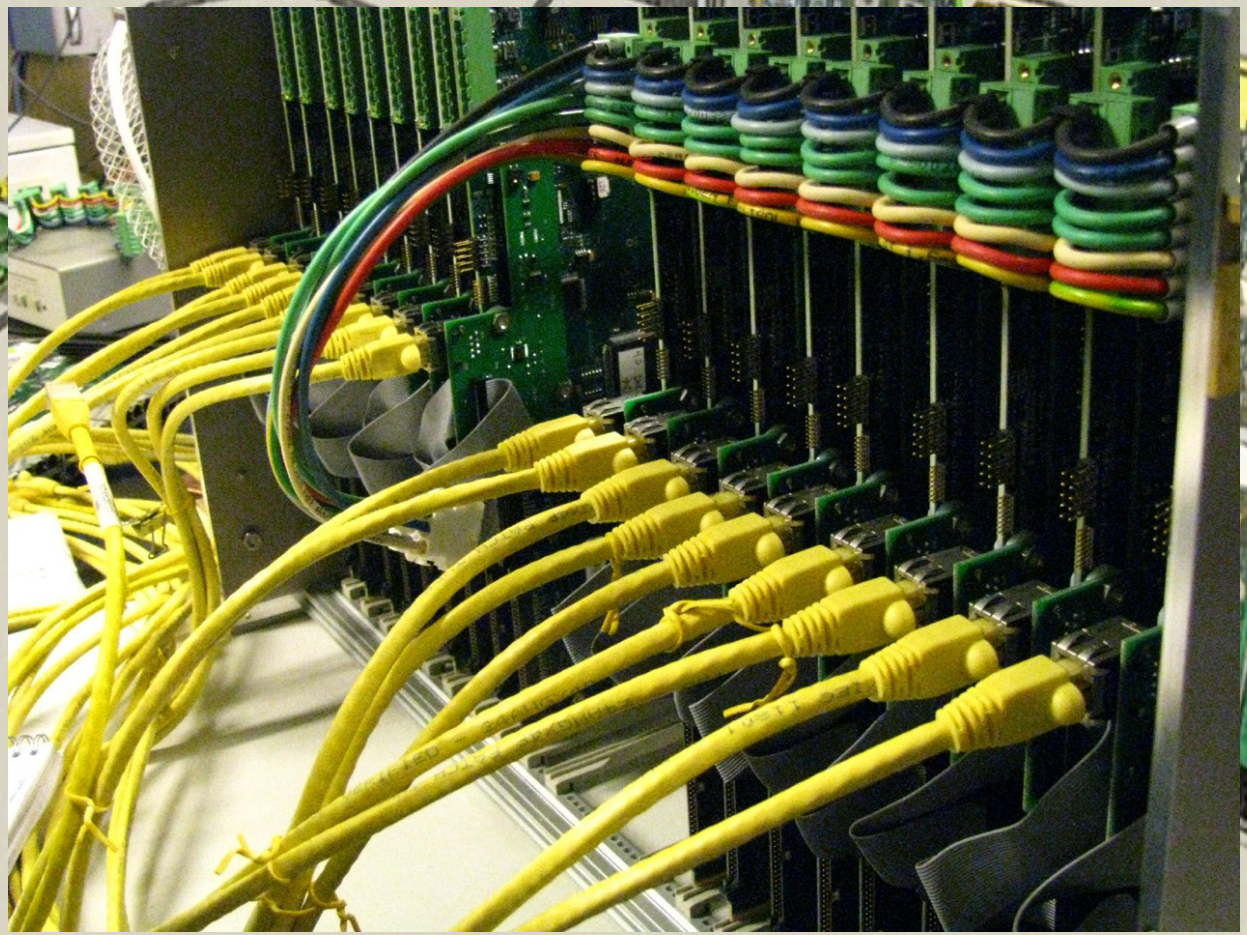
MicroMega test
with cosmic trigger

CSC –sized Micromega

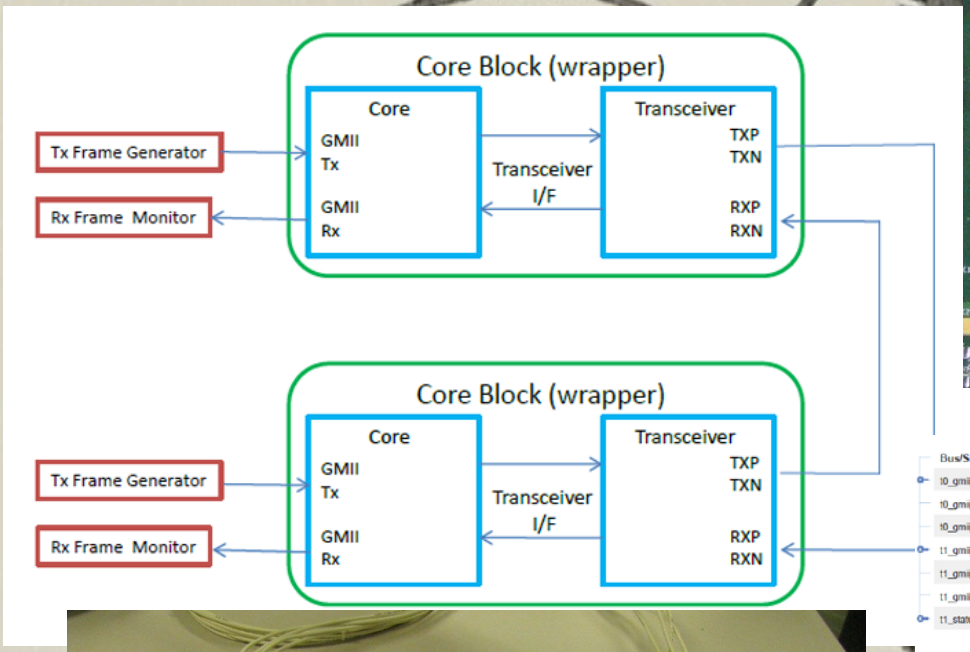
SRS in ATLAS Cavern

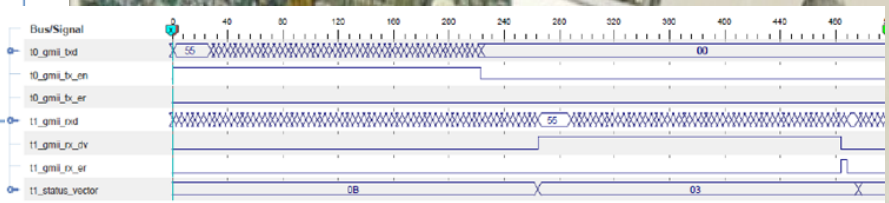
EMCal ALICE

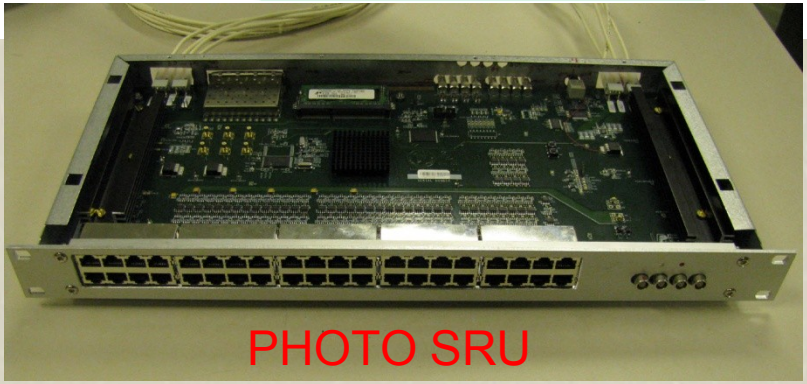
legacy ALTRO card readout via DTC links to SRU



SFP+ link on SRU works







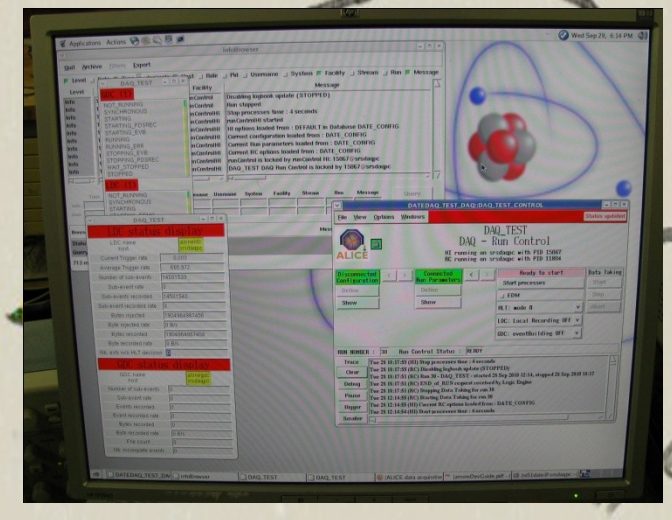
SFP+ hardware on SRU works!

- t0_gmii_txd is the data send out the transceiver T0 (one SFP+ transceiver)
- t1_gmii_rxd is the data received by the transceiver T1 (another SFP+ transceiver)
- T0 and T1 is connected via a direct SFP+ cable.
- There is some transmission delay between T0 and T1.

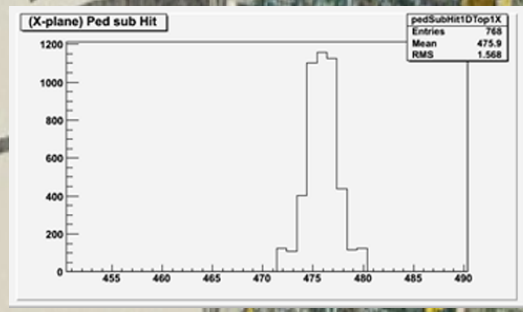
4/4/2011 | Fan.Zhang : SRU SFP Plus Hardware Test | 5

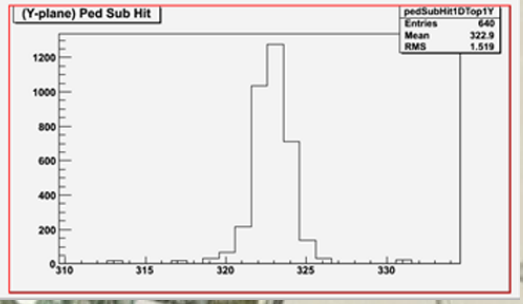
SRS online screens

DATE = default Online system

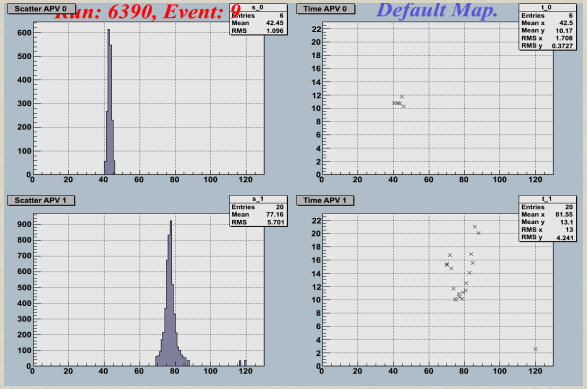


Root & AMORE

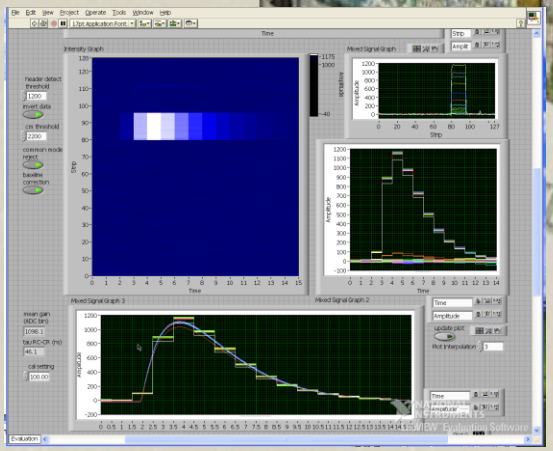




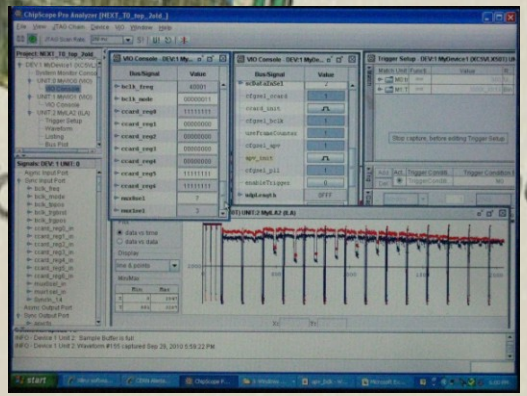
MMDAQ (Atlas MM)



Labview



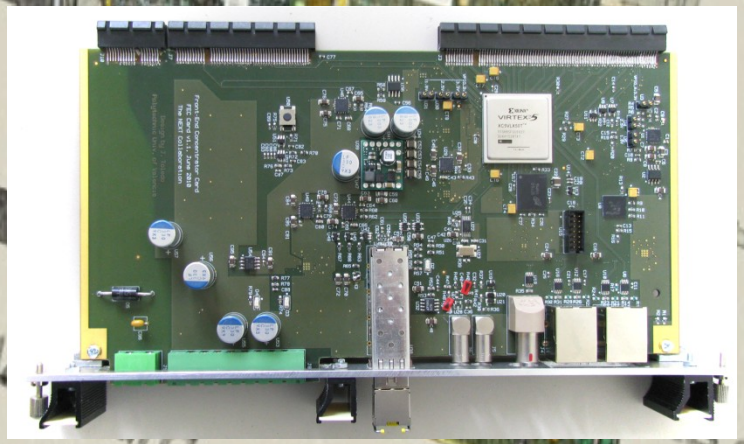
Xilinx ISE chip-scope



FEC cards

22 FECs V1.1 produced in 2010

16 FEC V1.3 awaiting production



Virtex-5 FPGA, Gb-Ethernet, DDR buffer
NIM and LVDS pulse I/O
High speed Interface connectors to frontend adapter cards

ADC frontend adapter

for APV and Beetle chip

18 ADC V1.0 produced in 2010

18 ADC V1.1 in production 2011

ADC plugs into FEC to make a 6U readout unit for up to 2048 channels

Frontend hybrids

so far all based on APV25 chip

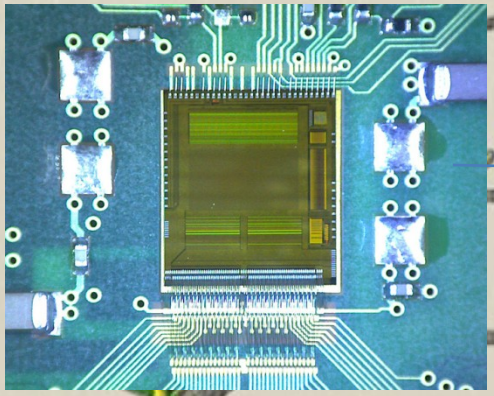
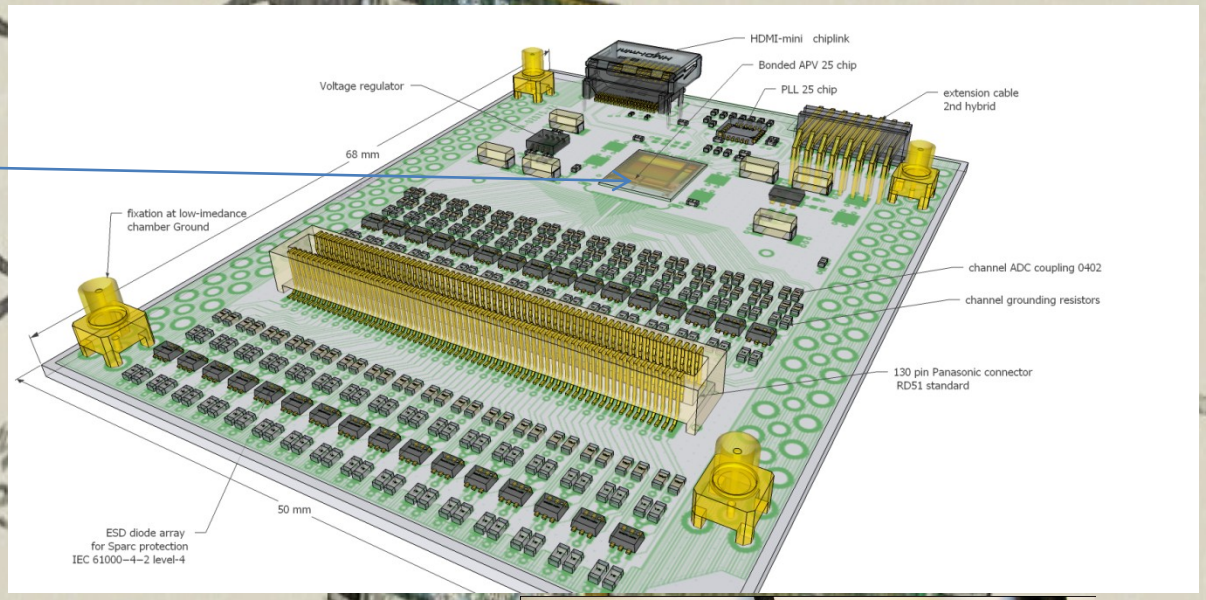
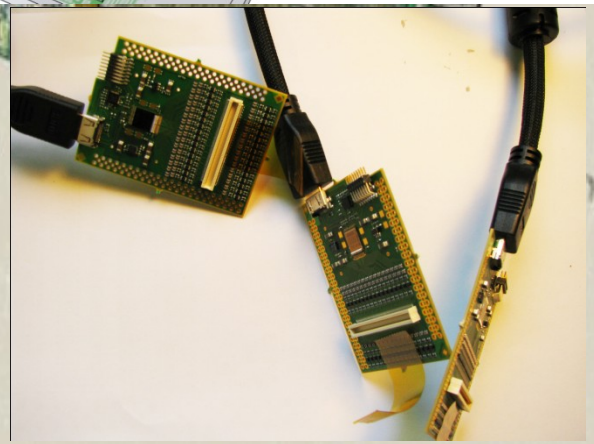


Photo of wire-bonded APV
on RD51 hybrid Version 3

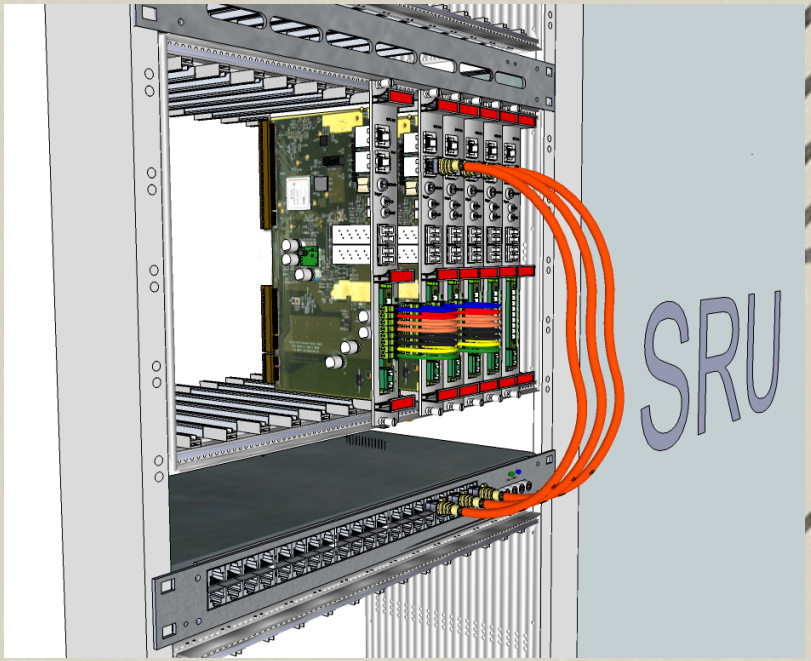




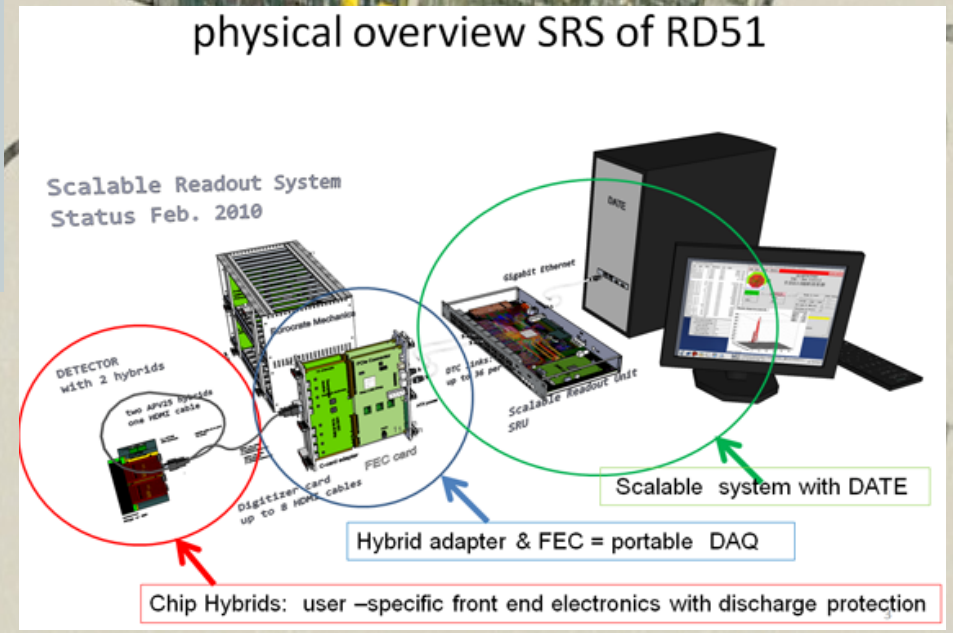
Version 1 proto: 5 working ones
Version 2 users: 11
Version 3 systems: 15 (CERN: Rui + bonding service)
292 (ELTOS + Hybrid SA)
under production this week

Large SRS system

become SRU-based readout Clusters

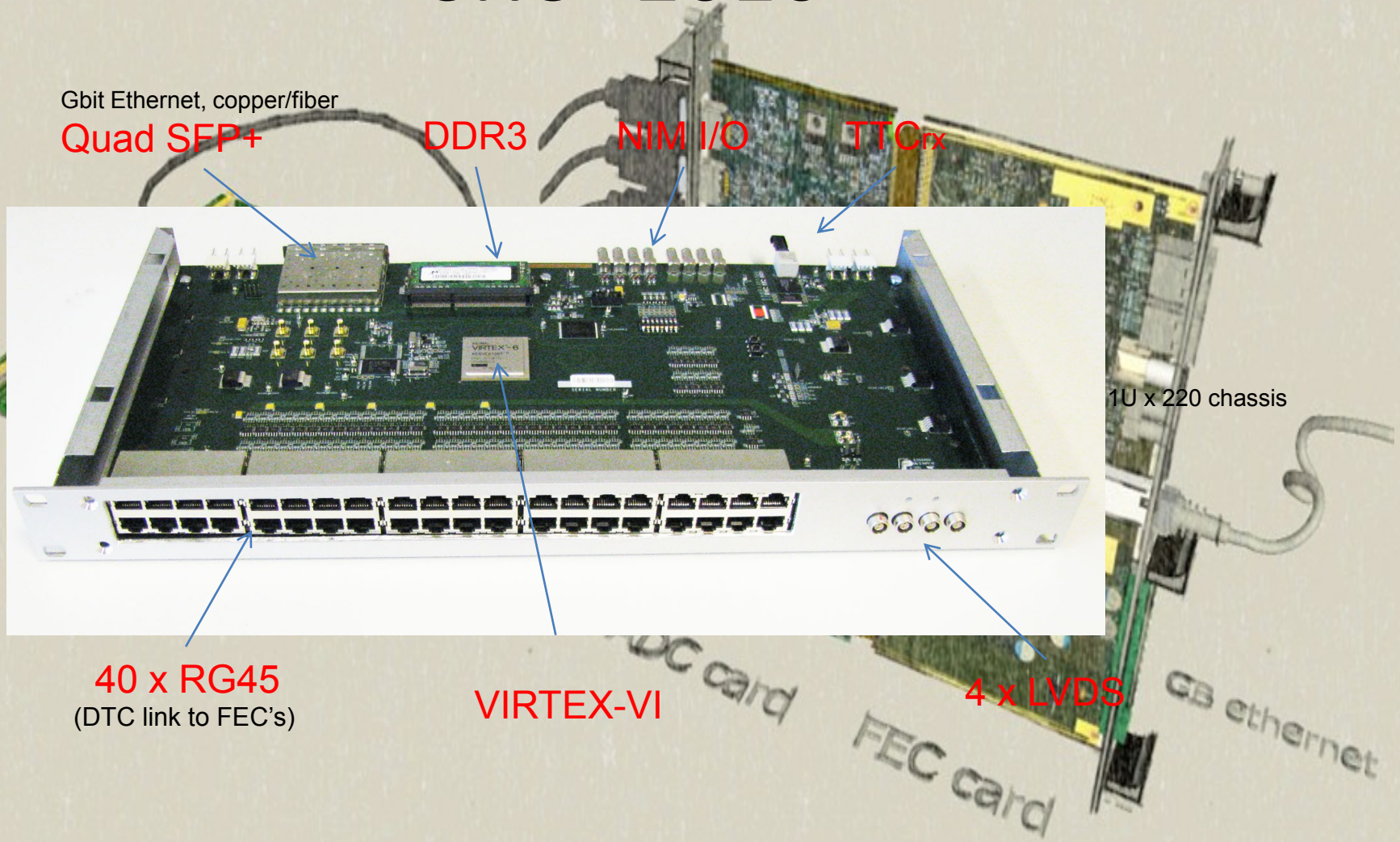


SRU box concentrates high speed links
from 40 FECs into
10 Gigabit Ethernet to Online
(84k channels = 1 SRU)

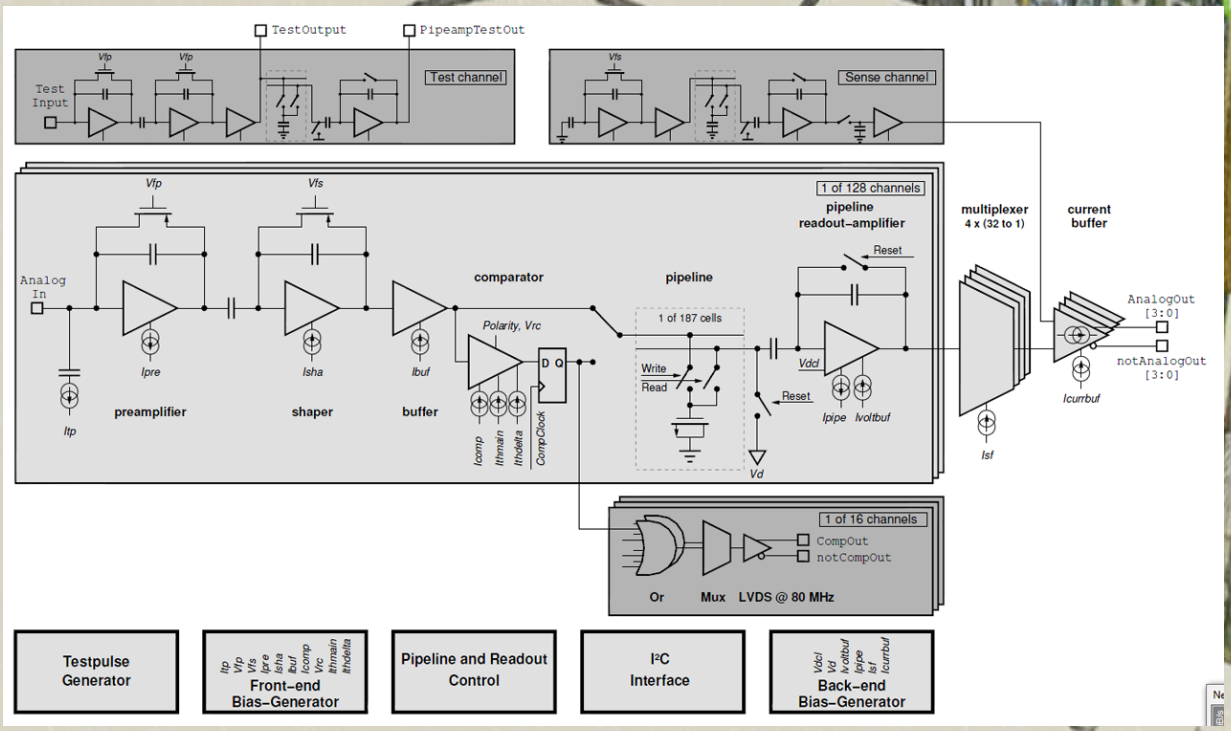


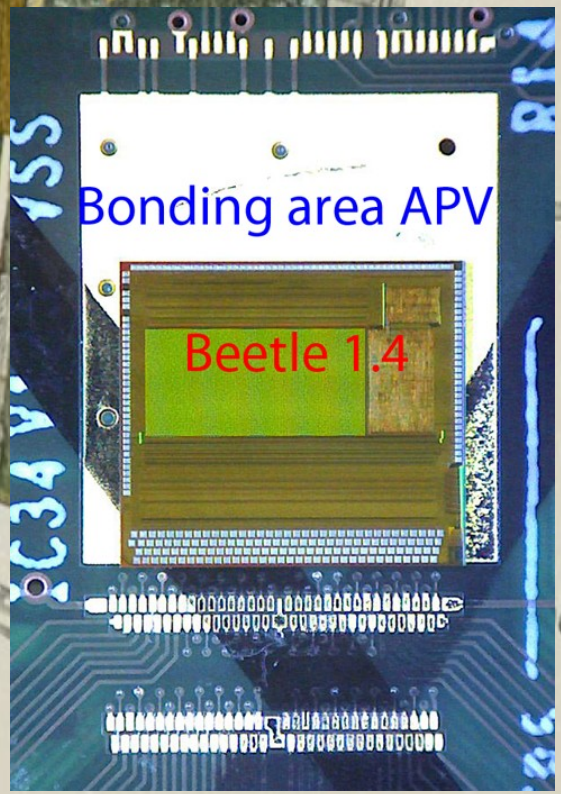
2 SRU's 2010 under test
6 SRU's awaiting production
15 SRU's 2011 for ALICE EMCal

SRU -2010

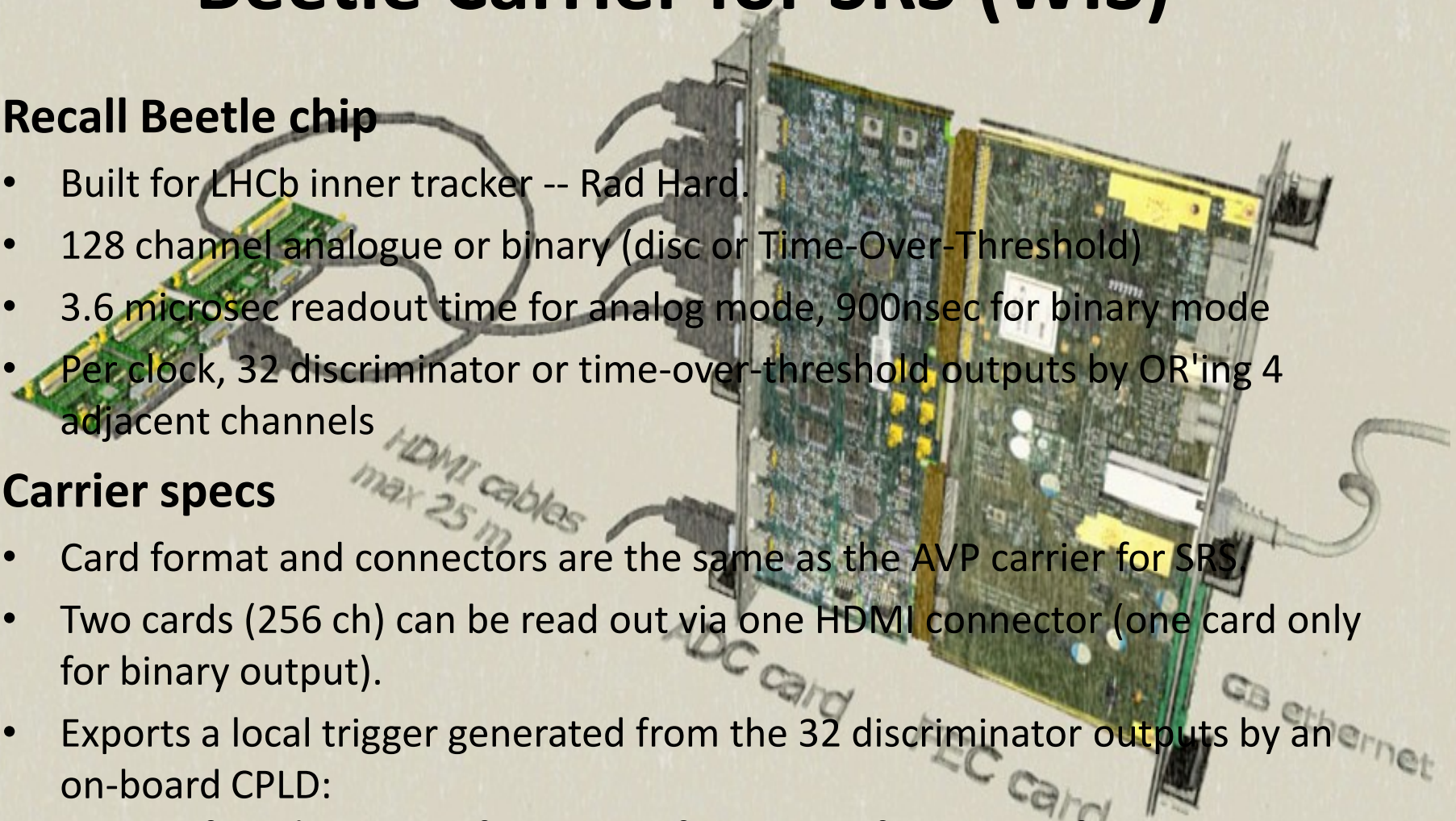

Gbit Ethernet, copper/fiber
Quad SFP+
DDR3
NIM I/O
TTCrx
1U x 220 chassis
40 x RG45
(DTC link to FEC's)
VIRTEX-VI
4 x LVDS
DC card
FEC card
GB ethernet

Beetle hybrid for SRS





Beetle Carrier for SRS (WIS)



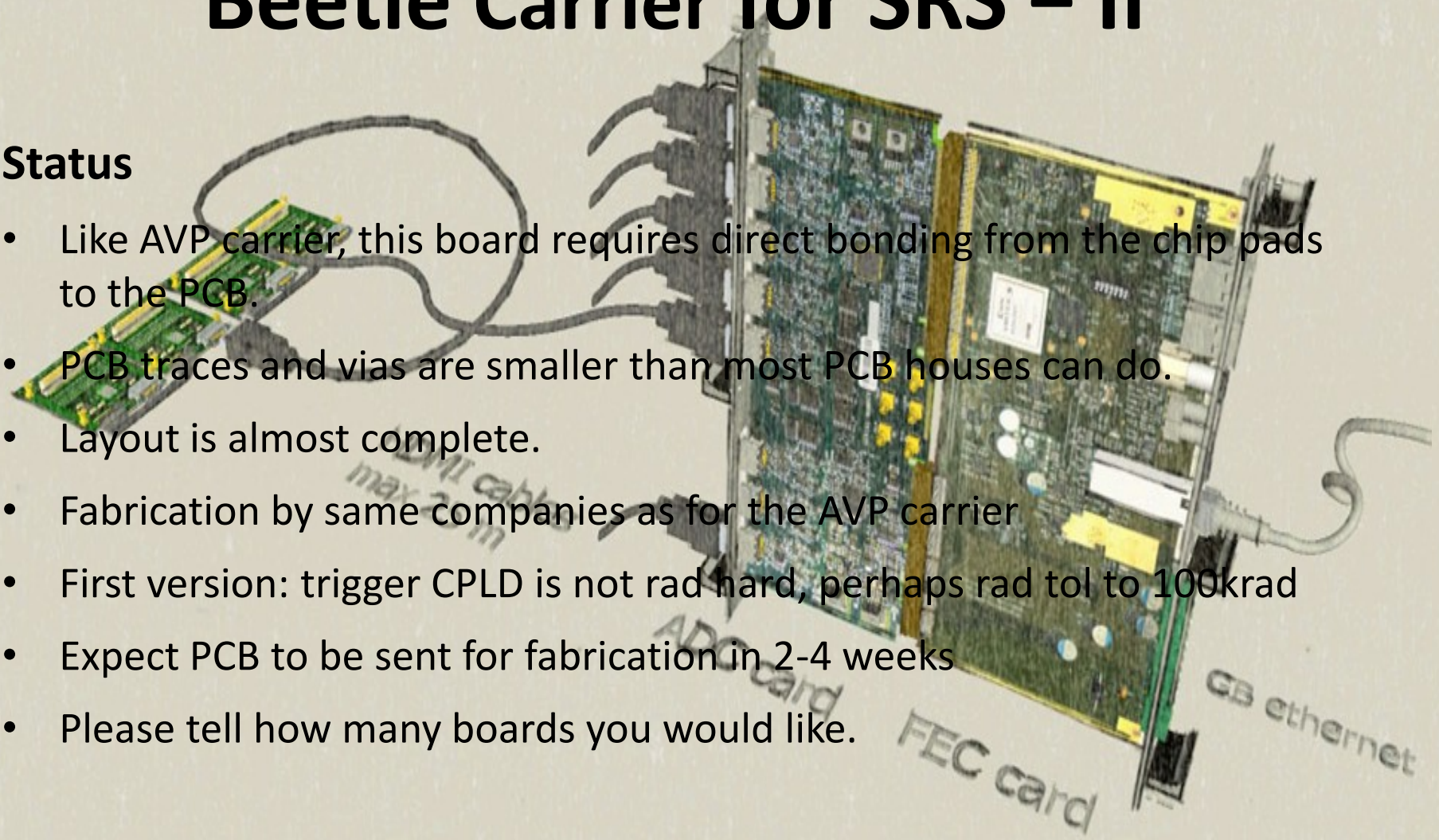
Recall Beetle chip

- Built for LHCb inner tracker -- Rad Hard.
- 128 channel analogue or binary (disc or Time-Over-Threshold)
- 3.6 microsec readout time for analog mode, 900nsec for binary mode
- Per clock, 32 discriminator or time-over-threshold outputs by OR'ing 4 adjacent channels

Carrier specs

- Card format and connectors are the same as the AVP carrier for SRS.
- Two cards (256 ch) can be read out via one HDMI connector (one card only for binary output).
- Exports a local trigger generated from the 32 discriminator outputs by an on-board CPLD:
  - e.g. found a 2-out-of-2, 2-out-of-4, 3-out-of-4, 4-out-of-4, etc.

Beetle Carrier for SRS – II

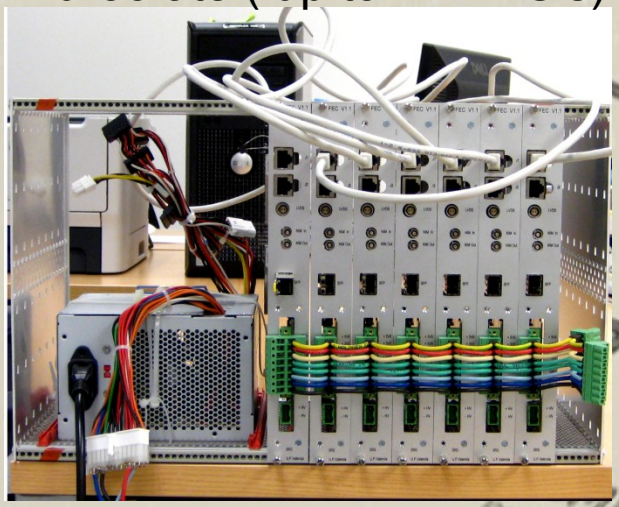


Status

- Like AVP carrier, this board requires direct bonding from the chip pads to the PCB.
- PCB traces and vias are smaller than most PCB houses can do.
- Layout is almost complete.
- Fabrication by same companies as for the AVP carrier
- First version: trigger CPLD is not rad hard, perhaps rad tol to 100krad
- Expect PCB to be sent for fabrication in 2-4 weeks
- Please tell how many boards you would like.

New SRS Minicrate

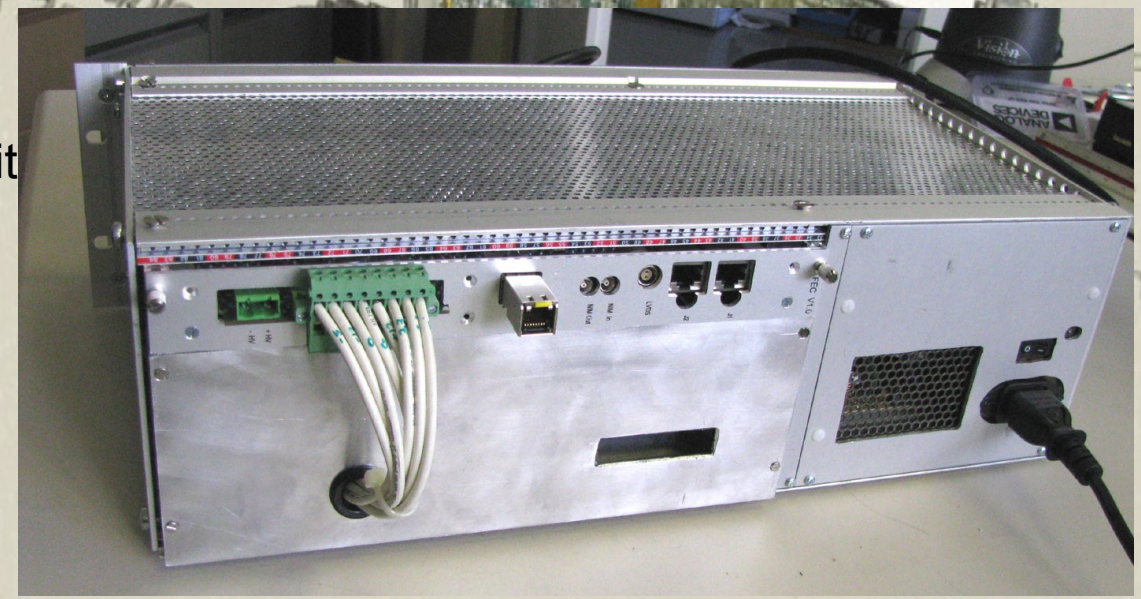
Eurocrate (up to 14 FEC's)



Medium sized systems

Initial small systems

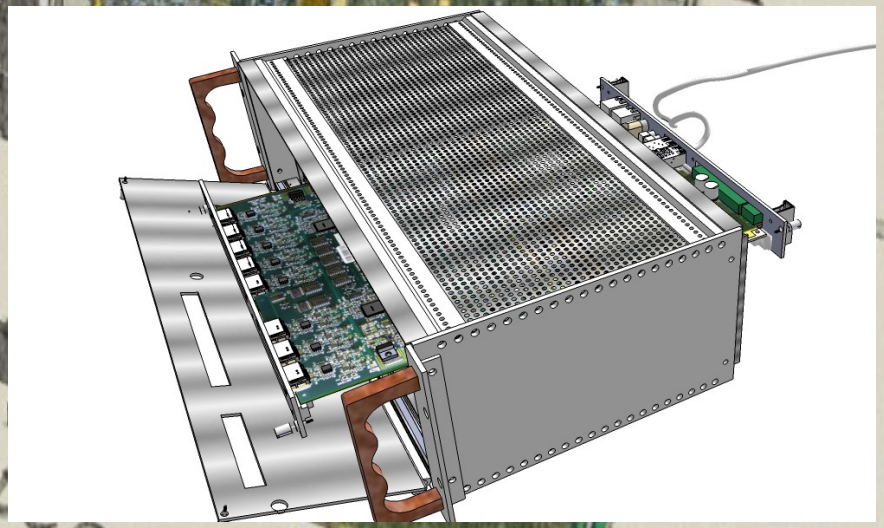
Minicrate (up to 2 FEC's)



5 kg portable 3U x220 unit
ATX power and ventilation
Included

Eurocrate vs Minicrate

Eurocrate 6U: up to 14 positions, power not included



Minicrate 3U , max 2 positions, power included

Power for SRS

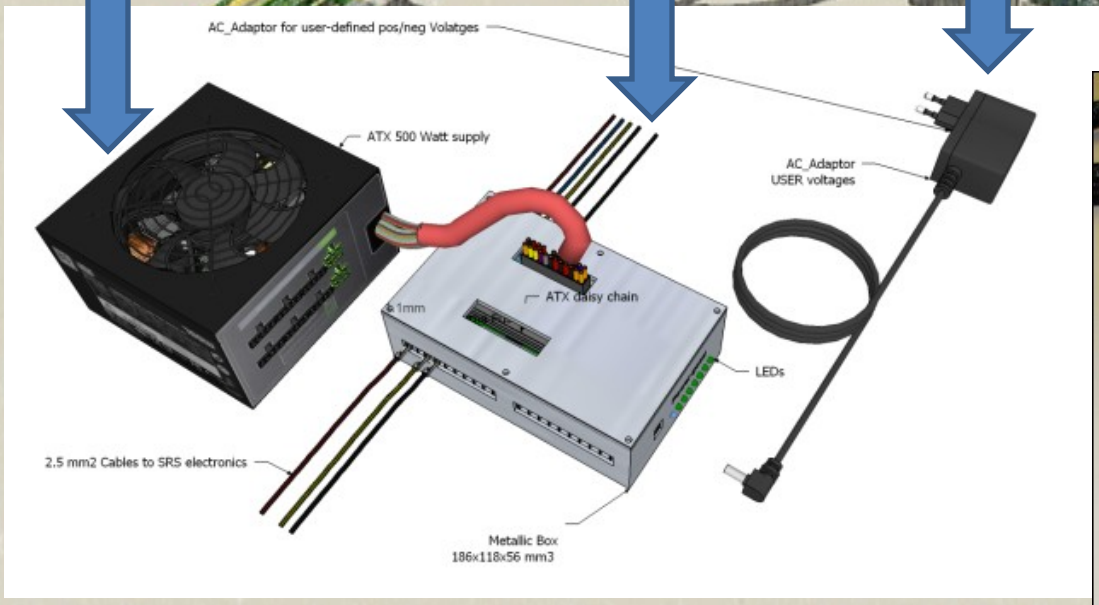
ATX Power => SRS Adapter => SRS

ATX power up 1 kW very cheap (but noisy and not earth-free)

➔ SRS ATX adapter adds EMI filtering and more Voltages + FUSES

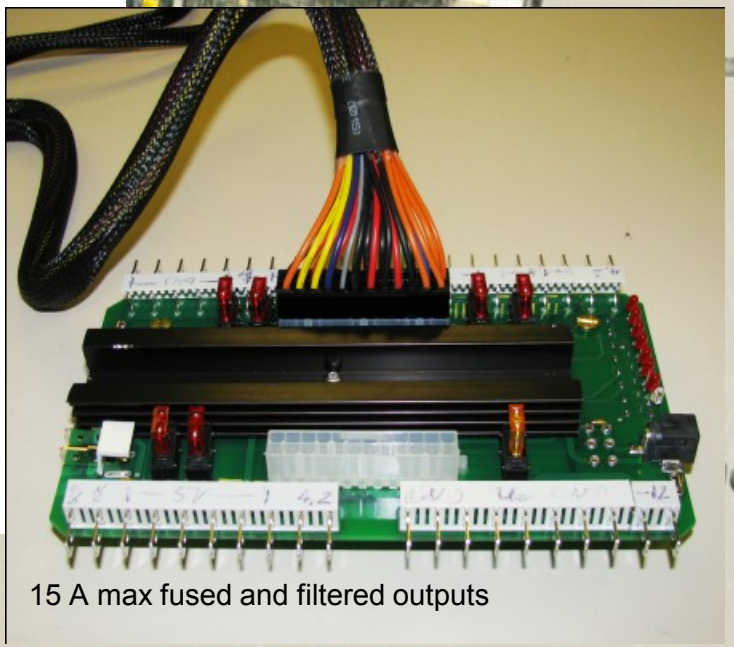
Remove earth-pin from mains plug

earth-free switching ADC adapters for user voltages (like -5V) not available on ATX



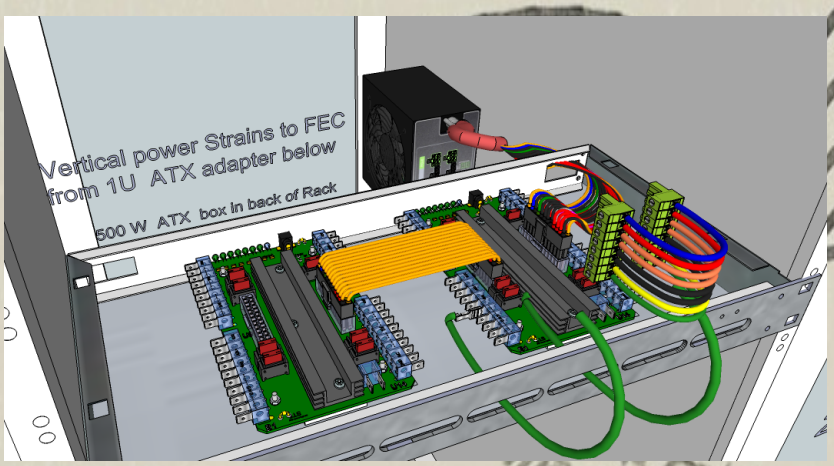
+5V0,+4V2,+1V8,+3V3,+12V,-12V,-5V0

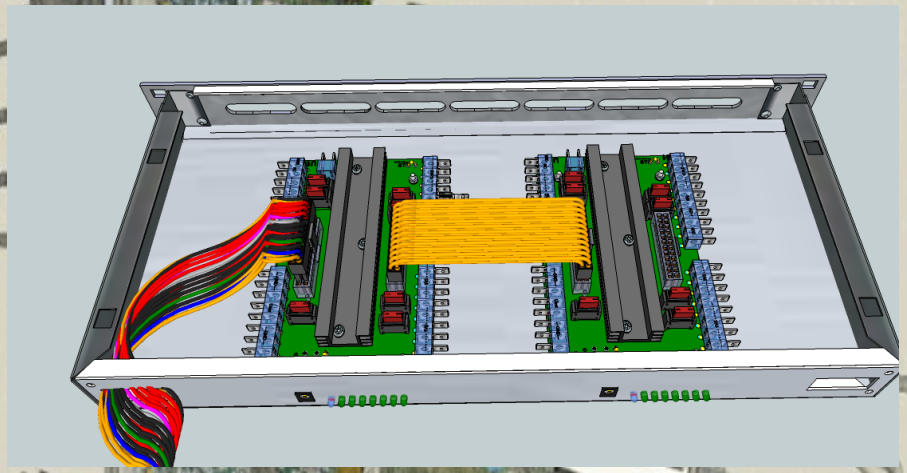
Photo 1st ATX adapter

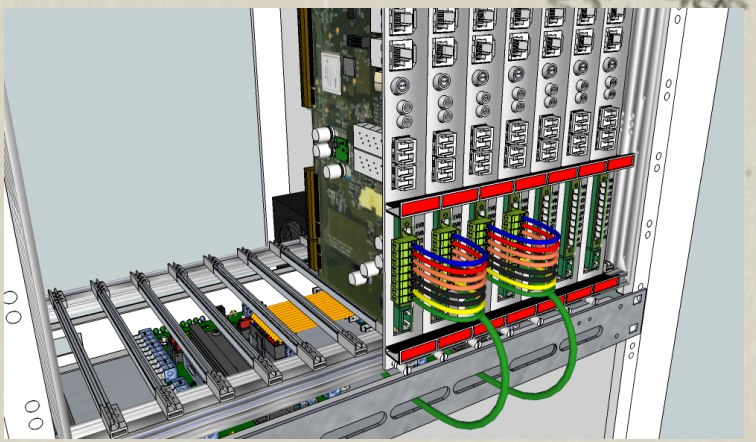


15 A max fused and filtered outputs

Power for SRS







Registered SRS Users

CERN experiments

- ATLAS CSC upgrade Micromegas
- ALICE EMCaL , SRU-based readout backend
- NA62 Straw tracker

Other HEP experiments

- NEXT Collaboration, dual Beta decay, SiPM, PM
- BUDKER, INP, Deuteron, triple-GEM

Applications with Cosmic Tomography

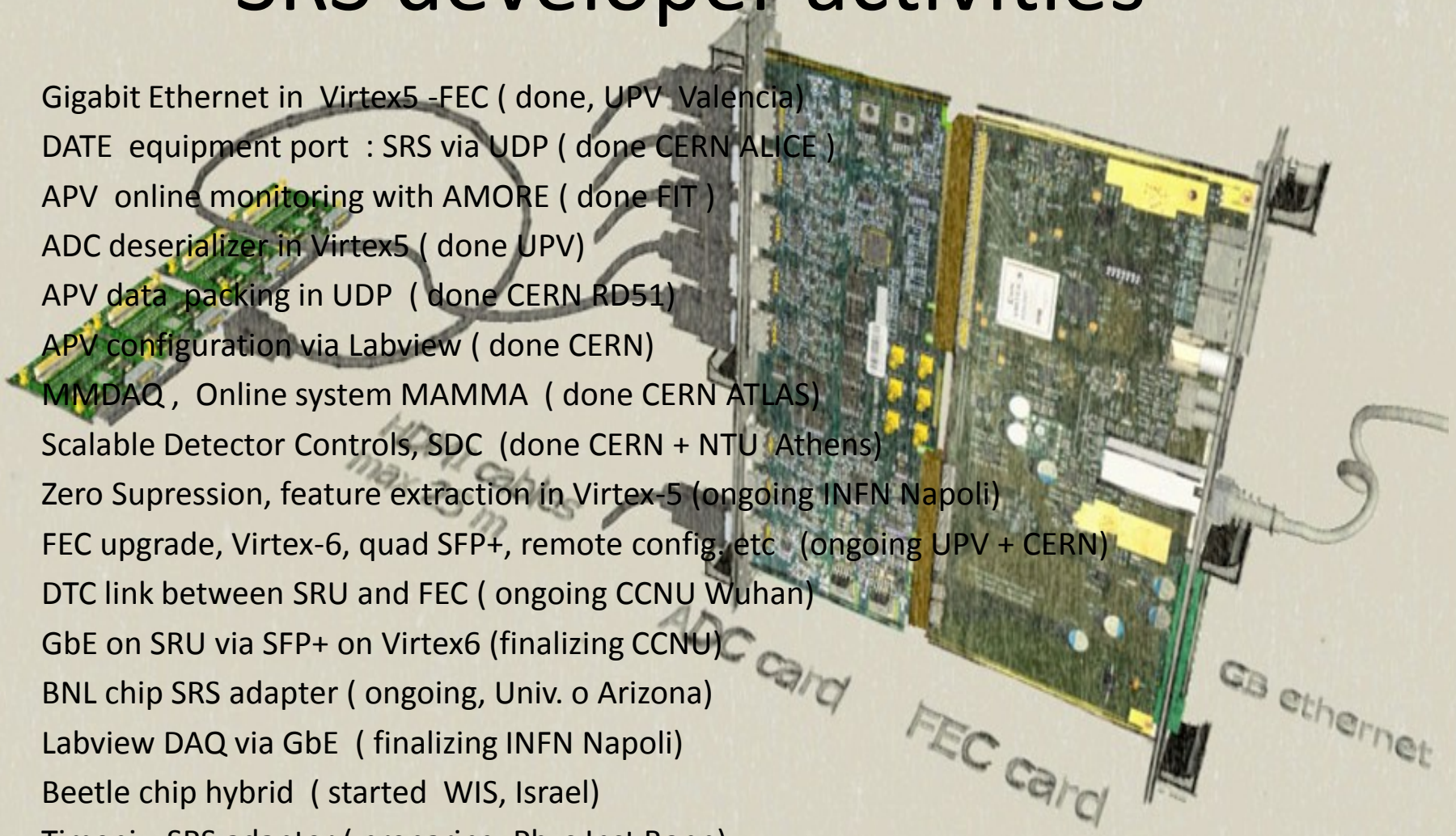
- FIT Florida, homeland security, GEMs
- Geoscienes Azur CRNS- Waterquality, MMegas

R&D with MPGD's (small systems)

- Weizmann Inst. Sci., THGEM tests
- Tsinghua Univ, GEM Imaging
- Bonn/Mainz Univ, Timepix readout
- Helsinki HIP, GEM detector
- LIP Coimbra, micropatten RPC, for PET
- INFN Trieste, THGEM photon detection
- MEXICO UNAM, THGEM
- SAHA Kolkotta, Micromegas
- USTC Shanghai, GEM and MicroMegas
- Zaragoza Univ, GEM and MicroMegas
- CE Saclay, Micromegas
- ..... some more non-confirmed

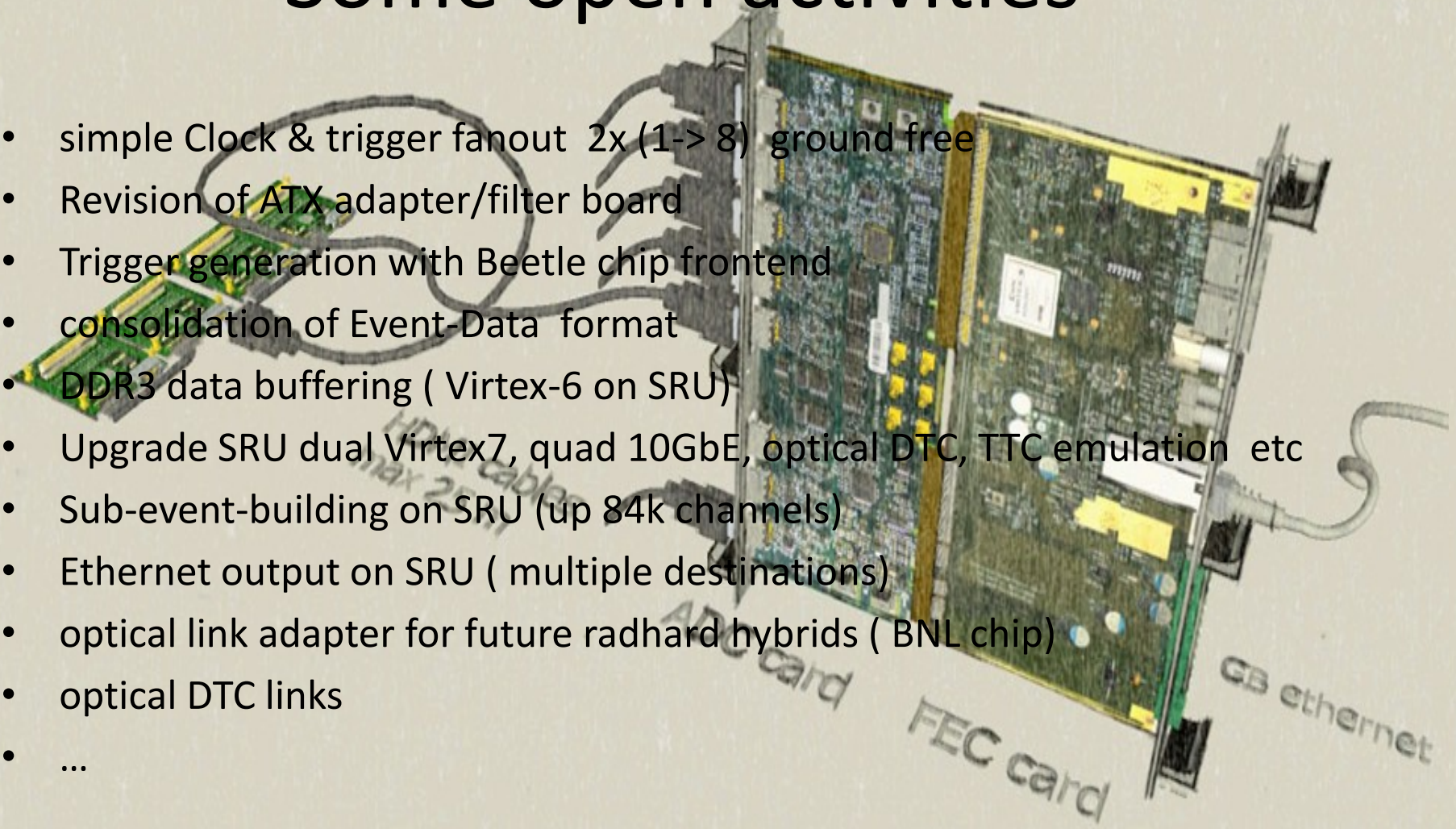
SRS developer activities

- Gigabit Ethernet in Virtex5 -FEC (done, UPV Valencia)
- DATE equipment port : SRS via UDP (done CERN ALICE)
- APV online monitoring with AMORE (done FIT)
- ADC deserializer in Virtex5 (done UPV)
- APV data packing in UDP (done CERN RD51)
- APV configuration via Labview (done CERN)
- MMDAQ , Online system MAMMA (done CERN ATLAS)
- Scalable Detector Controls, SDC (done CERN + NTU Athens)
- Zero Supression, feature extraction in Virtex-5 (ongoing INFN Napoli)
- FEC upgrade, Virtex-6, quad SFP+, remote config. etc (ongoing UPV + CERN)
- DTC link between SRU and FEC (ongoing CCNU Wuhan)
- GbE on SRU via SFP+ on Virtex6 (finalizing CCNU)
- BNL chip SRS adapter (ongoing, Univ. o Arizona)
- Labview DAQ via GbE (finalizing INFN Napoli)
- Beetle chip hybrid (started WIS, Israel)
- Timepix SRS adapter (preparing, Phys Inst Bonn)



Some open activities

- simple Clock & trigger fanout 2x (1-> 8) ground free
- Revision of ATX adapter/filter board
- Trigger generation with Beetle chip frontend
- consolidation of Event-Data format
- DDR3 data buffering (Virtex-6 on SRU)
- Upgrade SRU dual Virtex7, quad 10GbE, optical DTC, TTC emulation etc
- Sub-event-building on SRU (up 84k channels)
- Ethernet output on SRU (multiple destinations)
- optical link adapter for future radhard hybrids (BNL chip)
- optical DTC links
- …

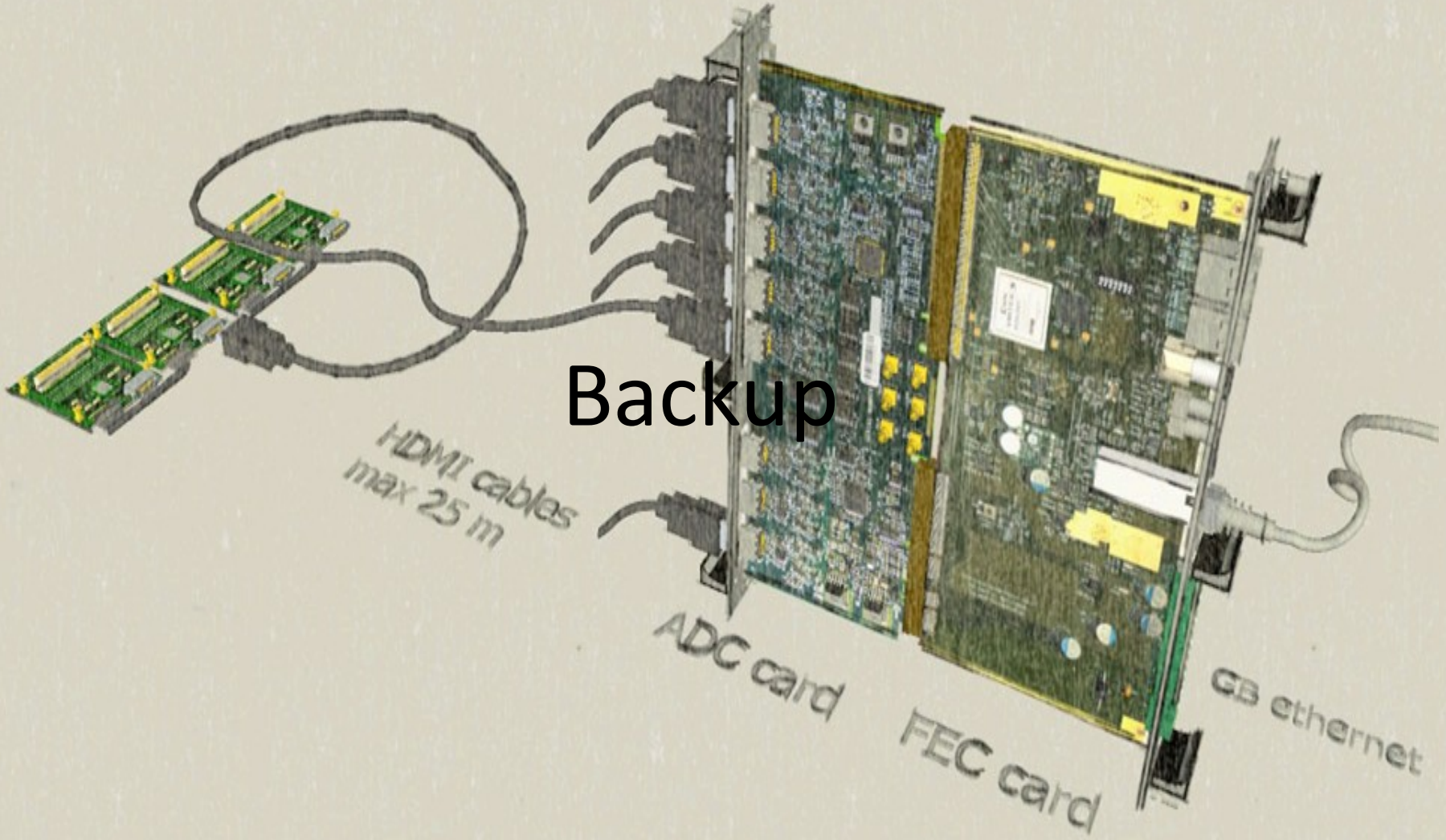


What next

- Finalize production of 14 systems on order
- SRS USER manual
- SRS technical production documentation
- Commercialize SRS as open system
- Retain small , medium, large SRS concept
- Encourage synergies with more detector types
- Encourage user-driven SRS developments

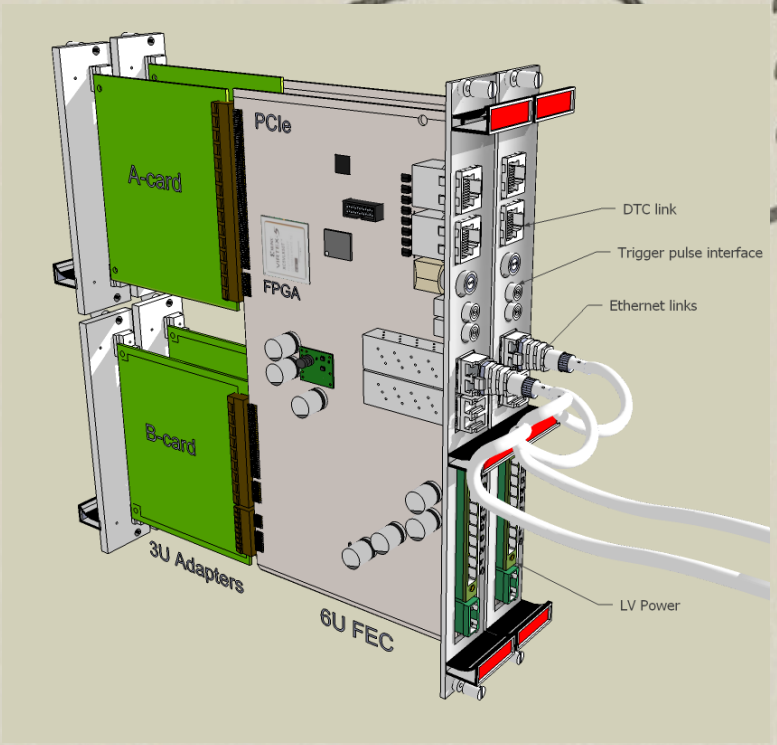
➔ Keep the momentum

Backup

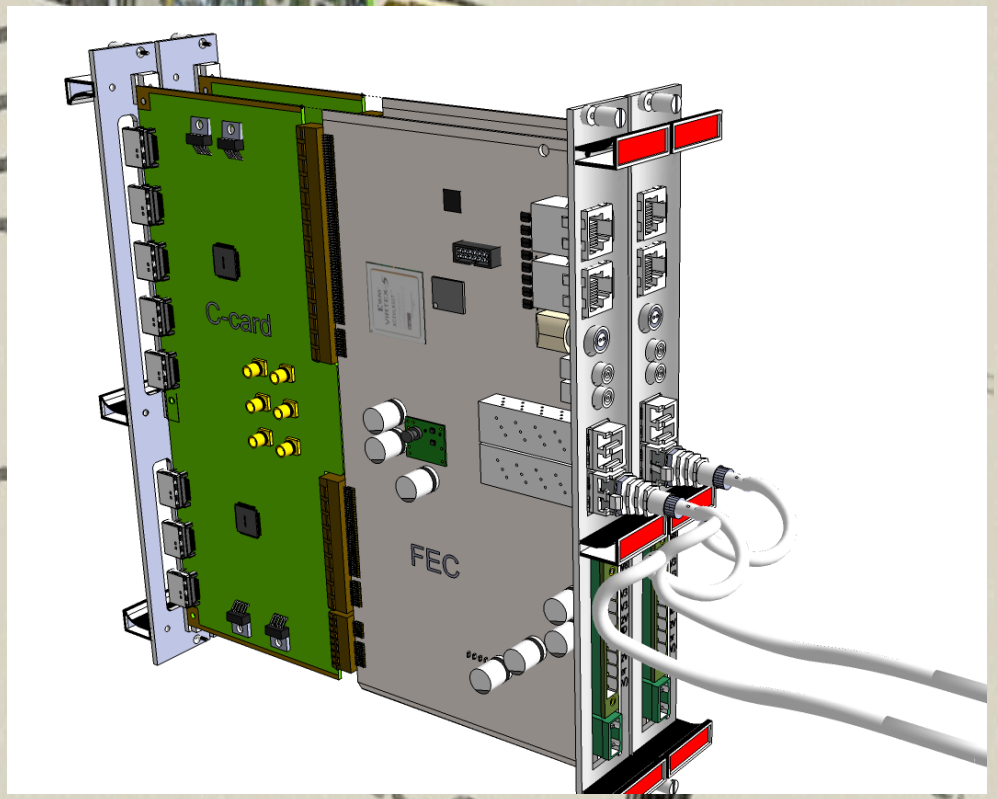


FEC and adapter cards

up to 14 units in one 6U x220 Europa Chassis



3U adapter cards (A+B)



6U adapter cards (C)

Design your own SRS adapter?

->FEC interface is important

A-card signals PCIe x16:

PCIe x16	32 bit bus alternat. 16 differential I/Os
	4x5V, +12V, -12V, (more on PCIex1)
	20 differential LVDS
	I2C, JTAG
	Acard_present, Acard_Pwer_good
	2.5-Gigabit (GBTA) 3 diff. Pairs

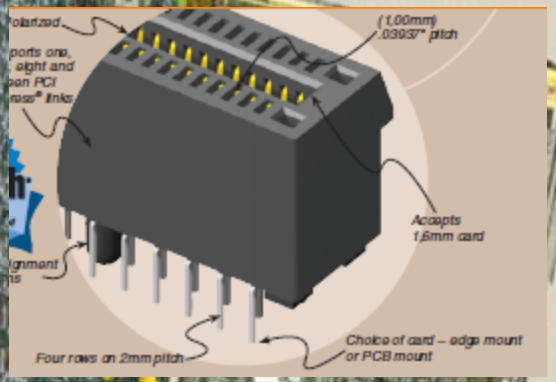
B-card signals PCI x8

16 bit bus, alt. 8 differential I/Os
I2C
Bcard_present, Bcard PWGood
2.5-Gigabit (GBTA) 3 diff. Pairs

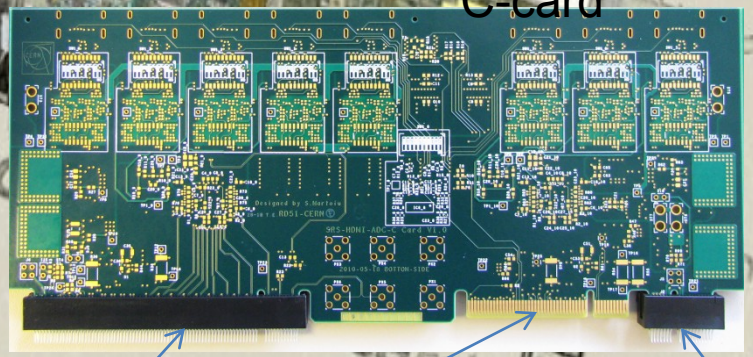
Power connector PCIe_x1 from F.Panel

5 x +5V, 2x +12V, 2 x -5V
7 x GND

PCIe-straddle mount

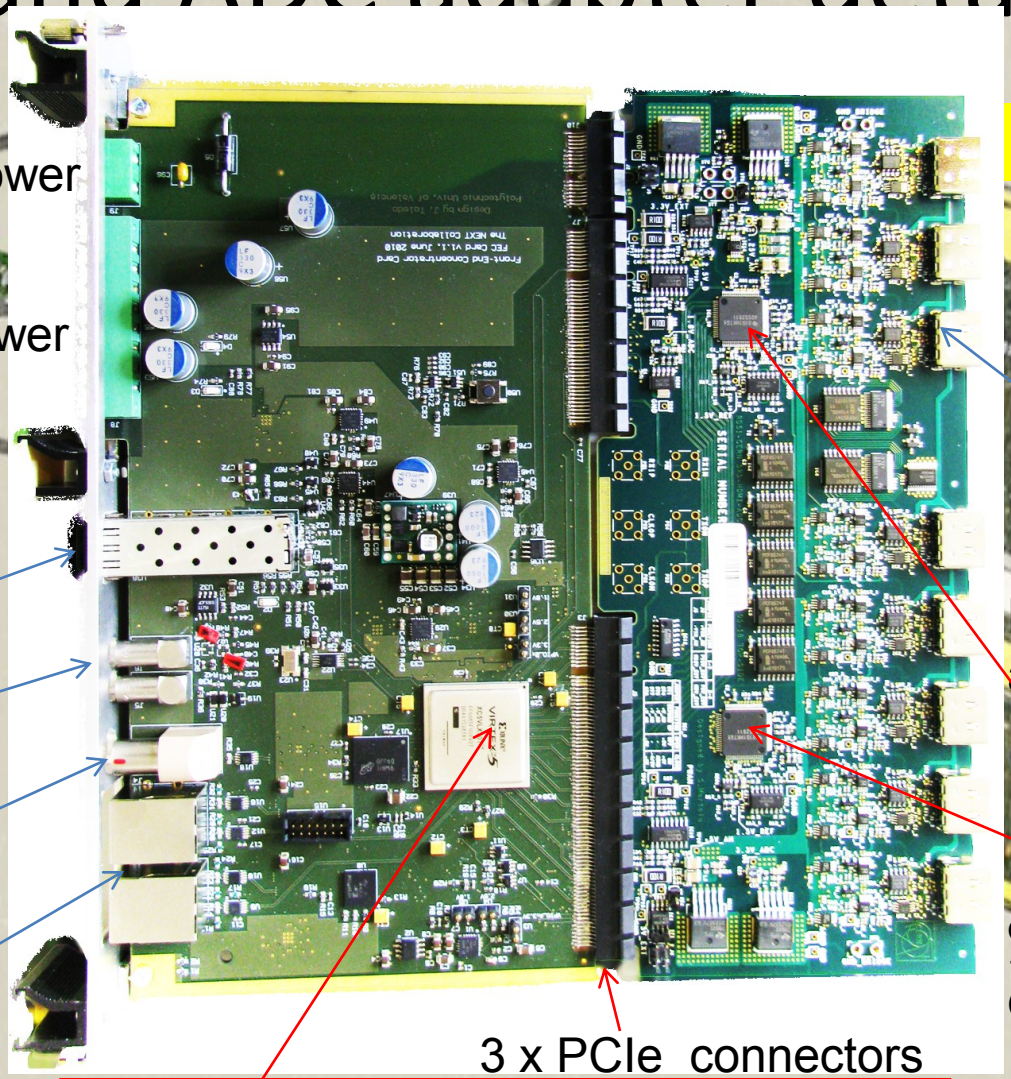


C-card



Note: we do NOT use the PCIe protocol

FEC and ADC adapter details



FEC card V1.2

HV power

LV power

GbEthernet
(New 2x)

NIM I/O (Trigger)

LVDS I/O (BUSY)

2x RJ45
DTC link to SRU

ADC card V1.0

HDMI chip links
8x

Firmware:
Data processing
and buffering

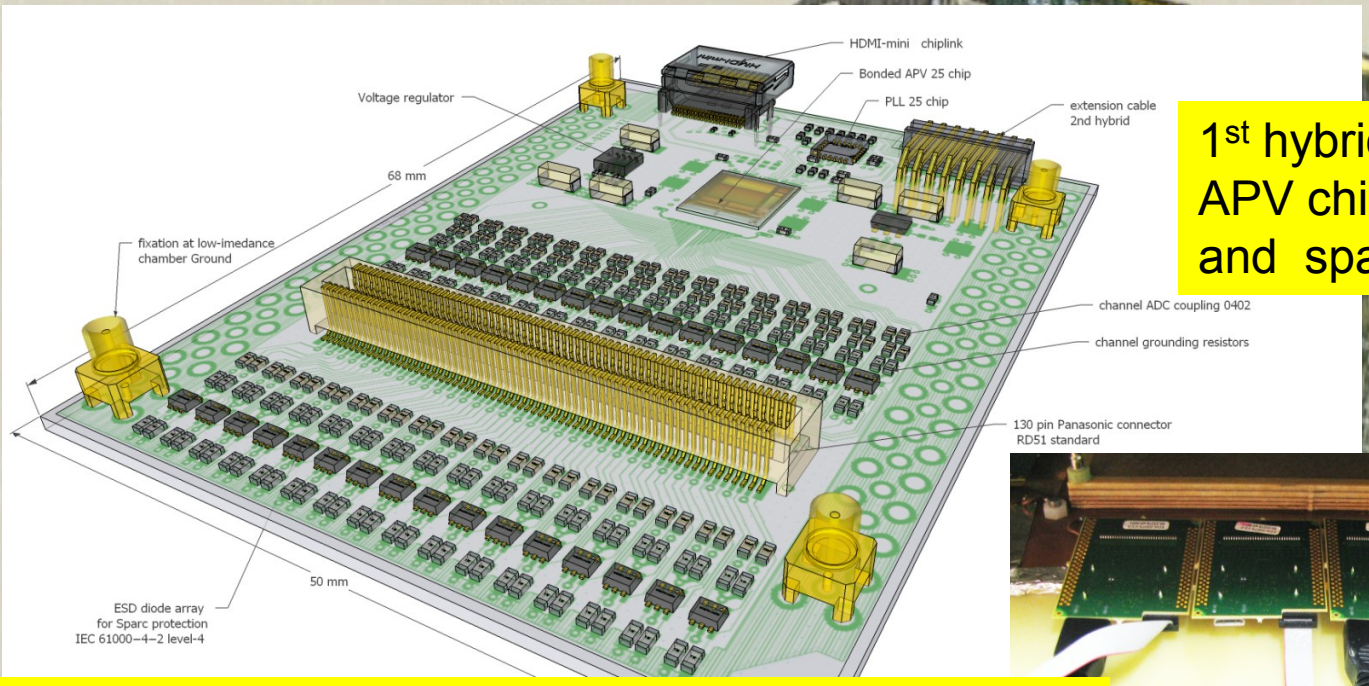
Octal ADCs
12 bit 40 MHz
(65 MHz in new version)

3 x PCIe connectors

Virtex 5 FPGA (Virtex 6 in new version)

SRS hybrid concept

-keep the backbone system
-exchange the ASIC hybrid on the detector



1st hybrid with 128 channel APV chip and HDMI readout and sparc protection

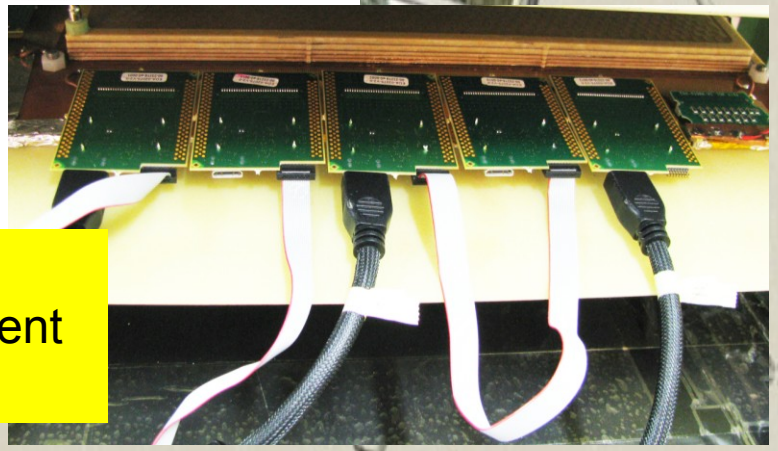


photo of APV hybrids on GEM chamber readout via HDMI cables

All SRS hybrids have a standard detector- and readout- interface. Individual hybrids have different readout ASICs

Hybrid APV25-S1 radhard, with Panasonic socket on hybrid: AXK5SA3277YG
Link interface HDMI-mini , hybrid power 3V3 500 mA max via HDMI cable
Extension interface for 2nd hybrid via Samtec FFSD-08-D-04.00-01-N cables (4.0 inch)
Protection diodes: NUP4114UPXV6T1G (15A clamp in1 ns, 1pF added capacity, reverse biased, quad package)
Lateral very low Impedance Ground & Clickin-fixation holes on hybrid for SAMTEC Jack MMXCX-P-P-H-ST-SM1
Readout chip: APV25-s1. 128 analogue channels. Wire bonded to hybrid in 2 layers.
Phase lock chip PLL25-LPCC radhard