Front End Electronics for the ATLAS Muon Phase 1 Upgrade

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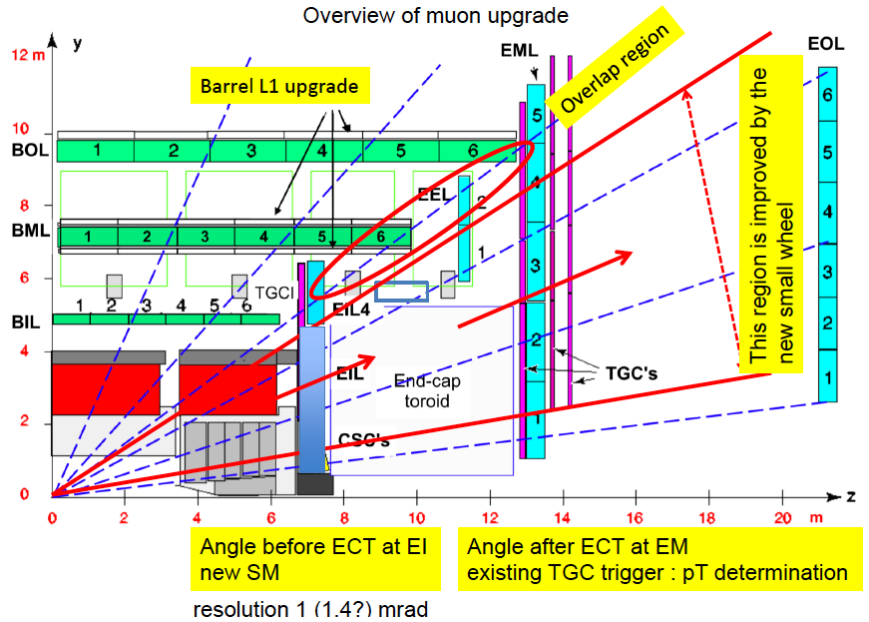
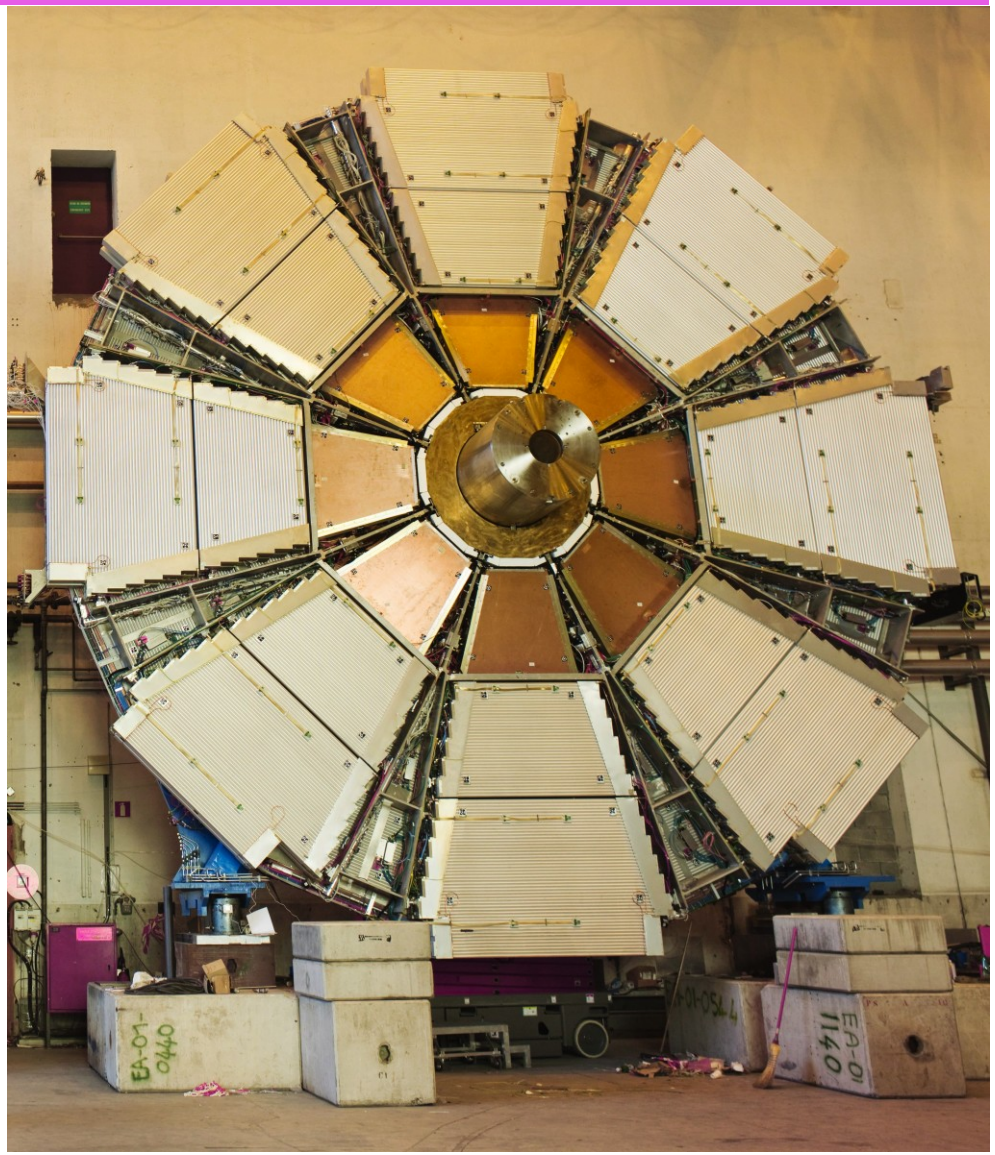
Replacement of the “Small Wheels”

- Diameter 9 m
- Currently Drift Tubes and Cathode Strip Chambers provide precision measurement
- If replaced with 8-layer Mmegas Detectors, would require ~1000 m2 of bulk detectors





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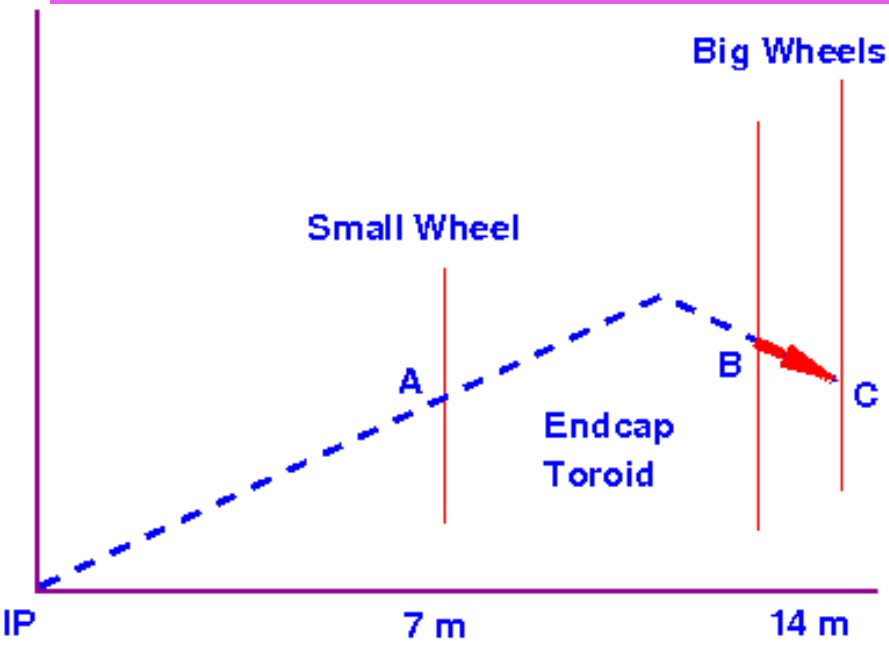
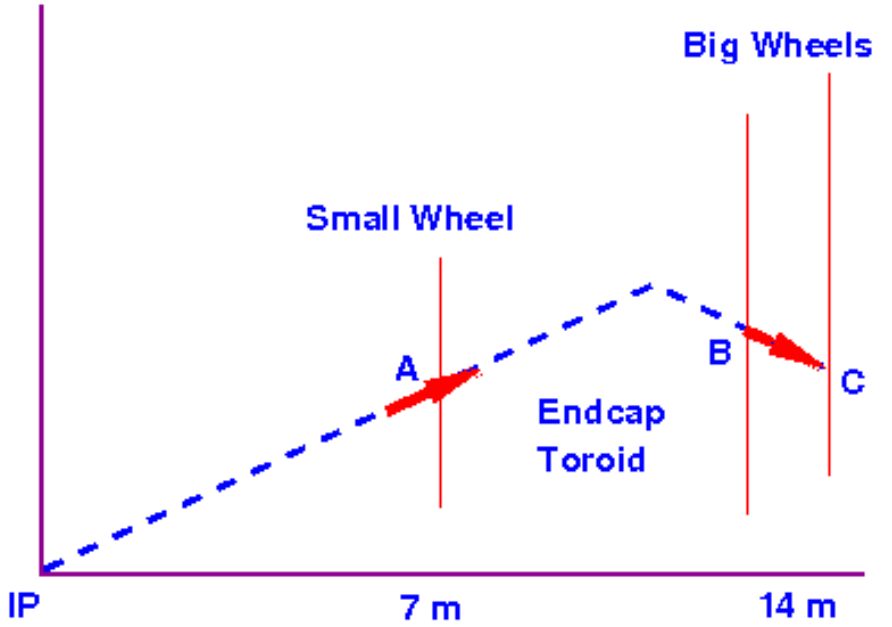
The Problem with High pT Triggers





Current Endcap Trigger

- Only a vector BC at the Big Wheels is measured
- Momentum defined by implicit assumption that track originated at IP
- Random background tracks can easily fake this

ProposedTrigger

- Provide vector A at Small Wheel
- Powerful constraint for real tracks
- With pointing resolution of 1 mrad it will also improve pT resolution
- Currently 96% of High pT triggers have no track associated with them

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Trigger Challenge to Electronics

- 1 mrad with a lever arm of ~0.5 m requires spatial resolution ~ 0.5 mm
- Trigger must be deadtimeless
- Pipeline @ 40 MHz
- Total time available 37 BC (includes 16 BC transit time to counting room)
- Must provide:
  - R
  - Φ
  - dθ

  R, ϕ are the coordinates and dθ the polar angle difference from an infinite momentum track.

Process/transmission	Time required (# of bunch-crossings)	Accumulated time
TOF to TGC	3	3
TGC response	1	4
ASD	1	5
Cable to Patch-Panel	1	6
Bunch-crossing ID and OR	2	8
Cable to Slave Board	1	9
Delay Adjust	1	10
3/4 or 2/3 coincidence	3	13
Cable to high-p_T coincidence	3	16
Delay adjustment	1	17
High-p_T coincidence matrix	4	21
Cable to USA15 (80m)	16	37
Sector Logic processing	8	45
Cable to MUCTPI (5m)	1	46
Total delay sum	46 BC	1.15 μs

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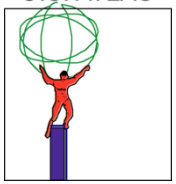

Two different approaches

- MicroMegas: Take advantage of fine (0.5 mm) granularity to achieve resolution with just the address of the hit
- TGC: Requires position calculation by charge interpolation in order to achiev required resolution with 3 mm elements

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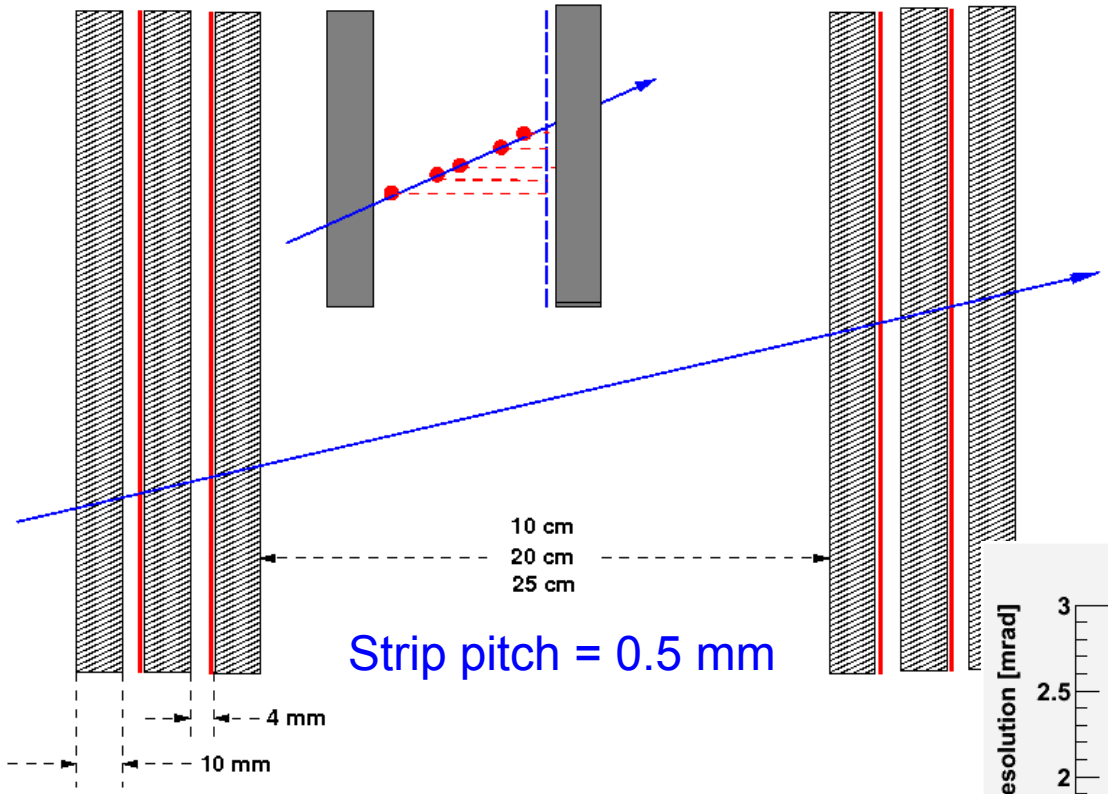
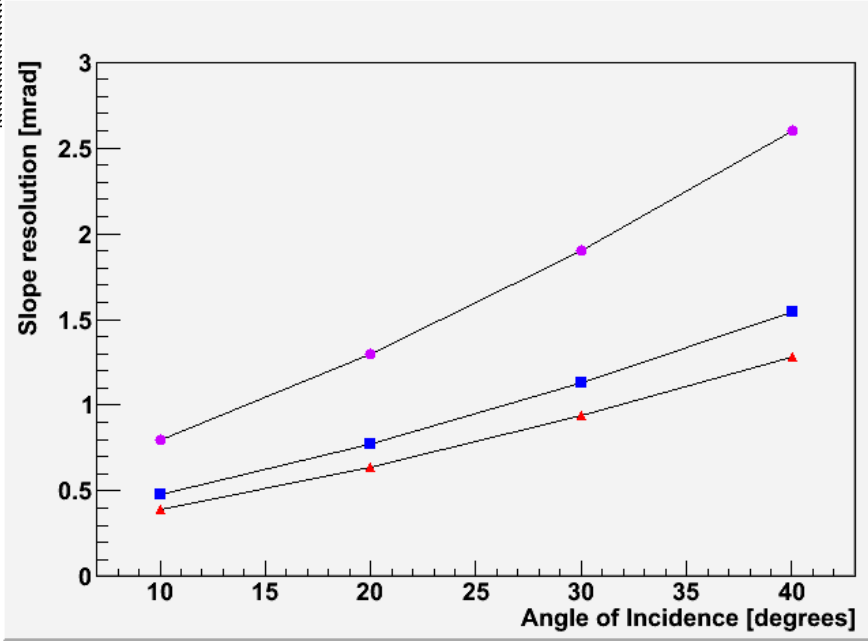
Micromegas Case

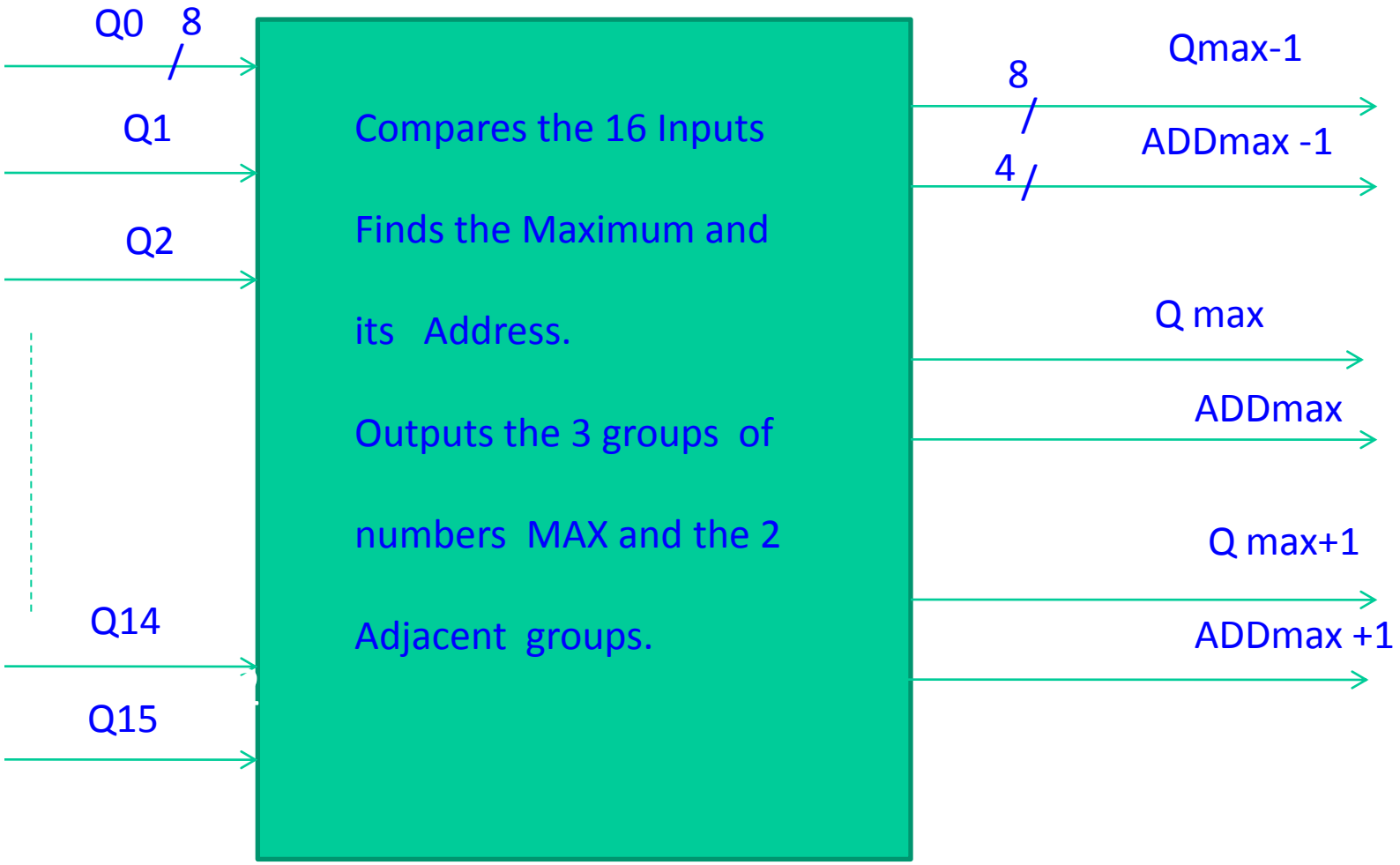


- Take strip with earliest time and charge over a certain threshold as the track's coordinate

Reconstruct track and calculate slope (done with lookup tables (content addressable memories)



TGC Trigger Strategy: COMPARATOR & SELECTOR to find the MAXIMUM CHARGE and its INDEX



Requires parallel output of all cha channels for further processing

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Electronics,for Phase 1 Muon Upgrade

- An effort was launched late last Summer do develop a system that:
  - Can be used by either mMegas or TGC detectors (most likely technologies)
  - Utilizes a peak detector and time stamp concept developed at BNL for several applications including a GEM-based TPC with similar signal processing requirements
  - This concept results in a data driven system with automatic zero supression
  - Simultaneous read/write with built-in Derandomizing Buffers
- Further design parameters
  - Able to provide Trigger Primitives for on-detector track segment finding logic
  - Built-in ADC

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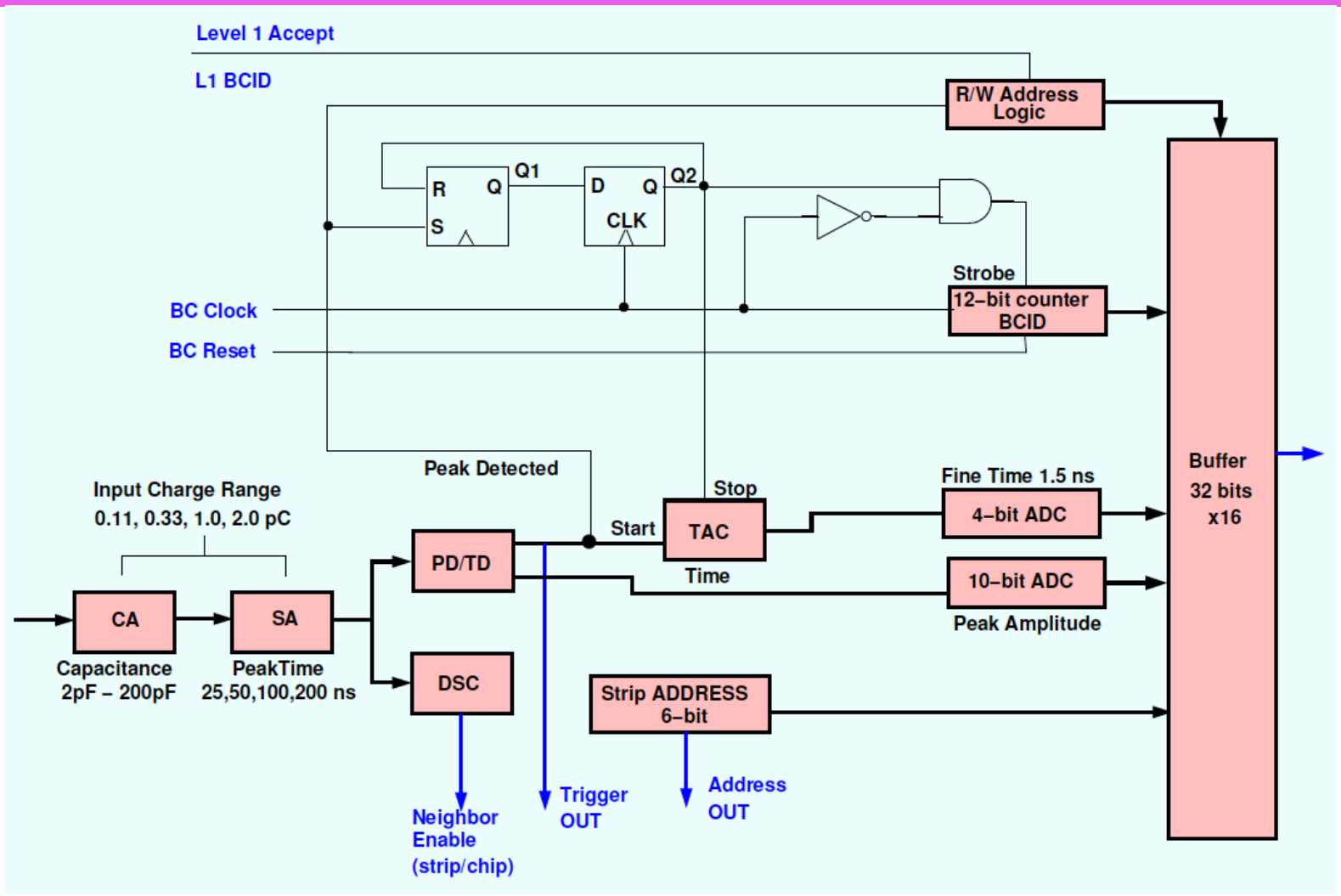
Block Diagram of the IC being designed



For TGC there will be fewer (16 or 32) channels with LVDS outputs of individual discriminators
All other features remain the same

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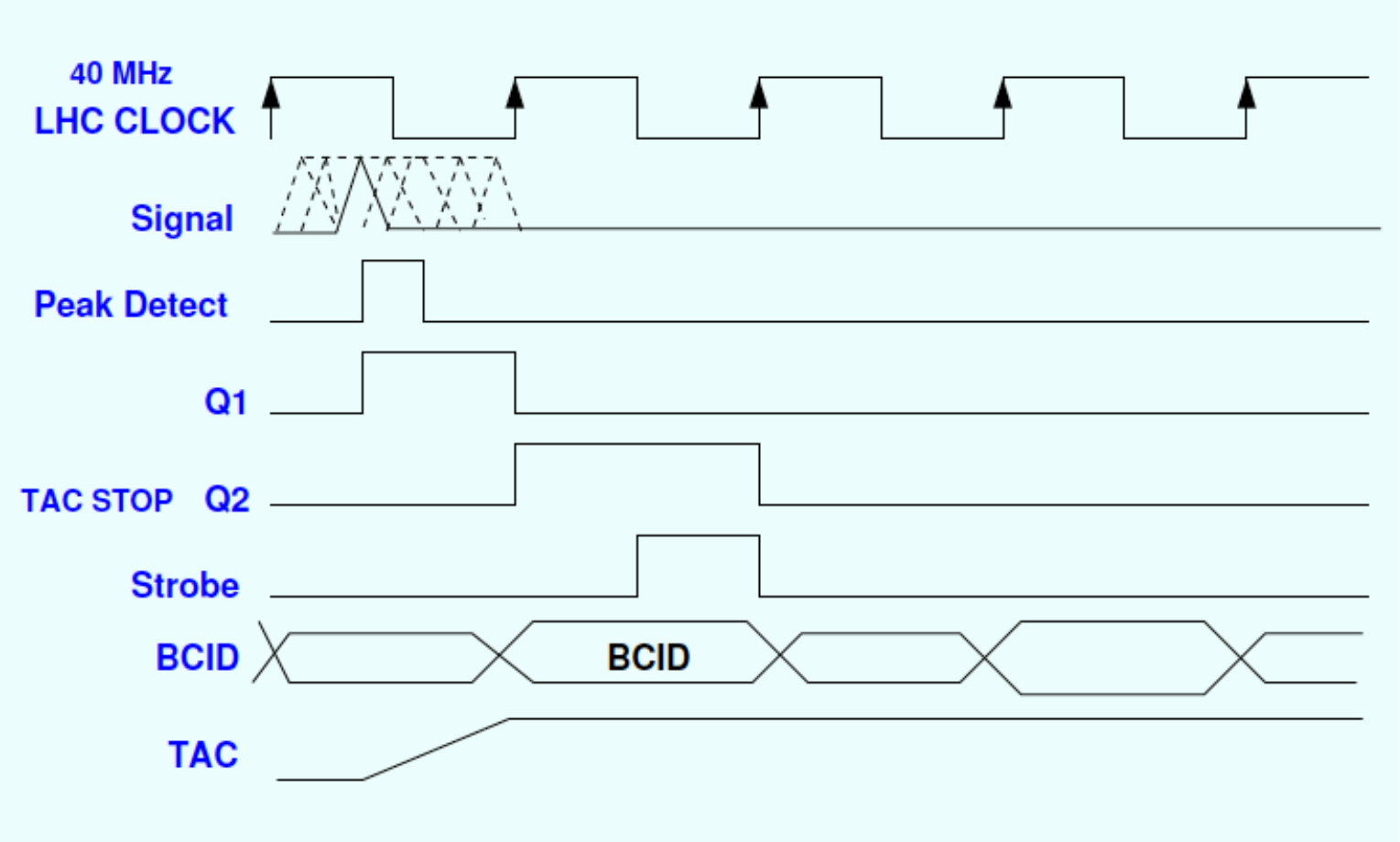
Timing Diagram



40 MHz BC clock convenient for LHC but any clock can be used to related hit with trigger accept

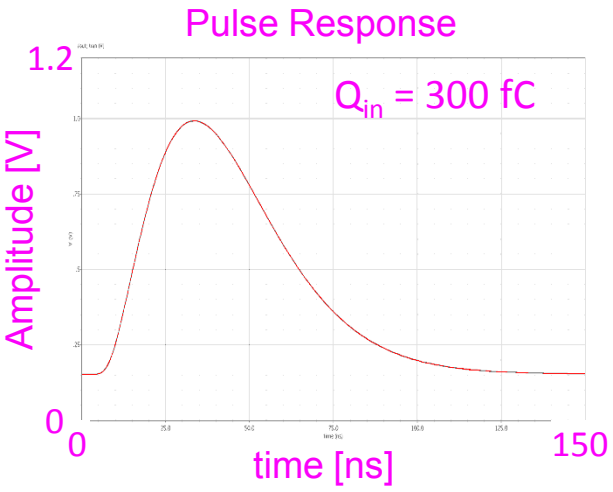
Additional features

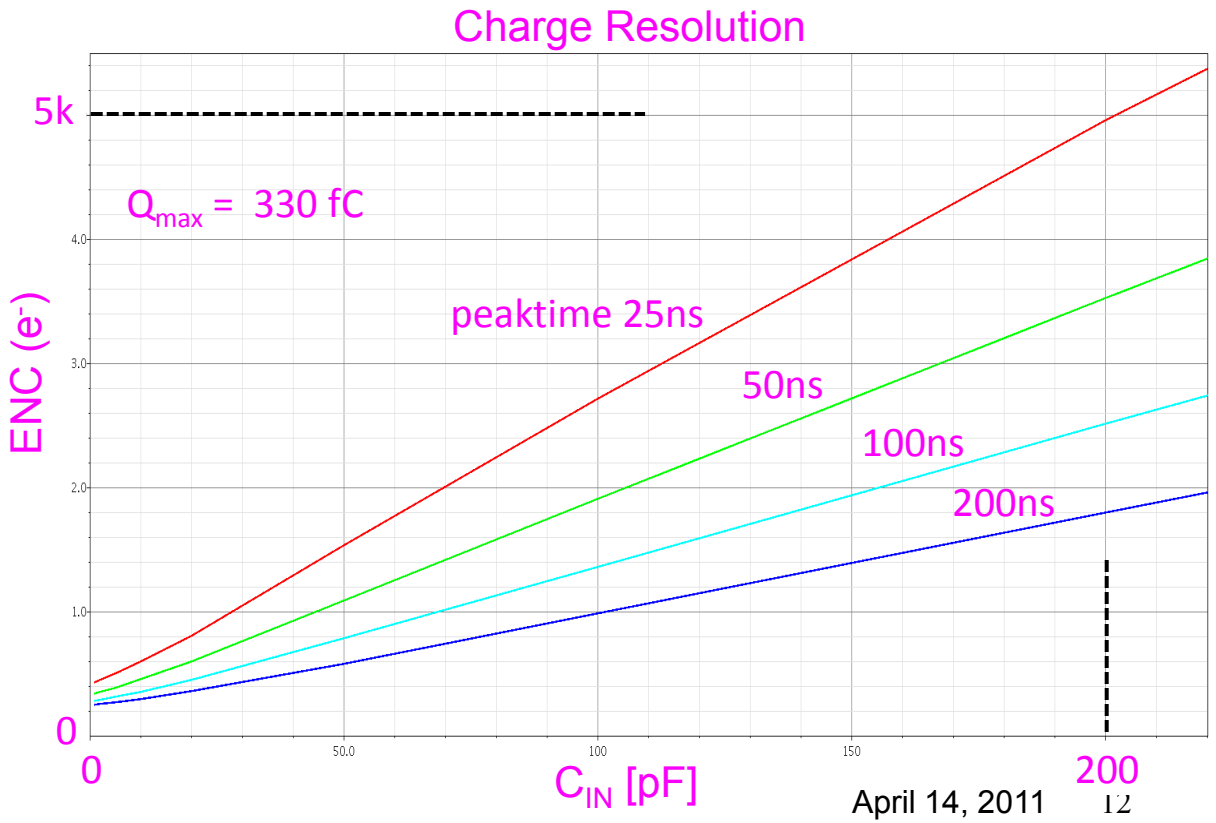
- 64 channels
- adj. polarity, adj. gain (0.11 to 2 pC), adj. peaking time (25-200 ns)
- derandomizing peak detection (10-bit) and time detection (1.5 ns)
- real-time event peak trigger and address
- integrated threshold with trimming, sub-threshold neighbor acquisition
- integrated pulse generator and calibration circuits
- analog monitor, channel mask, temperature sensor
- continuous measurement and readout, derandomizing FIFO
- few mW per channel, chip-to-chip (neighbor) communication, LVDS interface

VMM1 IC Schedule and Status

	status / notes
Analog section	**completed**
Peak/time detection	**in progress**
Common circuitry	**in progress**
Digital sections	
Physical layout	
Fabrication 1st prototype	CMOS 130nm, 1.2V, MPW, by Summer 2011

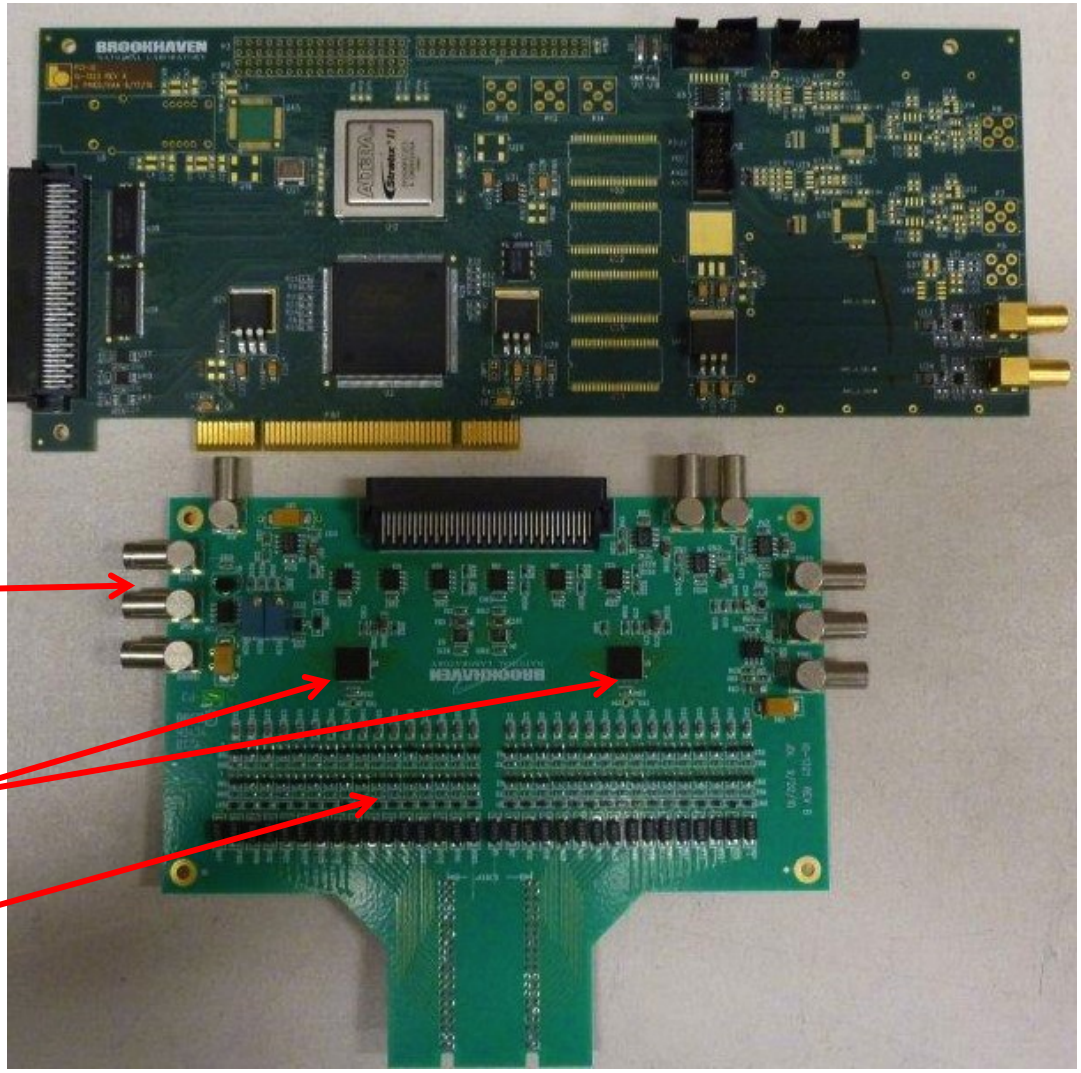
Analog section:
transistor-level simulations
power ≈ 4 mW



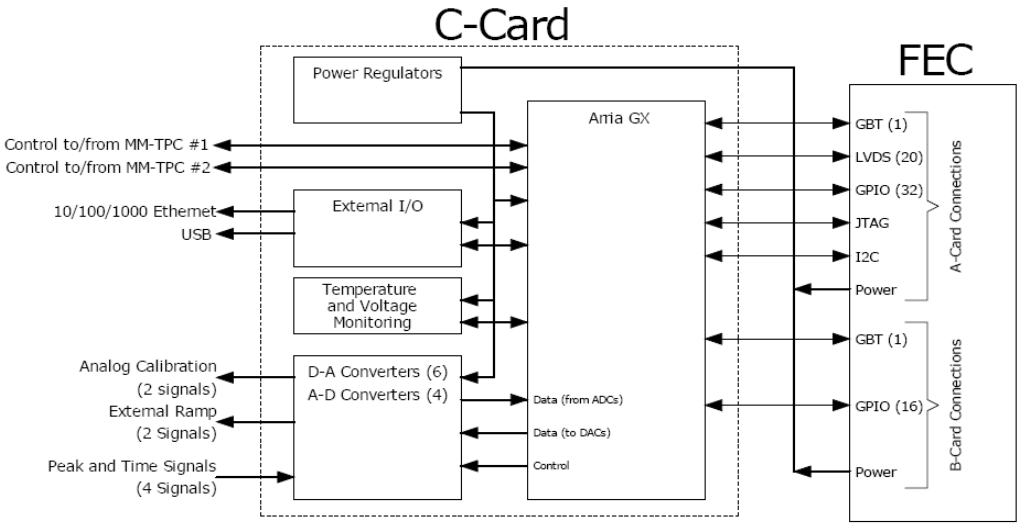


Test of the Concept with Existing, similar IC (developed for a GEM-based TPC)

PCI Readout Card
To be replaced with
SRS “C-Card”



Further Front End Card Development for prototype and future on-detector readout(U.Az)



- Integration of BNL ASICs into
  - Development of a "C-card" for
    - BNL "LEGS TPC" ASIC
    - BNL new "VMM1 " ASIC
- Development of "small format" front-end card for CSC size Micromegas
- Development of complete front-end system for CSC size Micromegas

Scalable Readout System
SRS
Common Readout System developed for use by the RD51 collaboration for beam tests at CERN but not only