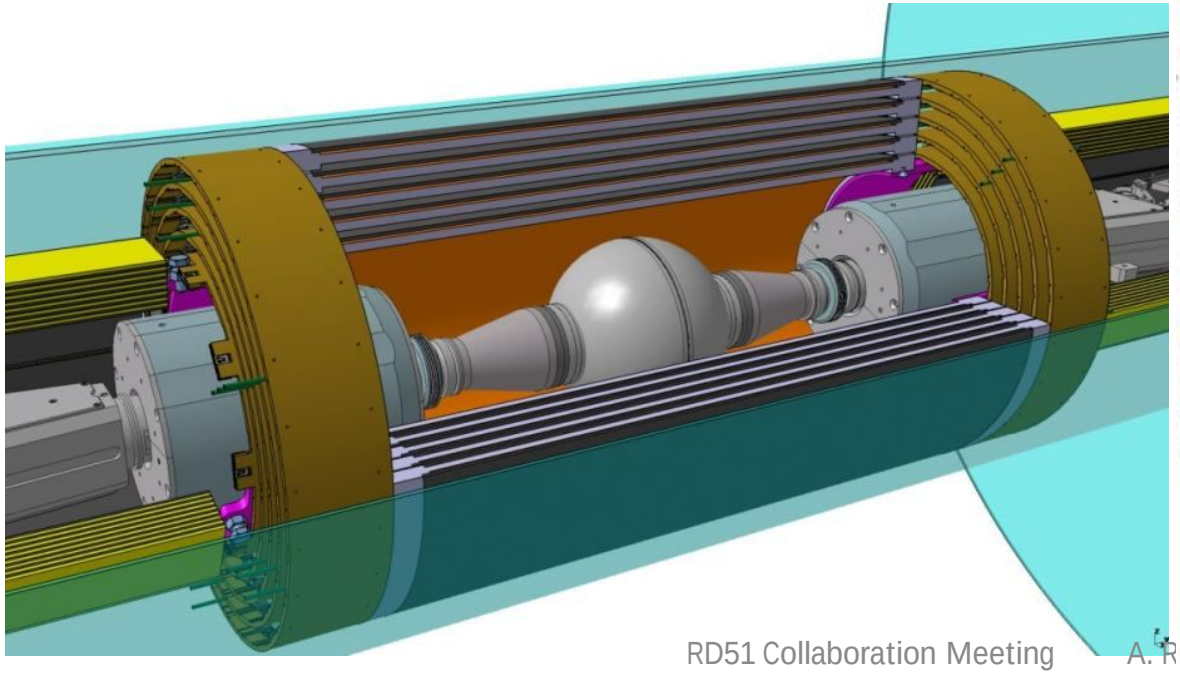
Time Domain Reflectometer project for KLOE2 IT

- The Inner Tracker detector of KLOE2
- The readout plane geometry
- The Time Domain Reflectometer project
  - results & prospects
- Conclusions

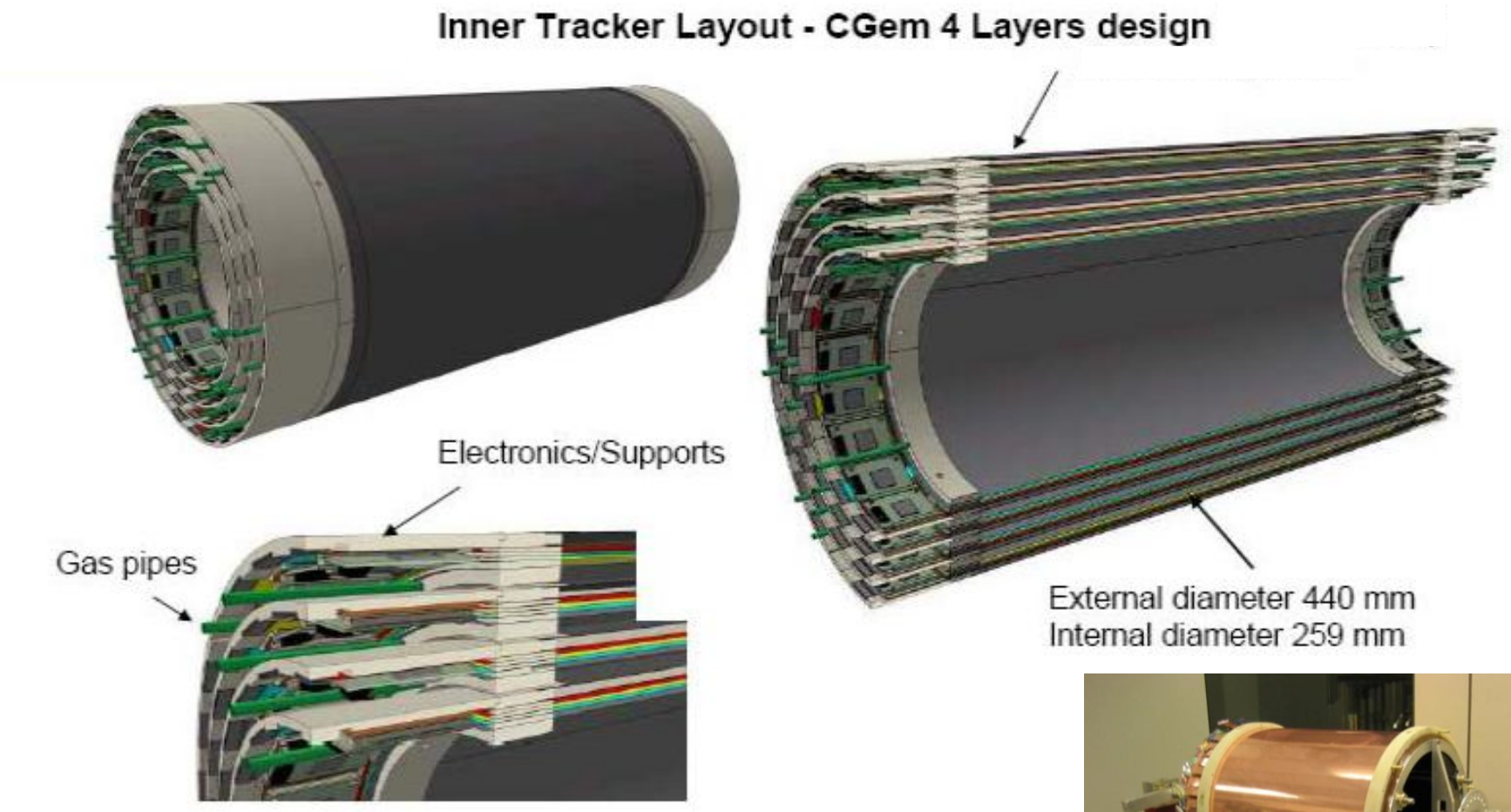
On behalf of IT KLOE2 Group

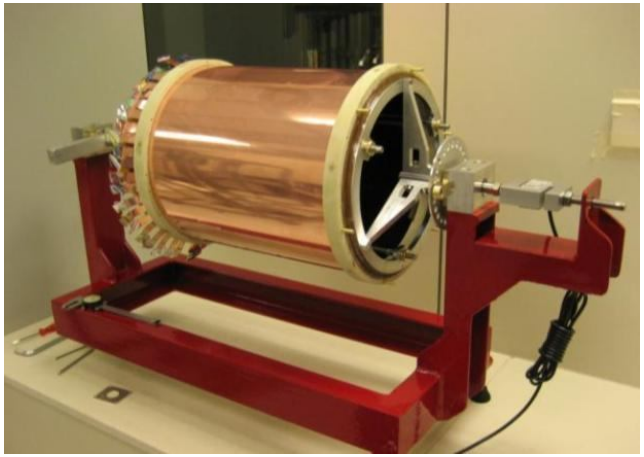
The cylindrical GEM IT detector for KLOE2 experiment @LNF

- Implemented with **Cylindrical-GEM** detectors
- 4 independent tracking layers for a fine vertex reconstruction of K_S and η
- 200 μm $\sigma_{r\phi}$ and 500 μm σ_Z spatial resolutions with XV readout
- 700 mm active length
- from 130 to 220 mm radii
- 1.8% X_0 total radiation length in the active region



The cylindrical GEM IT detector for KLOE2 experiment @LNF

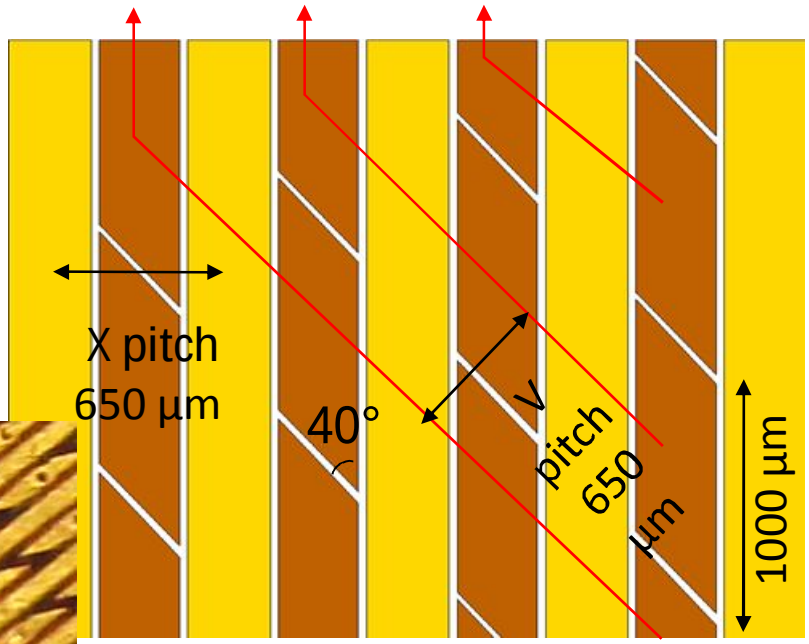


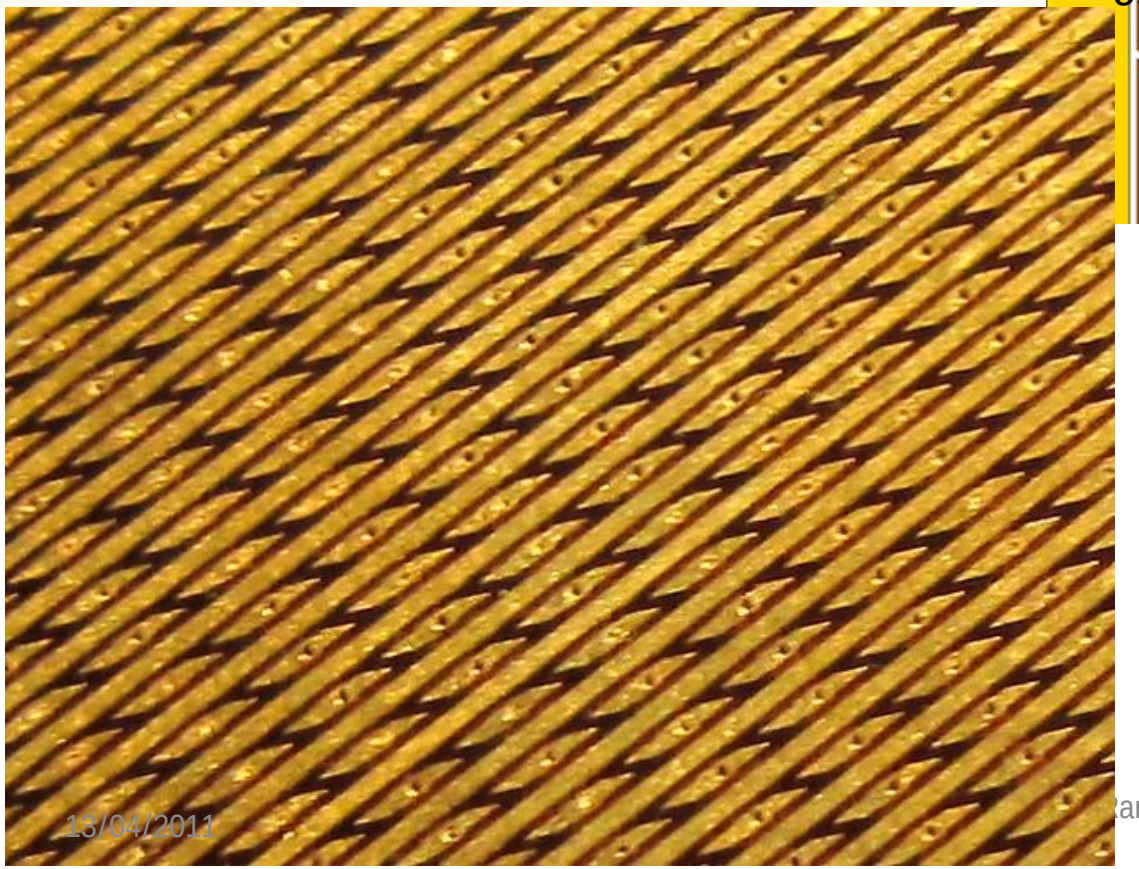


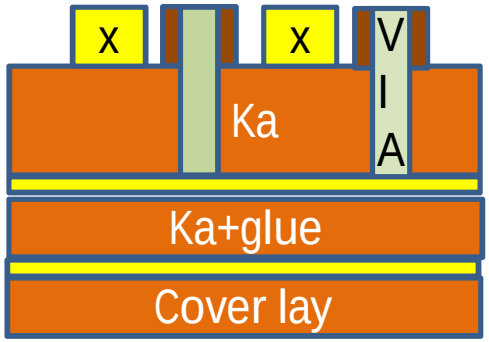
- 4 indipendent tracking layers [3 x (300 x 700 mm^2)]
- Total length: 944 mm

XV Readout

- Peculiar **XV readout** designed for the cylindrical geometry
- X Strips on a layer for rϕ coordinate
- V Strips at 40° formed by Pads connected by internal vias (~220.000 VIAs!)
- Crossing of X and V gives Z coordinate







IT: large area test beam @ CERN-PS

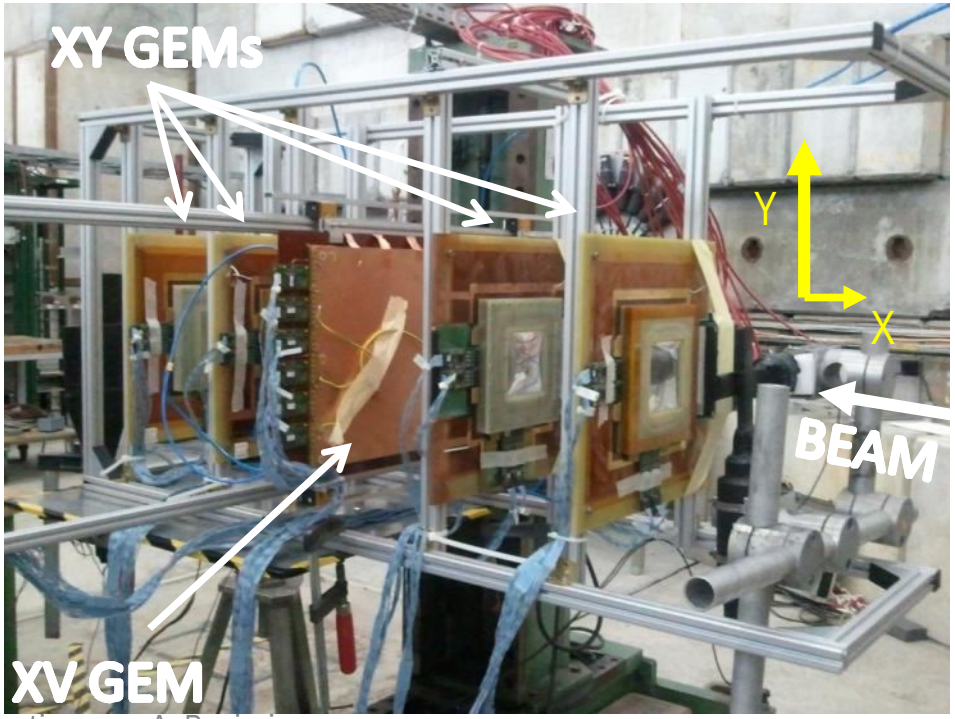
- May 2010: Large area planar prototype built
  First large-area GEM (300x700 mm^2)
- October 2010: at CERN-PS T9 beam-line with:
  - Final readout with XV pad-strip (220k vias)
  - GASTONE64 + Interface Board + General Intermediate Boards (GIB)+Software Interface

Gas: Ar/CO_2 = 70/30
Fields: 1.5-3.0-3.0-6.5 kV/cm
V_{GEM}: 395-385-375=1155V and
390-380-370 =1140V

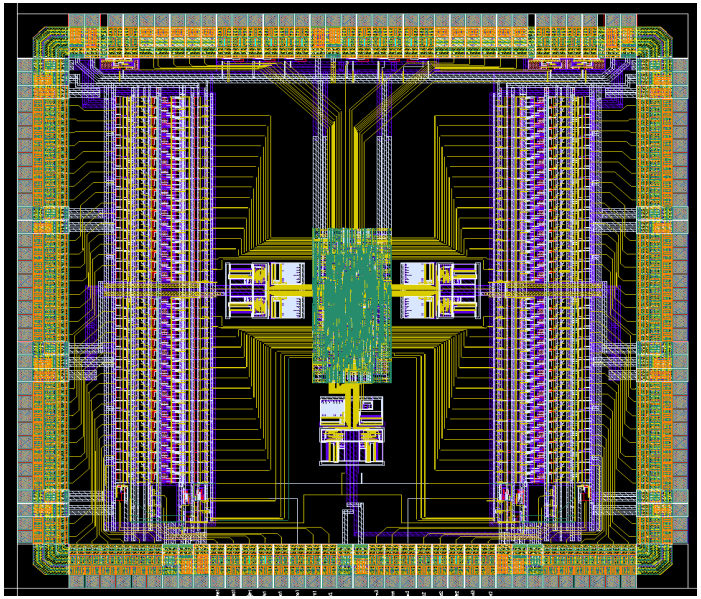
Trigger: 4 scintillators (2 upstream, 2 downstream)

External Trackers:

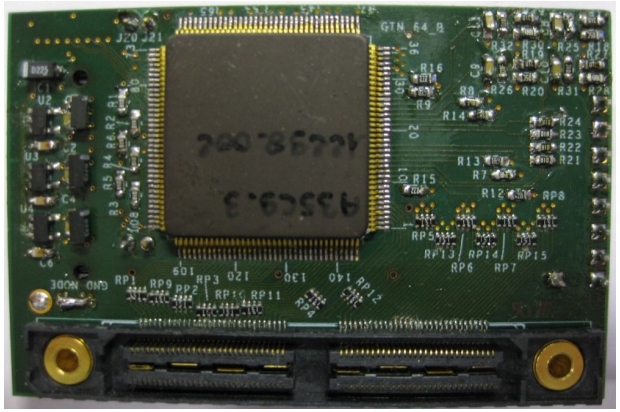
4 planar GEMs w/650 µm pitch XY strips



GASTONE64 FE readout for IT



Main features	
N. Channels	64
Chip dimensions	4.5x4.5 mm^2
Input impedance	400 Ω
Charge sensitivity	22 mV/fC (C_{det} = 0 pF)
Gain non-uniformity	< 6% (0 - 150 pF)
Noise (erms)	~ 800 e^- + 40 e^-/pF
Peaking time	80ns÷150 ns (C_{det} = 0÷100pF)
Power consumption	~ 7.5 mW/ch
Readout	Serial LVDS (100 Mbps)



- Final production (500 chips) already received
- Test Bench Board will be received in 2 weeks
- Production of FEB will start soon

Front-End Board dimensions (120 Channels): 62x40 mm^2

IT Read Out connectivity test

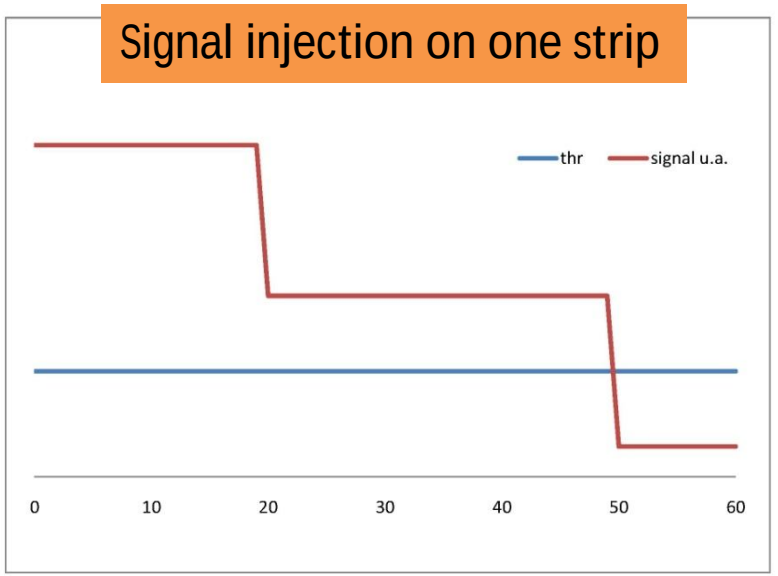
The Anode is shared out in a 2 dimensions layout having a XV geometry

X and V strips read out is shared out at both ends

Rotated by 40°, such strip's net provides 2D positioning for the particle passing through the layer.

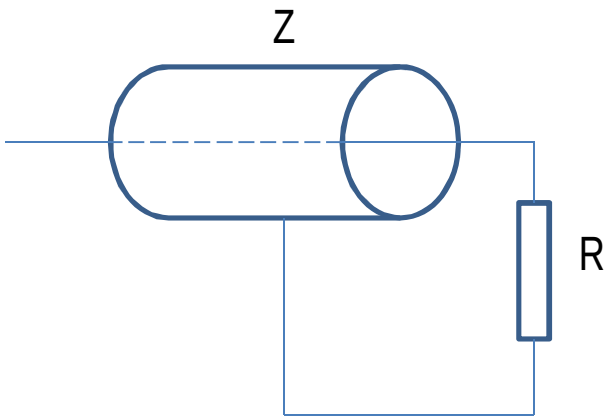
As strips have only one access we perform test on the reflected signal in order to verify circuit integrity for each strip.

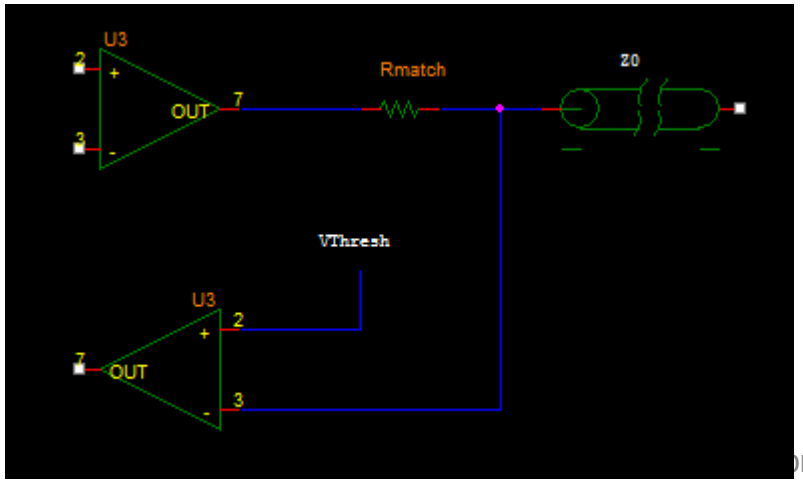
the drawing on the right shows the foreseen run of a signal injected into a open line.
You see the two edges, the first at the input while the second edge occurs when the signal comes back after been reflected by strip's end

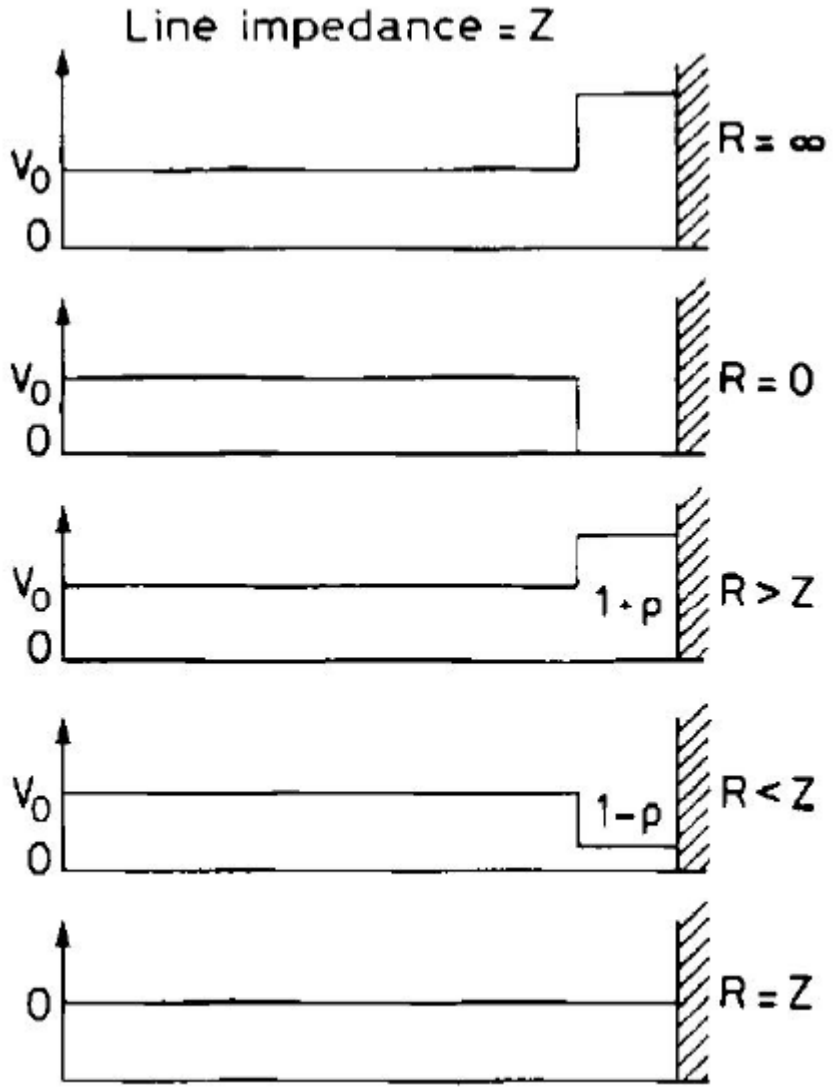


Transmission line and characteristic impedance

$$\rho = \frac{R - Z}{R + Z}$$







High resolution TDC system test design

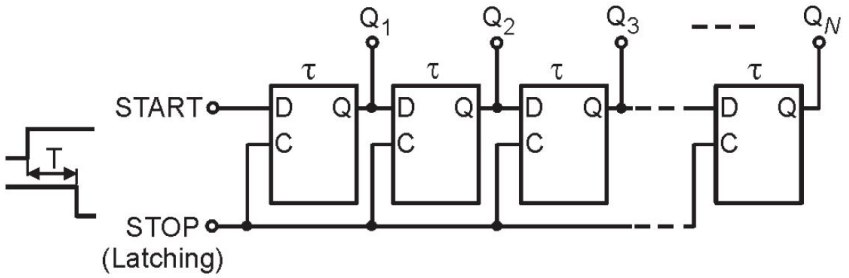
We have designed a circuit to check the strips integrity by measuring the timing of reflected signals.

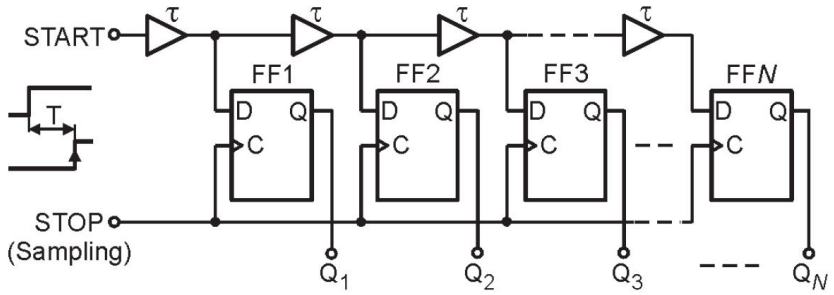
We have implemented a digital method based on a single FPGA (max clock @ 200MHz), based on:

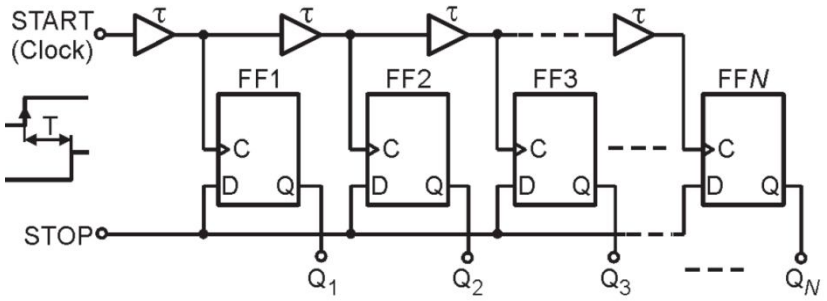
- A course counter with 4 ns resolution plus
- Time Digital Conversion by delay lines with a time resolution of ~100 ps

Very economic implementation based on one simple FPGA circuit (Xilinx XC3s400) only:
•versatile
•off-the-shelf component

Time Conversion by Delay Lines (basic idea)







HP5371A
Stephenson, 1989
→ Resolution 200 ps

0.8 µm CMOS
Gorbics et al., 1997
→ Resolution 46.9 ps

0.25 µm CMOS
Mota et al., 2000
→ Resolution 24.4 ps

0.6 µm CMOS
Mantyniemi et al., 2002
→ Resolution 29.6 ps

0.35 µm CMOS
Jansson et al., 2006
→ Resolution 12.5 ps

High resolution TDC system test design

The system has been designed:

1. To check lines connectivity (continuity)
2. To discover possible shorts

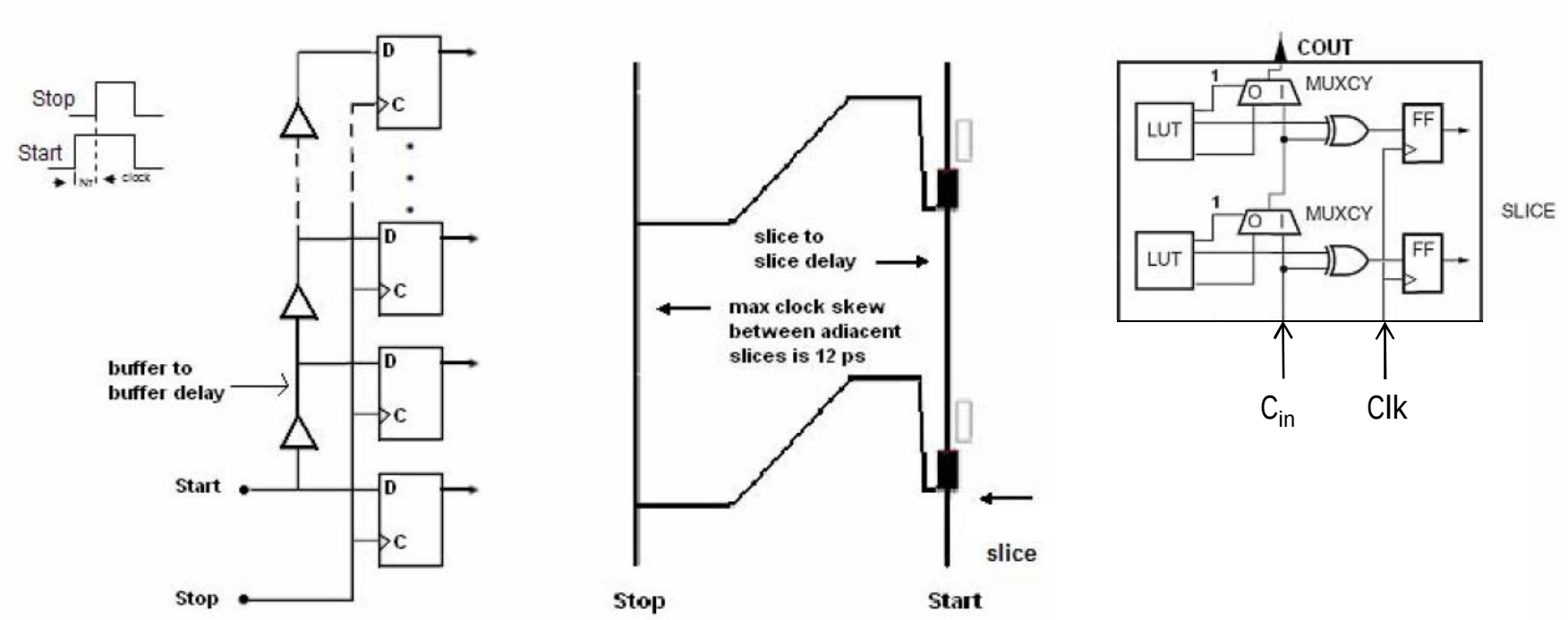
The system is based on a *delay chain* implemented inside FPGA-CLB measuring the propagation time of the reflected signal injected onto a microstrip.

The system features a delay line implemented inside one FPGA which contains :

- Analog interface towards strip
- Delay line and control logic for TDC
- Ethernet interface for data transmission
- A logic for short-circuit detection is also included

TDC lack of linearity in FPGA

A Lack of linearity in conversion is due to different positioning and routing of blocks in FPGA. Moreover there is a **skew** of the clock signal timing chain.

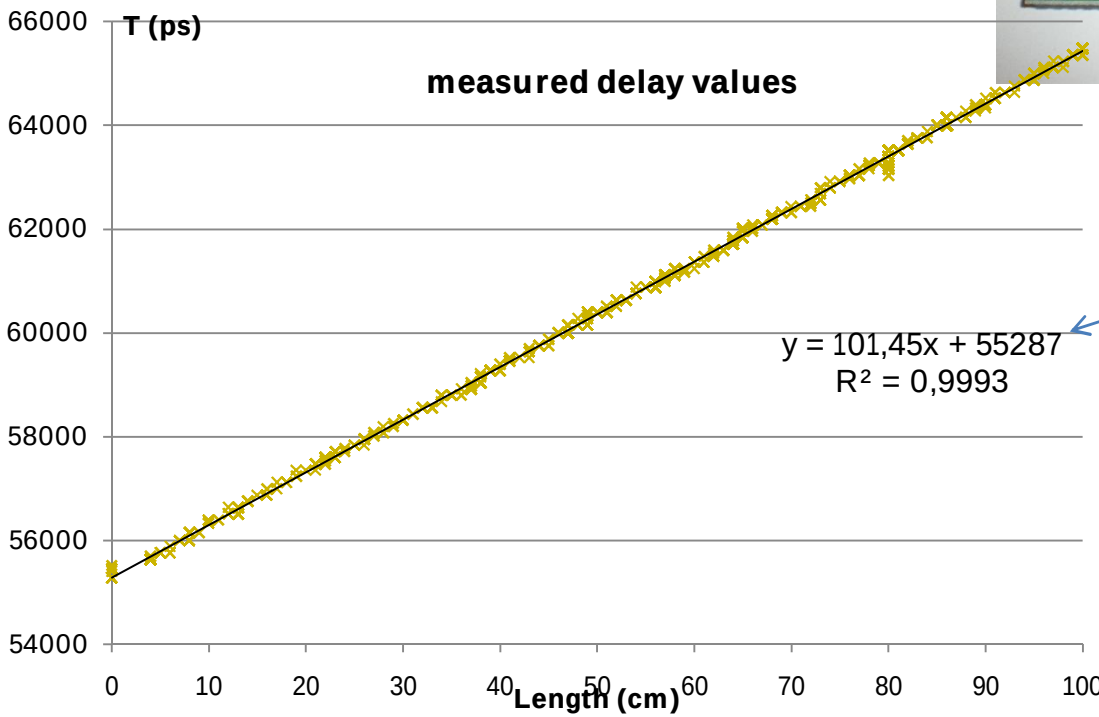


Propagation Time between input C_{IN} and output C_{OUT} of a slice ~ 120ps

Maximum skew of a clock signal within one "clock region" ~ 12ps

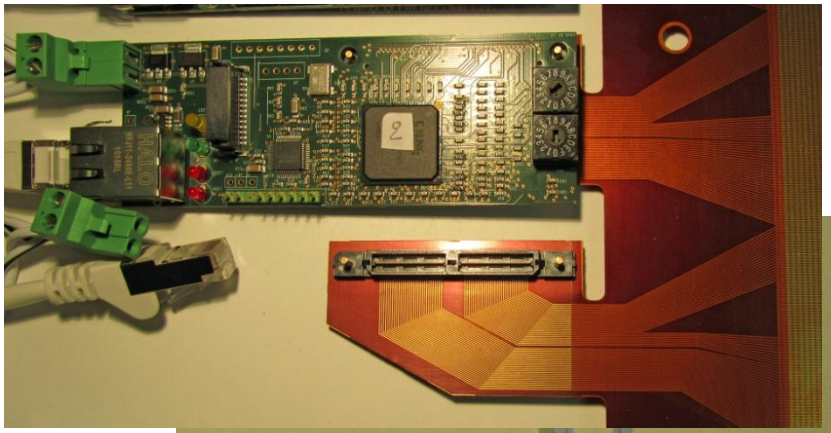
High resolution TDC : calibration tests

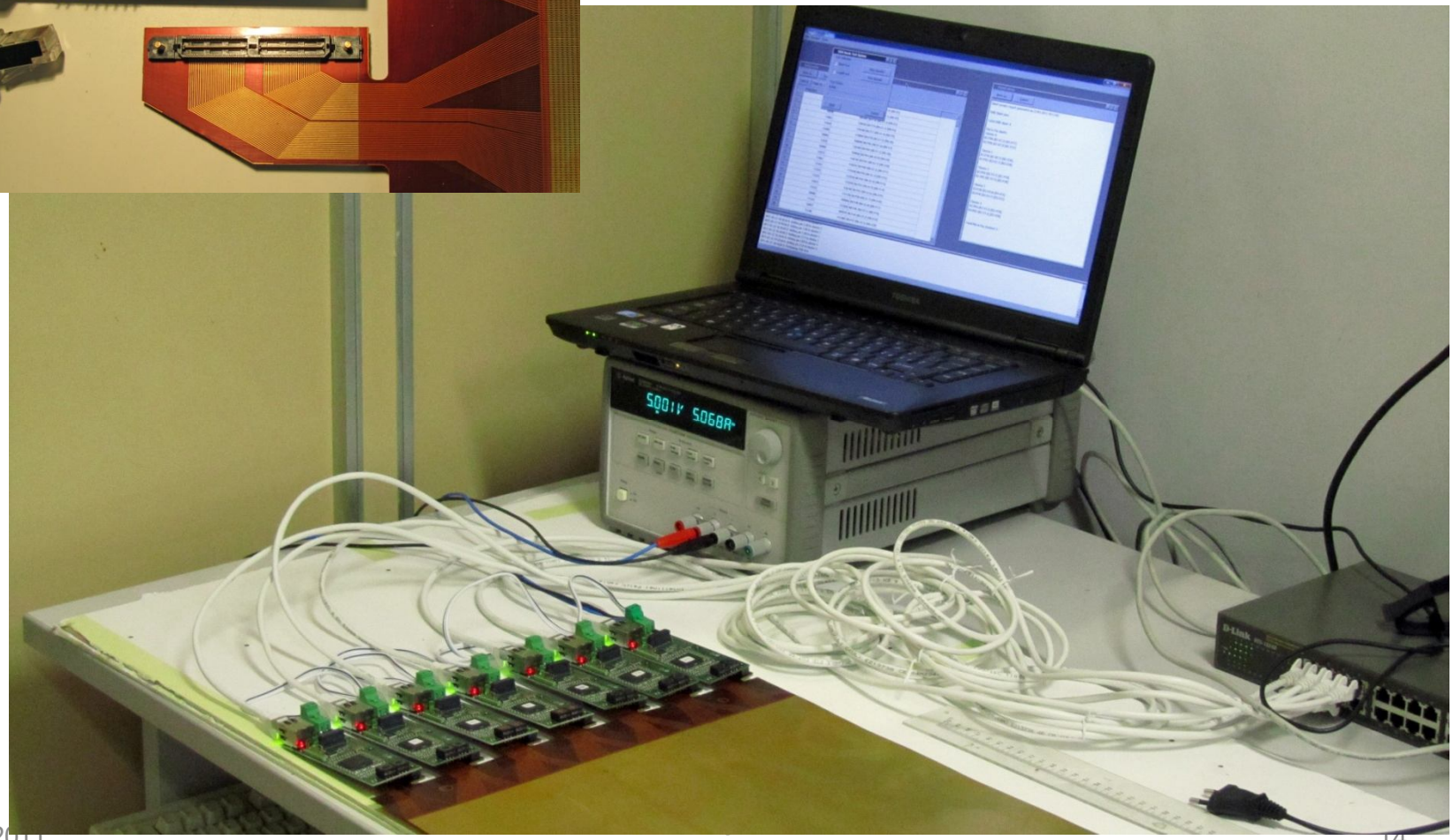
System sensitivity (fitted value) = 101.45 ps/cm



Latency introduced by pipelined encoding logic

Readout plane test system





Shorts report

Short circuits report generated on 21/03/2011 13:20:57

GND Short pins:
Total GND short: 0

Pin to Pin shorts:
Cluster 0
B2.P60 (B2.X2.2) [B2.X11]
B2.P58 (B2.X2.3) [B2.X12]

Cluster 1
B2.P10 (B2.X5.3) [B2.X36]
B3.P62 (B3.X2.1) [B3.X10]

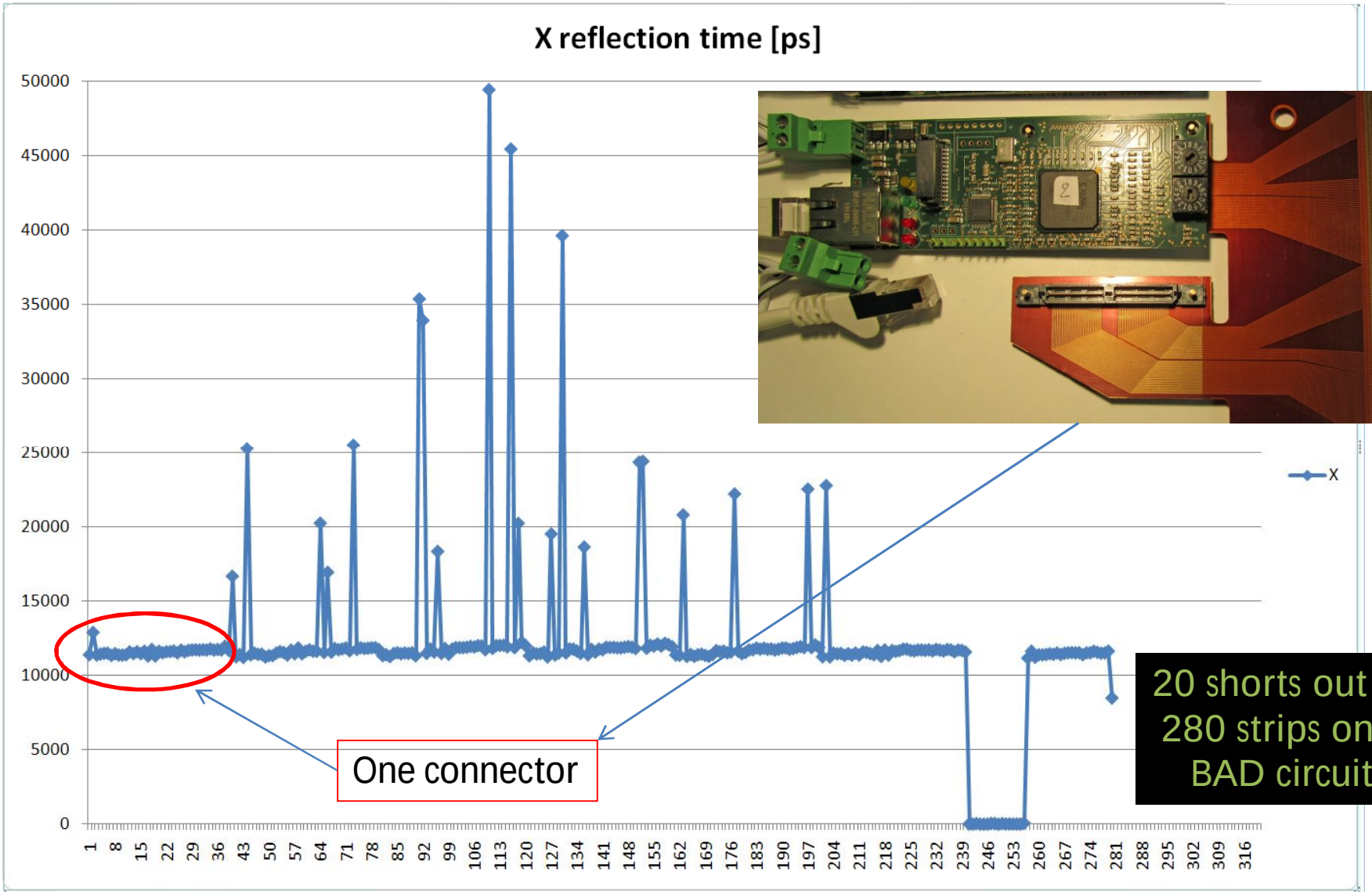
Cluster 2
B2.P84 (B2.V3.2) [B2.V19]
B2.P82 (B2.V3.3) [B2.V20]

Cluster 3
B3.P20 (B3.X4.6) [B3.X31]
B3.P18 (B3.X4.7) [B3.X32]

Cluster 4
B3.P84 (B3.V3.2) [B3.V19]
B3.P82 (B3.V3.3) [B3.V20]

Total Pin to Pin clusters: 5

Graphical log



Anodic plane defects discovered

System features summary

- 120 channels/board
- A few seconds for full test (shorts and lengths)
- System flexibility (impedance matching)

Conclusions

- A very reliable test system is available in Bari to test the readout plane of I.T. detector in KLOE apparatus
- Once the massive readout planes production will start we will be ready to test them in a while.