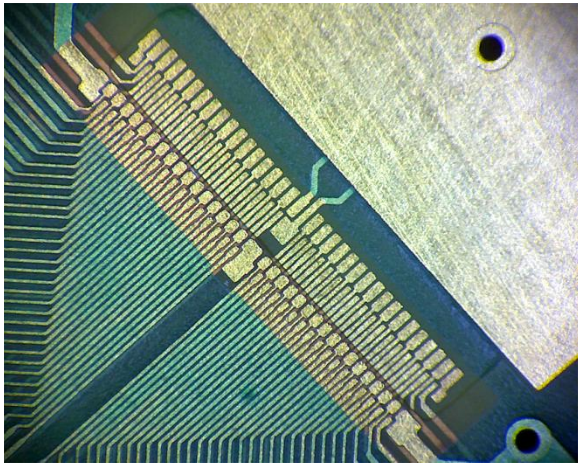
SRS Evolution
Hardware and Firmware

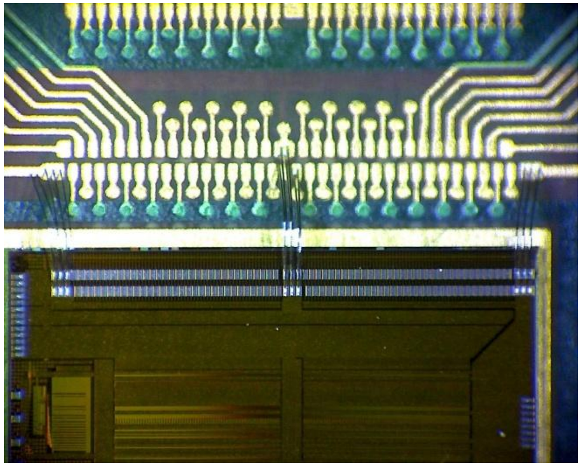
Sorin Martoiu, CERN

Overview

- Hardware Upgrades:
  - APV Hybrids v2 → v3
  - Multi-board SRS
- Firmware:
  - Slow-control over Ethernet
  - On-line zero-suppression under design
- Future work:
  - Beetle hybrid
  - Virtex 6 FEC
  - SRS GBT integration

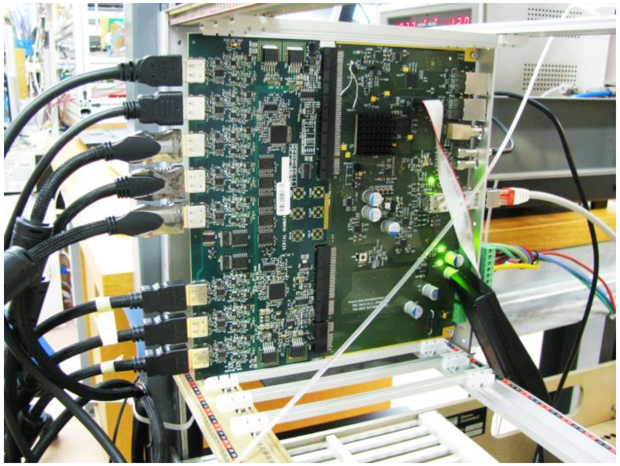
APV Hybrid v2 → v3

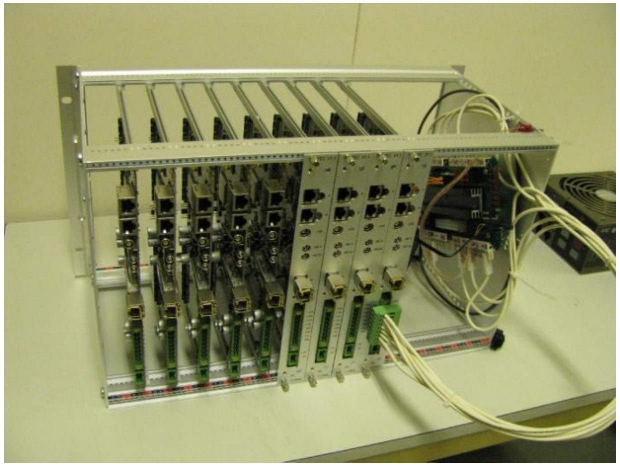




- Manufacturability issues
- Bonding cut-out replaced by microvias
- More relaxed clearances
- 300 PCBs produced in industry. On-going assembly

Multi-board SRS



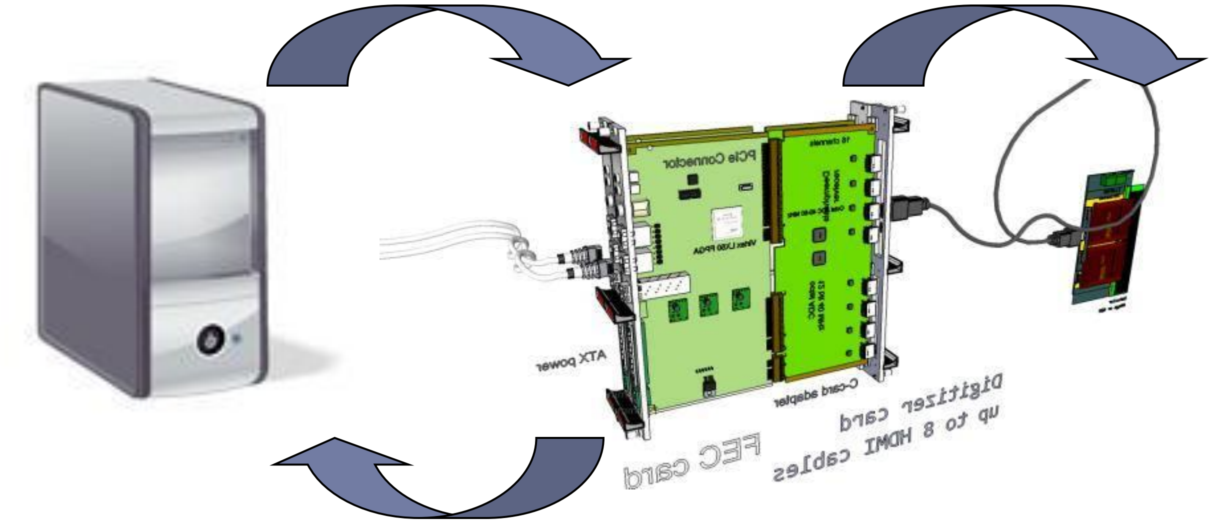


- All FEC boards are connected via a commercial Gigabit Ethernet Switch
- Old Chipscope-based slow-control had to be replaced by ethernet slowcontrol

SlowControl over Ethernet

SlowControl UDP/IP Request

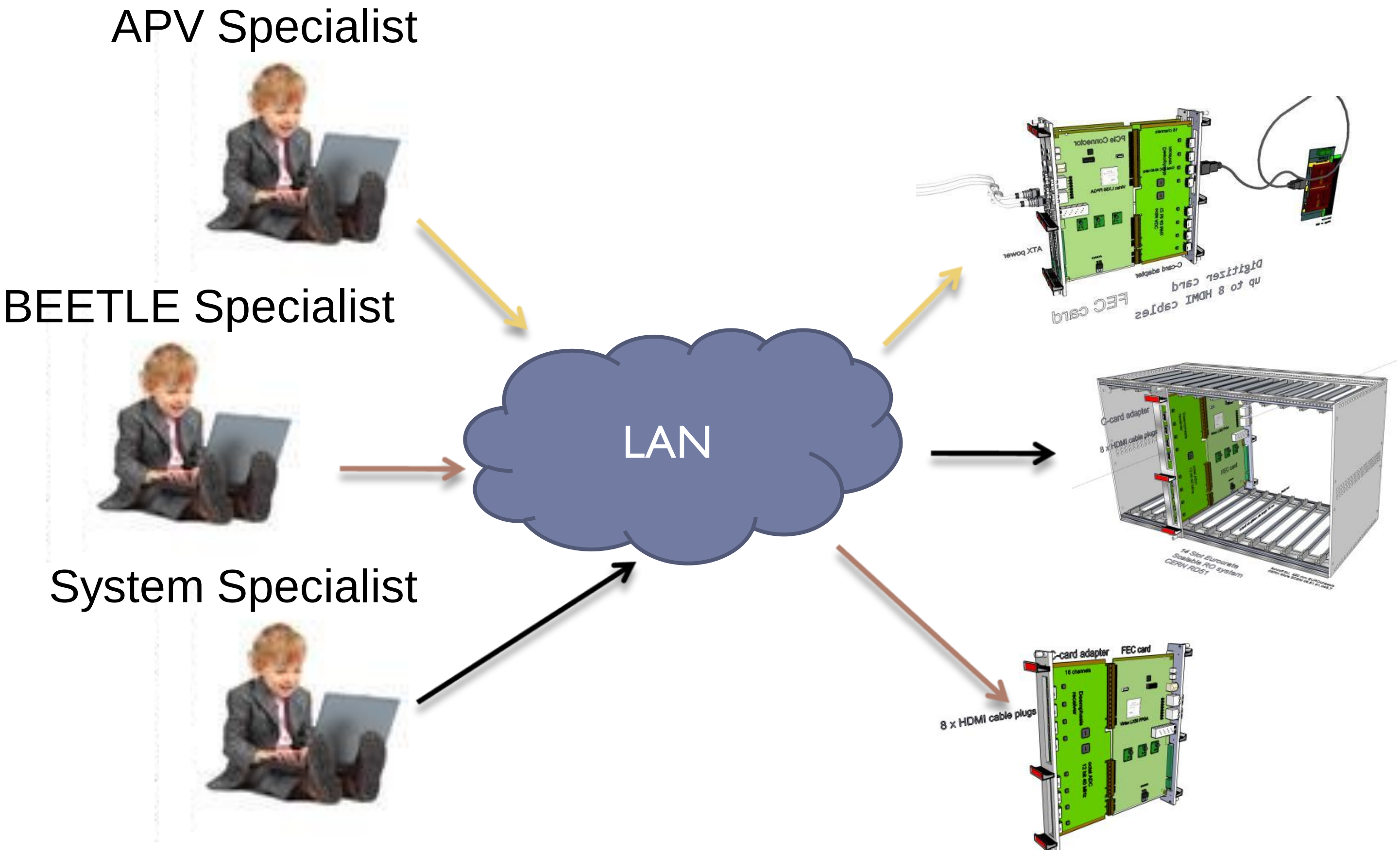
Data forwarded to peripherals



SlowControl UDP/IP Reply/Error

PC LAN FEC proprietary Peripherals

Slow-Control Scenario



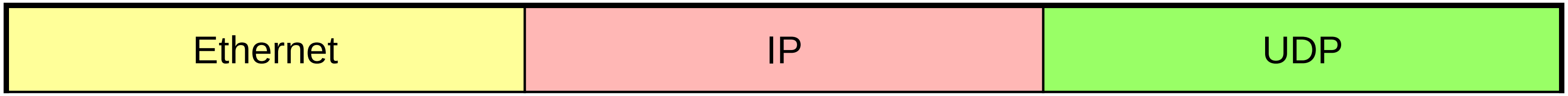
APV Specialist

BEETLE Specialist

System Specialist

LAN

Addressing

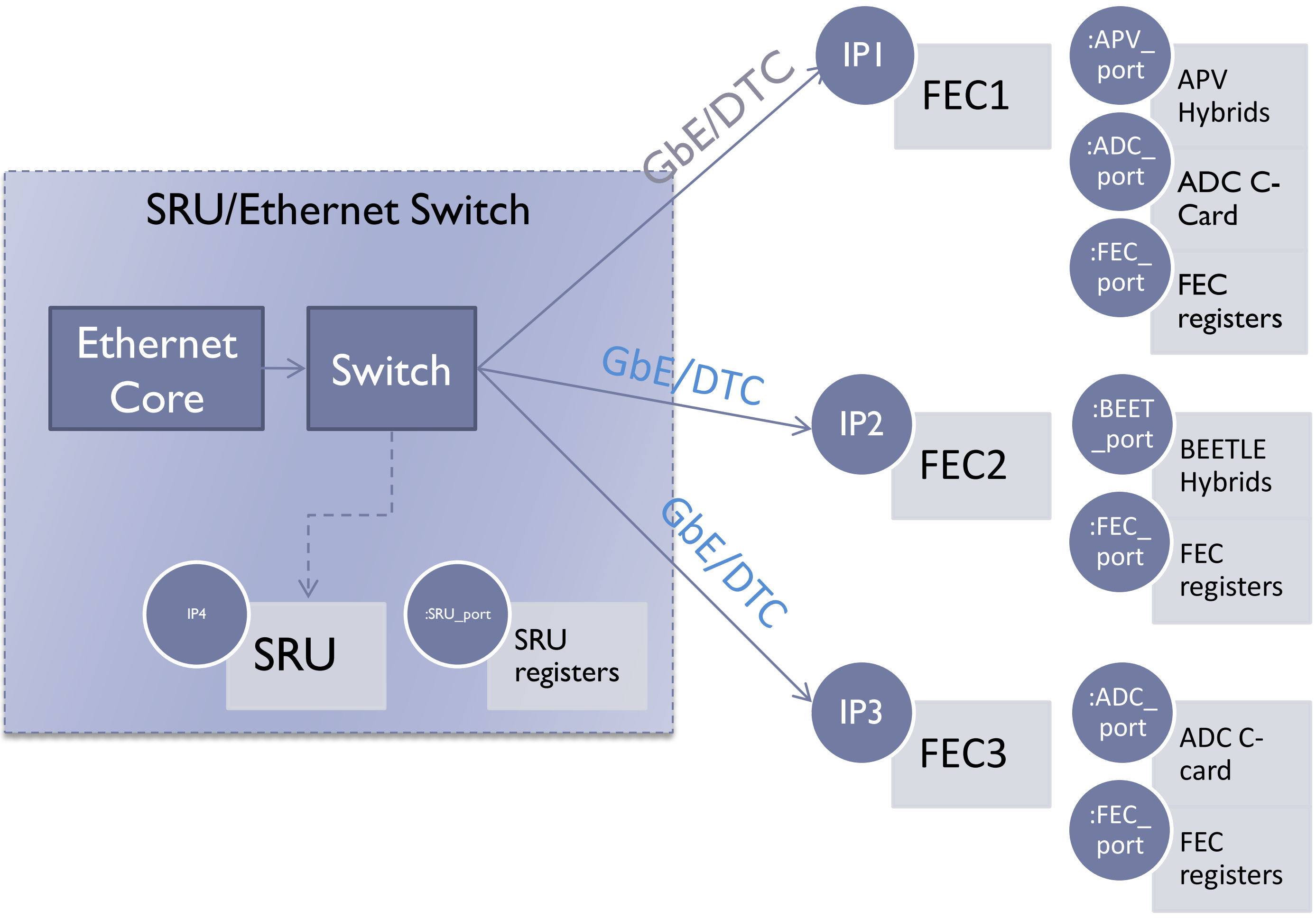


- Source MAC address
  - SlowControl PC
  - replies will go here
- Destination MAC address
  - Unicast: single FEC card
  - Broadcast: all FECs
  - Multicast: a set of FECs

- Source IP address
  - SlowControl PC
  - replies will go here
- Destination IP address
  - single FEC card
  - sub-networks can be defined for broadcast operations (eg. 10.0.0.255, 10.0.1.255)

- Destination Port
  - identifies the type of peripheral (APV_port, ADC_port, FEC_port, etc)
- UDP payload
  - request identifier
  - subaddress (eg. APV channel)
  - command (read, write, rst, etc.)
  - data (data to be written)

Addressing


SRU/Ethernet Switch
Ethernet Core
Switch
IP4
SRU
:SRU_port
SRU registers
GbE/DTC
GbE/DTC
GbE/DTC
IP1
FEC1
:APV_ port
APV Hybrids
:ADC_ port
ADC C-Card
:FEC_ port
FEC registers
IP2
FEC2
:BEET _port
BEETLE Hybrids
:FEC_ port
FEC registers
IP3
FEC3
:ADC_ port
ADC C-card
:FEC_ port
FEC registers

Mapping

- No global address space
- Each peripheral *type* has it's own address space starting from 0
  - Favors scalability (no need to enforce address boundaries for every new hybrid/module/etc.)
  - Provides generous address space for future devices (pixel chips, etc)
- Peripheral *type* identified uniquely by the port number (which should be hardcoded into software)
  - If the user tries to configure a peripheral which does not exists on a node, the operation does not corrupt the existing peripherals
- Protocol allows for flexible addressing of peripherals with multiplicity (eg. APV hybrids connected to the same FEC)
  - Subaddress field

Protocol

Request

<table>
<tr><th>31</th><th>0</th></tr>
<tr><td colspan="2">Request ID</td></tr>
<tr><td colspan="2">SubAddress</td></tr>
<tr><td colspan="2">Cmd Field 1</td></tr>
<tr><td colspan="2">Cmd Field 2</td></tr>
<tr><td colspan="2">Data</td></tr>
<tr><td colspan="2">….</td></tr>
<tr><td colspan="2">Data</td></tr>
</table>

Reply

<table>
<tr><th>31</th><th>0</th></tr>
<tr><td colspan="2">Request ID</td></tr>
<tr><td colspan="2">SubAddress</td></tr>
<tr><td colspan="2">Cmd Field 1</td></tr>
<tr><td colspan="2">Cmd Field 2</td></tr>
<tr><td colspan="2">Error</td></tr>
<tr><td colspan="2">Data</td></tr>
<tr><td colspan="2">…</td></tr>
<tr><td colspan="2">Error</td></tr>
<tr><td colspan="2">Data</td></tr>
</table>

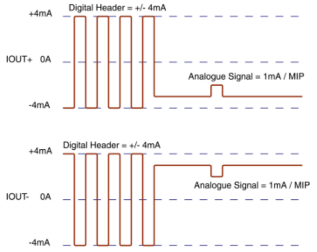
Error

<table>
<tr><th>31</th><th>0</th></tr>
<tr><td colspan="2">Request ID</td></tr>
<tr><td colspan="2">Error code</td></tr>
</table>

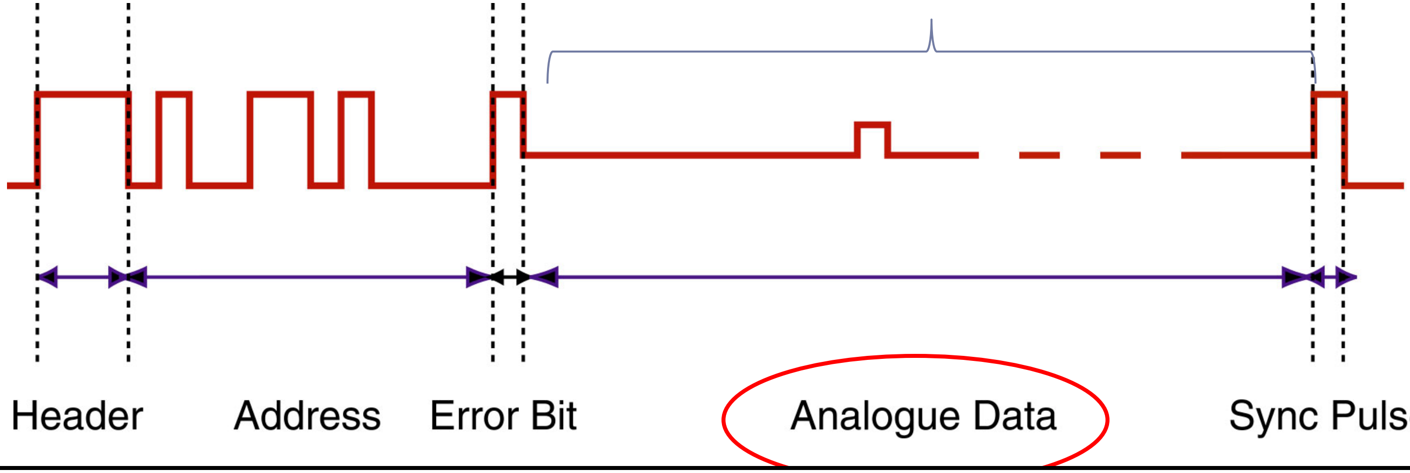
On-line Zero-Supression

- Firmware development started by Raffaele Giordano in Napoli
- First modules were recently tested on real system and data
  - Data synchronization
  - Clock synchronization
- Modules under design
  - Pedestal subtraction
  - Common-mode rejection

APV analogue data stream

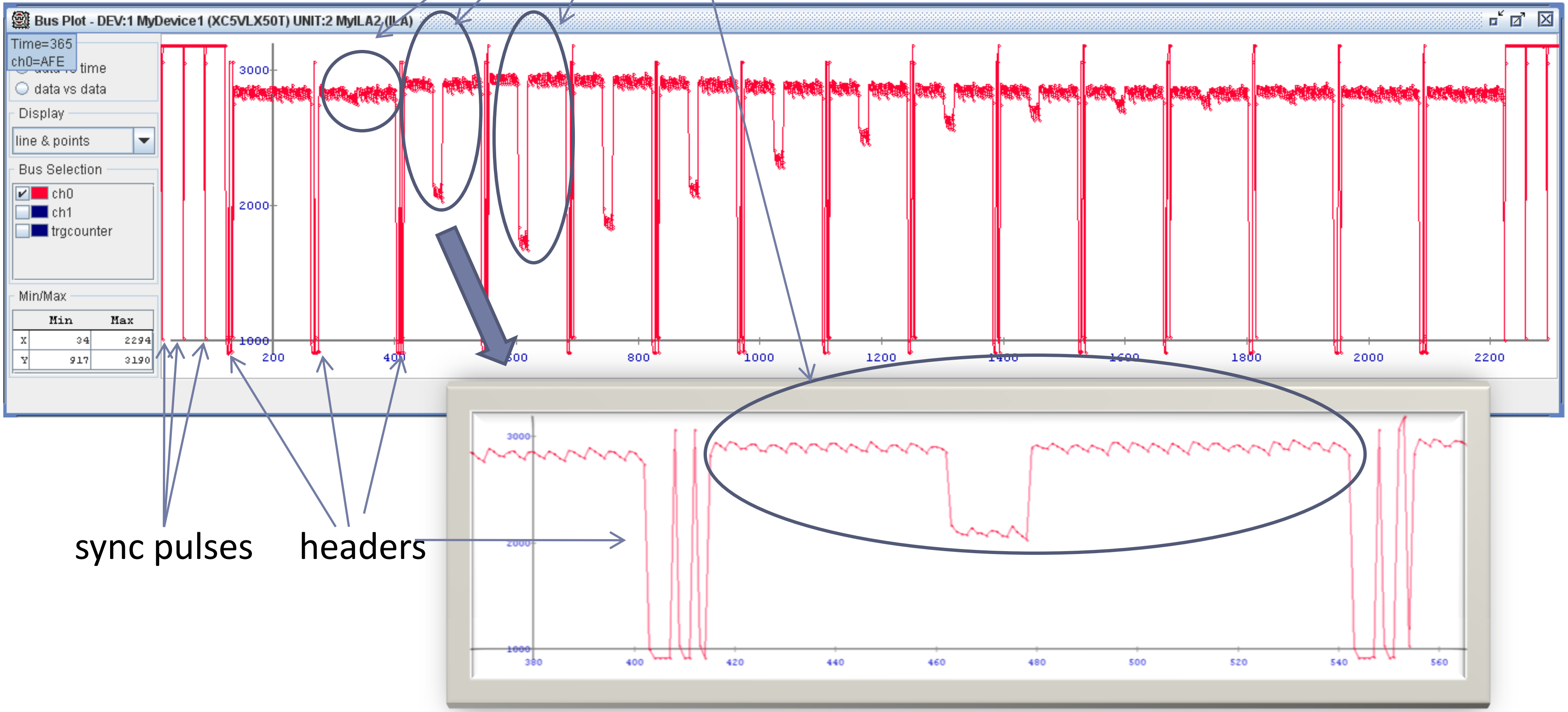


- one time sample
- 128 channels



The output from the APV25-S1 chip is in differential current form in the range +/- 4mA. When there is no data to read out, the output of the chip is at the logic 0 level, with synchronization pulses every 70 clock cycles (in 20 MHz mode) or 35 clock cycles (in 40Mhz mode). When an event is triggered, the chip waits until the start of the next (70 or 35) clock cycle period before any data is output. A data set is then made up of four parts: a digital header, a digital address, an error bit, and an analogue data

Acquired APV data stream



Analogue data (128 channel samples)

sync pulses

headers

Bus Plot - DEV:1 MyDevice1 (XC5VLX50T) UNIT:2 MyILA2 (ILA)

Time=365
ch0=AFE

○ data vs time
○ data vs data

Display: line & points

Bus Selection

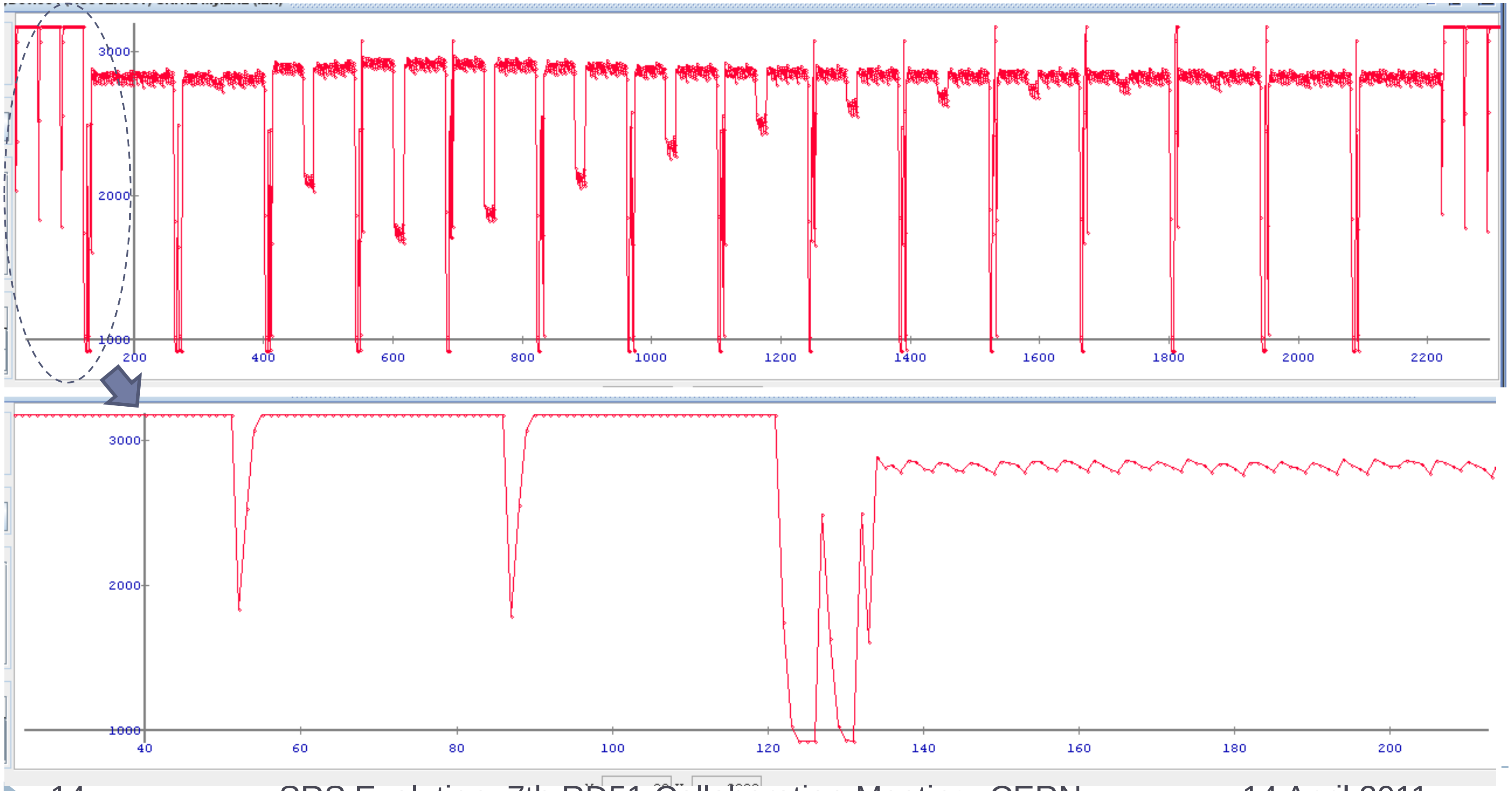
☑ 🟥 ch0
□ ch1
□ trgcounter

Min/Max

	Min	Max
X	34	2294
Y	917	3190

Clock synchronization

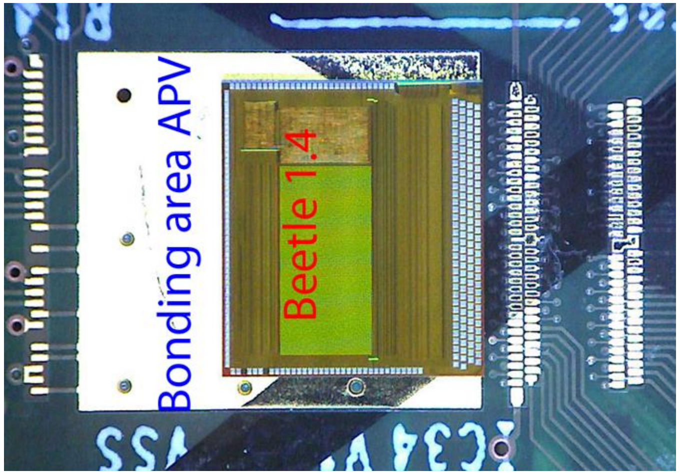
- Wrong clock-edge sampling; resync using the on-hybrid PLL25 chip



Future Work

- BEETLE Hybrid
- Virtex 6 FEC card
- Rad-hard optical FE interface (GBT Project)

BEETLE Hybrid

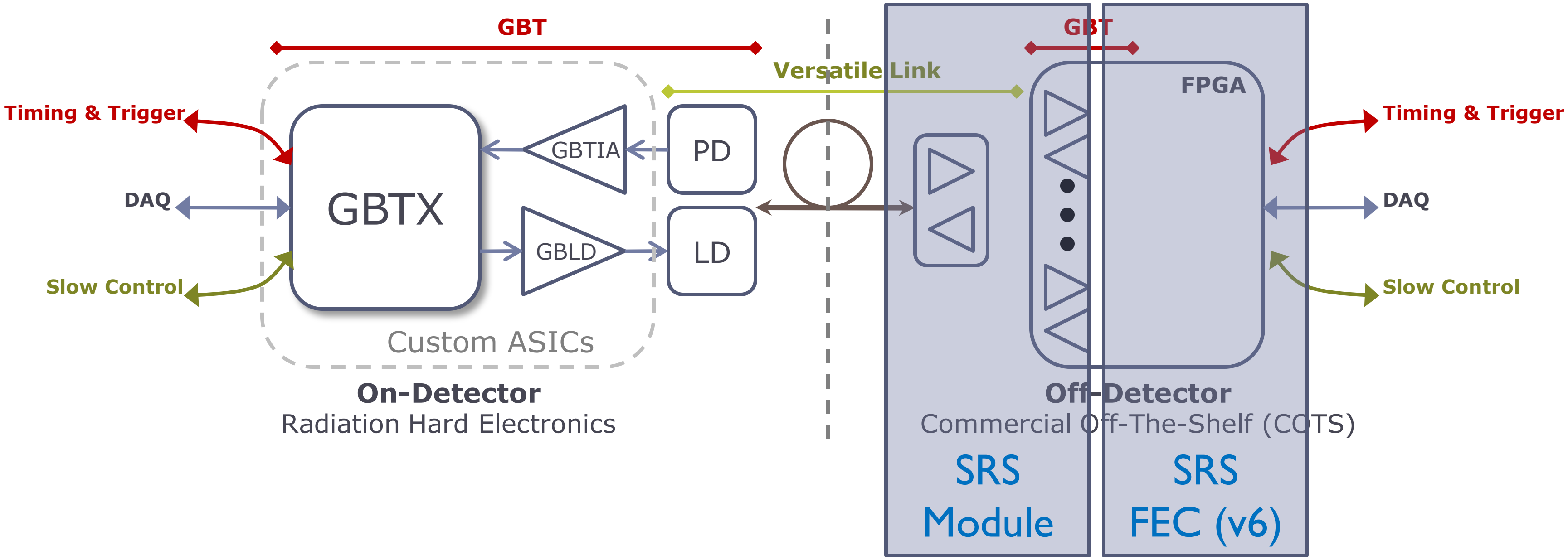


- BEETLE provides similar functionality as the APV + trigger output
- Digital (binary) mode optional
- Design started in Weizmann Institute of Science, Israel (Lorne Levinson)

FEC Upgrade

- Virtex 6 FPGA (*built-in SEU protection, more resources, …)*
- A/B extension interface (PCIE conn)
  - 20 differential
  - **80/40** single-ended/diff
  - 2 x I2C, 1 x JTAG
  - **4(8) x 5Gbps** RocketIO GTP transceivers
- 200 MHz local clock oscillator
- **DDR3 RAM (SO-DIMM)**, 1kb GP FLASH
- **4xSFP+/5Gb Ethernet**/DTC interface
- NIM/LVDS GPIO
- Power control and distribution ; HV feed-through

SRS GBT Integration



- GBT Interface module card with optical inputs (SFP)
- GBT Protocol decode inside the FPGA (Xilinx GTX transceivers), *code provided openly by GBT design community*
- Data buffering in local DDR3 RAM
- High-speed up-link data transmission (up to 10 GbE)

Thank you