A few notes on MicroSemi FPGAs

Tullio Grassi

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Meeting with MicroSemi (formerly Actel) reps in Cern on 16 March 2011

“The ProASIC3 RT parts differ from non RT parts only in term of qualification and testing”.

This is not always clear from the documentation.

Fusion and SmartFusion FPGAs use the same silicon technologies of ProASIC3. They have not been tested for radiation by MicroSemi. The analog part may be soft because some of the configuration bits are stored in flip-flops, not on flash cells.

SEL and SET:

http://www.actel.com/documents/CN1010_RT3P_SEL.pdf

"SEL observed at LET levels of 86.9 MeV/cm^2/mg and higher,

at room temperature and at an operating temperature of 125°C, in tests at Texas A&M University. The SEL events were observed only at high I/O voltage levels (VCCI = 3.3 V) and not at lower levels (VCCI = 2.5 V or lower)"

Irradiations of a decapsulated ProASIC3-250 with Kripton ions (756 MeV, LET=31MeV/mg cm2, range 92 um) at Louvain, by a group from Torino, Eng. Dept. (Luca Sterpone); non published data:

"Observed one SEL every 12000 SET (with a design that maximize SETs)"

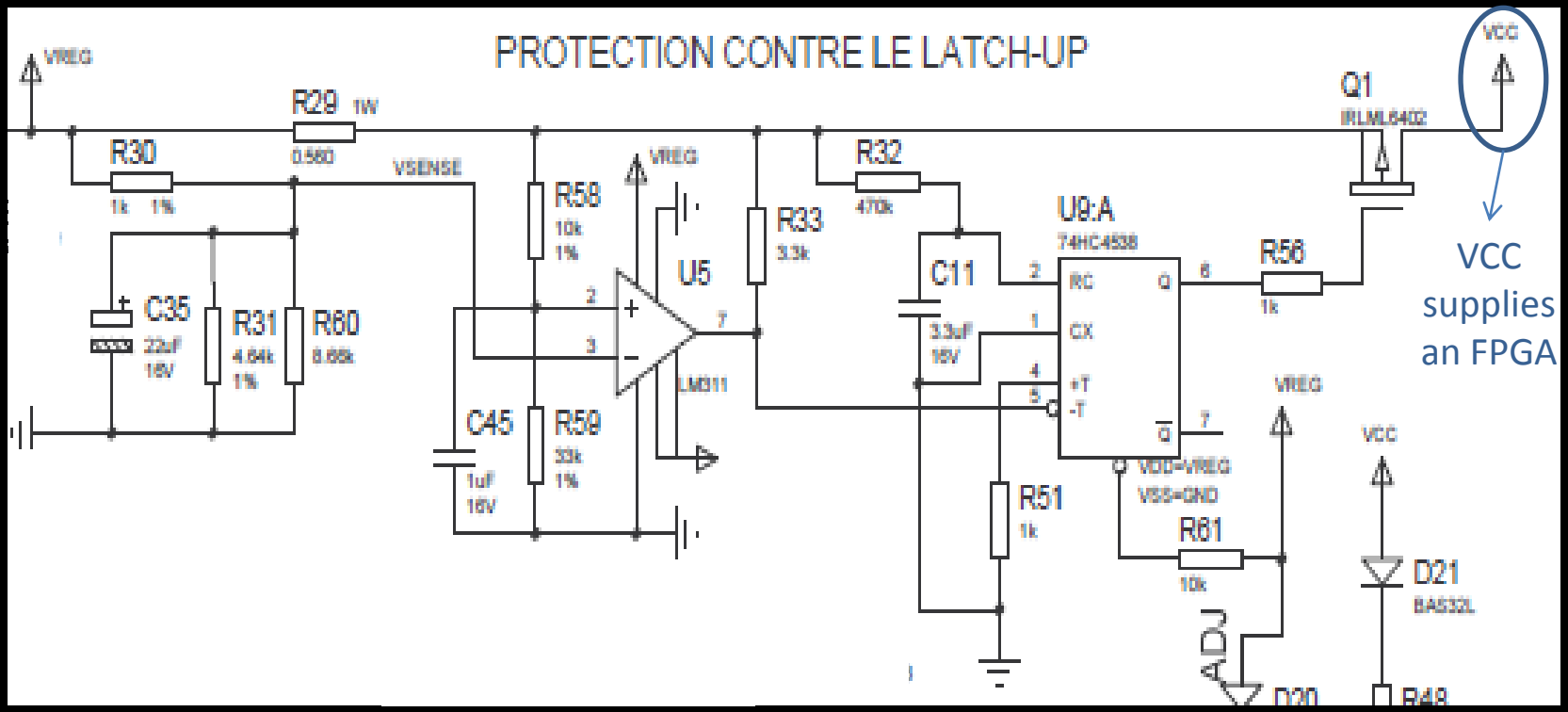
→Are SELs a real problem in the LHC environment ?

→ the guy from Torino has volunteered to review Actel designs in order to look for SEE (he my use it for his publications).

Prevention of SEL

External circuits could detect a latchup and do a power-cycle. The problem is that these circuits could fail and interrupt the normal operations, even if the FPGA is ok.

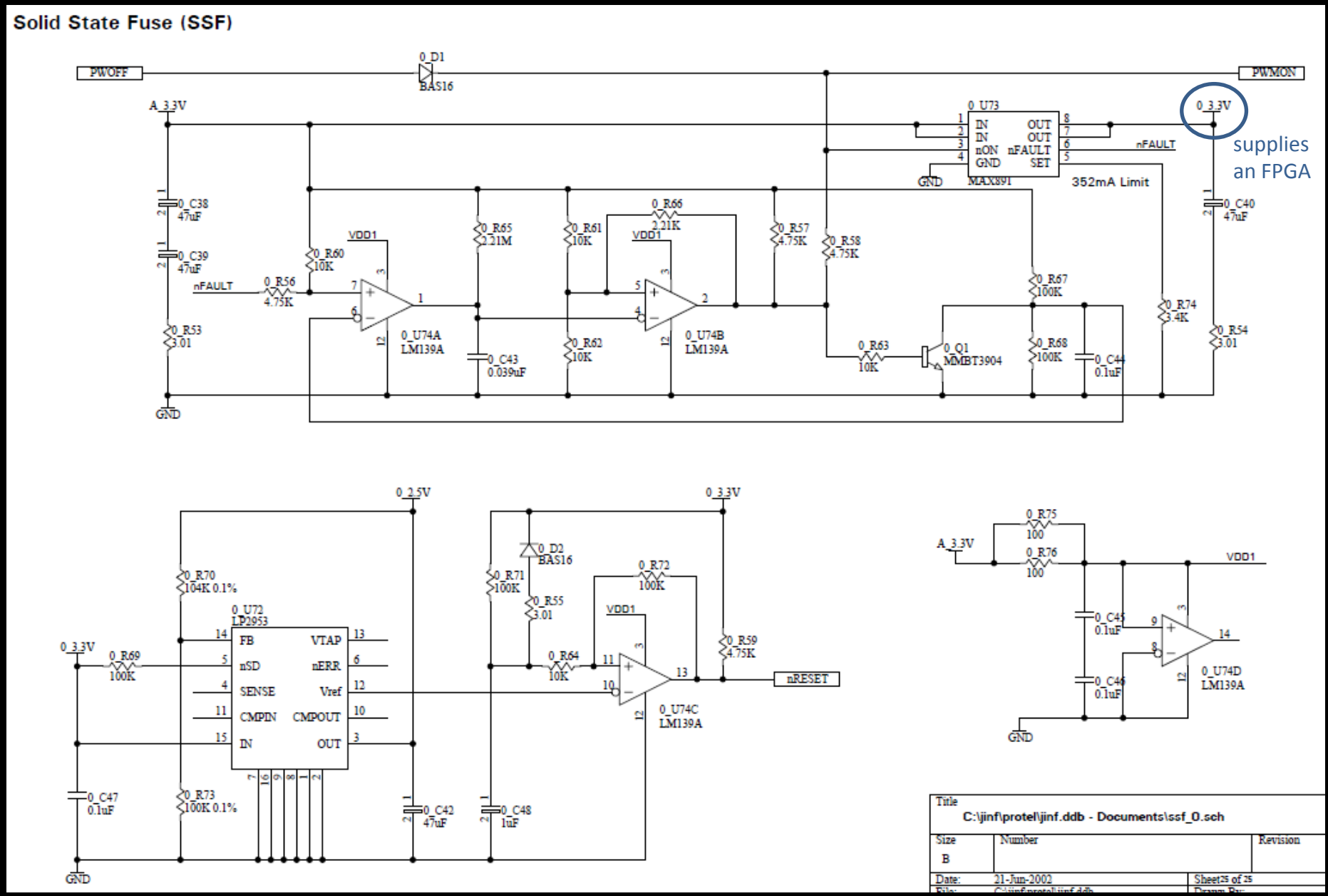
Example from the “RepFIP” card used in the LHC control system: measure the current flowing across R29, if it is above a threshold, the monostable U9 will temporarily open the switch Q1 → power-cycle.



This card is installed, it has been tested under radiation, in one case the component U9 (L4931CD25) has failed at 2×10^{11} p/cm2 (corresponding to TID 100 Gy).

→ I’ll follow the developments

Prevention of SEL: AMS experiment



Design with TMR

There are two synthesisers that can do automatic TMR of flip-flops, in order to prevent SEU:

1) Synplify: http://www.actel.com/documents/SynplifyRH_AN.pdf
   This is available on CERN DFS, on Services\caeprogs\synopsys
   It is being use in Cern by an accelerator group, so far so good.

2) Precision RT:
   https://espace.cern.ch/electronics/Lists/Latest%20News1/DispForm.aspx?ID=6&Source=https://espace.cern.ch/electronics/default.aspx
   also available at CERN.

As of today for Actel FPGAs either of them can do TMR of flip-flops (aginst SEU), but no TMR of combinatorial logic (against SET).

Prevention of SET

- TMR that includes combinatorial logic
- filtering with guard-gate

We need to watch the evolution of CAE tools.

Web-seminar from Mentor:
http://go.mentor.com/or3a