FPGA IRRADIATION @ NPTC-MGH (Part 2)

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Outline

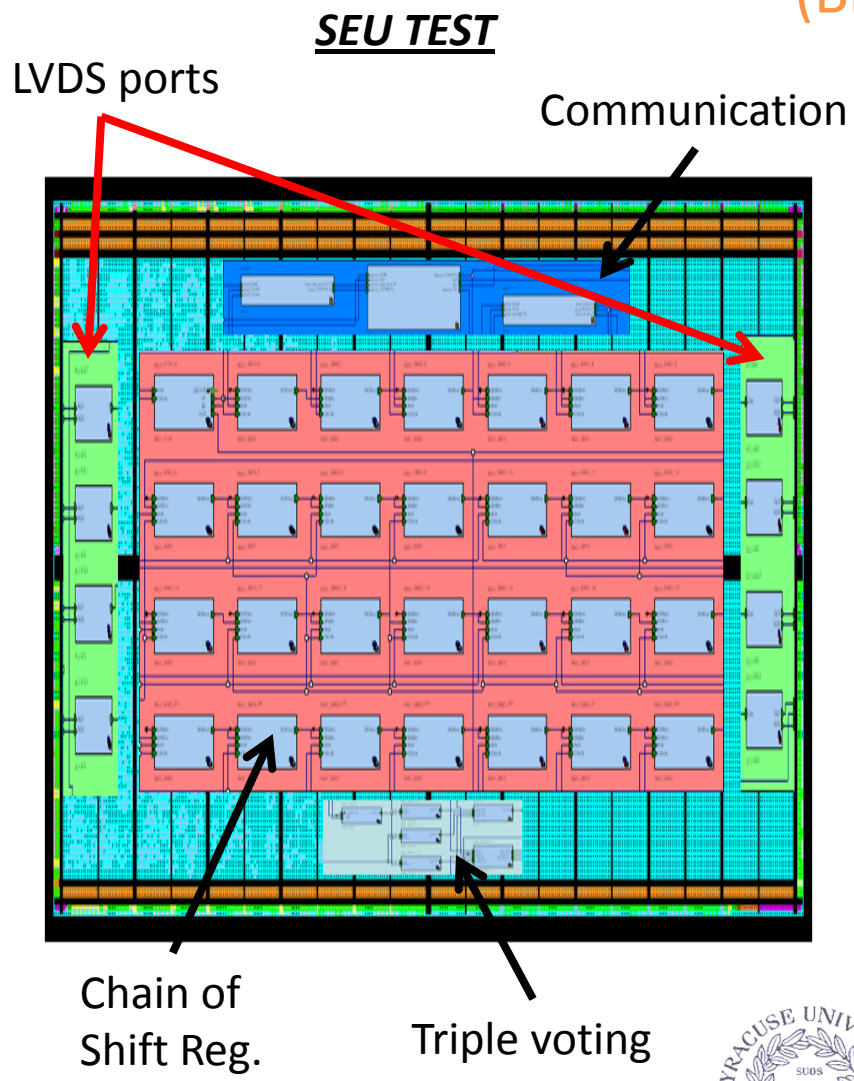
- **Progress with firmware**
  - Solved timing/delay issues, …
- **Progress with hardware**
  - New Eval-PCB, FPGAs, current measurement, annealing (partial)
- **Next irradiation test**
  - Still work and testing to do, new schedule: test >~1 mo away
- **(Non-)Contact w/ Actel rep**
  - Samples, delivery, NDA, est. info path, RT, Univ/Lab program, …

THIS IS STILL WORK IN PROGRESS !

Progress with firmware

- **Had major problems with timing and synchronization at MGH**
  - Difficulties with comparator, communications, etc.
  - Traced to delay module not functioning
  - Now considered solved (see next slides)
- **Re-coded SEU test**
  - Streamlined algo and comm
  - Incorporates new delay scheme (works)
  - Modified to run for a fixed amount of time (~3 mins)
  - Different frequencies: 40, 120, 240 MHz tested, now functional (may adjust if 320 works)
  - Added triple voting into the design on error counter (works)
  - Bench tested for several weeks, seems stable … see no SEUs (!)
  - Communications still needs to be tested
- **RAM/ROM Memory tests**
  - Take SEU test as baseline
  - Coding in progress
- **Physical constraints for loading code can now be implemented**
  - Select region of logic tile space for program, or for specific module of code
  - Can constrain for irradiation, and also for timing purposes

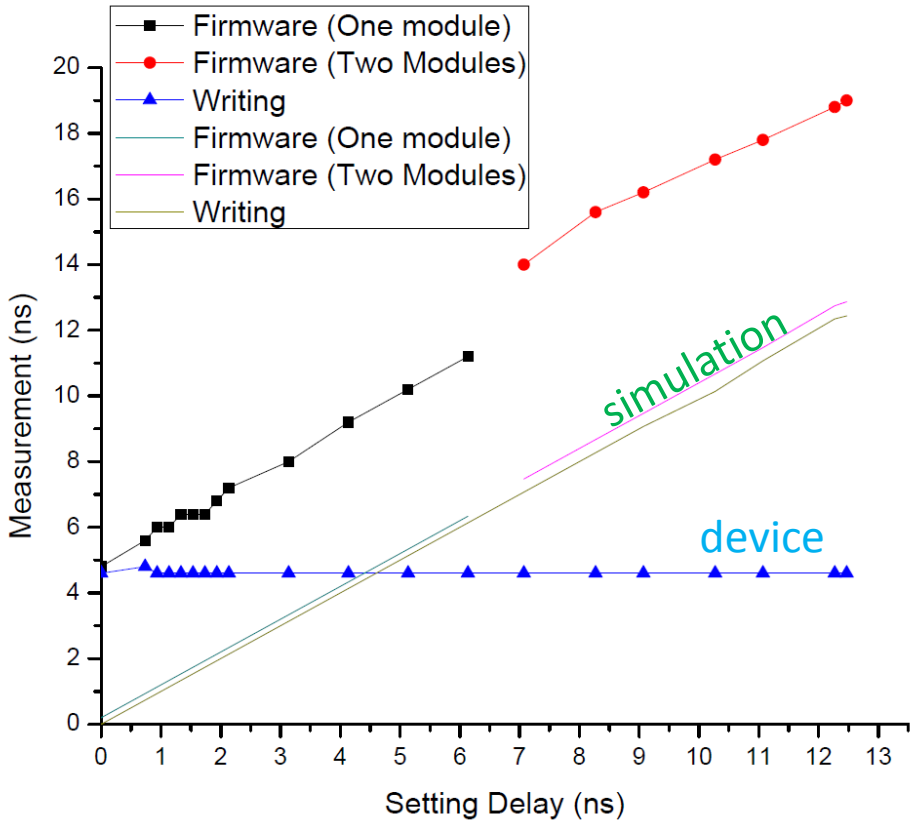
(Bin)



Timing Issues (1)

from last meeting

- **Some systematic studies of timing**
  - Use a small project, with counter, "firmware" delay (i.e., Actel module), and "writing" delay (VHDL code)
  - Set delay in code, measure delay on scope, get plot shown
- **Timing changes when recompile but not reconfigure**
  - Known (offsets in this plot)
- **Timing delays using Actel module works, timing delays using VHDL block does not work at all**
  - Simulates correctly, of course!
  - Syntactically-correct VHDL
  - Actel compiler didn't flag this as an "error" for this FPGA
  - Really problematic, since Actel module is limited to ~7 ns delay
- **Still have not fully sorted all timing issues**



still not explained, but now we have a workaround

Timing Issues (2)

(Bin)

	Works?	Time Delay	Measured Value	Time Increment	Linear?	Offset	Physical Size	Usage
Firmware delay (standard Actel block)	YES	0–6.735 ns	set-value + ext.offset [1]	~0.2 ns	YES	<~5 ns / module [1]	global buffer: max. 18	limited to very fine delays
Write delay (VHDL code)	NO	any value	~2ns (i.e., not functional)	—	NO	constant (~2ns)	0	DON'T!
Shift Register delay (FIFO)	YES	N*25 ns (N=2–512 per module) [2]	set-value + ext.offset [1]	25ns / bit [2]	YES	small	depends on length (e.g. 0.12% core for N=20)	large delays (max 12.8 us each SR)
Trigger delay (N-bit Counter, use MSB)	YES	2^N *25 ns [2]	set-value + ext.offset [1]	variable, $\log_2$	YES	small	0.46% core (approx. constant)	control or enable lines

N = number of bits in register

checked these methods, take no chances

Notes:

[1] External offset is a random offset, due to intrinsic physical propagation delays between logic tiles. Can be controlled by fixing location of module in FPGA. Typically <~5 ns/module.

[2] Clock speed 25 ns (for 40 MHz operation).

Progress with hardware

- **Devices**
  - Eval-PCBs: have 3 in hand now
  - FPGAs: have 2 working (+ 1 rad damaged)
- **Setup now for irradiation of two Eval-PCBs at once**
  - Work in progress
  - Most hardware in place, need new transition board, another channel in ac power relay, and few other items for second setup
  - Will take a few more weeks to finish, then test
- **Current monitoring**
  - Current measurement on high side of REG in place
  - Remote monitoring being implemented
- **Annealing tests**
  - Partially done (see next slide)

Annealing

- **Previously…**
  - After 90–127 kRad(Si) dose, latch-up (apparently) caused large current draw in FPGA
  - Reduced Vcc (1.5 V DC core power level), as delivered to chip, and it dropped below lower limit (1.425 V)
  - FPGA stopped functioning. We saw:
    - firmware failure (no comm),
    - configuration failure (EXIT -24, unstable vpump voltage levels),
    - verification failure,
    - no recovery in situ (via power cycle)
  - Estimated Icc ≈ 1 A draw (or more)
  - Similar to other hard errors:
    - RT54SX (antifuse device) – current sinking with dose, Icc spikes >80 kRad
    - Other A3P devices – adverse effects (propagation delay, frequency degradation) at doses >70 kRad
- **Follow prescription from Frédéric and Jorgen: 100°C for a week**

- ***So far…***
- **Measure current at 9V DC input to Eval-PCB (pass thru)**
  - High side of REG
  - Expect 0.2 A
  - Measure 2.0 A (max for LDO REG!)
- **FPGA heats up very fast – few sec to BBQ temps**
- **Method: Cook @ 100° C, check every 24 hr**
  - Start: 2.0 A
  - After ~24 hr: 2.0 A
  - After ~48 hr: 0.35 A
  - After ~72 hr: 0.35 A
- **However, cannot program the FPGA**
  - Get same error as previously seen (EXIT-24 fail)
- **So, continue cooking…**

Next Irradiation Test

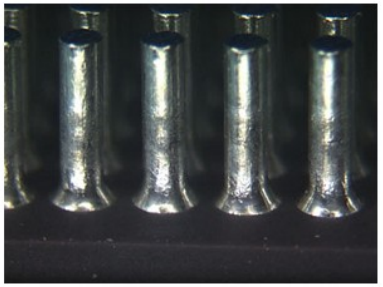
- **Our plan was to settle the issues we found and if successful do another round of irradiation (planned for the current time period)**
- **We have settled the timing issue and most of the associated coding issues on SEU test**
- **Still have some work to do to on memory tests, and some of the hardware**
- **Negotiating with MGH for beam schedule; may join with another user**
- **Currently we have resources for one more irradiation test**
- **Revised plan:**
  - Irradiation in May(-ish) time period
  - Two Eval-PCBs at once
  - 3-5 FPGAs to be irradiated

Actel Rep, etc.

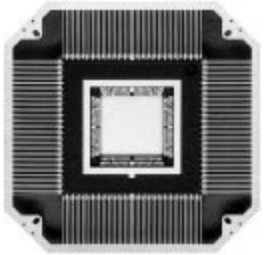
- **"Our" Actel rep**
  - Initial meeting 10/15, then effectively disappeared for ~3 mos, due to merger with Microsemi (which seemed chaotic, not a good sign, but hopefully one time thing)
  - Some technical info exchange, but other contact attempts were redirected
  - Resurfaced recently, re-tasked to us, meeting 3/18
  - Next meeting tenatively scheduled for week of 4/11, with "real" engineer and rad tolerant "expert"
- **Several broader issues**
  - NDA: in process since 12/15, yet to establish efficient info path
  - Samples: requested 5, but they appear to be very stingy (we may get 2)
  - Distributors: limited to Future, Mouser, Avnet Memec (Microsemi), Actel Direct (US)
  - Delivery schedules: always appears to be long (8-10 wk)
    - Have "Actel Direct" website for ordering small quantity orders. North America only , probably some European equivalent also? Take advantage of WIP that can be diverted, so can improve lead time. Claim is: can reduce to 4 wk.
  - University/Laboratory program:
    - Actel/Microsemi does not have a University program of any kind in place and it is clear that they really do not know how to handle University or Laboratory groups.
    - Advantageous to try to establish this kind of relationship with them.
    - It would go a long way in dealing with them to represent to them that if we would decide on Actel devices, we will make a centralized buy. That would give them some incentive to be more timely in their response and also provide us with better support and samples.
    - This is something to consider and decide in the long term.
    - For the moment, the line I am taking is that we will order 10 K devices from them in bulk. So we'll see what kind of response that generates, and if we can establish a program with them.

Actel RT ProASIC3

- **Rad-tolerant version of ProASIC3**
  - Many irrad measurementss already made by Actel
  - Recently space qualified (MIL-STD-883 Class B)
- **RT3PE600L and RT3PE3000L are based on ProASIC3-L**
  - Low power
  - ProASIC3-L max oper freq: up to 781.25 MHz
- **Cost**
  - Probably in 1K$ range
  - Compare $150 for A3PE1500, ~$70 for A3P1000L
- **Package**
  - CCGA/CLGA or CQFP only (not PQ208 now)
- **Actel rep: does not think rad data for A3P is going to be requested by Actel (due to RT devices)**
  - So the lever arm for information share back may be minimal
- **Might be useful to investigate RT further…**



Ceramic Column Grid Array (Pb/Sn Columns, + Cu)



Ceramic Quad Flat Pack