The CMS Pixel Tracker detector: performance and operational challenges in Run3

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UZH Seminar

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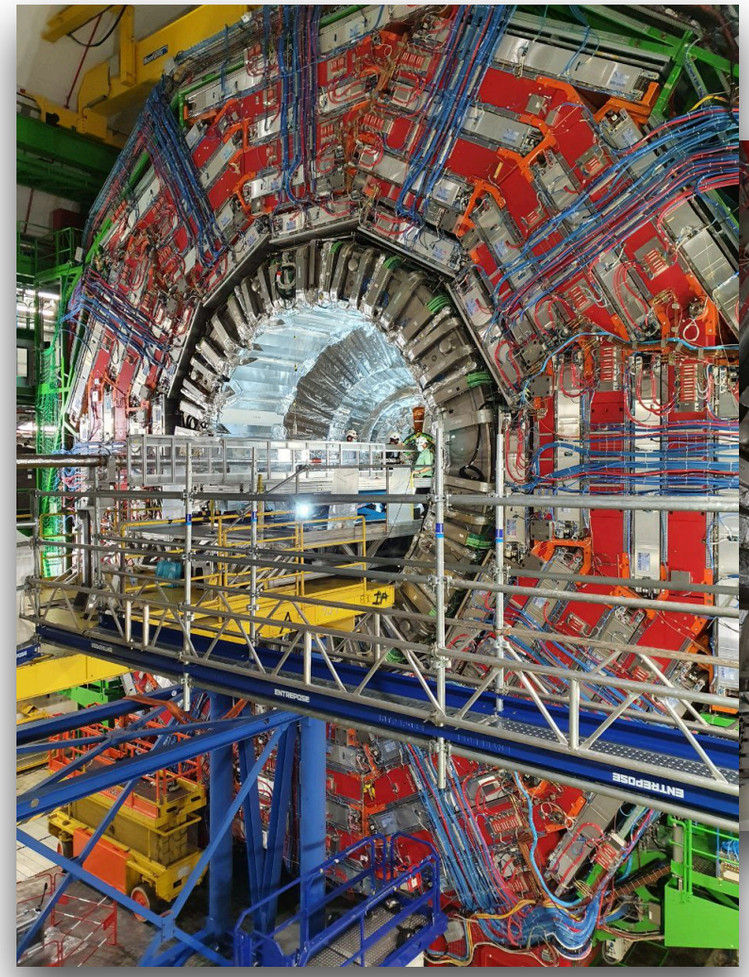
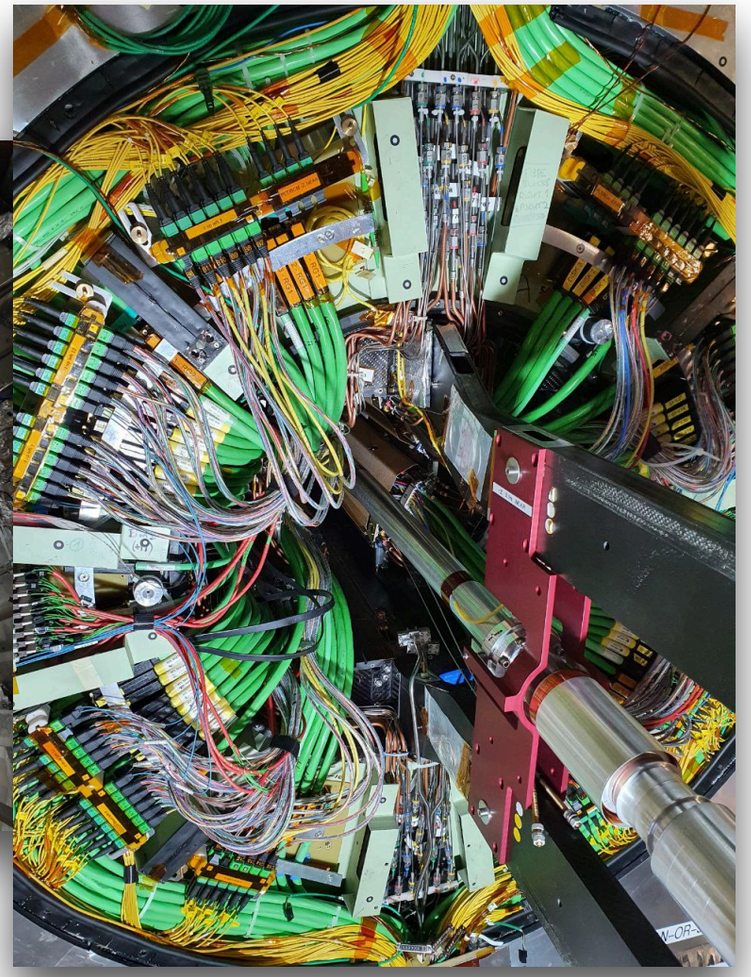


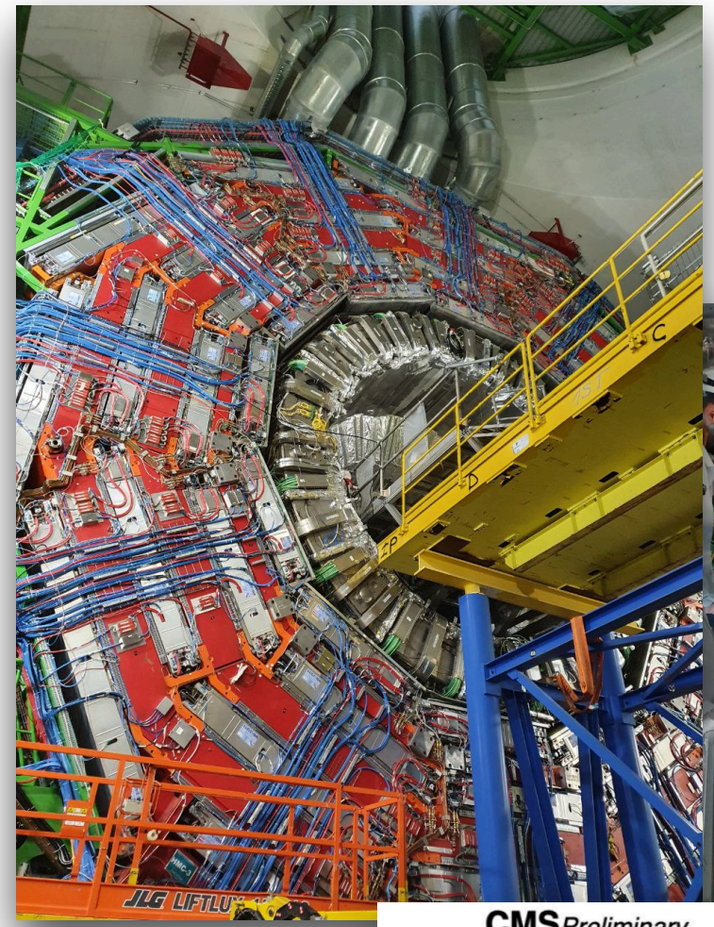


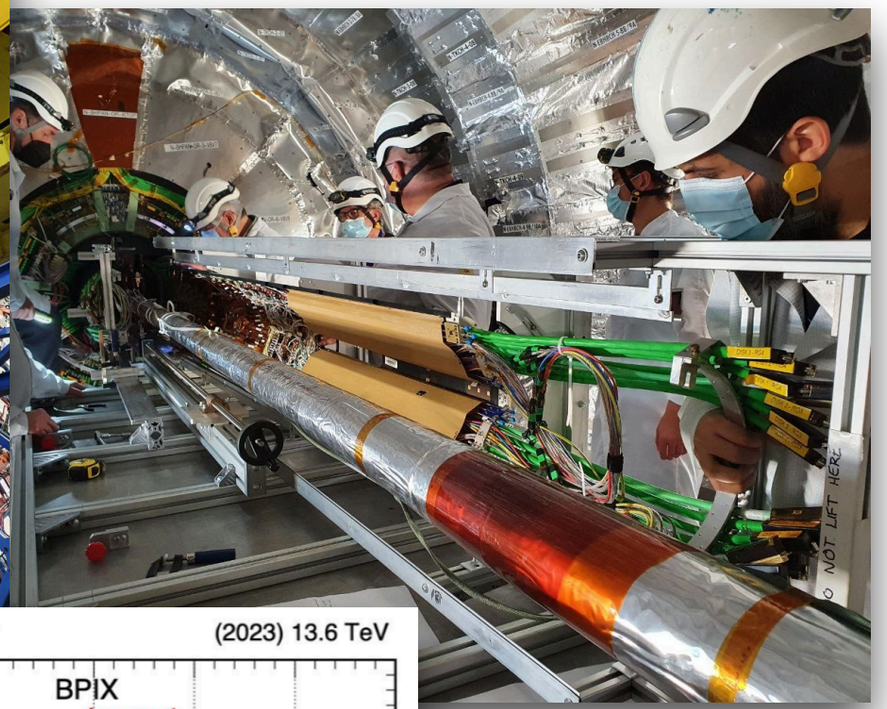
Overview

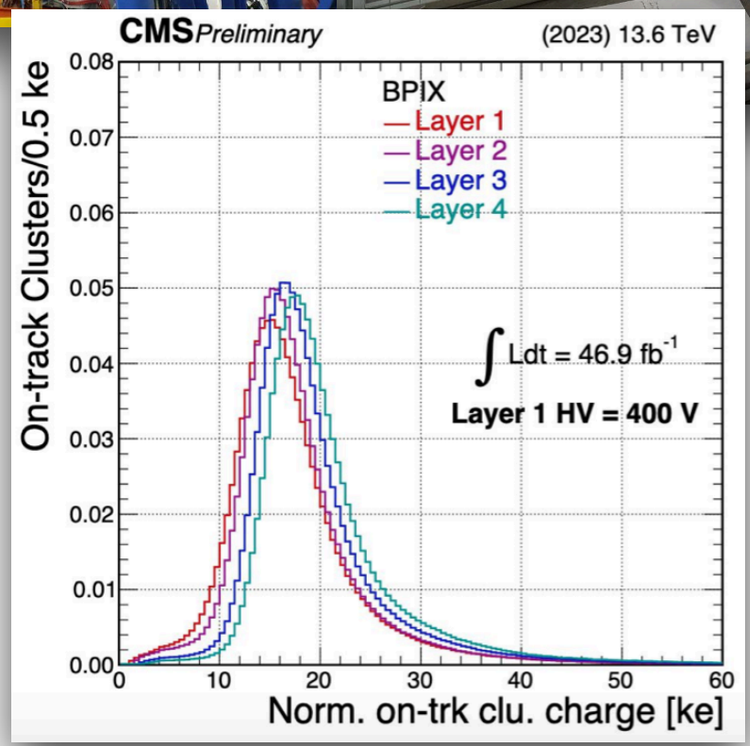
- **CMS Pixel detector**
  - Tracker detector
  - Pixel modules
  - Powering & signal path

- **LS2 activities**
  - Refurbishment
  - Installation
  - Commissioning

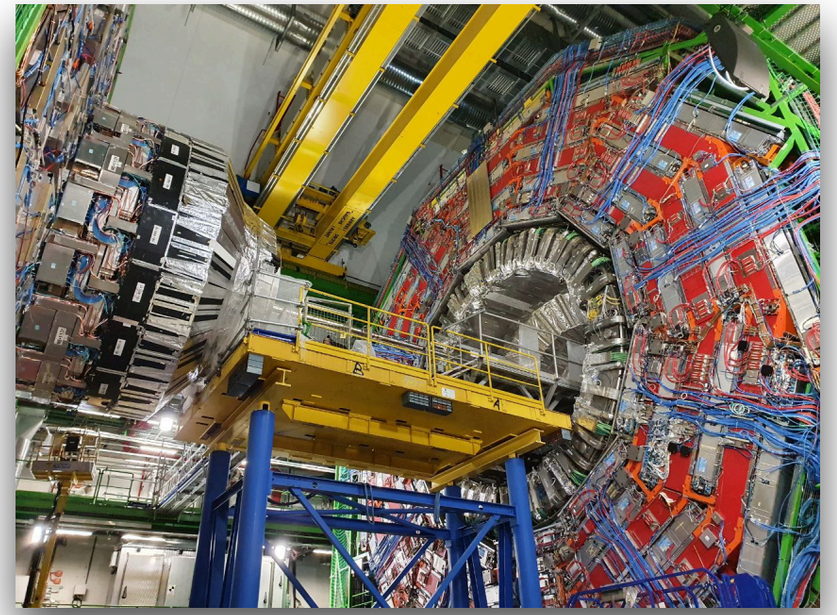
- **Run 3 data-taking**
  - 13.6 TeV collisions
  - First performance
  - Operational challenges

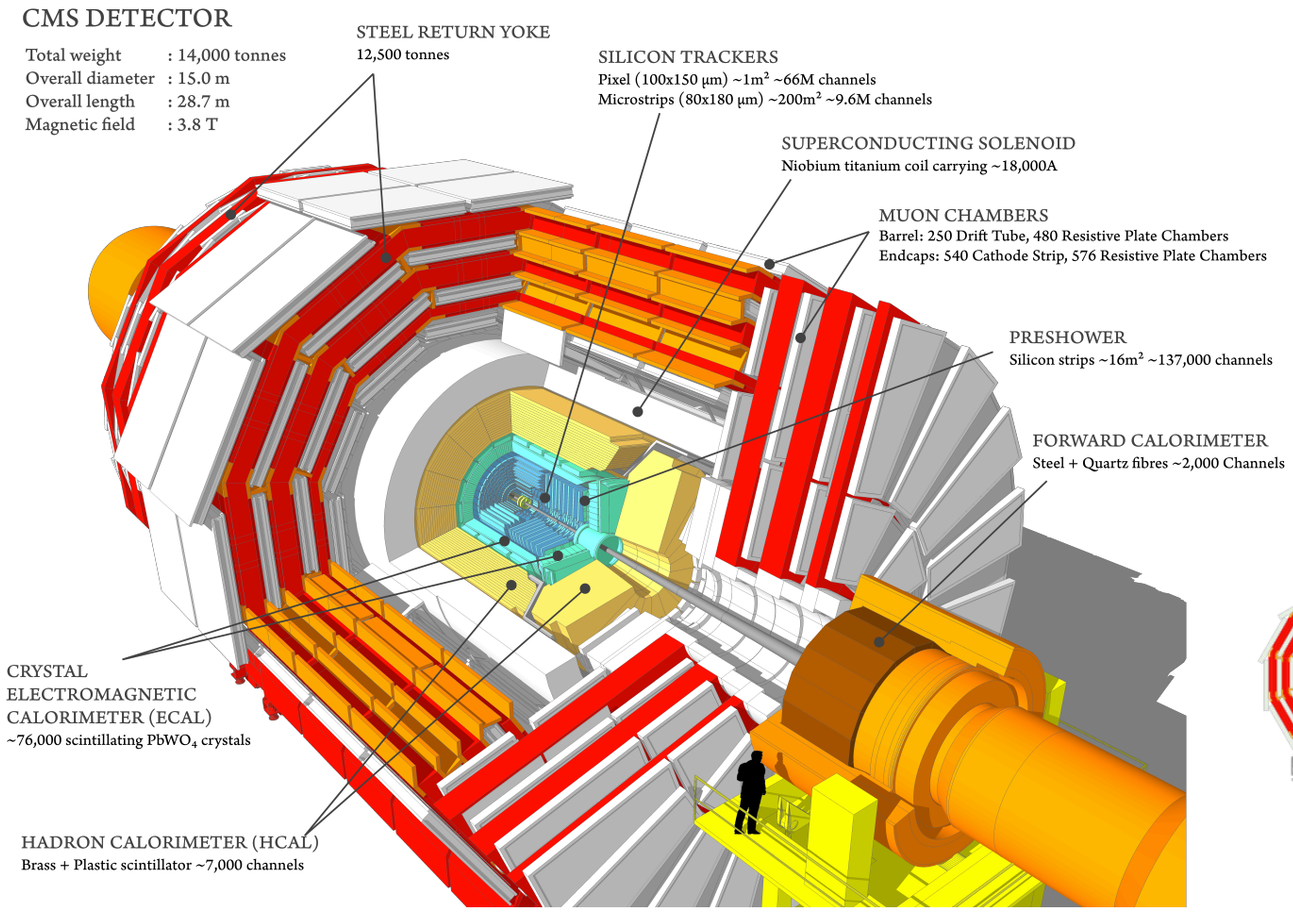


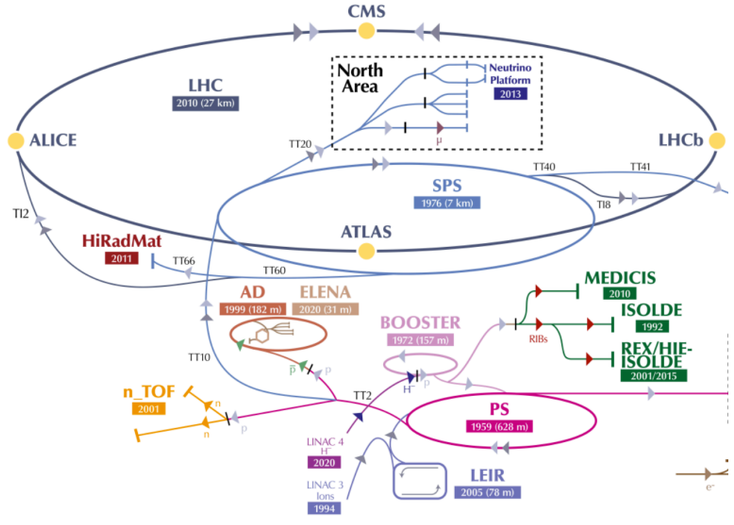


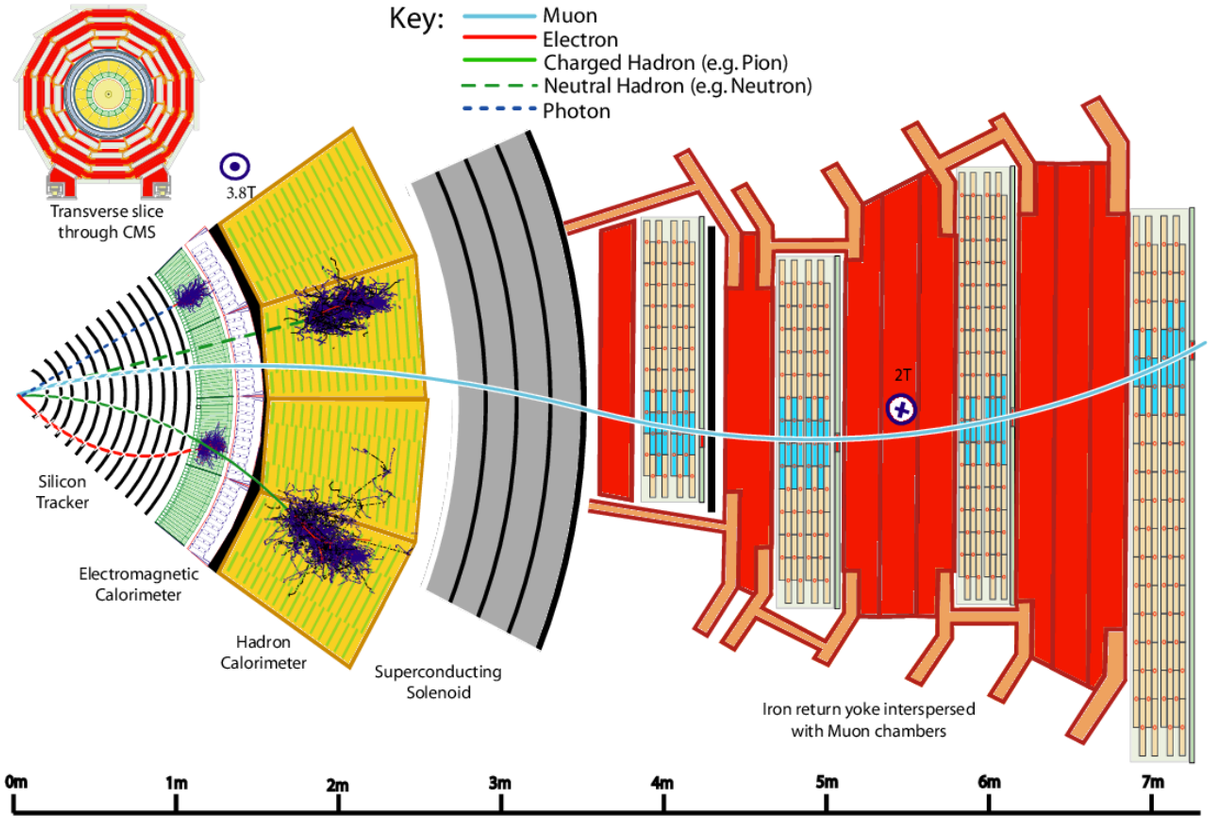


The CMS experiment





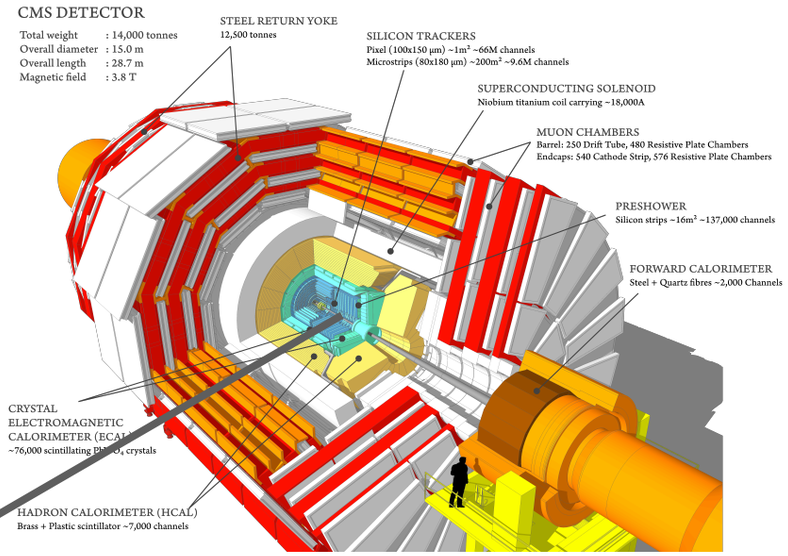


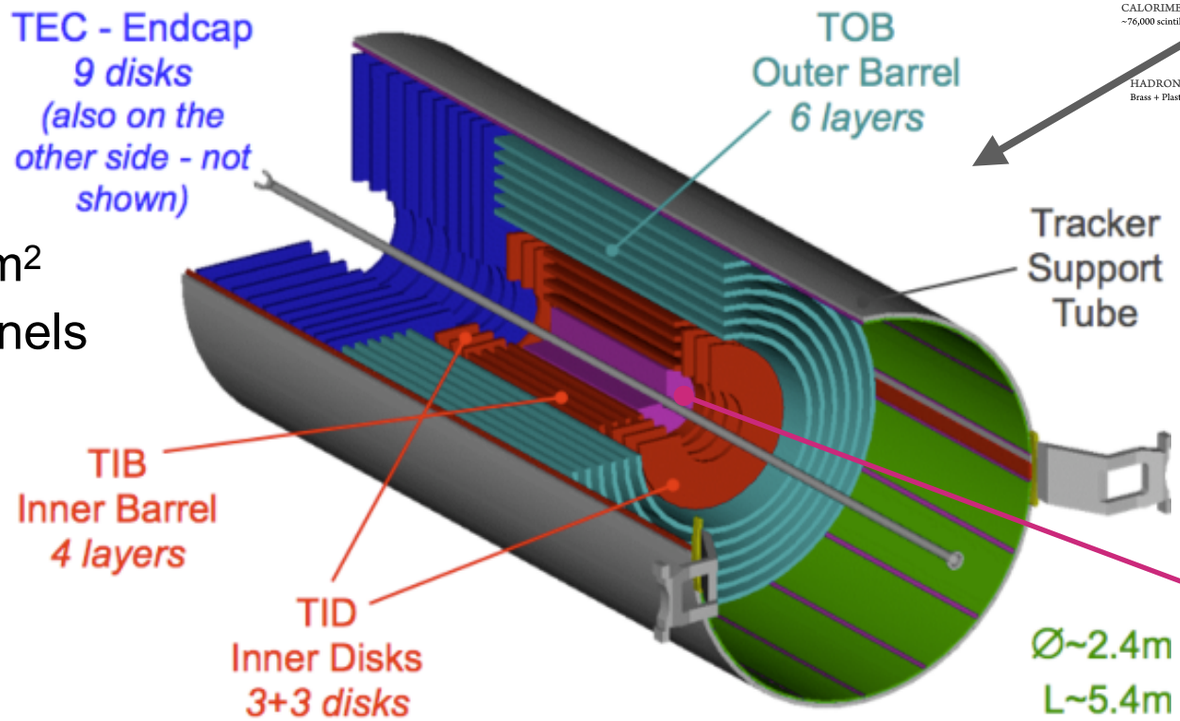


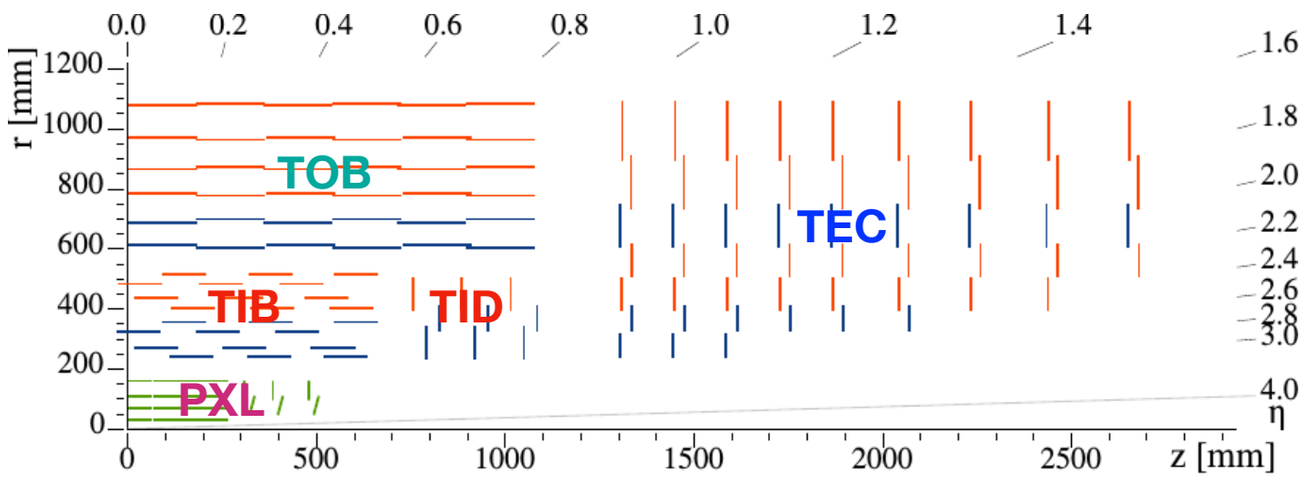
The Tracker detector

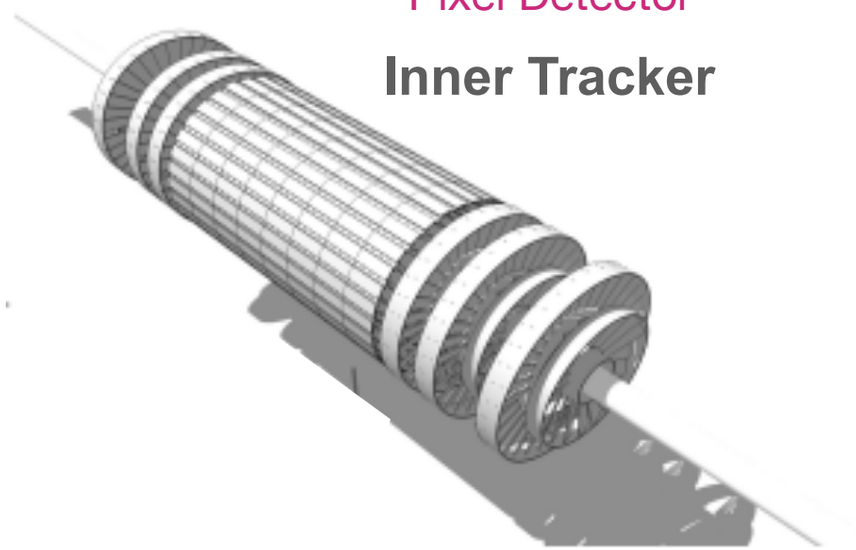
Outer Tracker
= Strips Tracker

- TIB, TID, TOB, TEC
- active material ~200 m²
- ~10M electronic channels







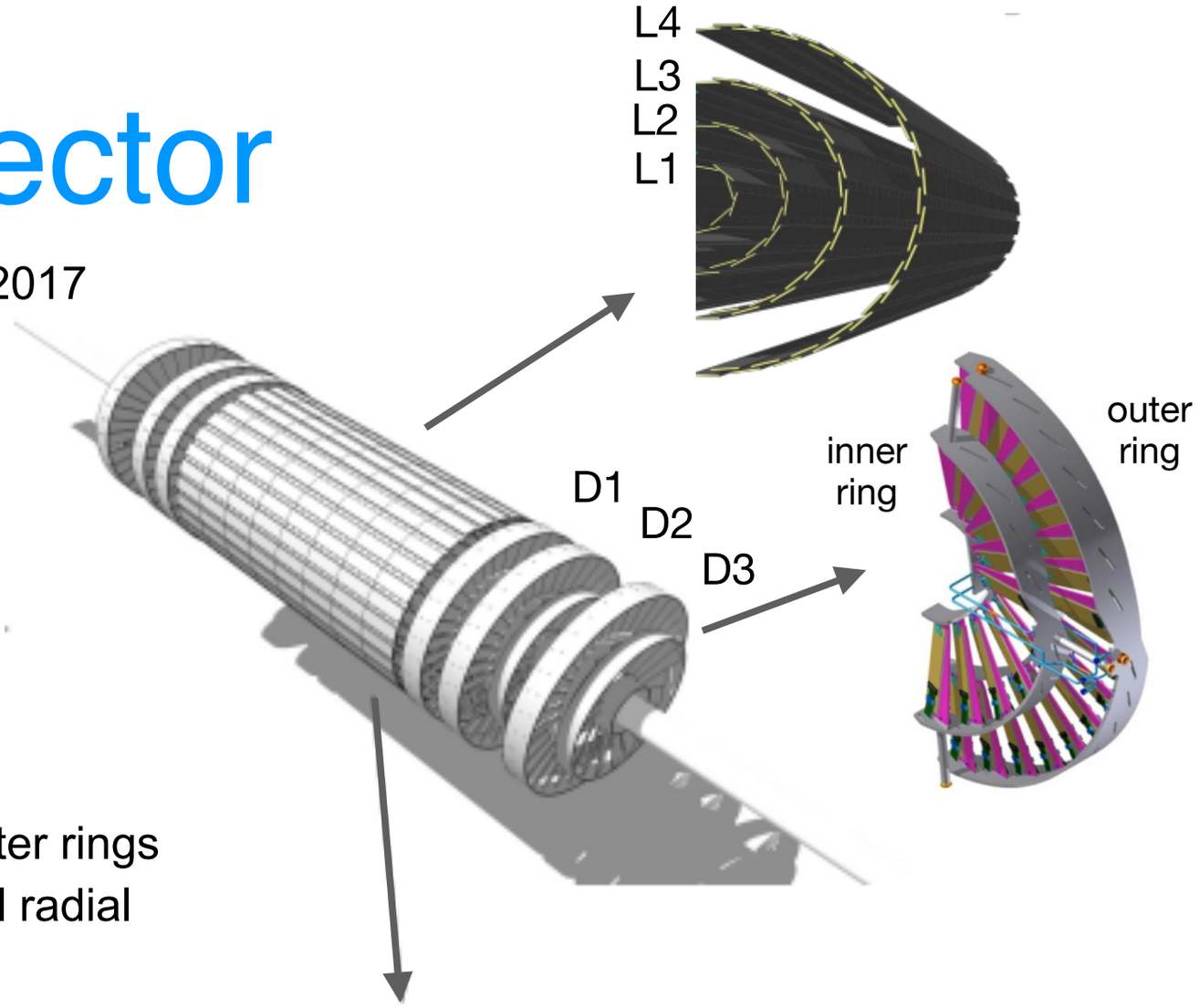


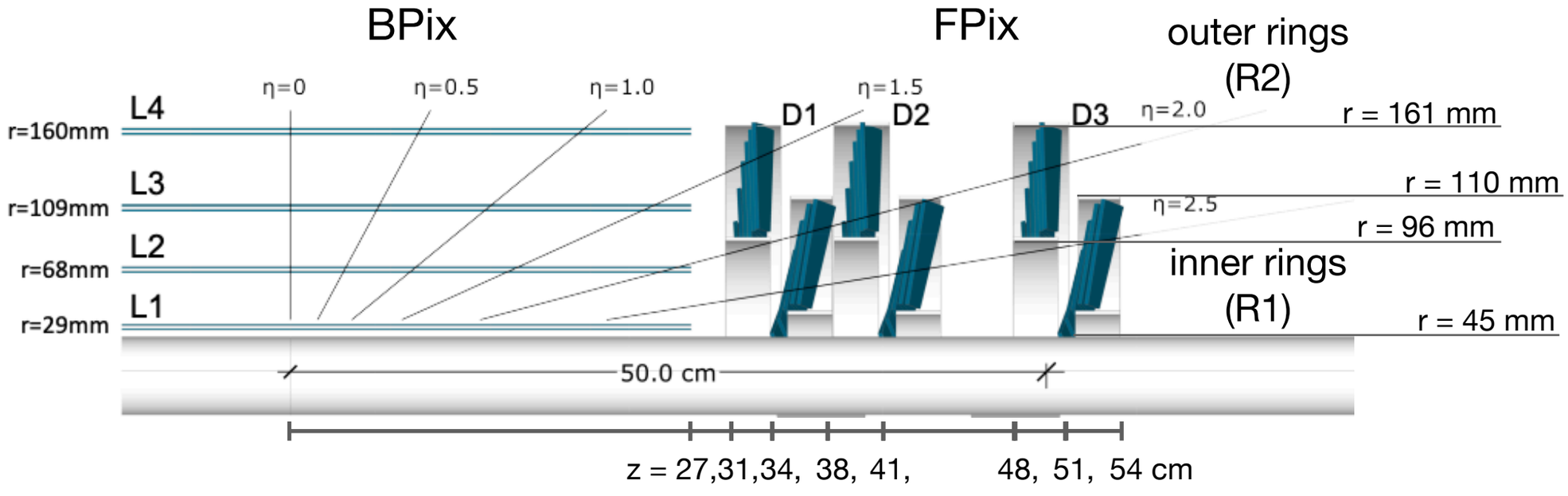
The Pixel detector

- Phase-1 detector installed in winter 2016-2017
- 4-hit coverage up to $|\eta| < 2.5$
- **124M readout channels in ~1.9 m²**

- **Barrel Pixel (BPix): 4 Layers**
  - pixels oriented with the long side parallel to the beam line

- **Forward Pixel (FPix): 3 Disks * 2 Rings**
  - turbine-like module arrangement in outer rings
  - modules in inner rings tilted for optimal radial and azimuthal resolution





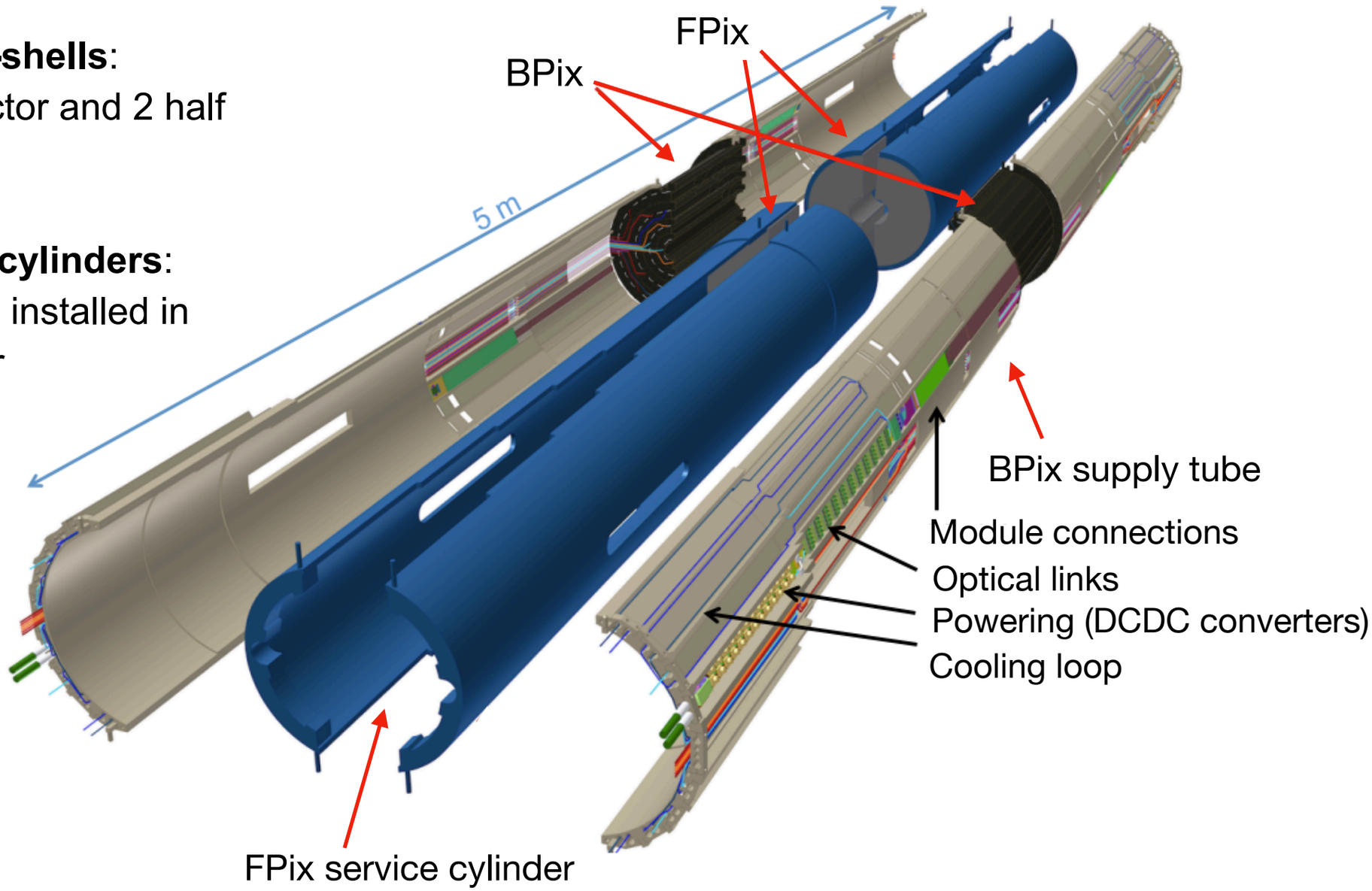
On-detector services

- BPix/FPix supplied by **supply tubes/service cylinders**:
  - holding **readout electronics, power and cooling lines**
  - modular, easy-to-access design

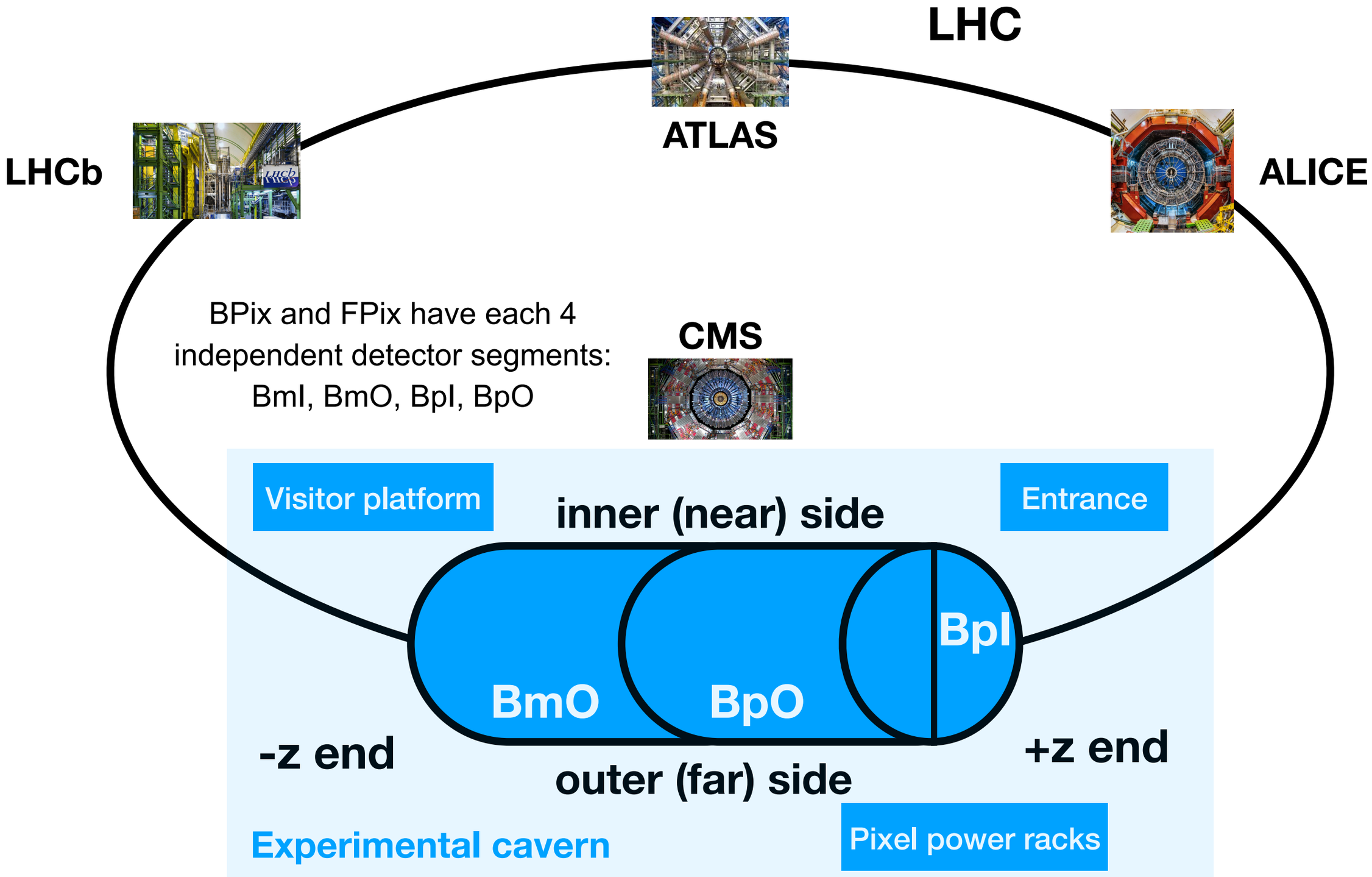
- **BPix divided into 2 half-shells**:
  - each with 1 half detector and 2 half supply tubes

- **FPix divided into 4 half-cylinders**:
  - each with 3 half-disks installed in a service half-cylinder

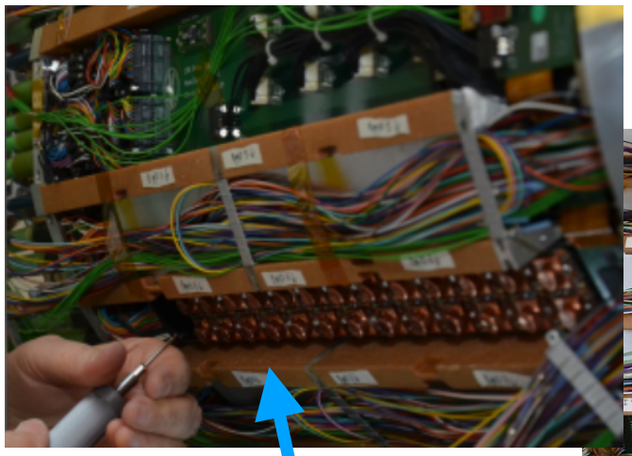
Goal = minimize material used in the detector to optimize tracking and vertexing resolution

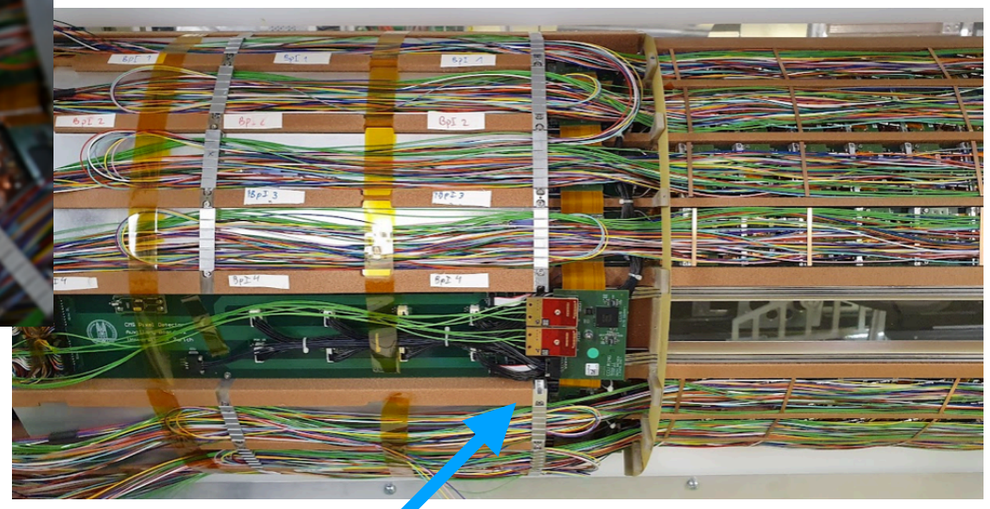


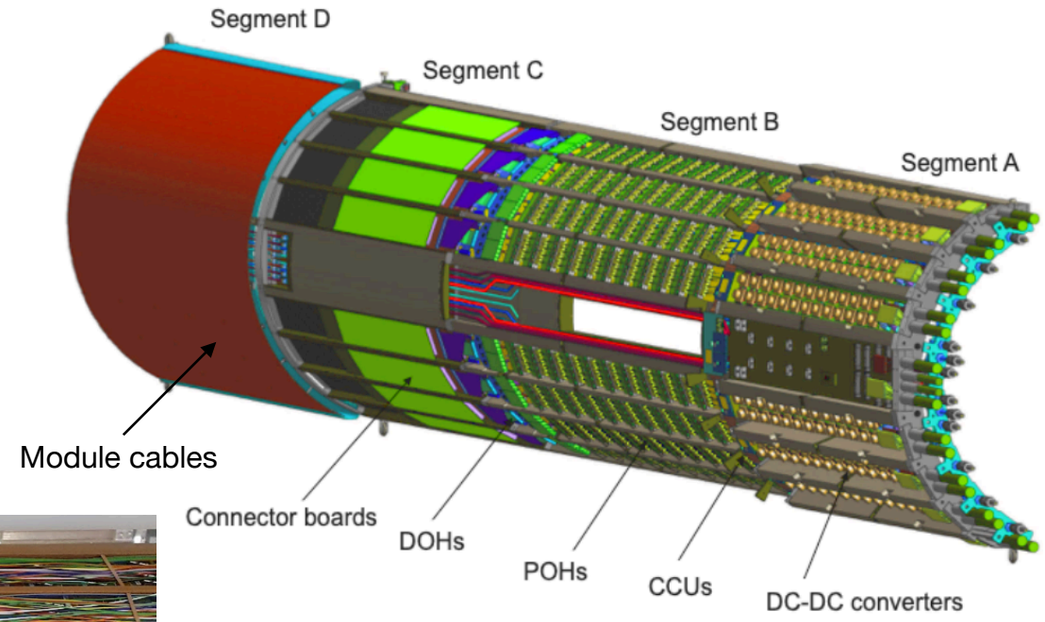
Detector coordinates

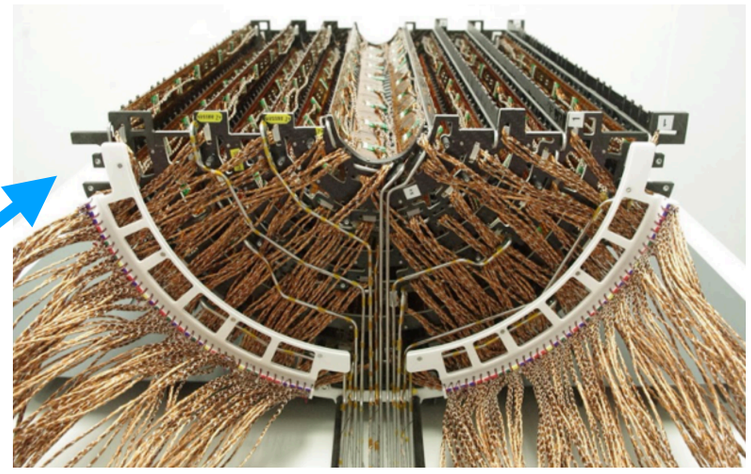


BPix half shell





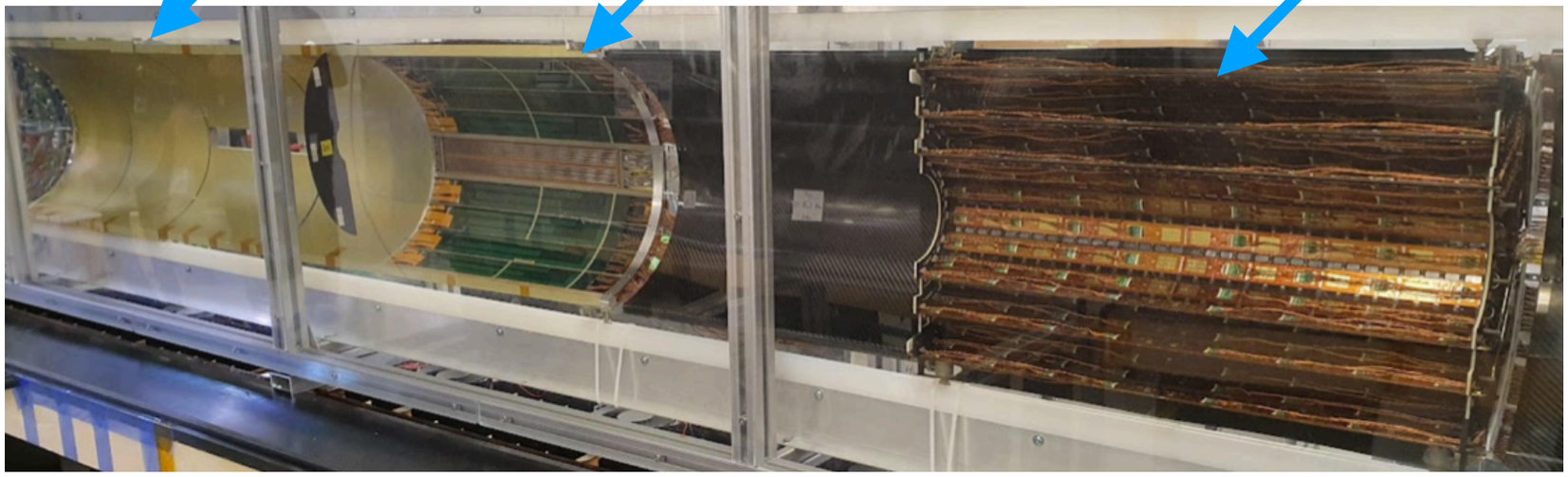




DCDC converters

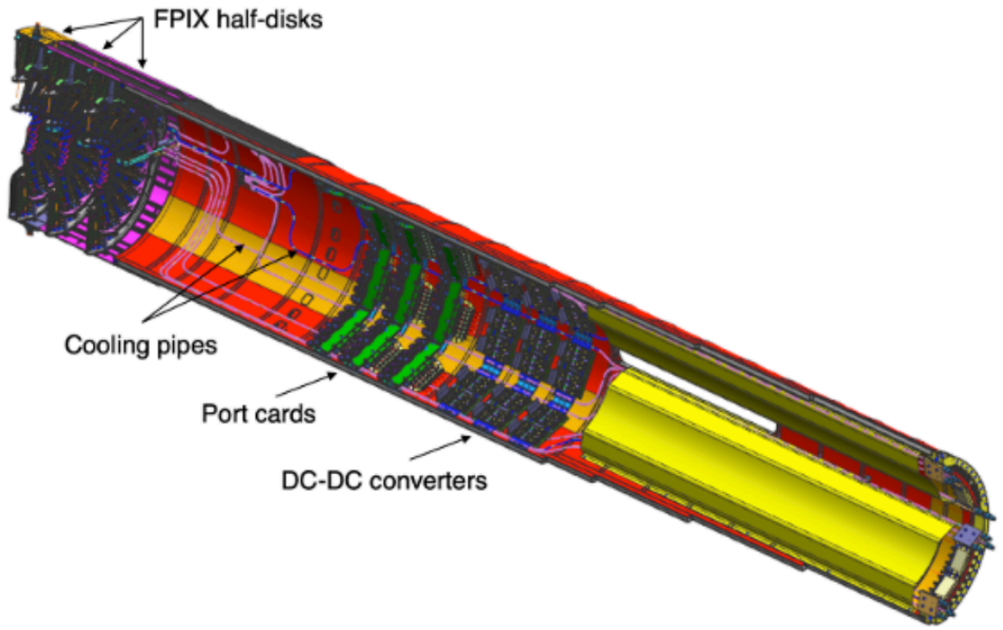
Opto-electronics

Modules

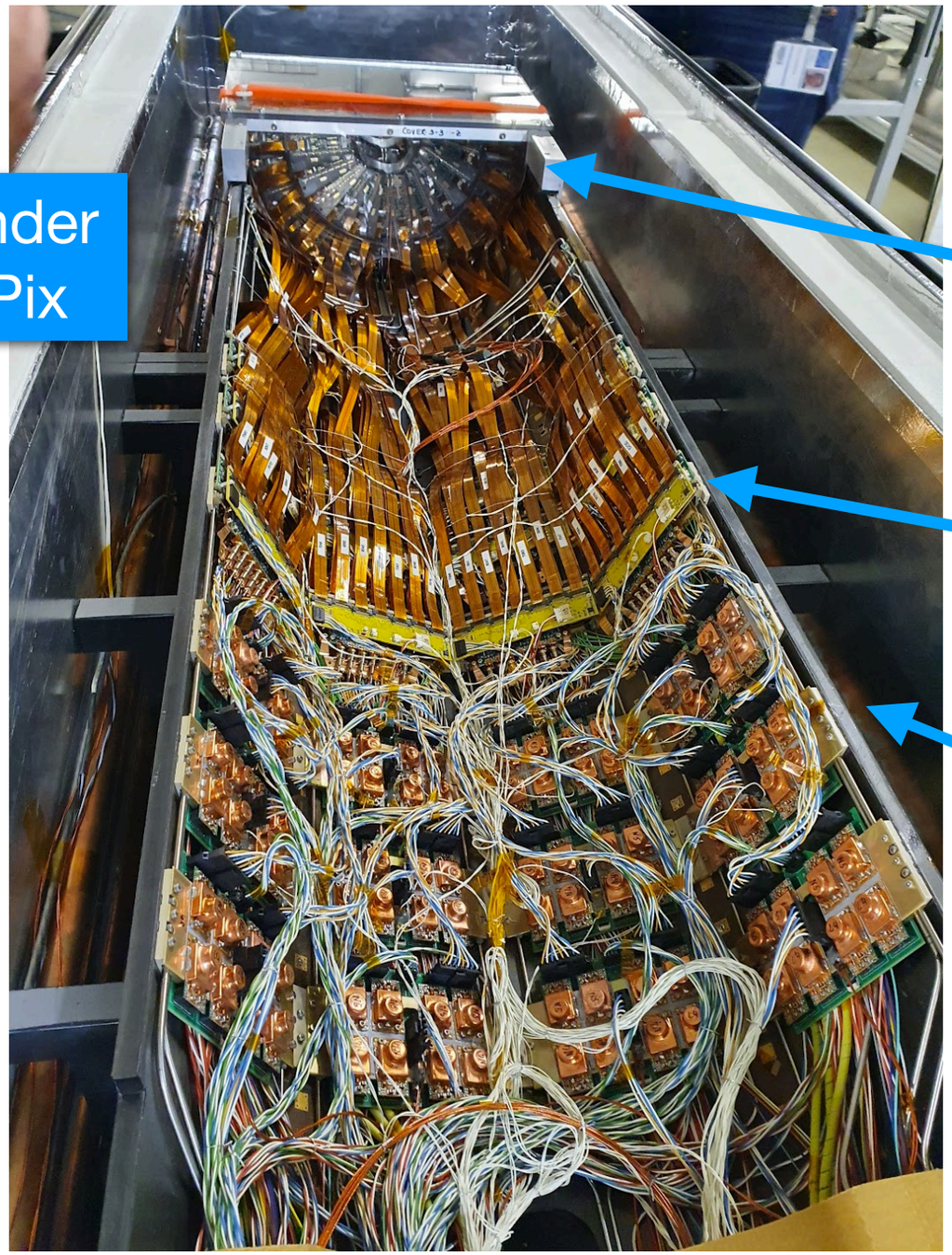


Half shell
= 1/2 BPix

FPix half cylinder



Half cylinder
= 1/4 FPix



Modules

Electronics
(port cards)

DCDC
converters

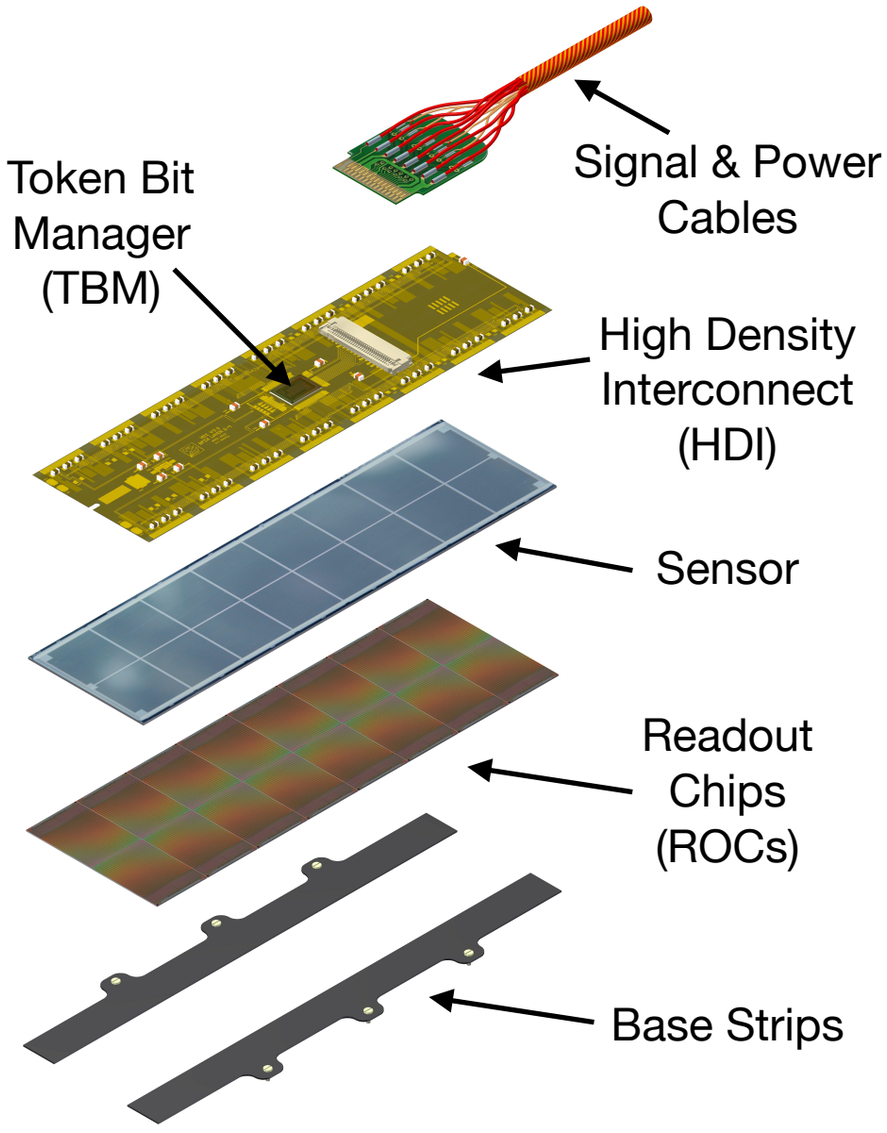
Modules

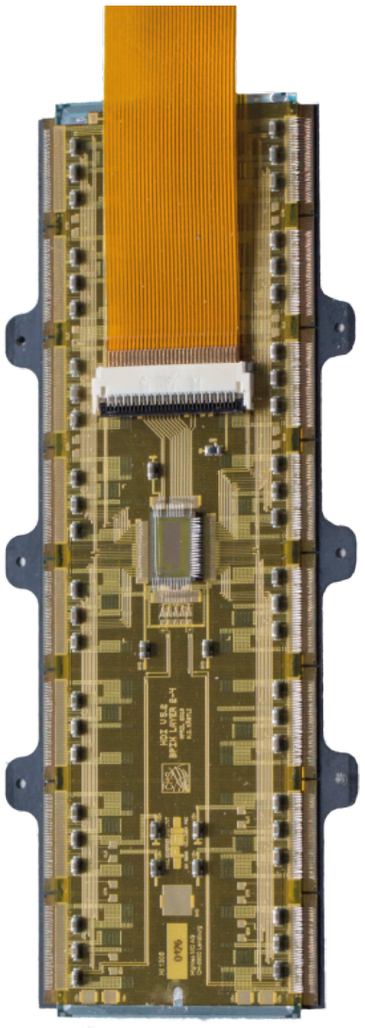
- **Planar n-in-n silicon sensor**
  - 18.6 x 66.6 mm², ~280 µm thick
  - **standard pixel size = 100x150 µm²**
  - bump-bonded to array of 2x8 ROCs

- **Read out chips (ROCs)**
  - read signals from sensor, process them and send them to TBM

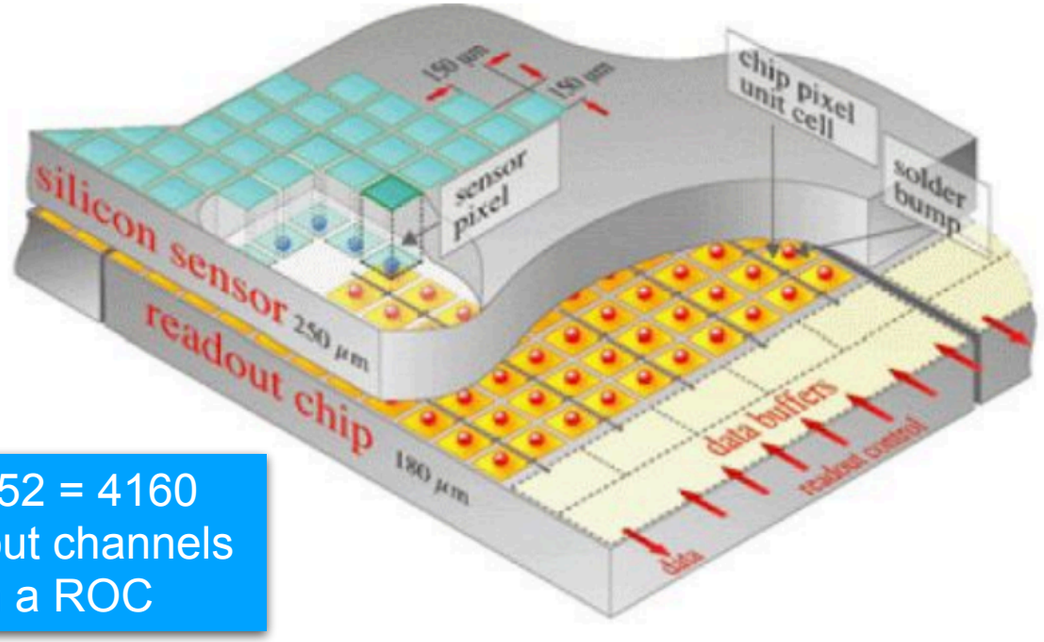
- **Token Bit Manager chip (TBM)**
  - mounted on top of HDI
  - controls readout of a group of ROCs
  - **2 TBMs for Layer 1**

- **High-density interconnect (HDI)**
  - flex printed circuit glued on top of the sensor and wire-bonded to ROCs
  - routes control and data signals between ROCs and TMBs
  - routes high-voltage to the sensor





160x416 = 66560 pixels in a sensor



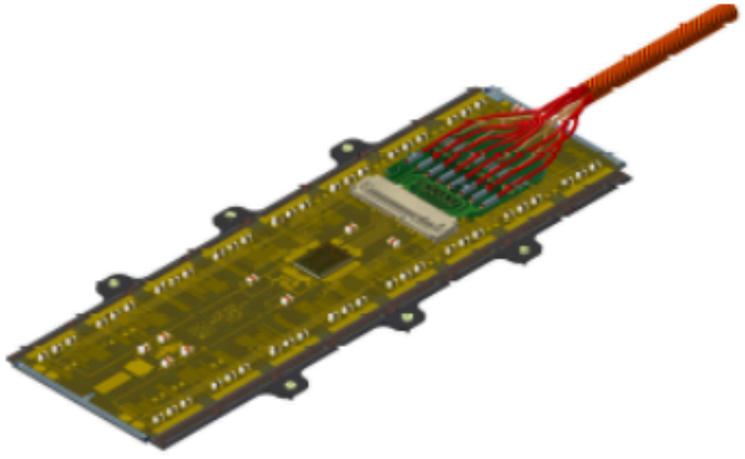
80x52 = 4160 readout channels in a ROC

BPix and FPix modules

1856 modules:
1184 in BPix
672 in FPix

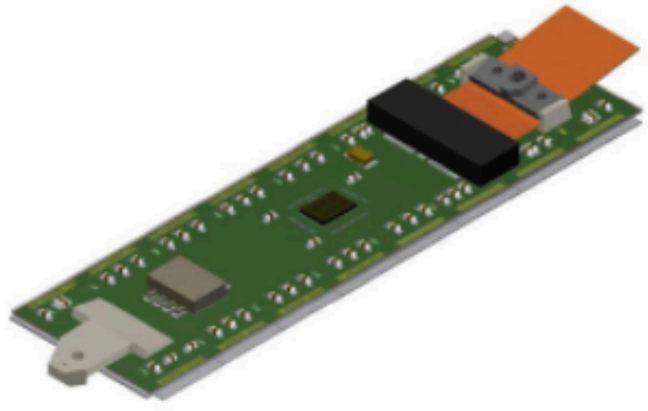
BPix L1

- 96 modules
- ROC = PROC600v4 - **designed to cope with high particle hit rate**
- Pixel hit rate: 600 MHz/cm^2
- Dose: 250 Mrad



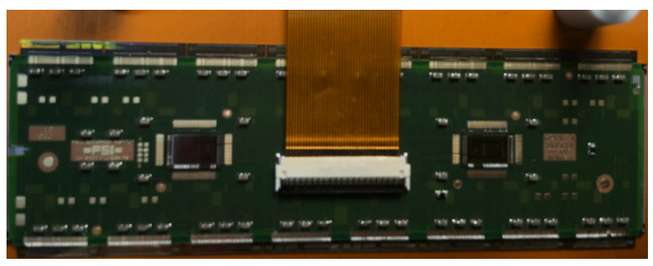
BPix L2-4

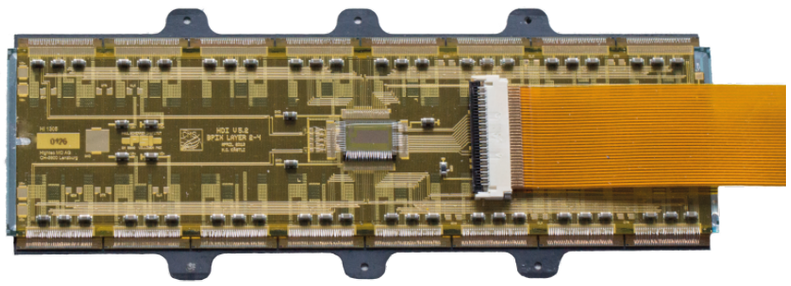
- 1088 modules: 224 in L2, 352 in L3, 512 in L4
- ROC = PSI46dig
- Pixel hit rate: 30-120 MHz/cm^2
- Dose: 15-50 Mrad

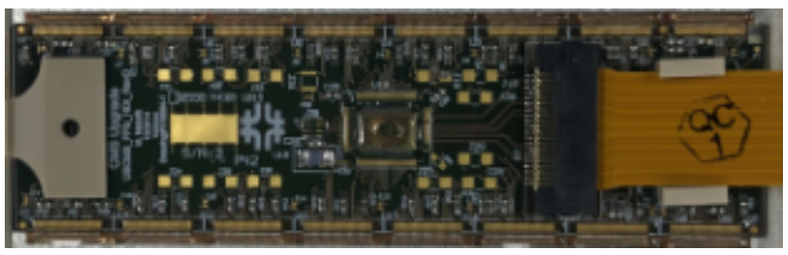


FPix

- 672 modules: 88 in each inner ring, 136 in each outer ring
- ROC = PSI46dig
- Pixel hit rate: 30-250 MHz/cm^2
- Dose: 15-100 Mrad

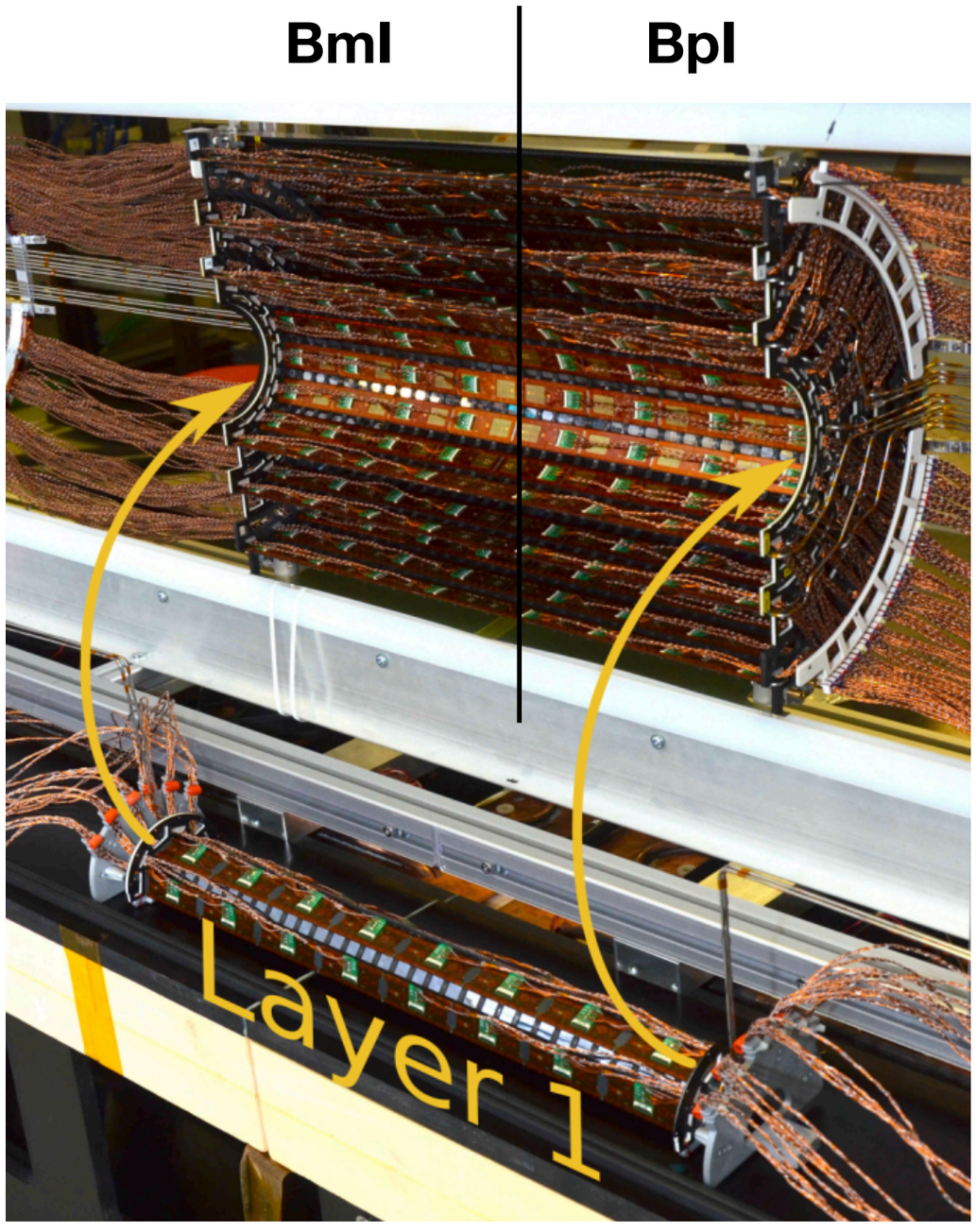




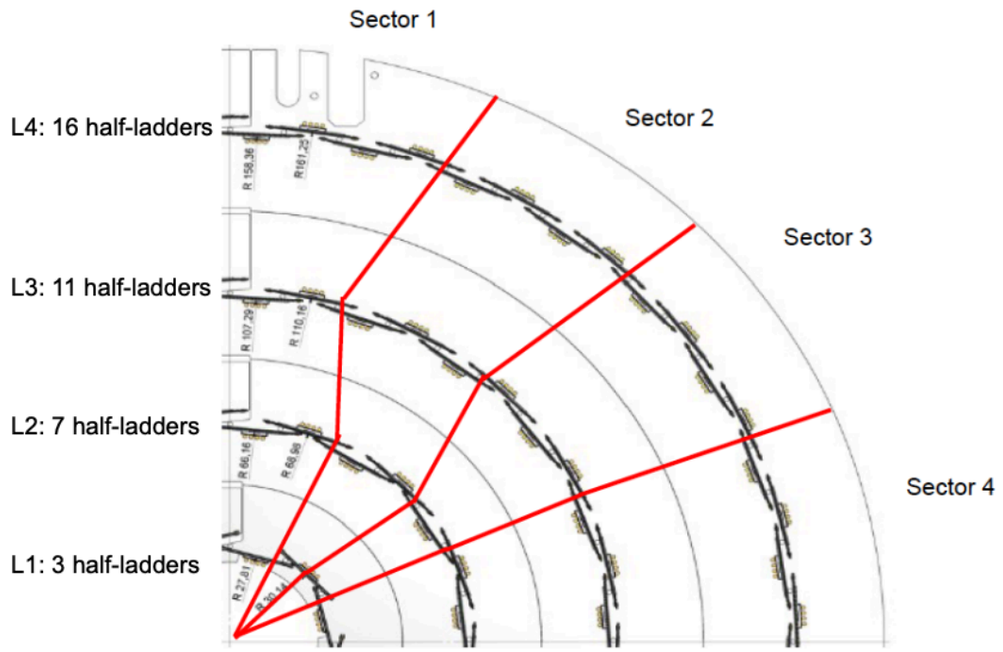


All components suited for high integrated and instantaneous luminosities

BPix modules

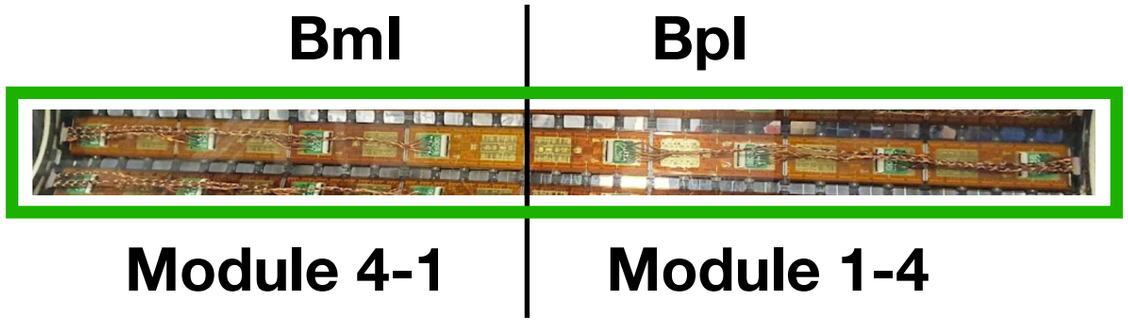


Modules on 4 layers and 8 sectors in each half-cylinder



Modules mounted on inward and outward facing sides of inner and outer **ladders**, partially overlapping in coverage

Each half-ladder has 4 modules

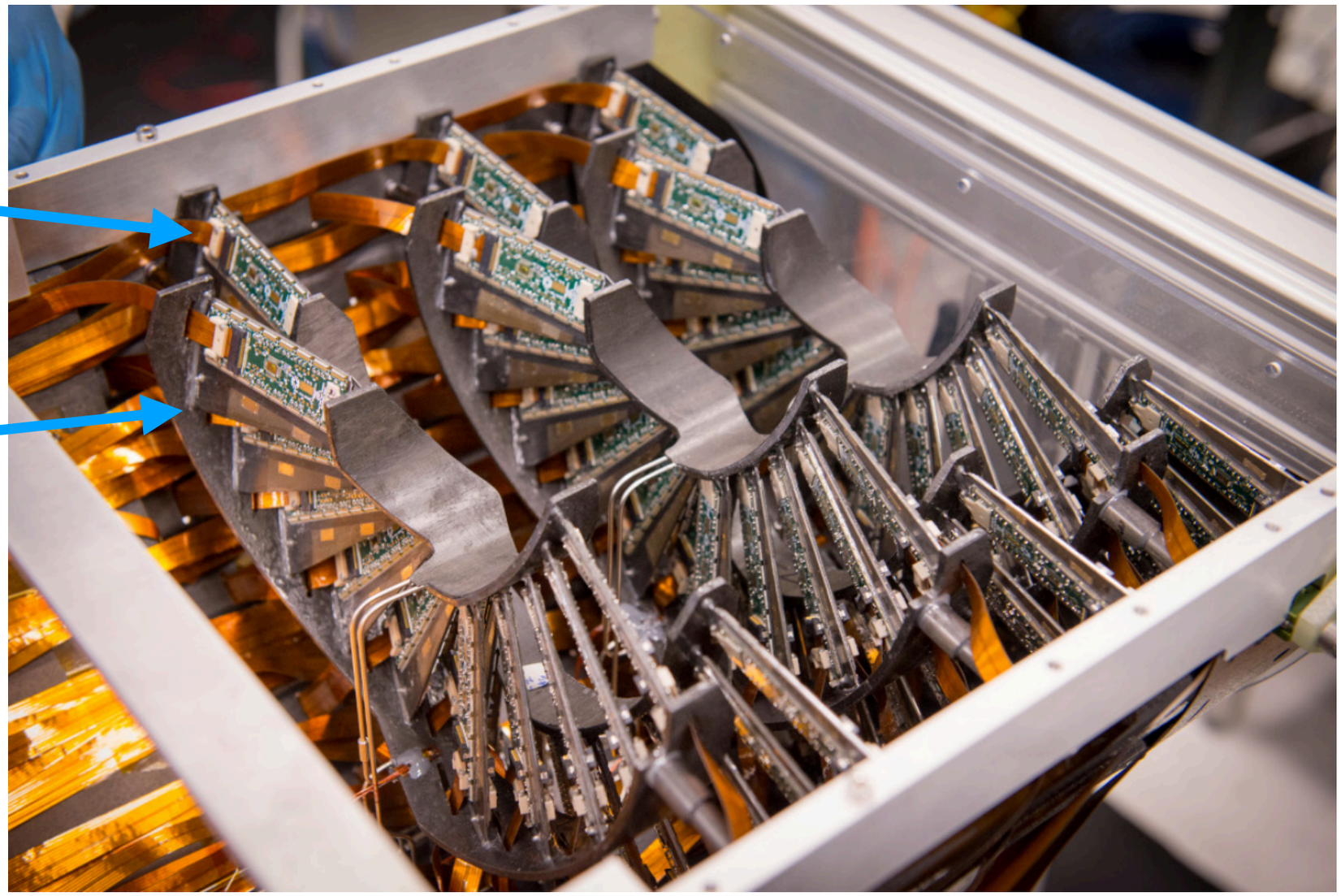


FPix modules

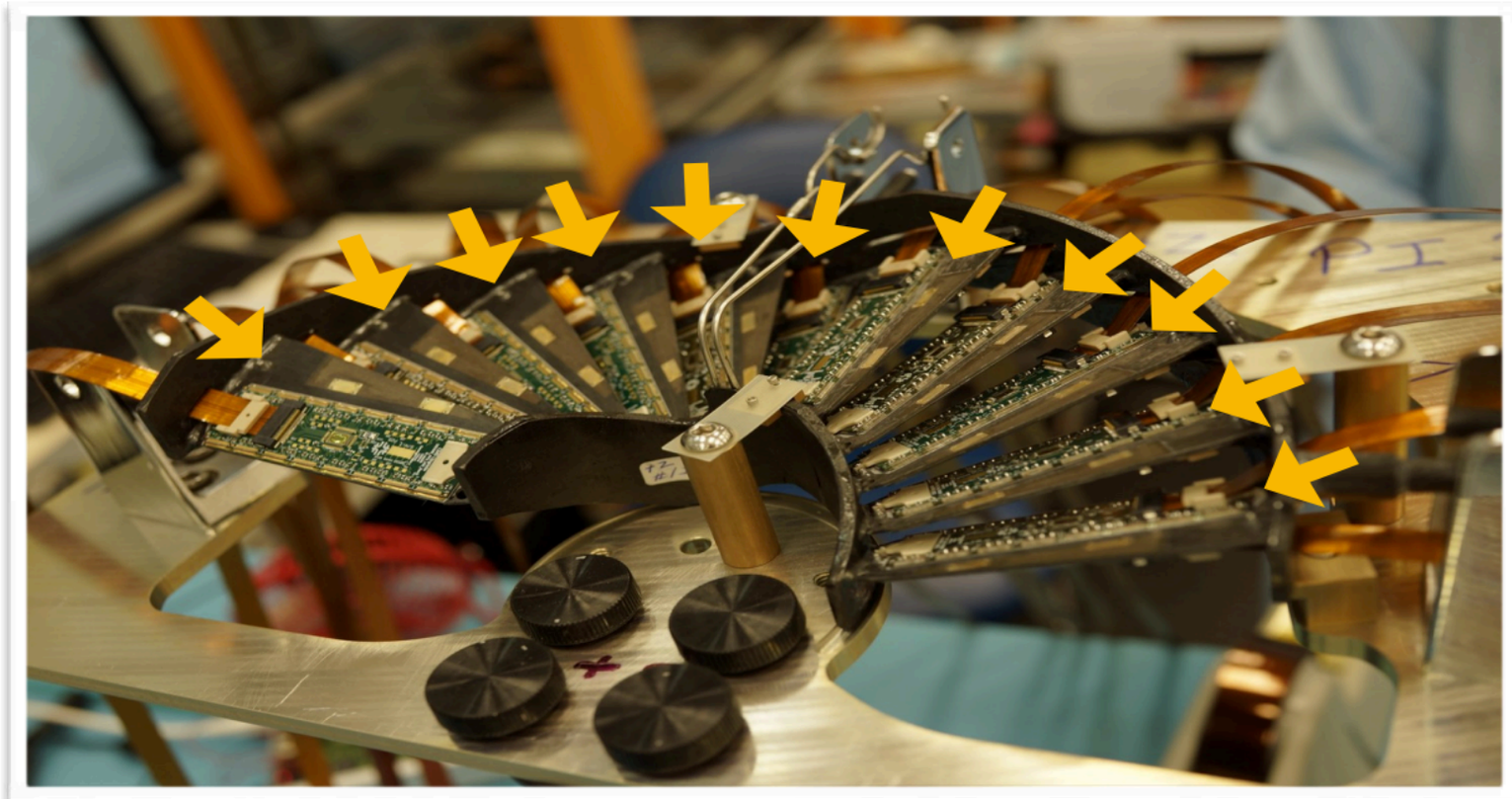
Modules on 3 inner and 3 outer half disks
in each half-cylinder

Large (outer) disk

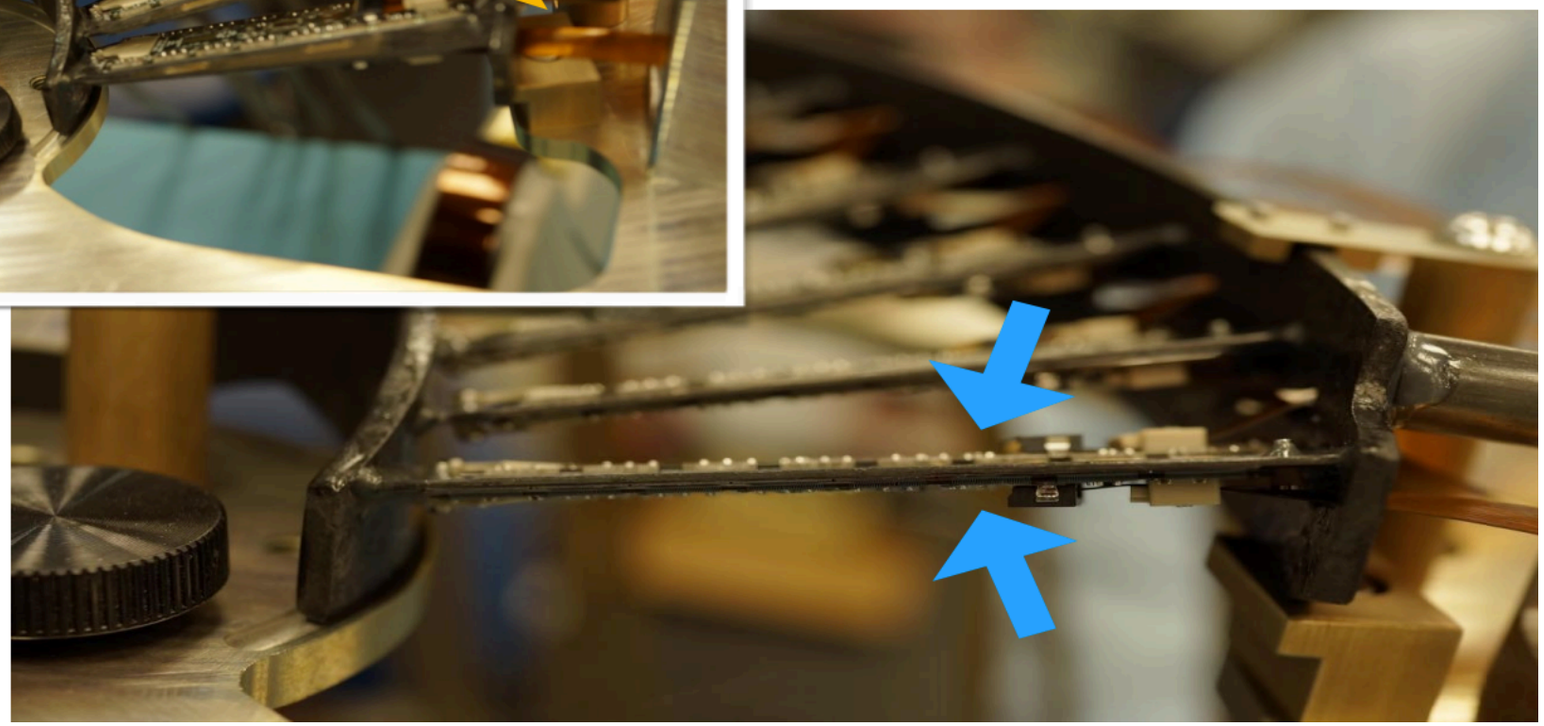
Small (inner) disk



FPix modules

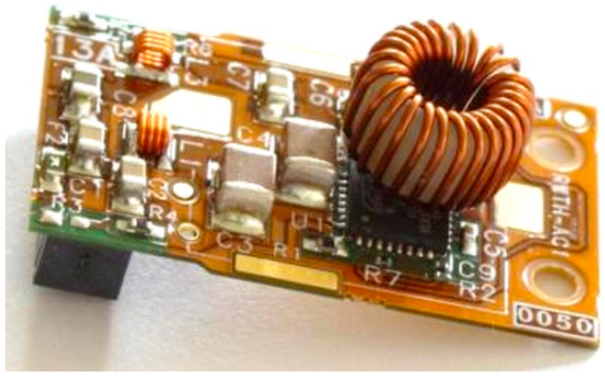


Inner and outer half disks consist of 11 and 17 **blades**, respectively



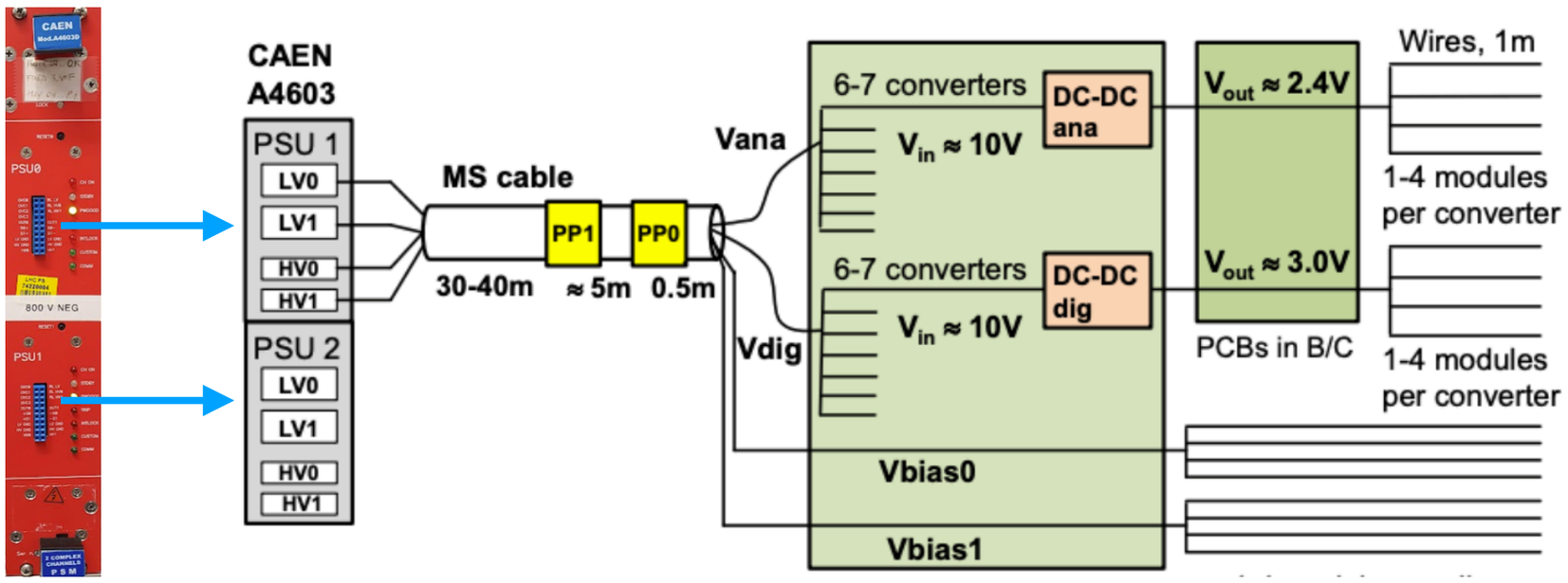
Each blade carries 2 **sensors**, 1 on each side and partially overlapping in coverage

Powering



- Powering concept based on **DC-DC conversion technique**
- **1216 DCDC converters with radiation tolerant FEAST v2.3 ASIC** receive input voltage of ~10V and convert it into output voltage of:
  - 2.4V for analog part of ROC
  - 3.3V (L1, L3, L4) and 3.5V (L2 and FPix) for TBM and digital part of ROC
- **1 pair of DC-DC converters delivers the analog and digital voltage**
  - placed roughly 1m away from the detector modules
  - connected in parallel to a power supply channel

Type	Required
2.4 V (= Analog)	608
3.3 V (=Digital, BPix)	320
3.5 V (=Digital, FPix & BPix L2)	288



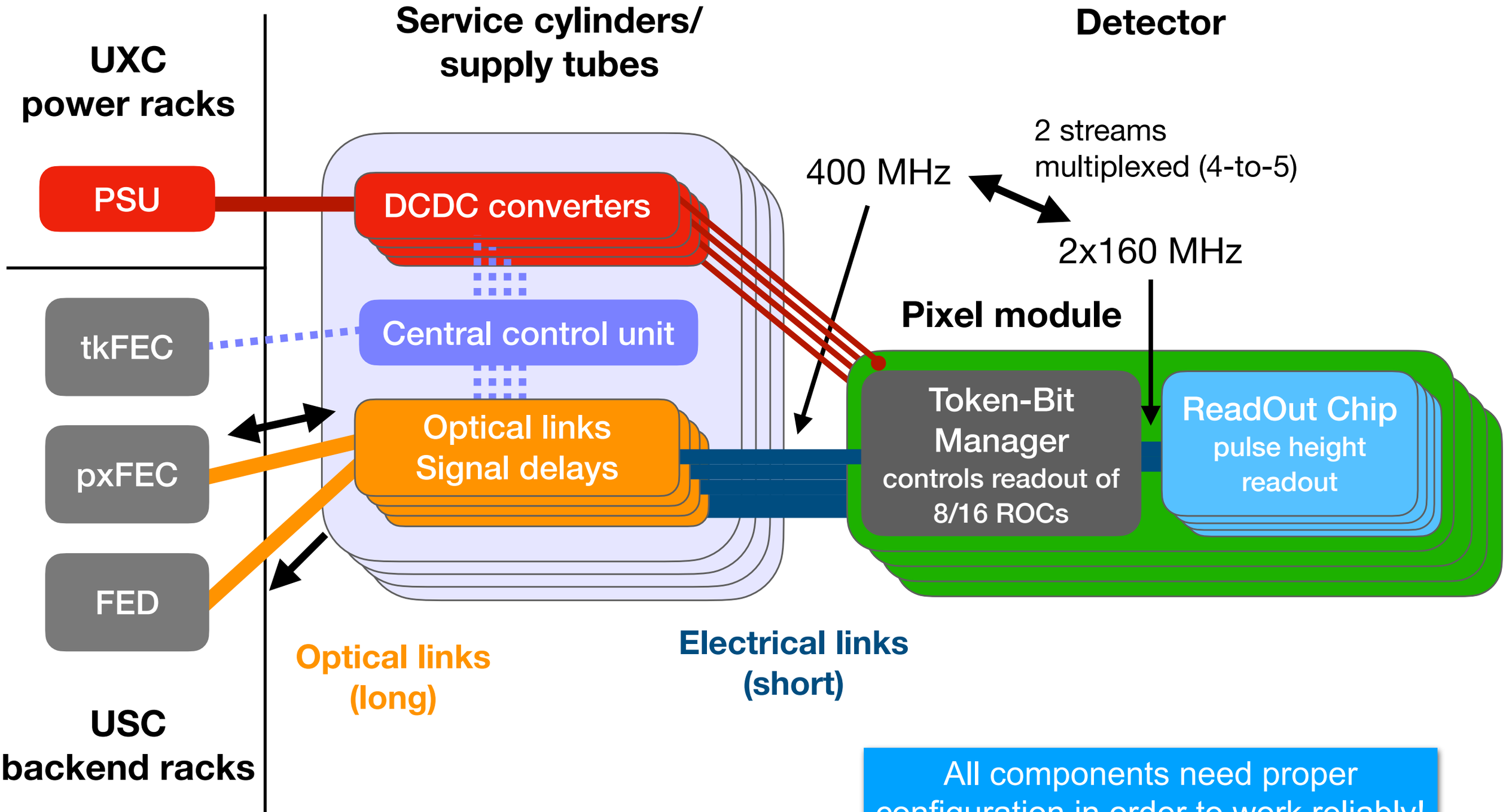
Different power requirements

- Low Voltage: Analog and Digital module power
- High Voltage: Sensor power
- Control Voltage: Auxiliary electronics power

PSU = Power Supply Unit
MS cable = Multi-Service cable
PP1 = Patch Panel 1

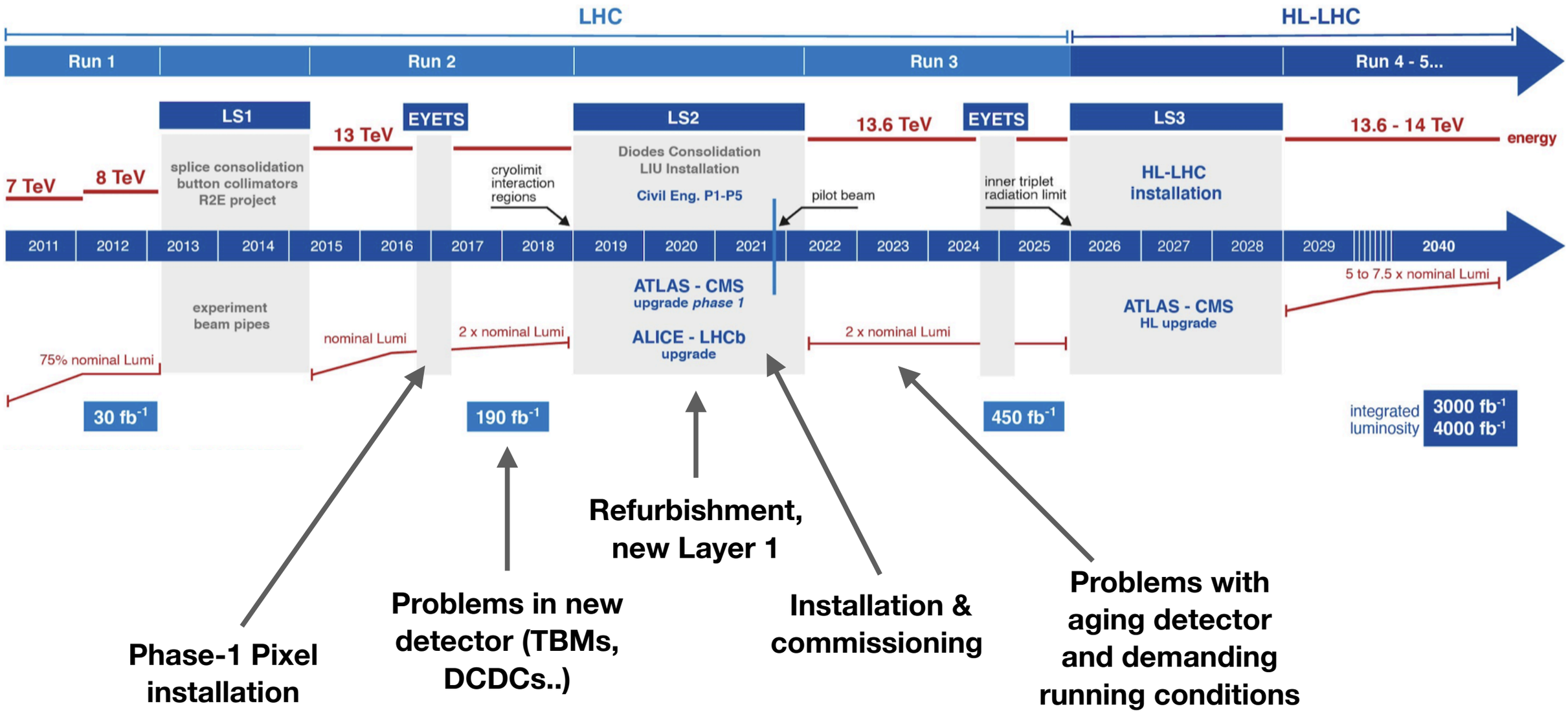
Signal path

FEC = Front-end Controller
FED = Front-end Driver
USC = Underground Service Cavern
UXC = Underground Experimental Cavern



All components need proper configuration in order to work reliably!

LHC schedule



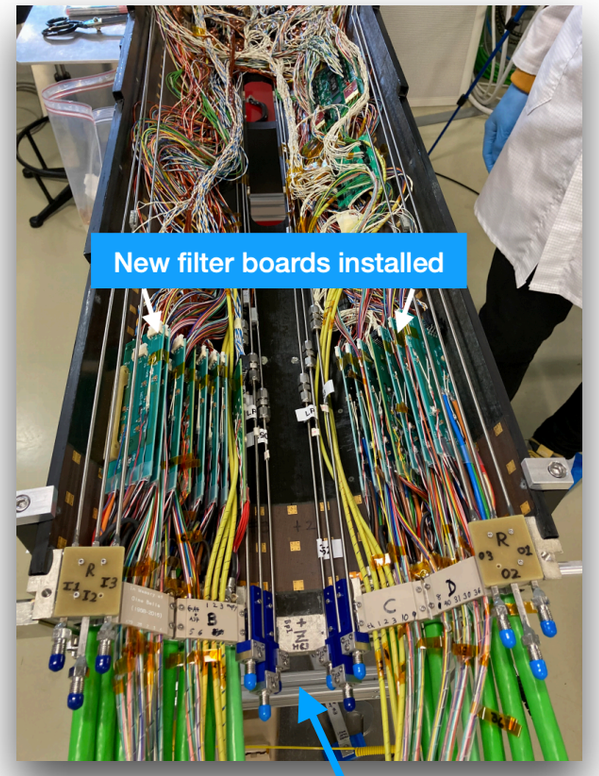
- **Pixel detector is the closest detector to the interaction point so irradiation is very high**
  - components are damaged by radiation so refurbishment/upgrade work needed during Long Shutdowns

Activities during LS2

- **Detector was extracted from underground cavern** at the end of Run 2 (early 2019)
  - **kept cold and dry** in boxes to protect the silicon sensors

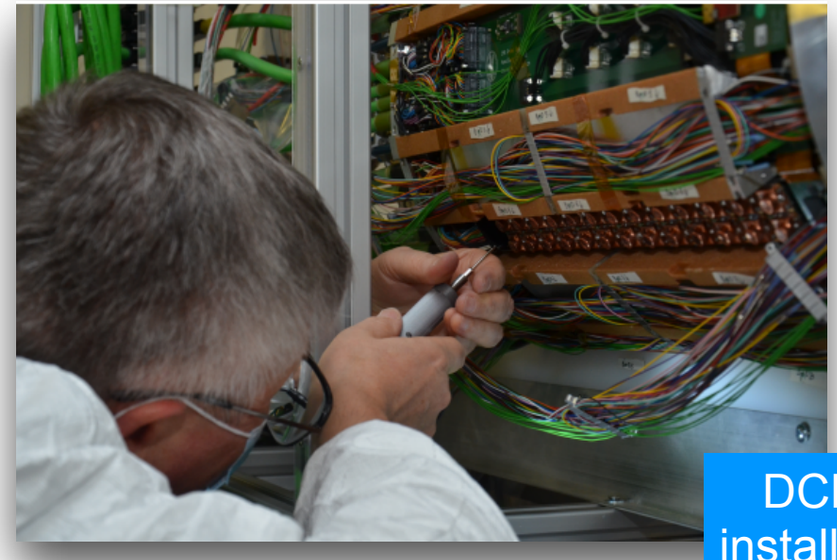
- **Refurbishment work during Long Shutdown 2 (LS2):**
  - installed new Layer 1
  - replaced (accessible) Layer 2 DCDC-damaged modules
  - installed new DCDC converters in both BPix and FPix
  - consolidated FPix CO_2 cooling connection
  - replaced FPix filter boards for better HV granularity

1/4 FPix in cold box



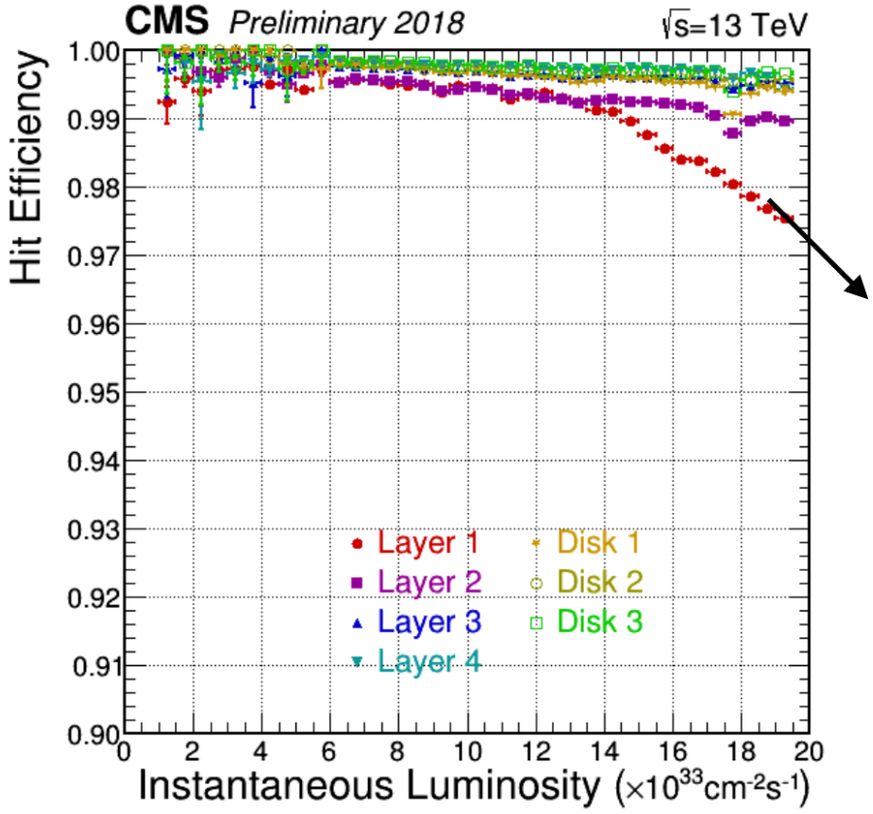
New cooling inlets


Layer 1 cabling

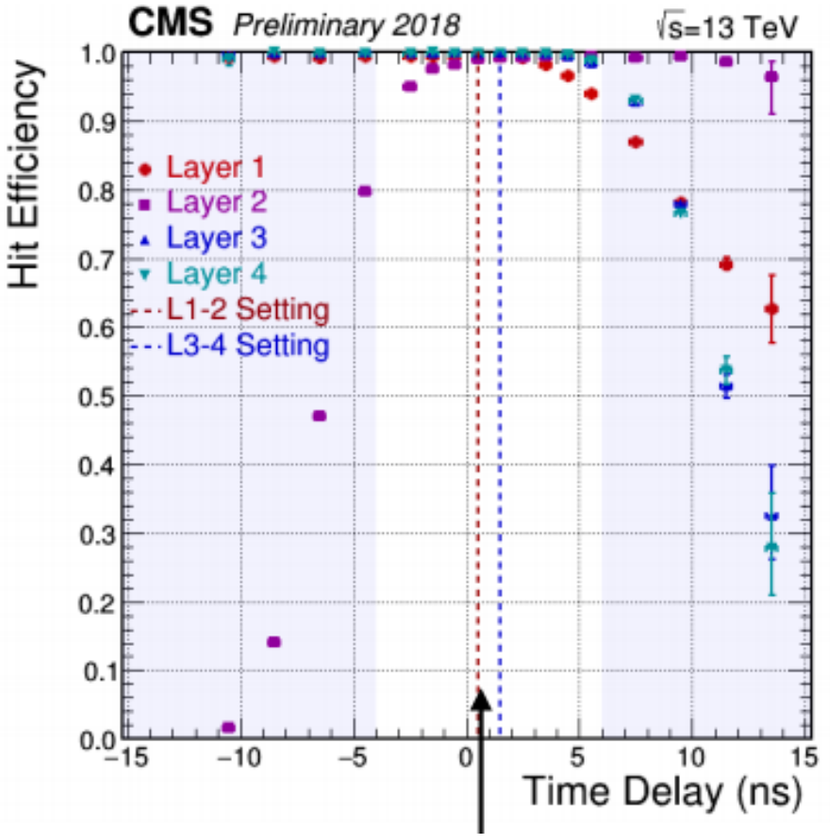

DCDC installation

New Layer 1

- We needed a new Layer 1 after Run 2 so we made it better!
- **New readout chip (PROC600v4)**
  - fix dynamic inefficiency issue & reduce crosstalk noise
- **New Token-Bit-Manager (TBM10d)** with delay and power reset option
- **New HDI design** to eliminate HV issues



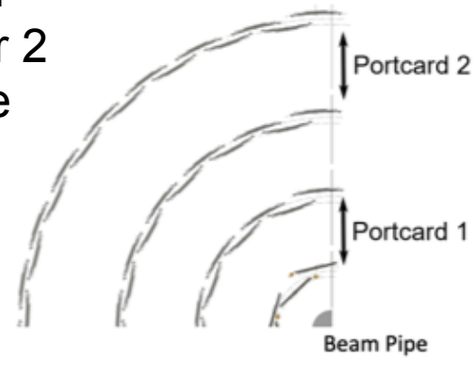
Dynamic inefficiency addressed in new ROC



Optimal range very narrow and efficiency on the edge for Layer 1+2

New TBM10d allows a relative delay of Layer 1 w.r.t. Layer 2

In old modules, 1 common setting for Layer 1 and Layer 2 because they shared same delay chip (portcard)



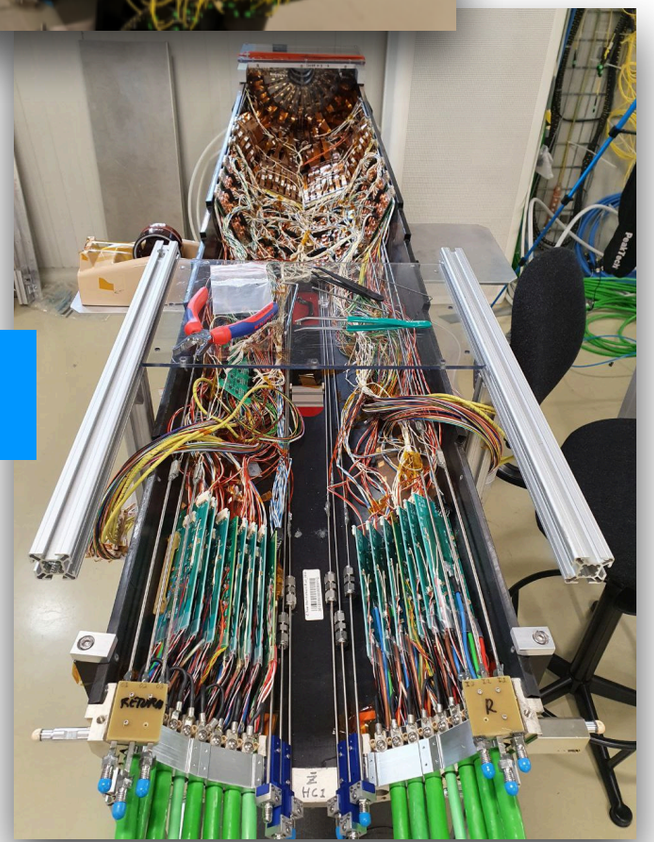
Tests before installation

- **BPix:**
  - **Hardware intervention completed** in March 2021
  - **Warm and cold tests in clean room completed** by the end of April 2021
  - Few connection related issues were taken care of
  - **No major issues, modules in good shape**

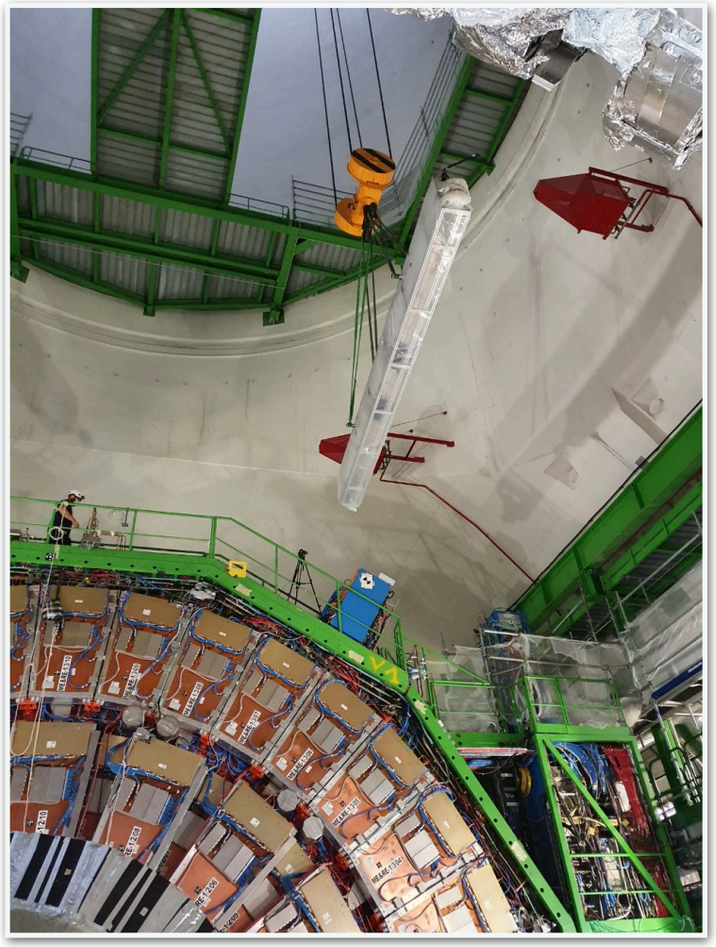
- **FPix:**
  - **Fully repaired and cold tested** in the clean room by the end of April 2021
  - No powering or cooling related issues observed after the repair work
  - One faulty filter board was replaced
  - **Modules in good condition, no new problems**

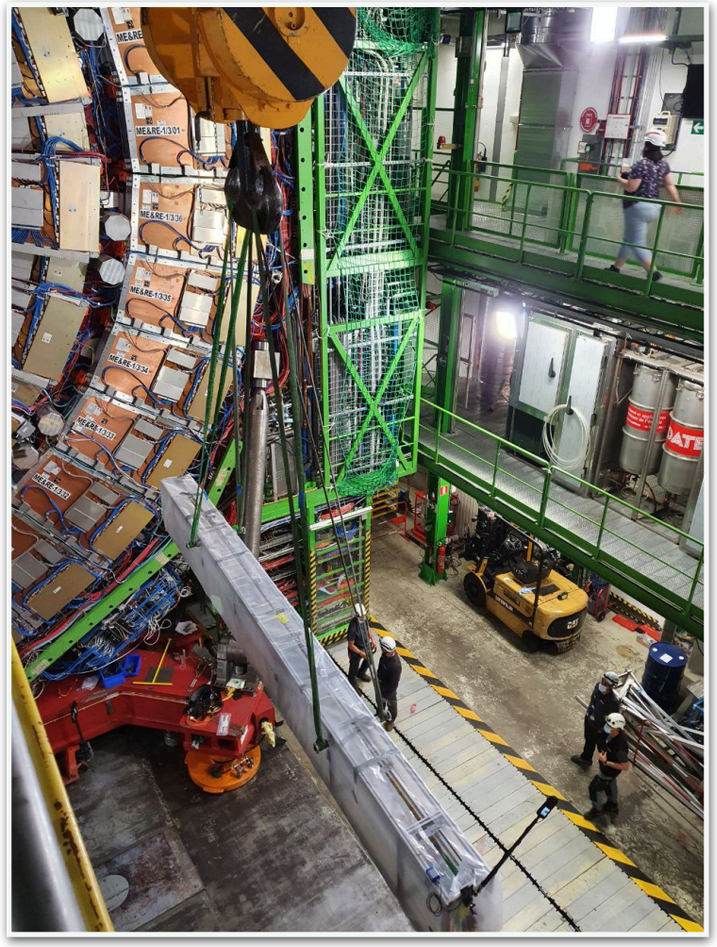
Cold box under test

1/4 FPix completed

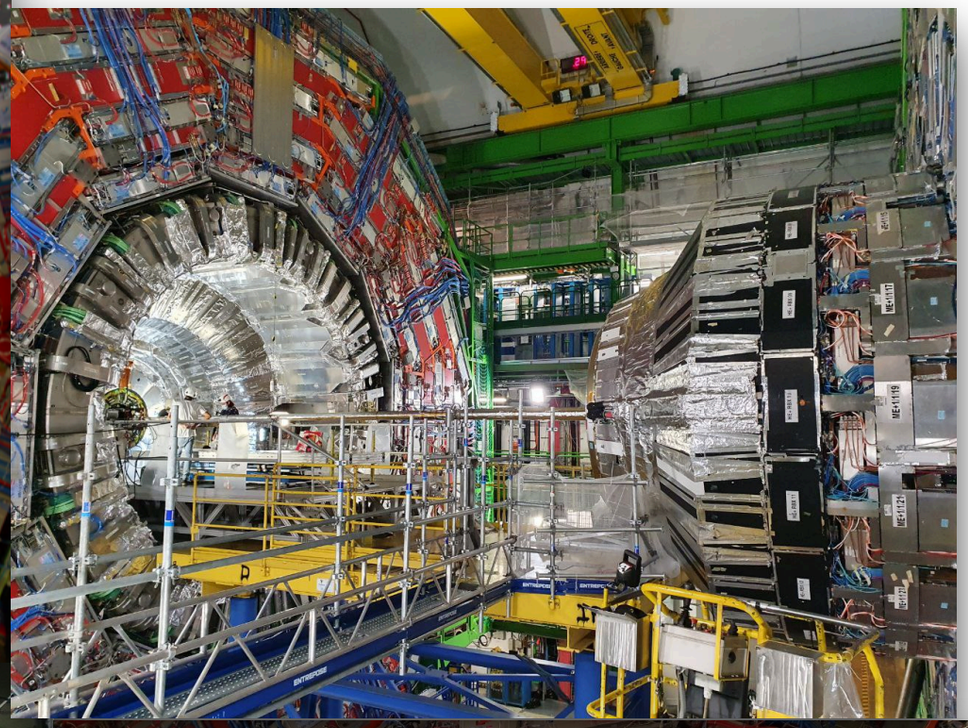


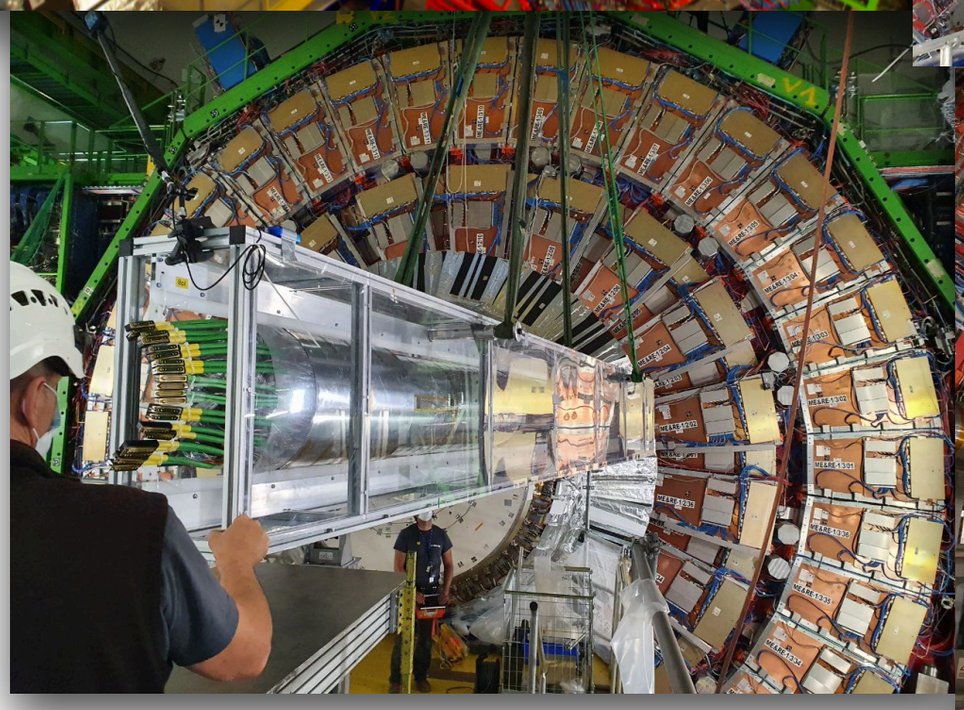
From surface to underground





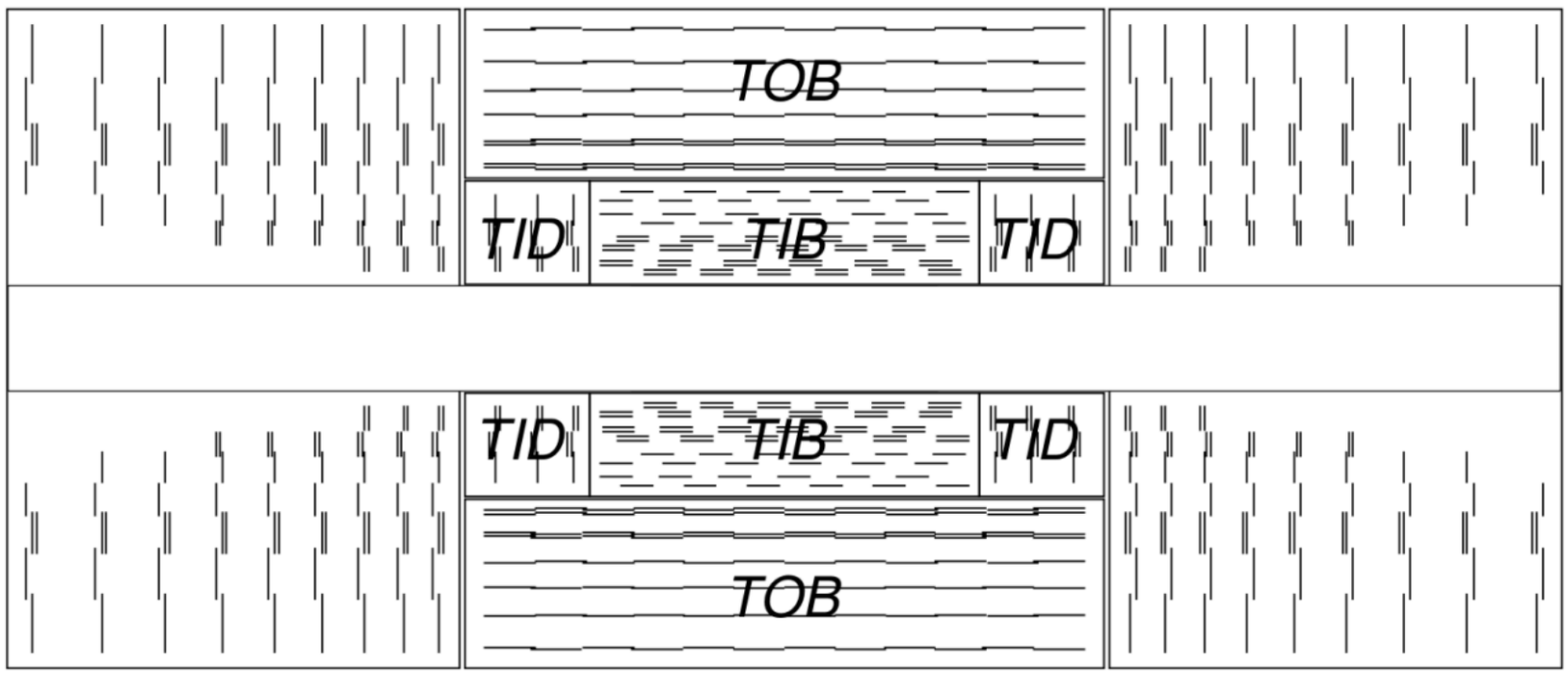
In the cavern





Pixel installation sequence

- **BPix is installed first:**
  - in two detector halves, both about 6 m long



Pixel installation sequence

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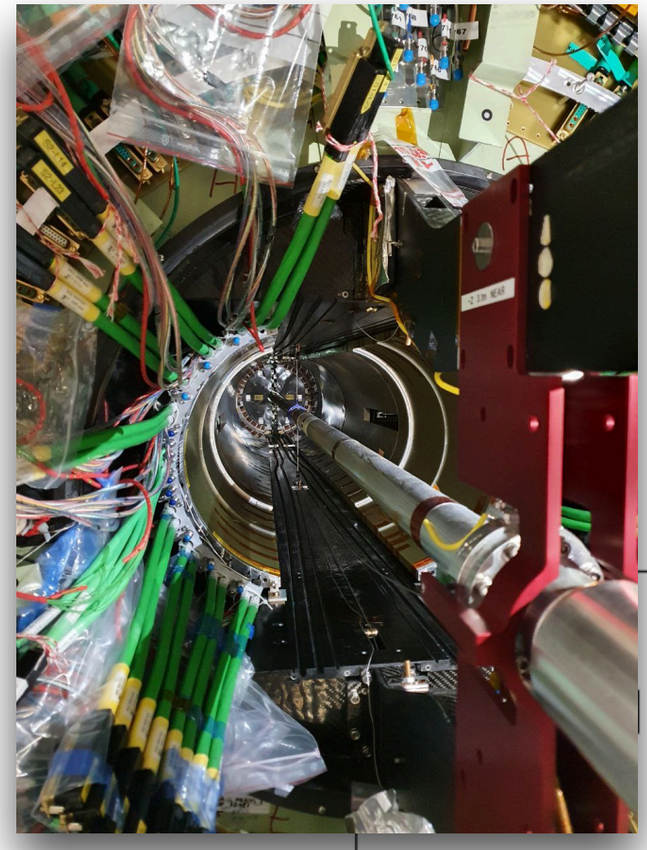
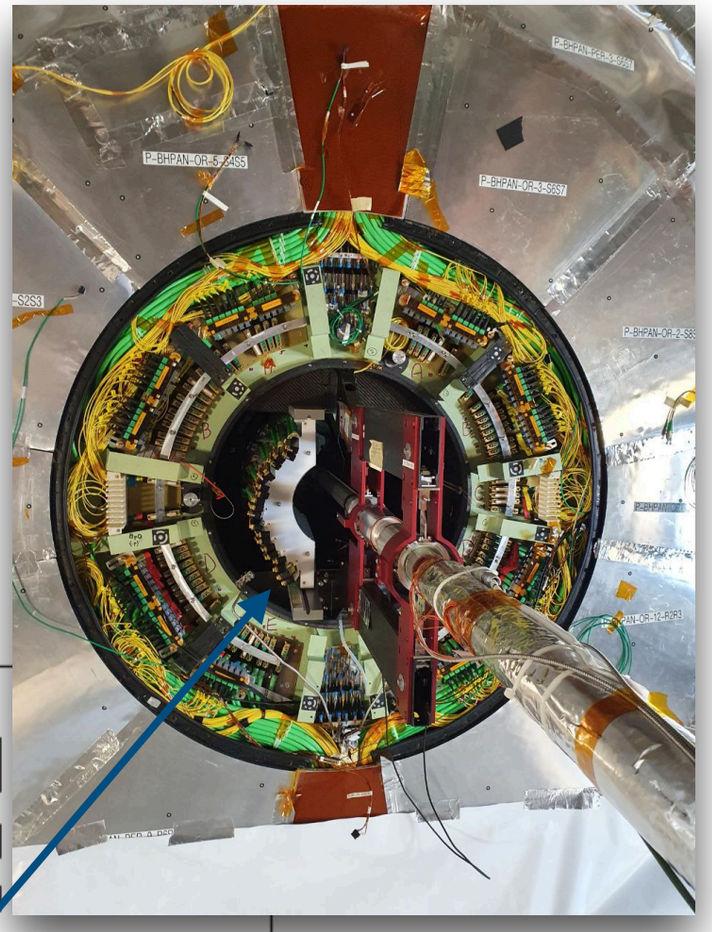
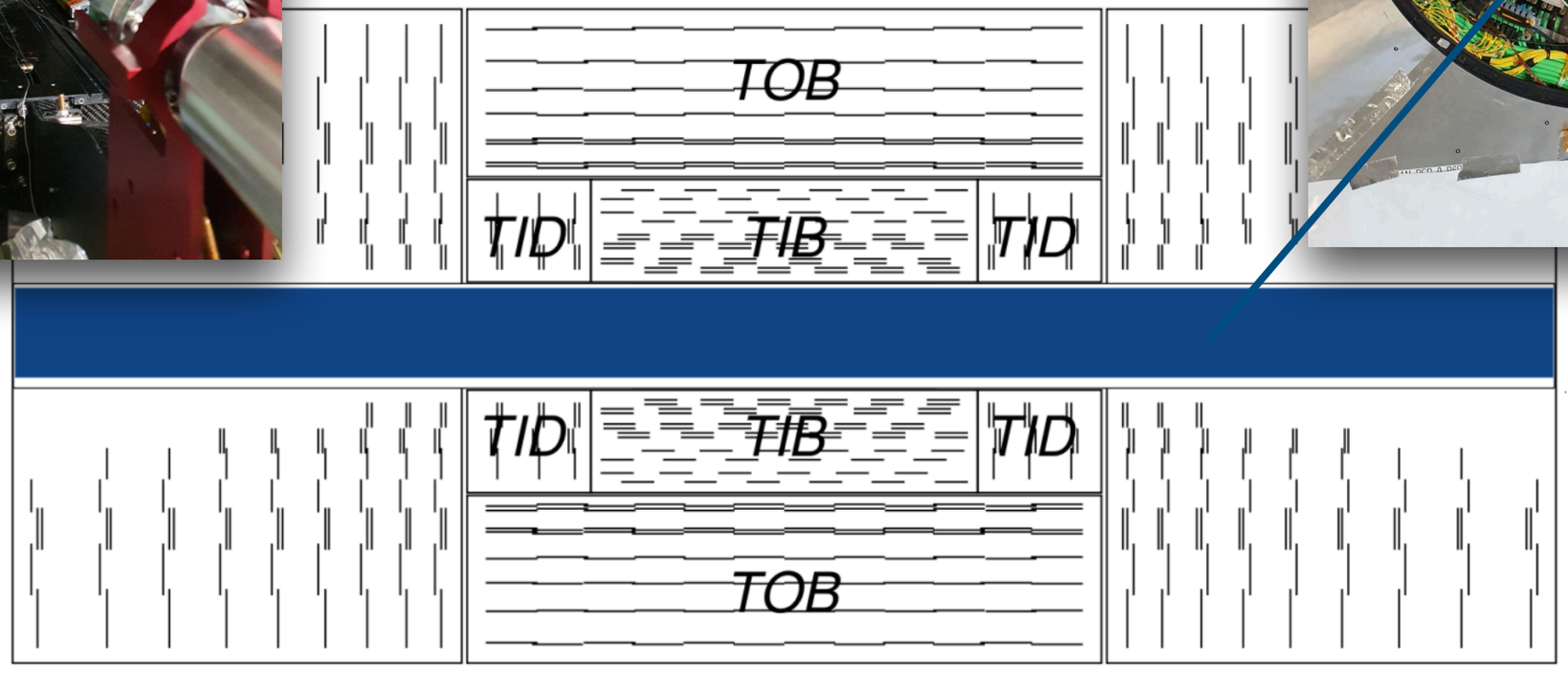


BPIX insertion with supply tube
(2 pieces)

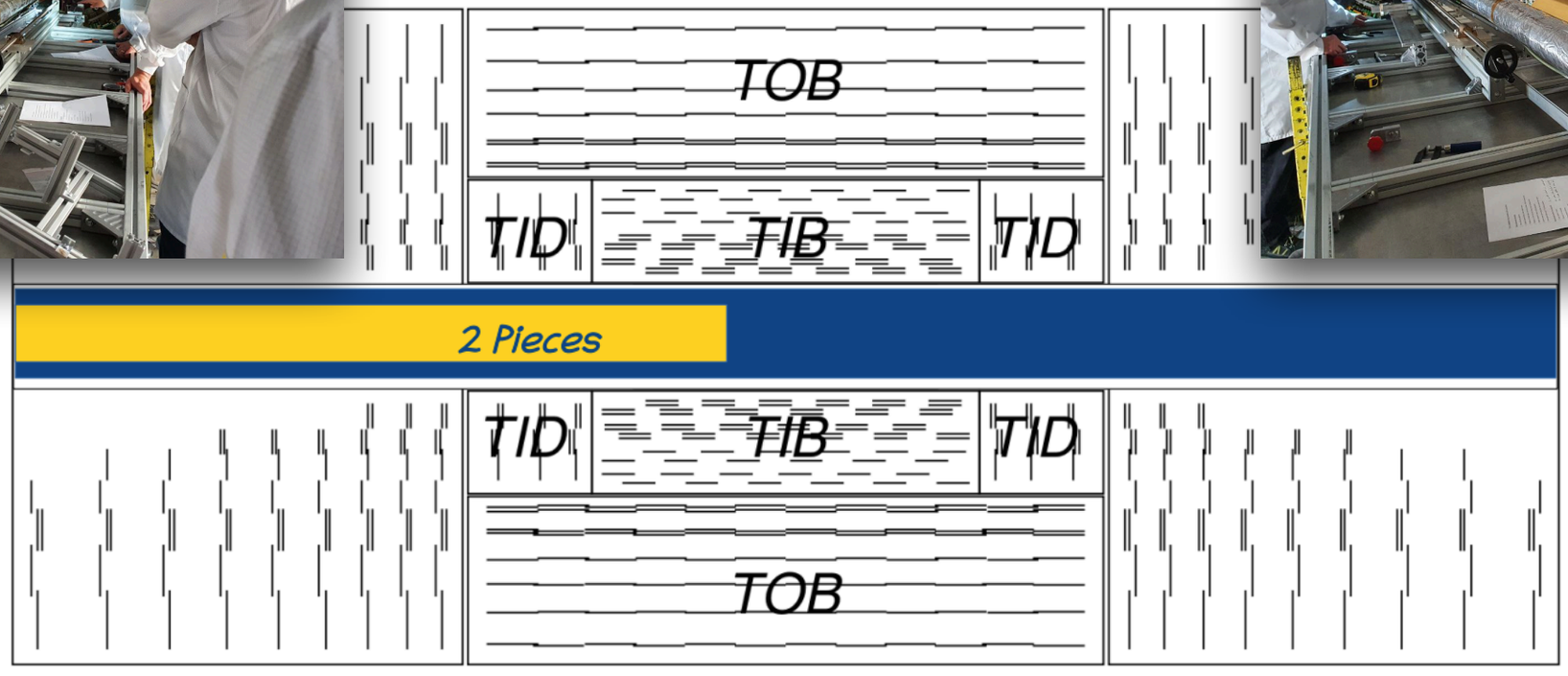




Pixel installation sequence

- **BPix is installed first:**
  - in two detector halves, both about 6 m long
- **FPIX is installed next:**
  - in four half-cylinders, all about 2.5 m long
  - first one end, then the other

FPix insertion with service cylinders
(4 pieces, 2 per end)



Pixel installation sequence

- **BPix is installed first:**
  - in two detector halves, both about 6 m long
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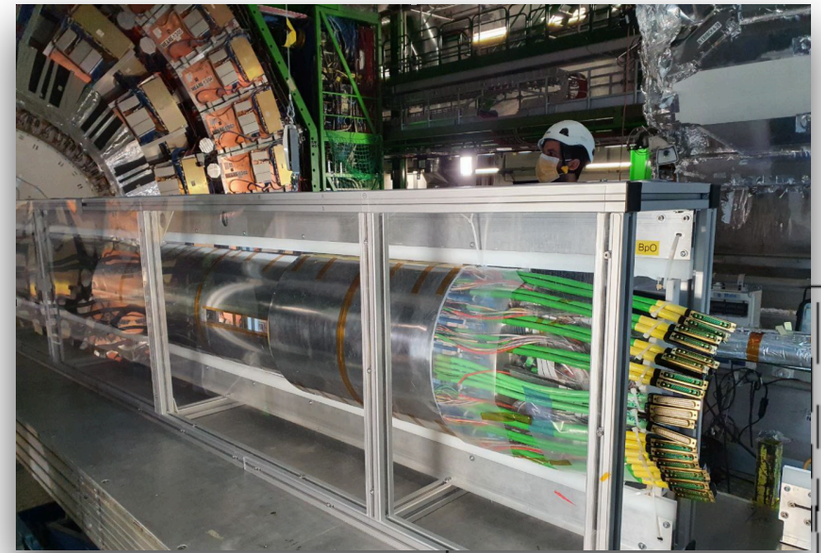
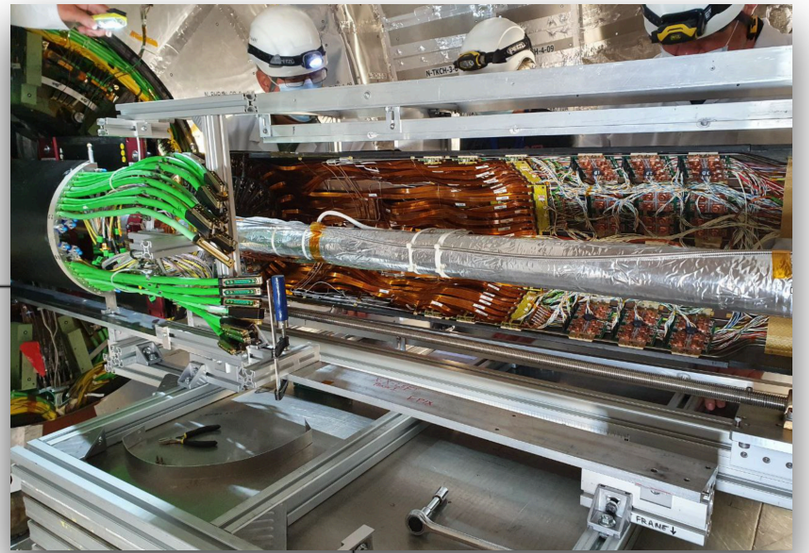
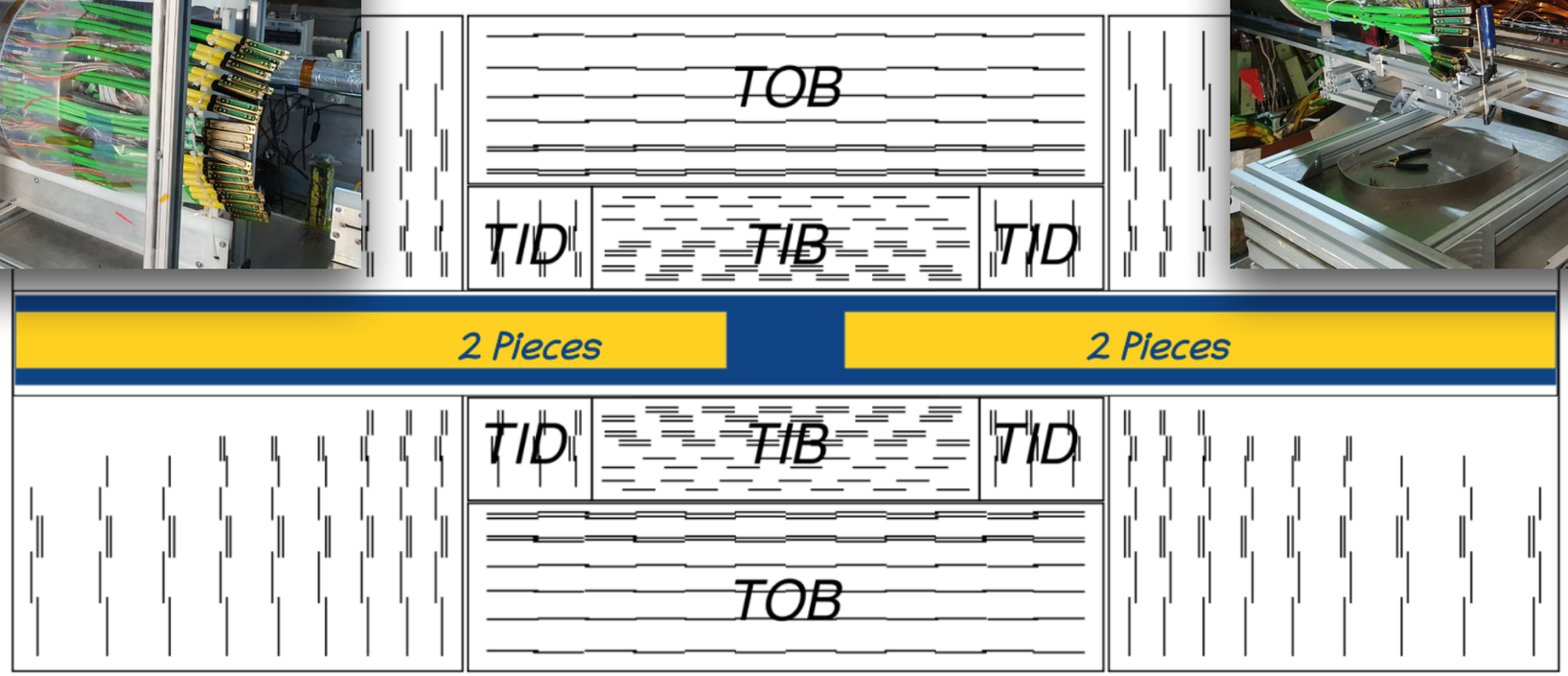


FPix insertion with service cylinders
(4 pieces, 2 per end)





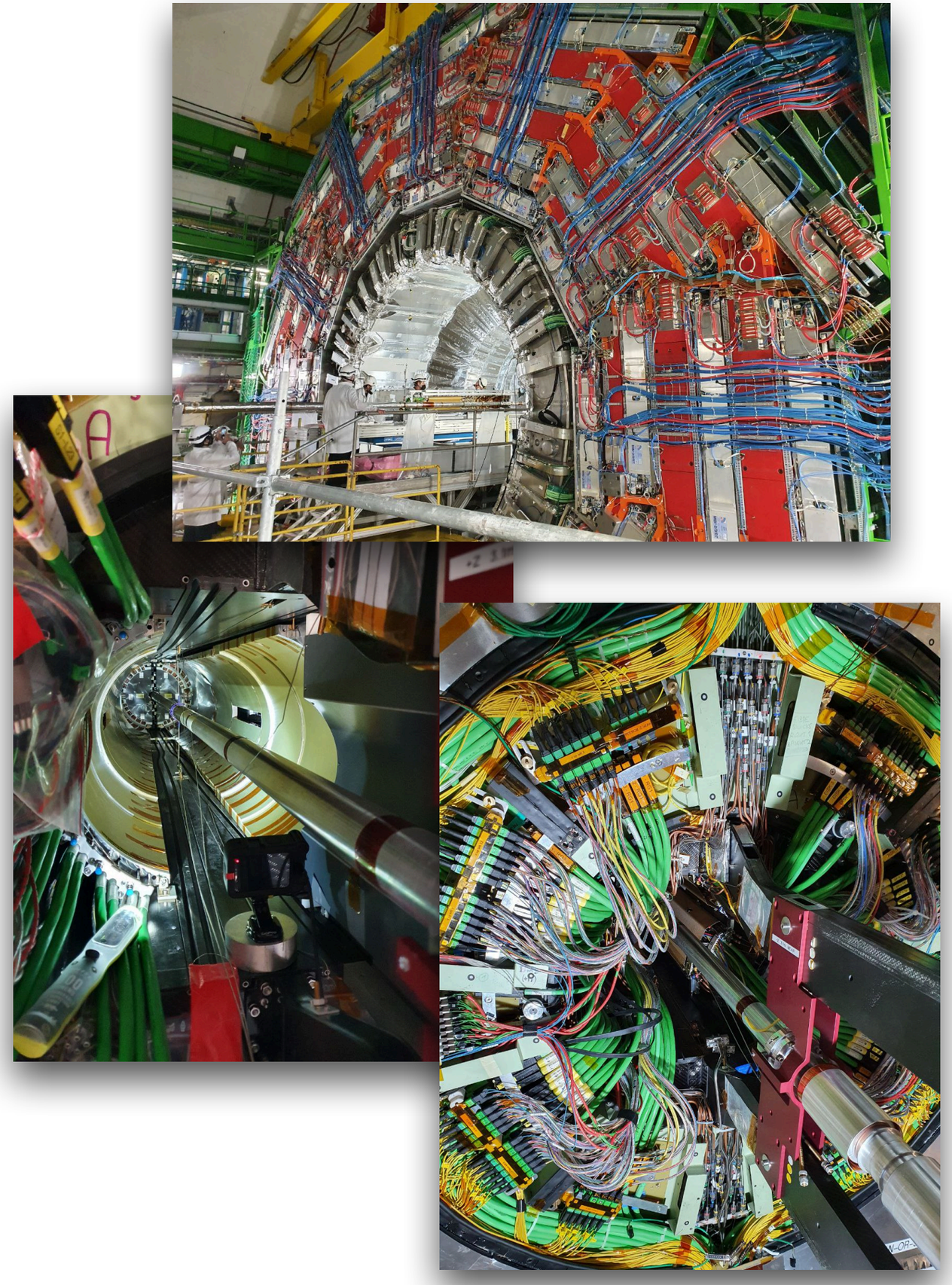
Installation

- **Detector installed inside the cavern at the end of June 2021**
  - cooling connection and leak test
  - pressure test for new Layer 1 lines
  - power and readout connections
  - CO_2 flow established at +17 degC

  → very smooth installation

- **Detector fully commissioned after installation**
  - warm (+17 degC) and cold (-20 degC) checkout with full calibration cycle
  - no new problems observed after installation (compared to lab checkout)
  - only minor power supply glitches

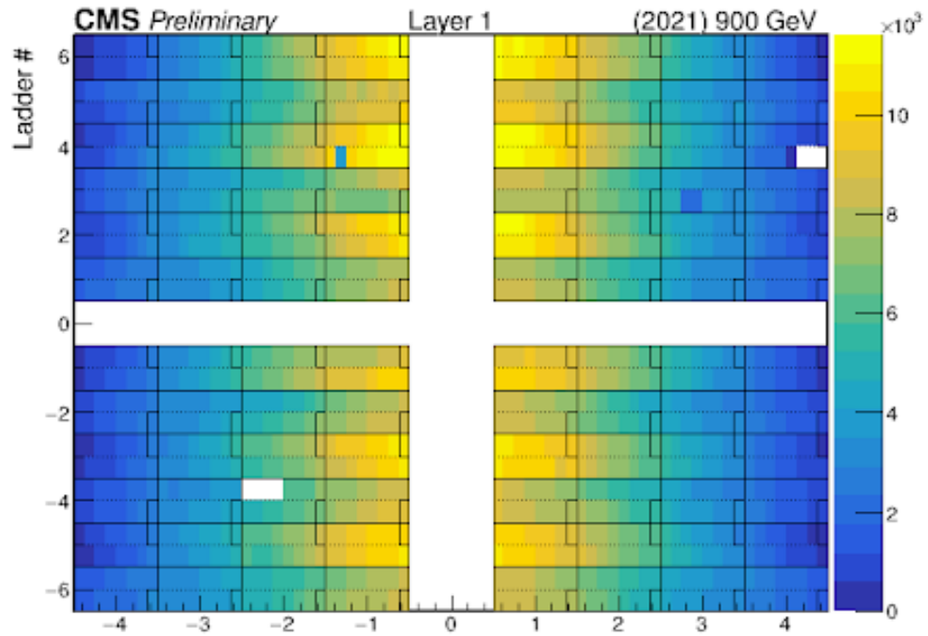
  → detector in good state

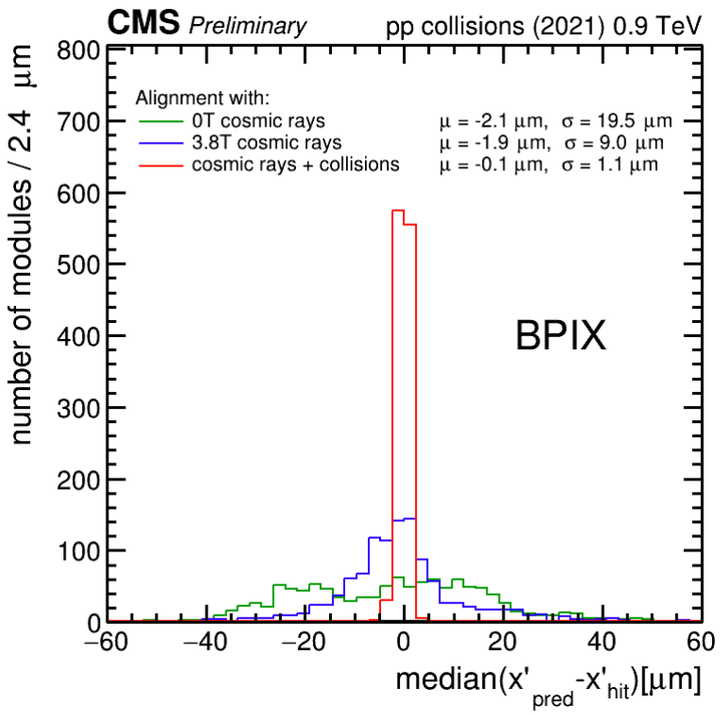


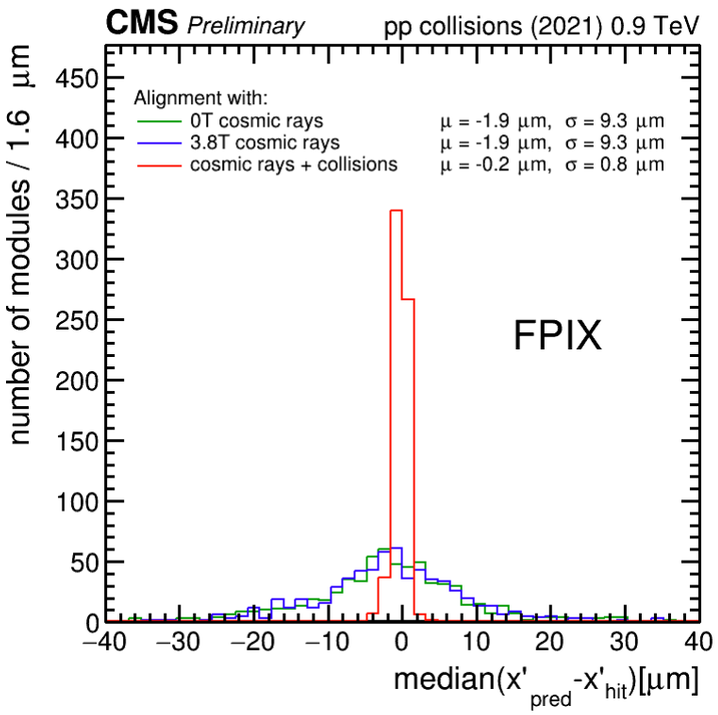
Commissioning

- **Stable beams in October 2021.. after almost 3 years!**
  - very stable operation from Pixel detector
  - detector newly realigned after installation - improved residuals with collisions data
- **Standard commissioning checks and tuning performed in February-March 2022**
  - threshold and pulse height optimization, tuning of unstable modules, masking of noisy pixels, ...

→ detector optimally calibrated and ready for Run 3



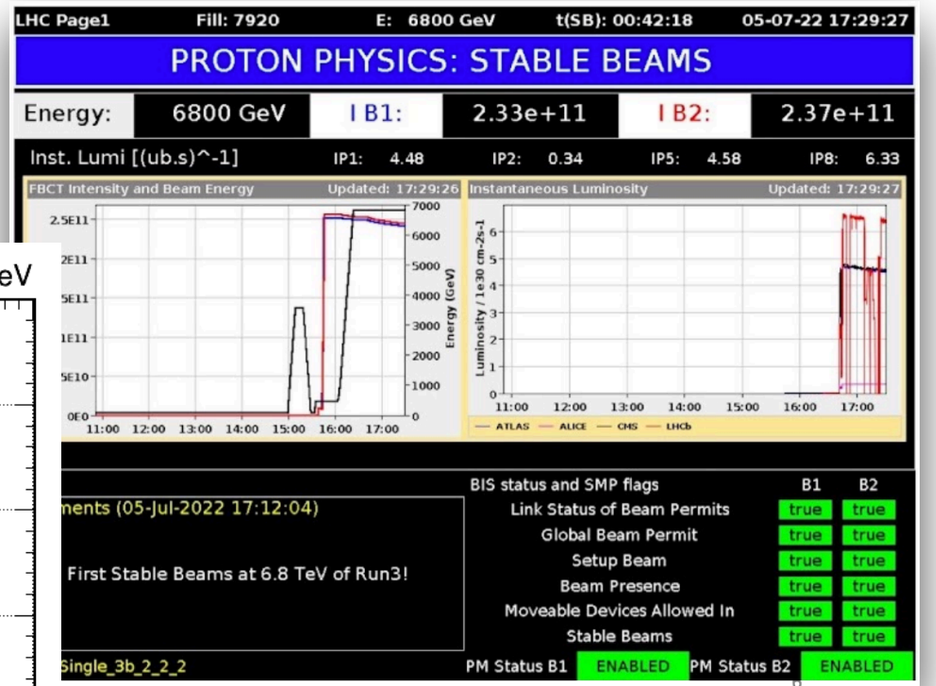


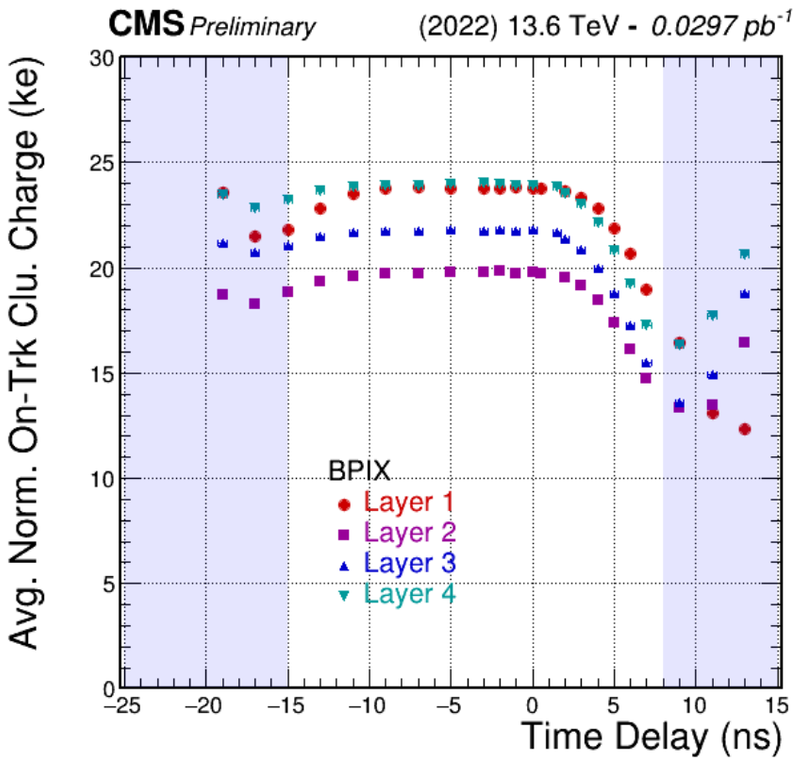


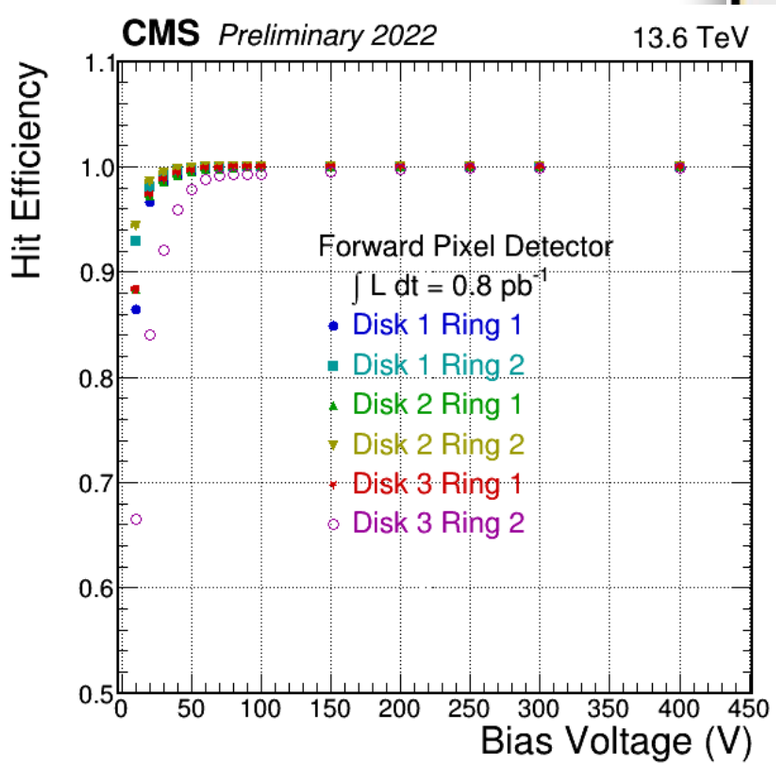
First Run 3 collisions @13.6 TeV

- **Pixel successfully participated in the first 13.6 TeV stable beams on July 5th 2022**
  - **collected good data quality!**

- **Performed a full timing scan and a full HV bias scan on July 5th-6th 2022**
  - new TBM feature used to set a relative delay between Layer 1 and Layer 2
  - **optimal delay and HV settings found for full detector**







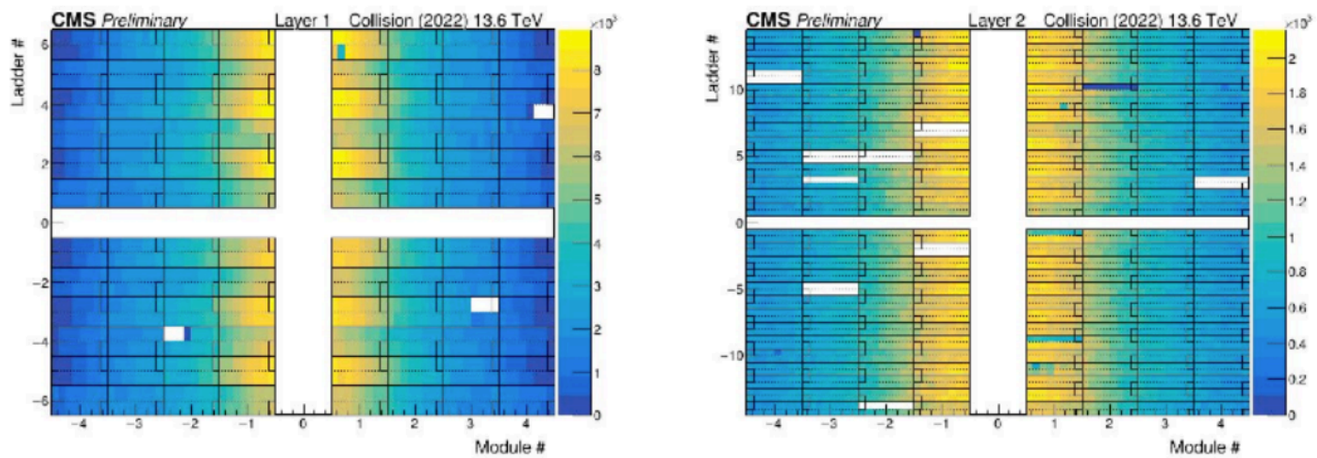
Active Detector Fraction

- **Occupancy plots with bad components = non-functional readout chips (ROCs) masked at detector level**
  - **BPix: 316 ROCs (1.6% of BPix)**
    - end of 2022: 300 ROCs
    - after installation: 168 ROCs
    - end of Run2: 1068 ROCs
  - **FPix: 224 ROCs (2.1% of FPix)**
    - end of 2022: 218 ROCs
    - after installation: 162 ROCs
    - end of Run2: 184 ROCs

- **Temporarily bad components are also visible, as well as fractionally damaged ROCs (components with partially lower occupancy)**

Fraction of alive channels:
consistent with 2022,
slightly worse w.r.t. 2021 (after installation),
improved w.r.t. end of Run 2 for BPix

BPix ~ 98.4%



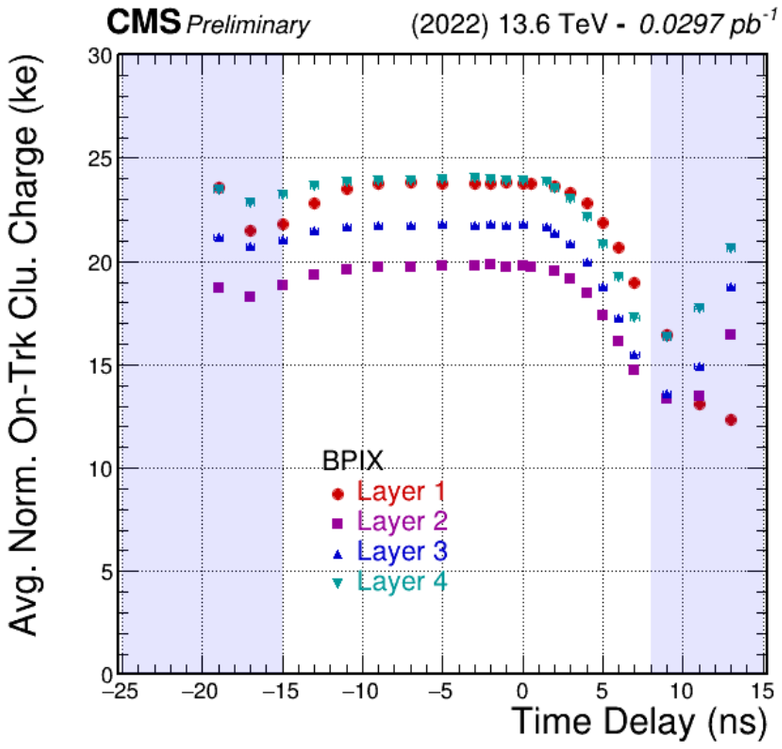
FPix ~ 97.9%

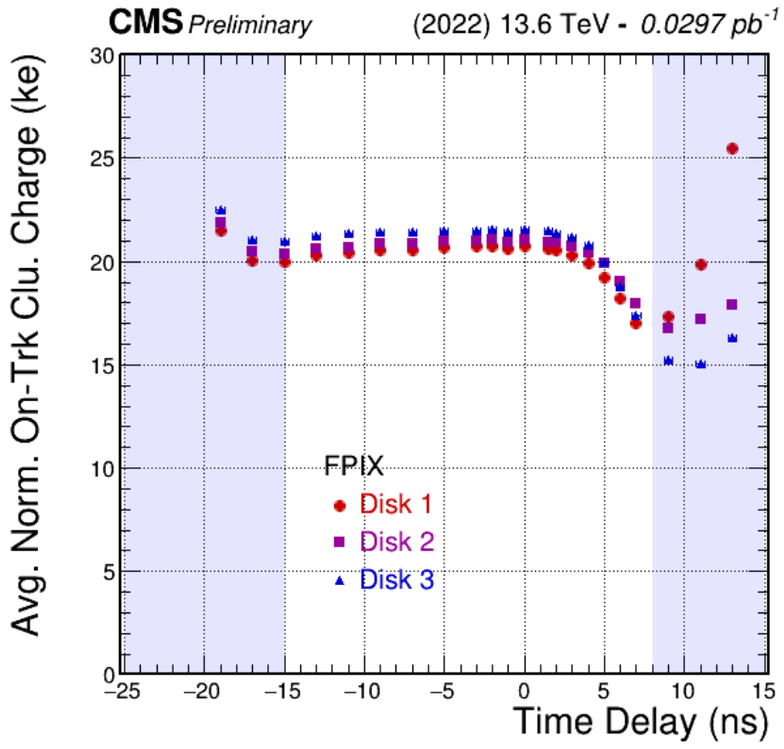
Timing scan

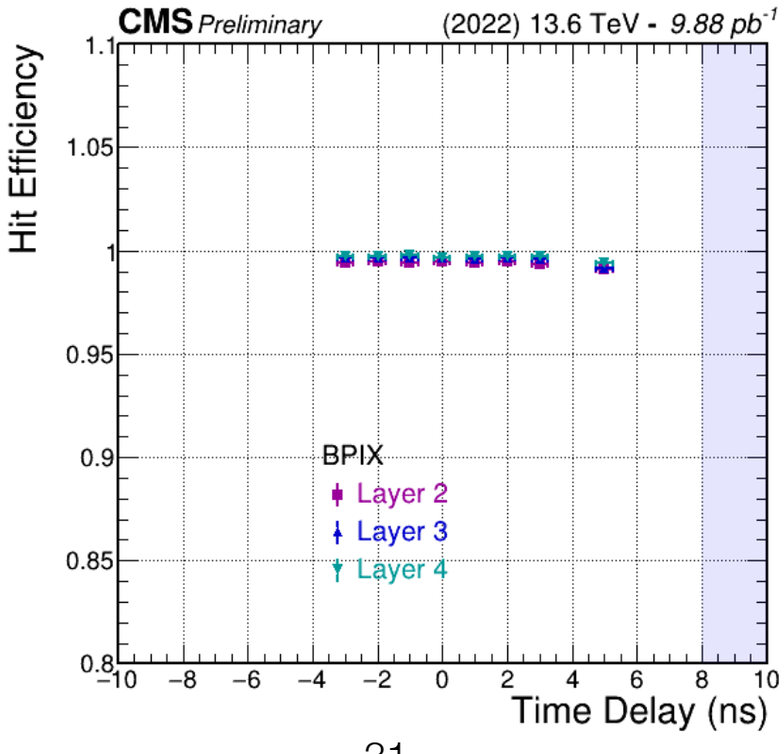
- **Timing scan done to ensure that the correct hits are read out and to find the best delays such that we have a uniform response from the detector**
  - the pixel detector is read out on receipt of a Level-1 Accept (L1A) signal
  - not accounting the delays properly could result in mismatch between L1A and bunch crossing!

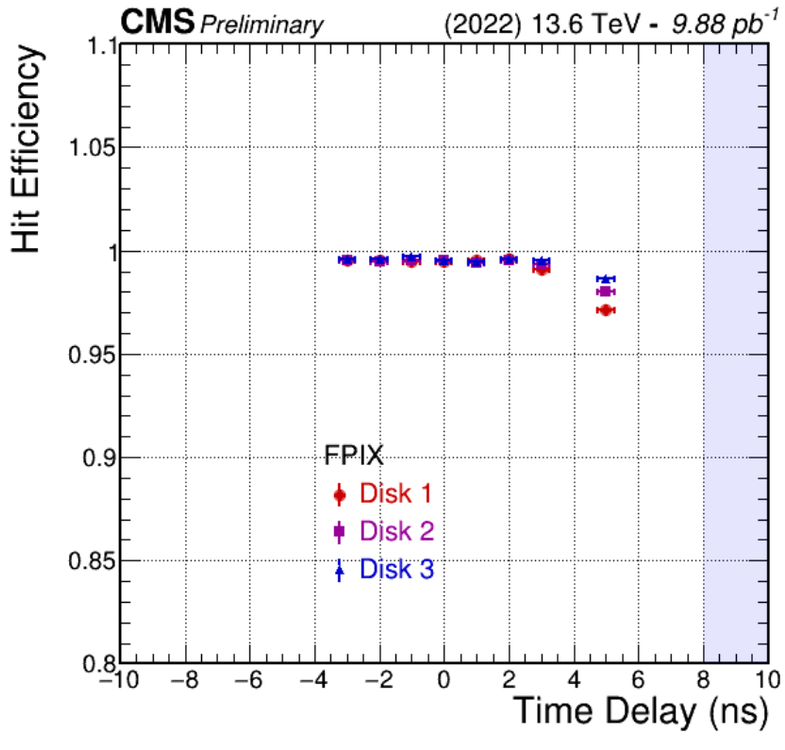
- Mini-timing scan performed to verify that **applied timing settings are correct**
  - 2023 delay settings in line with what observed in 2022

trigger delay = delay between the bunch-crossings and when the L1A arrives to the pixel ROCs









Cluster charge

- **Cluster properties are good** and comparable to Run 2 performance
- On-track cluster charge consistent across detector
- Cluster charge measured as function of bias voltage to monitor the evolution of the silicon bulk due to radiation

Operational voltages

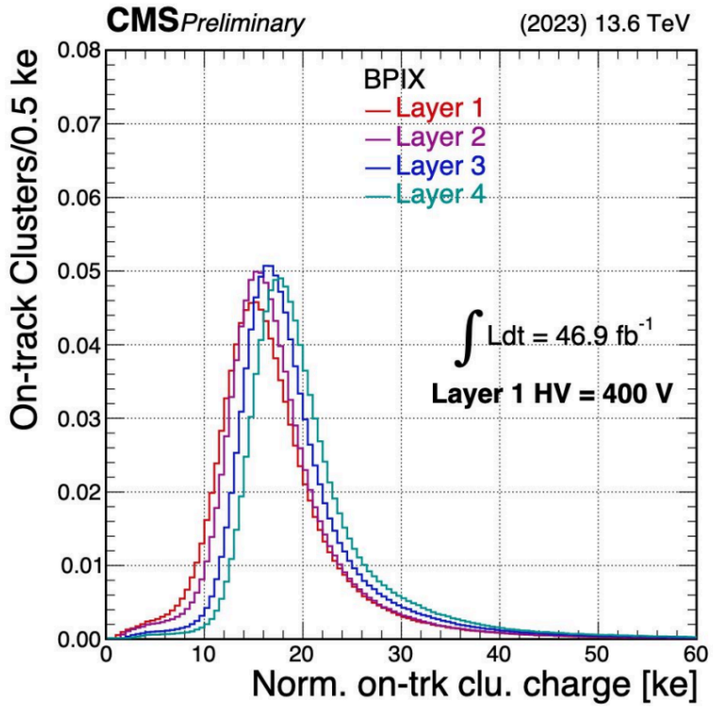
Layer 1: 450 V

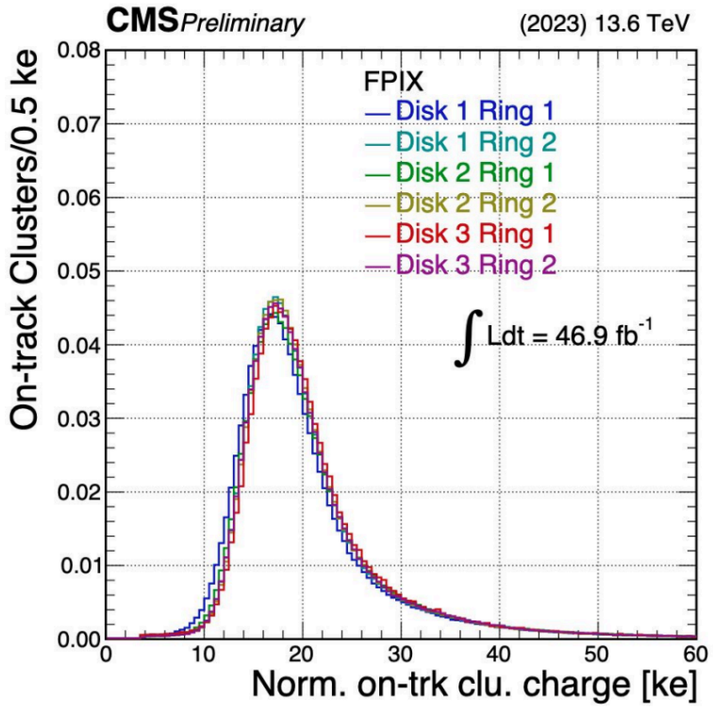
Layer 2: 350 V

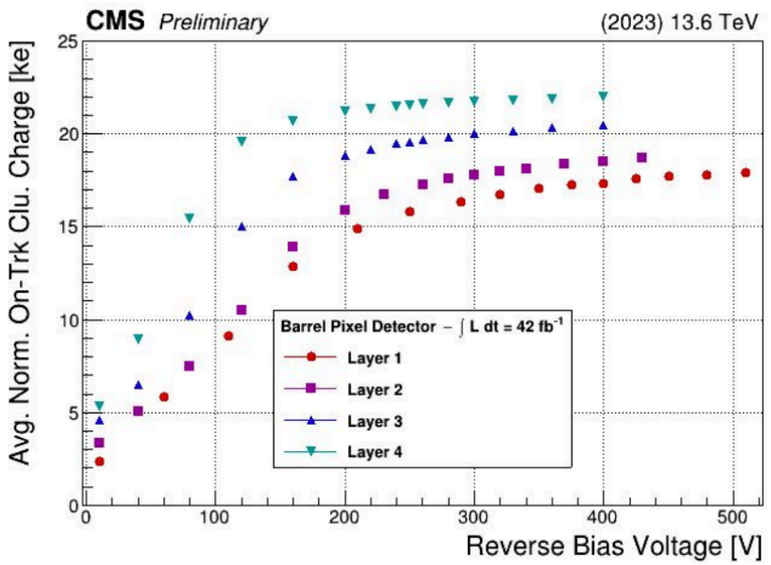
Layer 3 & 4: 250 V

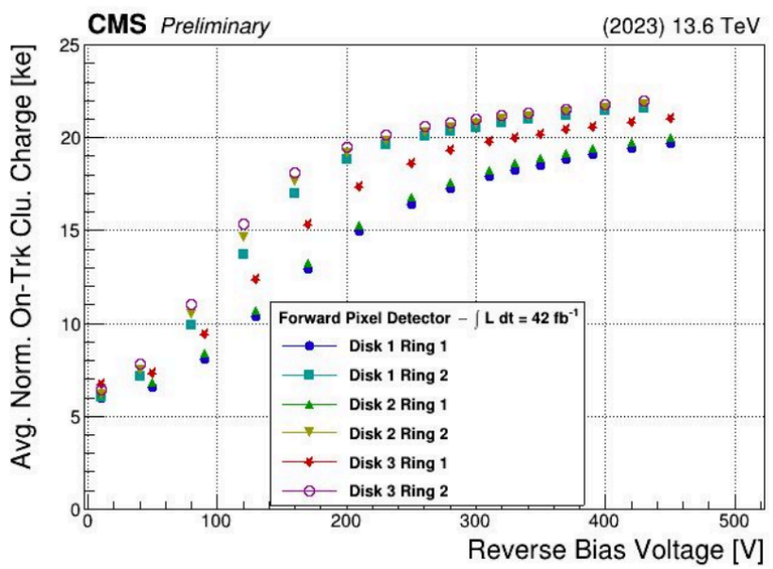
Ring 1: 350 V

Ring 2: 300 V





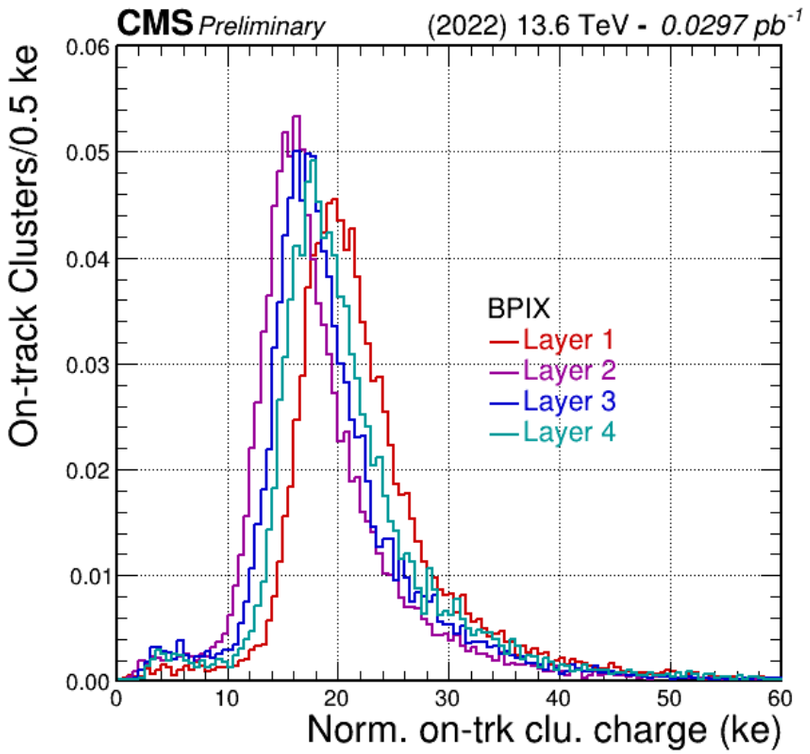




Radiation damage in Layer 1

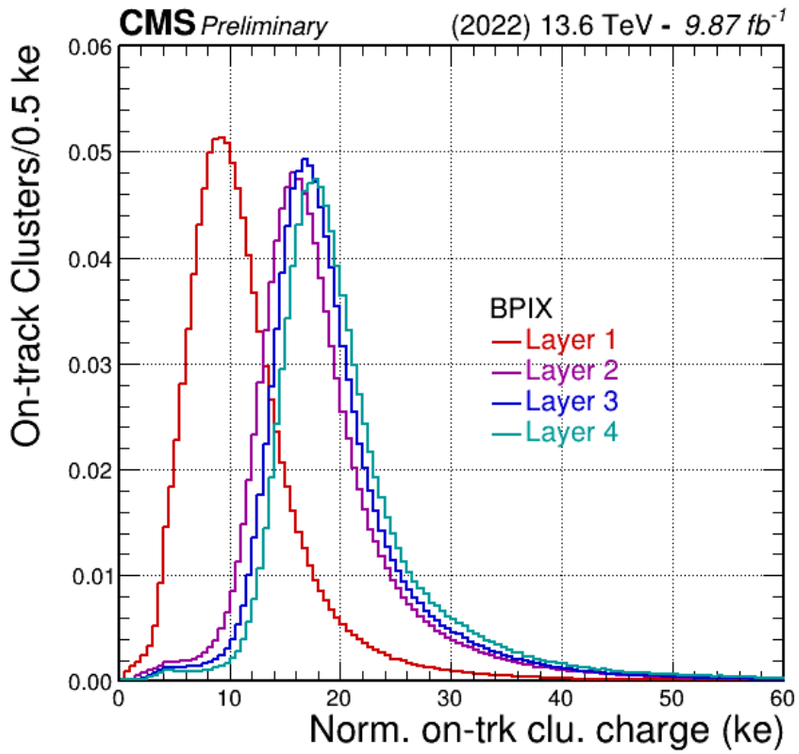
- **Strong effect of radiation damage observed in cluster properties**

Layer 1 @ 150 V



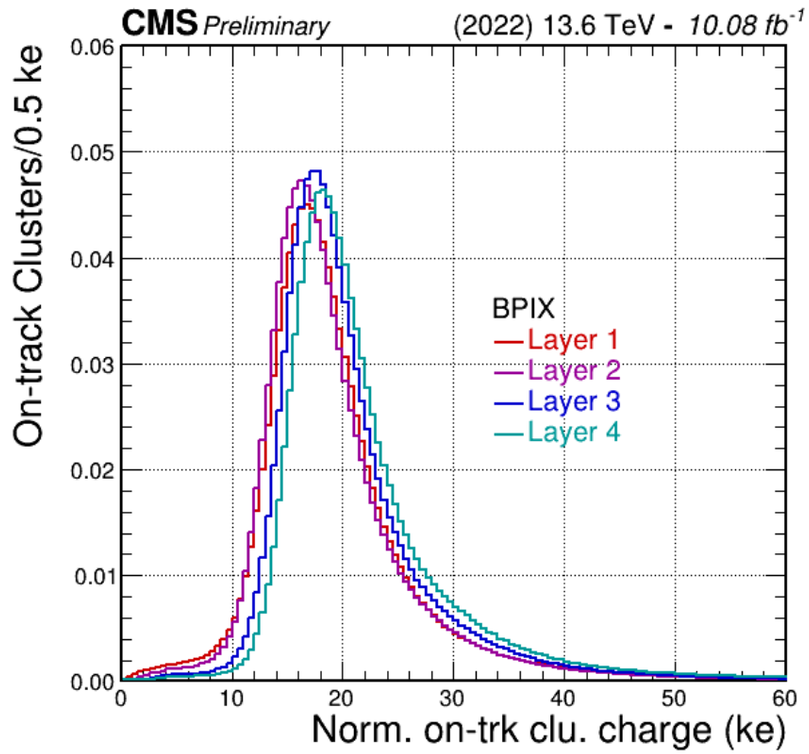
Layer 1 fully replaced during LS2 → started with no radiation damage, i.e. higher cluster charges

Layer 1 @ 150 V



large charge efficiency loss due to radiation damage observed within first 10 fb^{-1}

Layer 1 @ 300 V

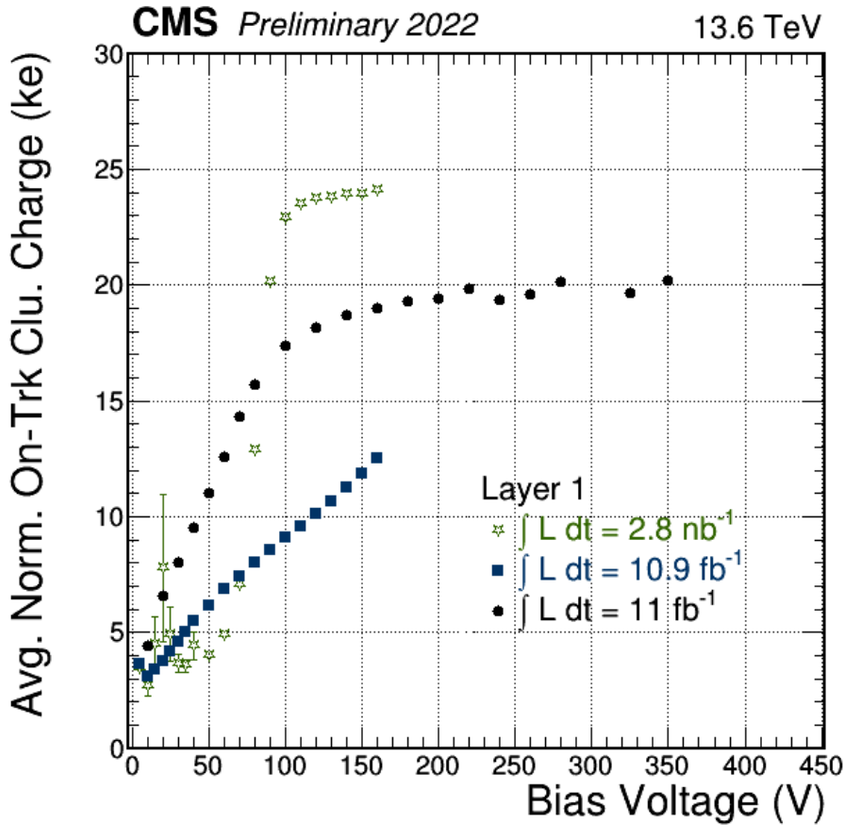


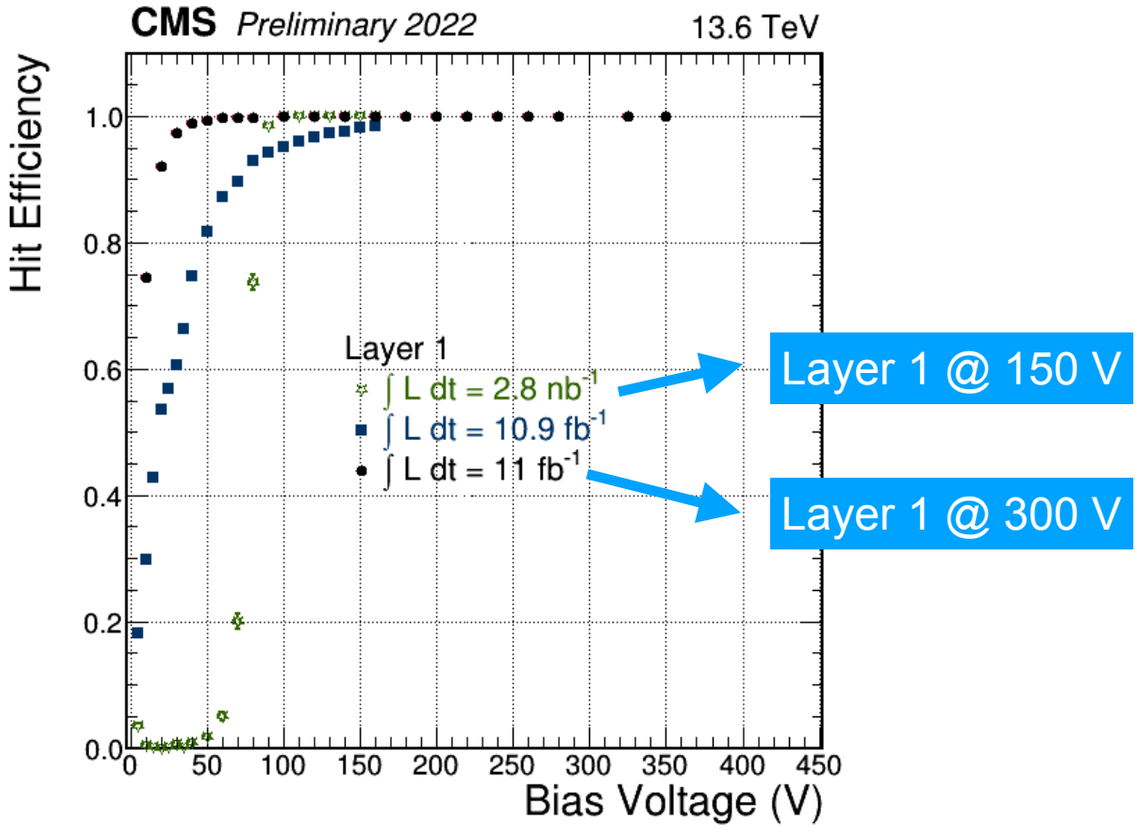
recovered by raising bias voltage from 150V to 300V

Radiation damage in Layer 1

- **Effect of irradiation in Layer 1 also visible in different bias scans:**
  - ~3 nb^{-1}: not much radiation damage accumulated yet
  - ~10 fb^{-1}: radiation damage higher than expected due to quick luminosity ramp up at beginning of Run 3
  - ~11 fb^{-1}: **charge collection efficiency improved thanks to positive annealing** during the period without data-taking (no beam for ~4 weeks due to LHC cooling incident)

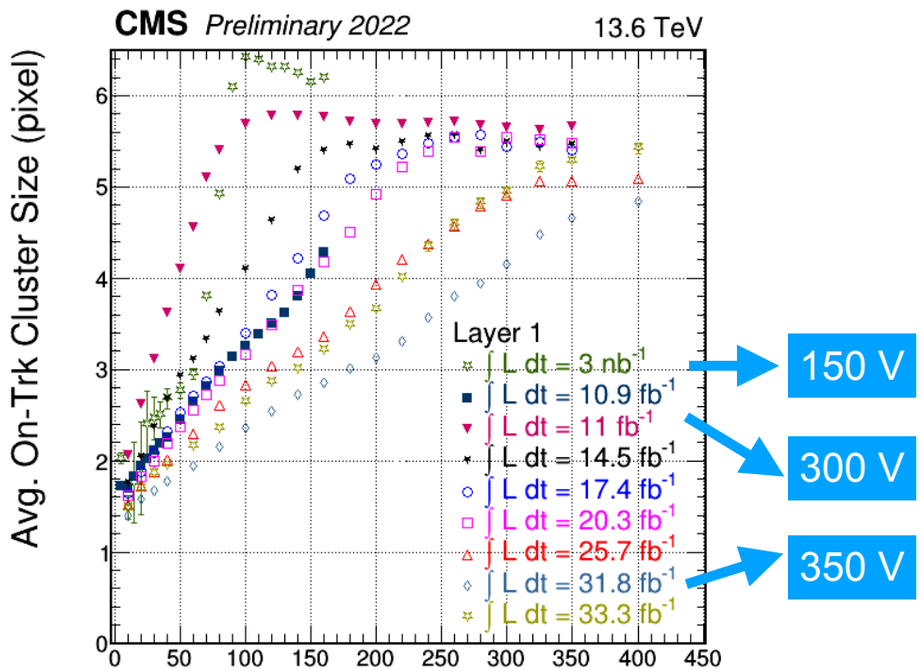
→ need to monitor closely the evolution of the situation with scans once a week to decide when to change operational HV settings

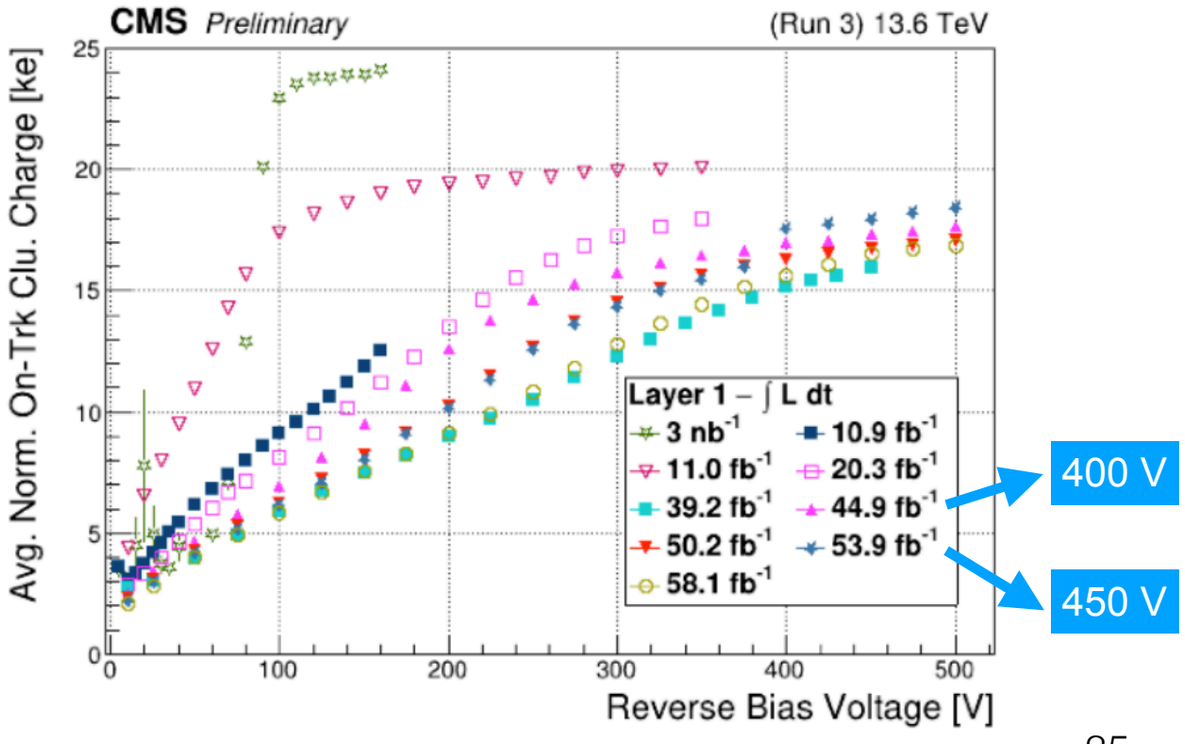


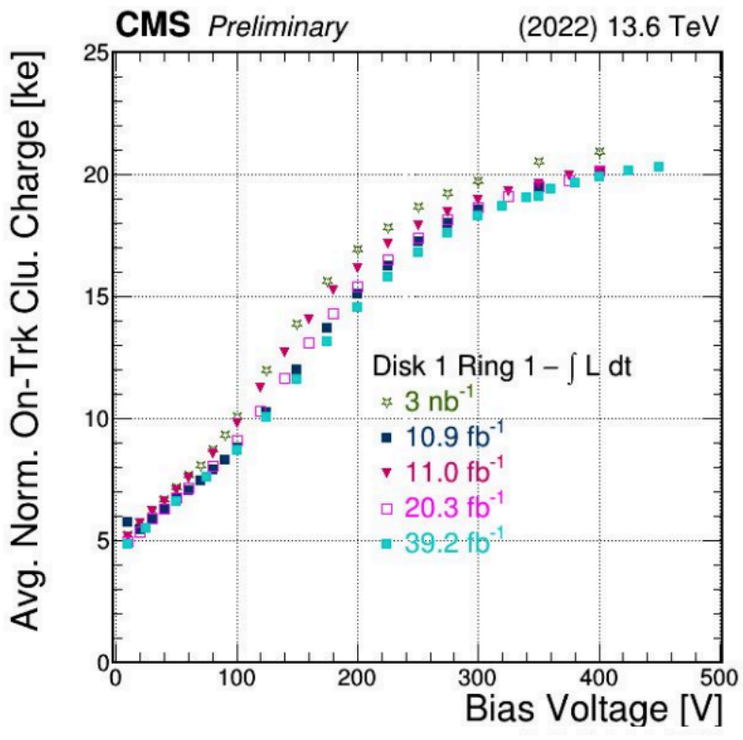


HV bias scans

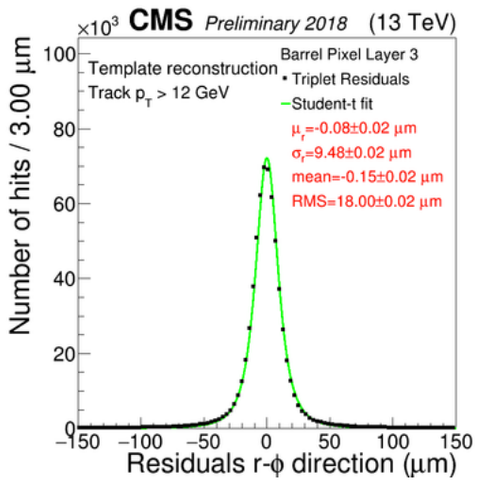
- Bias voltage scans are now performed regularly to determine when settings should be adjusted
- **Layer 1 is in better shape compared to 2022 thanks to annealing during YETS**
- Other parts of the detector don't show big changes



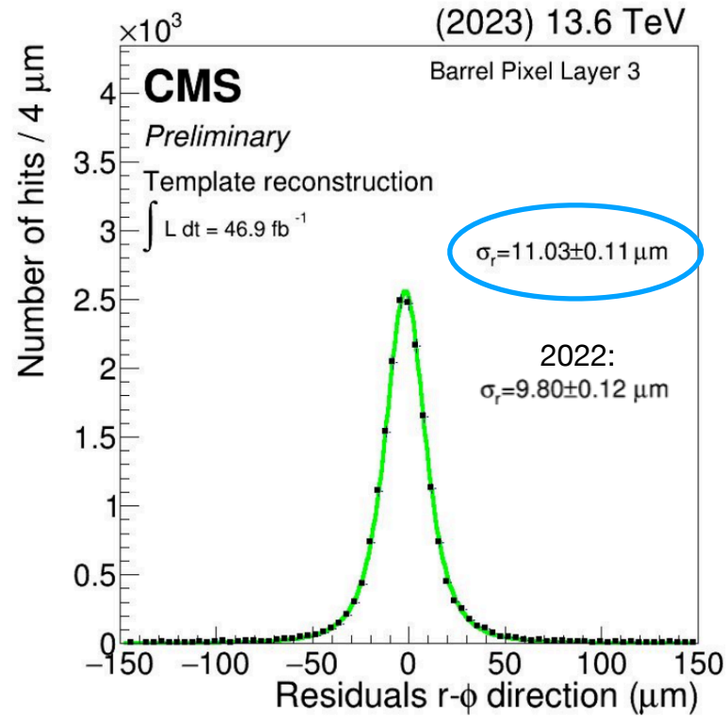


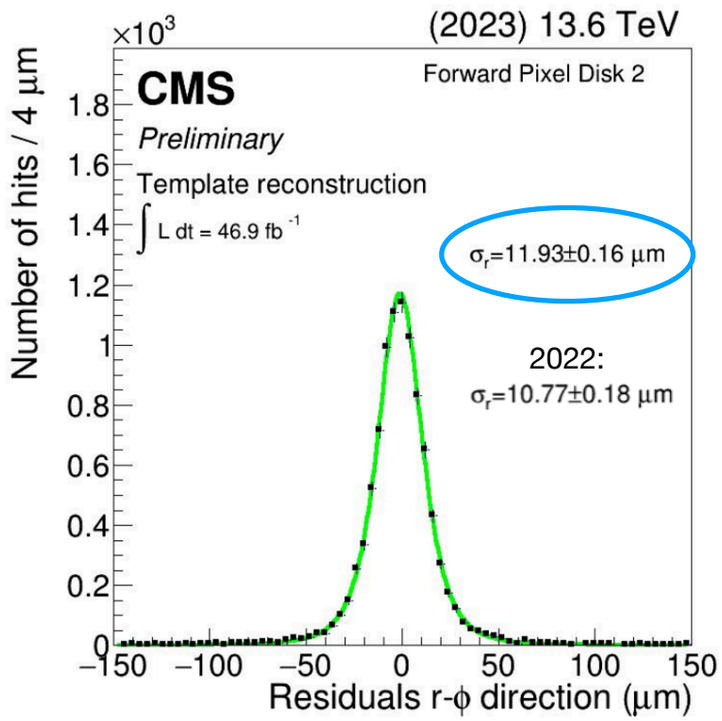


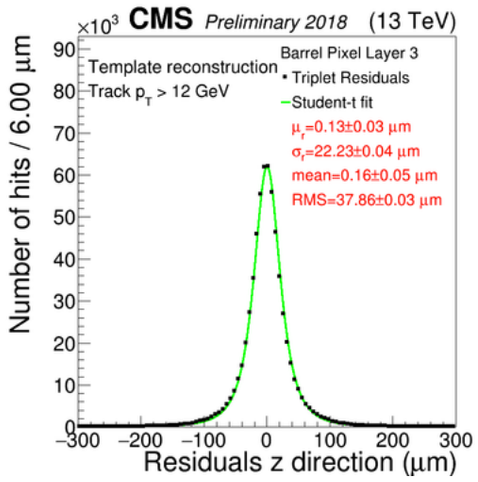
Resolution



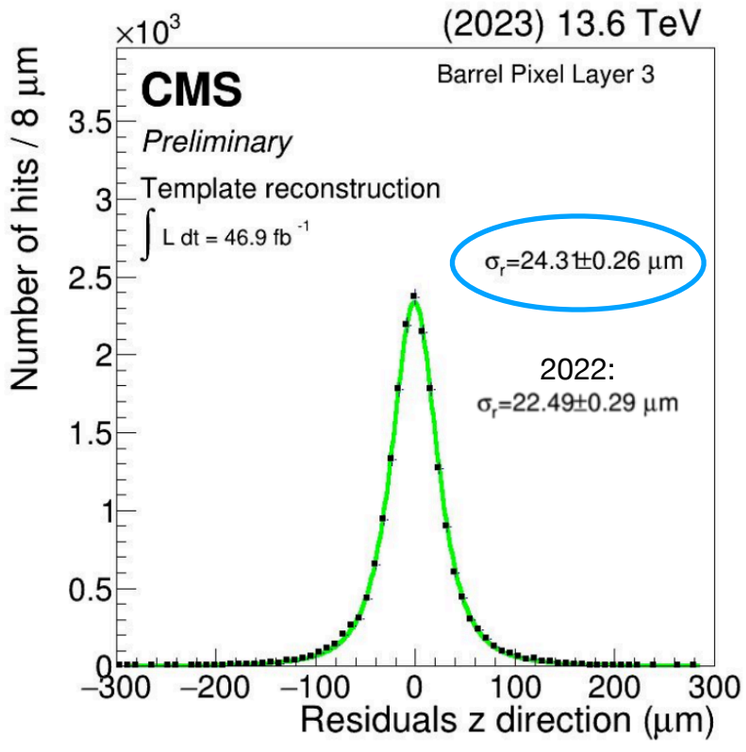
Comparable to Run 2 and 2022 performance

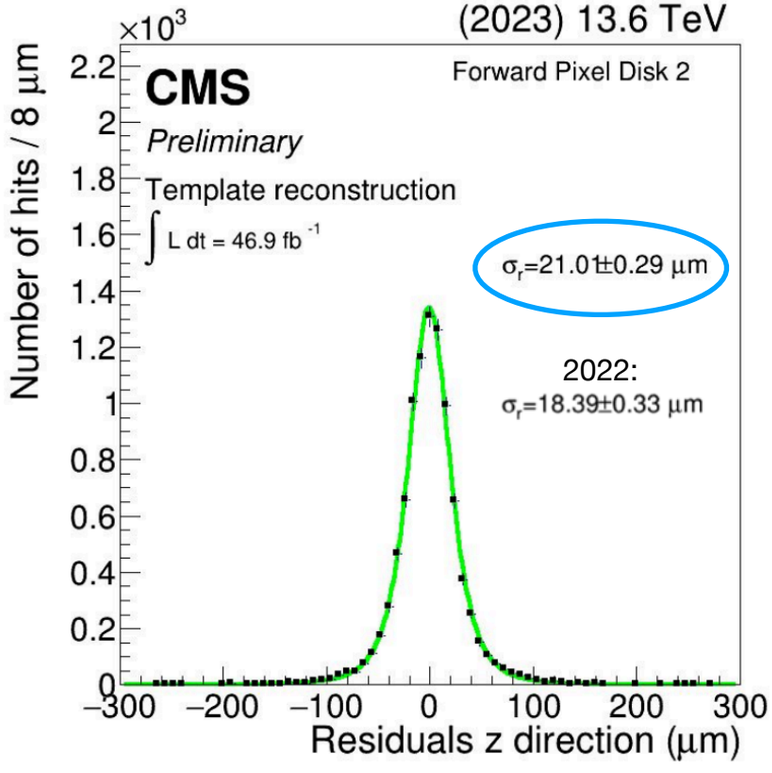






Excellent position resolution in both BPix and FPix

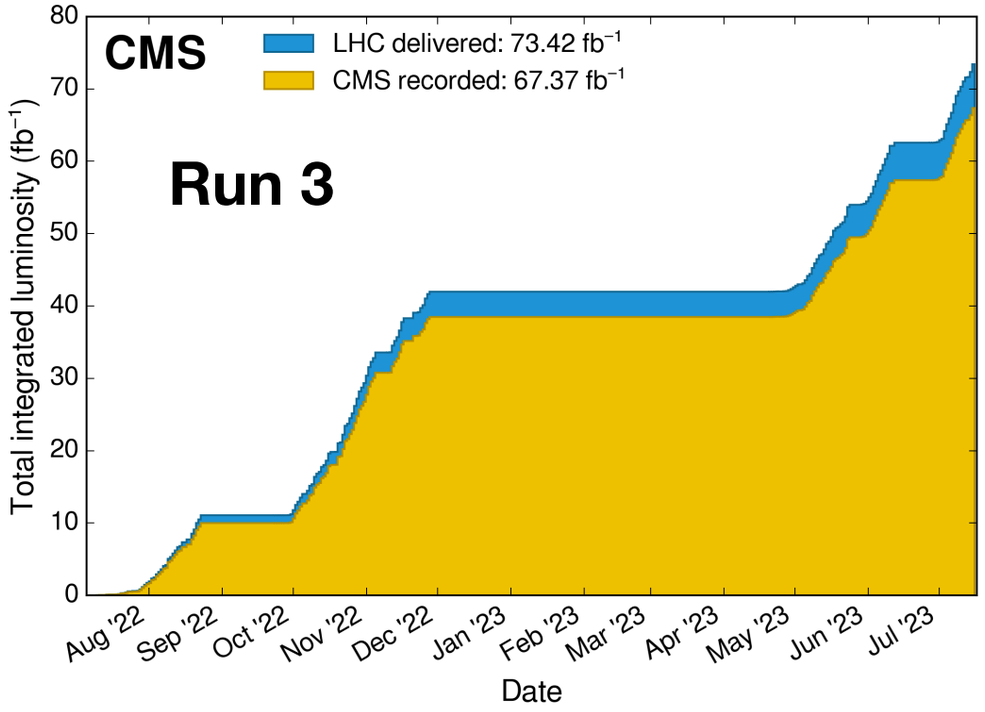




CMS data-taking

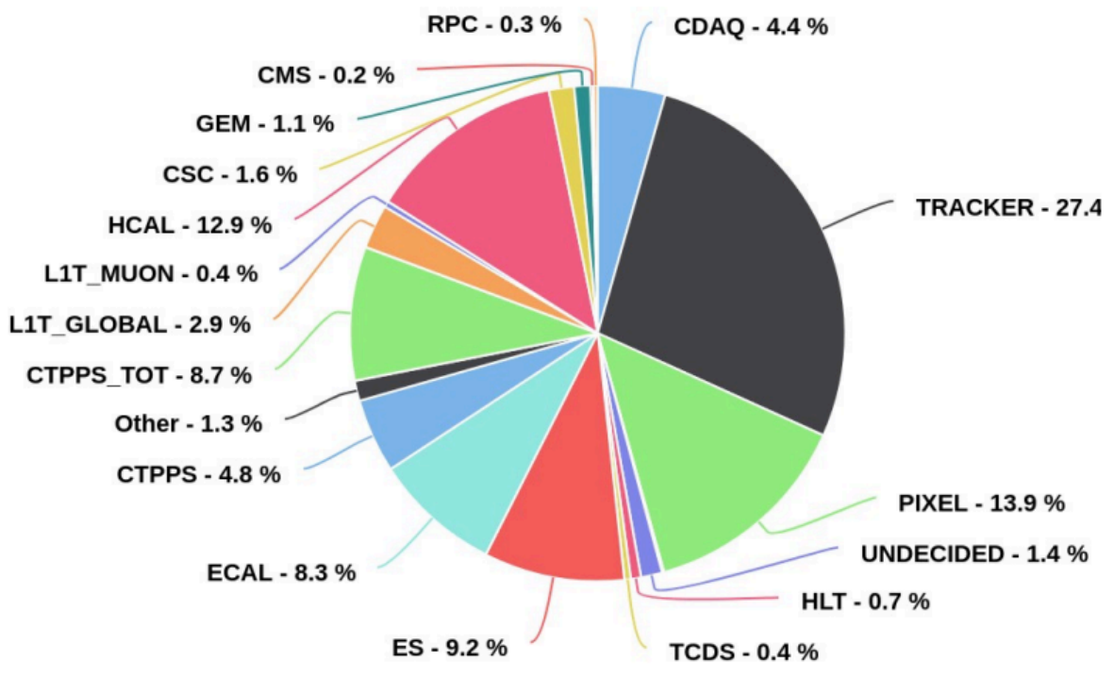
- **Data recorded by CMS are a fraction of data delivered by LHC** because sub-systems might go into error causing downtime, i.e. time without data acquisition

- ***Good operations = lot of good data !***
  - i.e. if there are issues with data-taking, try to understand and solve them as fast as possible in order not to loose (good) data



- **Main contributions to Pixel downtime was due to Soft Error Recoveries (SERs)**

Soft Error Recovery (SER) = procedure triggered to recover high number of auto-masked channels, i.e. channels masked during data-taking due to readout errors



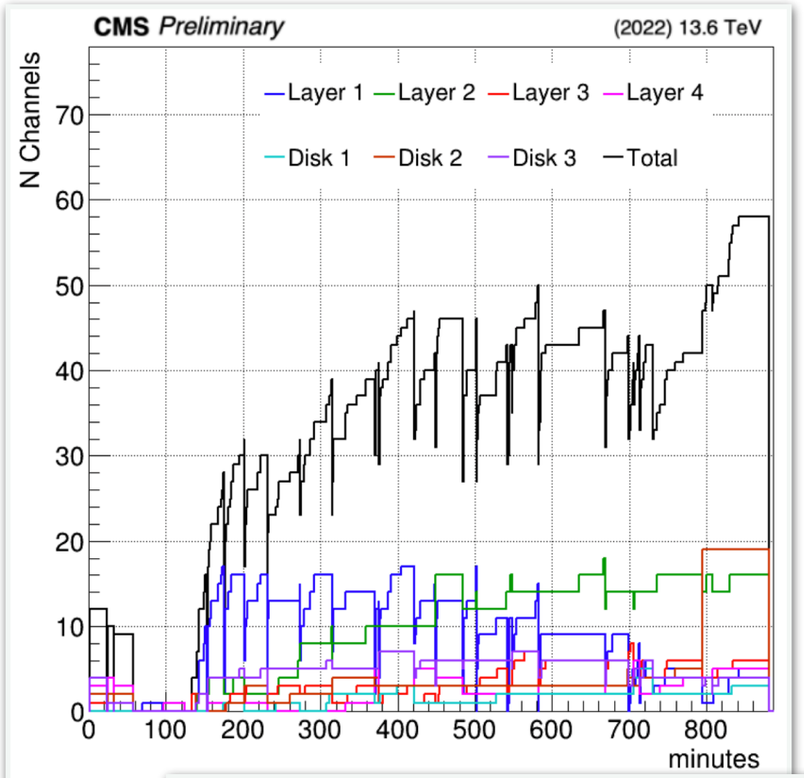
Soft Error Recoveries

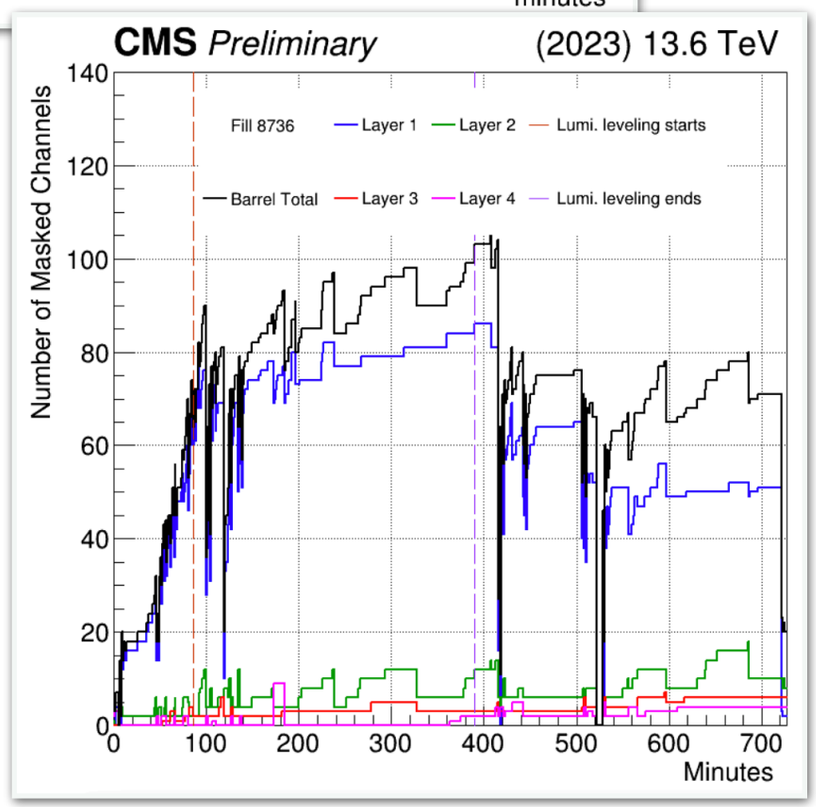
- **Main Pixel downtime in 2022 was caused by storms of SERs**, i.e. SERs happening very often

- **No clear cause was identified**
  - fills with similar conditions had very different number of auto-masked channels

- **Plans for investigation:**
  - create trends of auto-masked channels over large period of time and correlate them with changes in conditions (HV change, FW update, software changes, ..)
  - get statistics of auto-masked channels to understand if there are ones masked more often

- **In 2023, smooth running until 900b fills but similar issue re-appeared with 999b fills**
  - **high number of auto-masked channels (mostly in Layer 1) triggering frequent SERs**
  - seemed related to higher pileup (PU) and trigger rates used





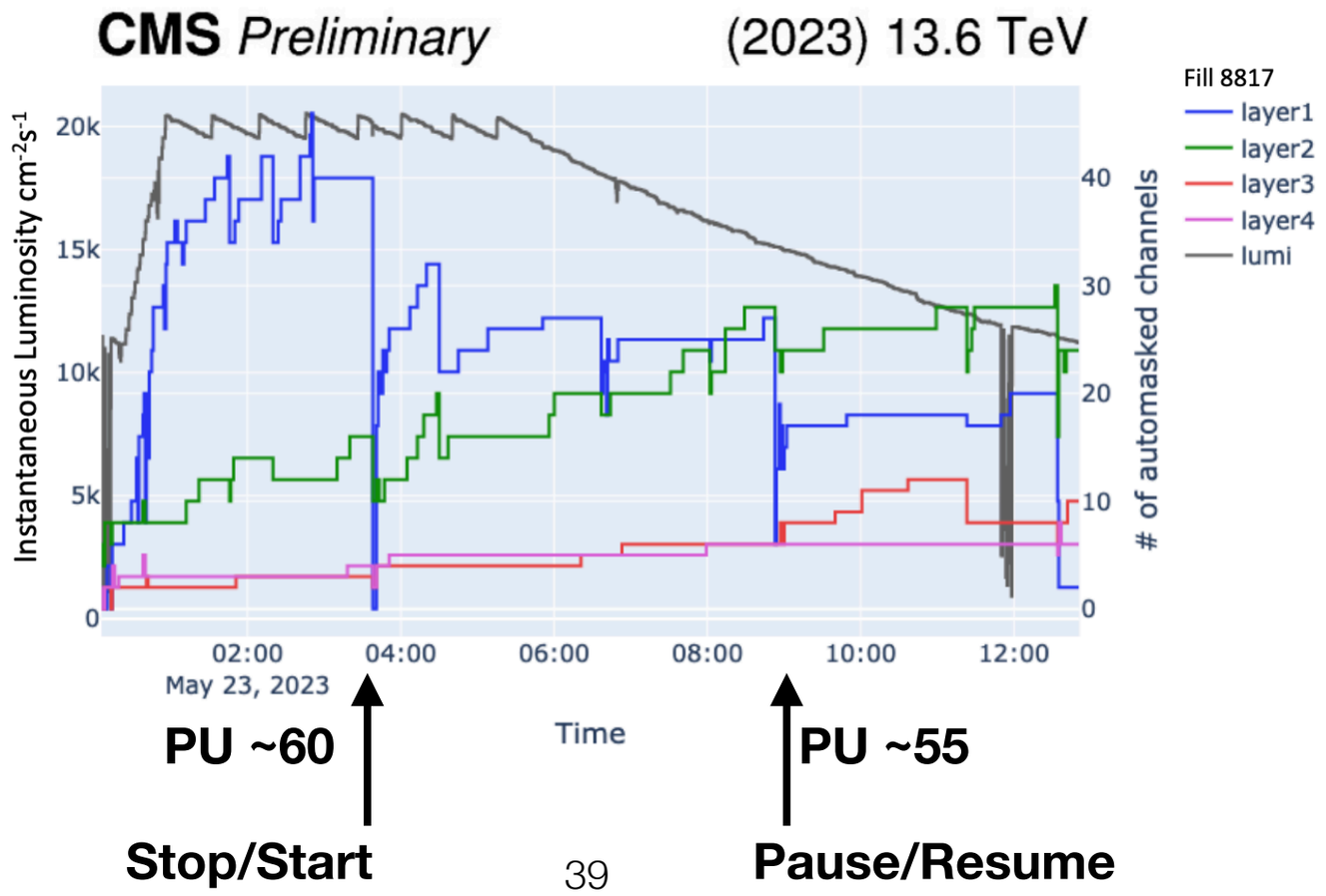
Auto-masked channels

- **High number of channels masked during data-taking due to readout errors**
  - **dependence from both PU and trigger rate** observed in PU vs trigger rate scan
  - Layer 1: operational problem mitigated by recovery action (Pause/Resume run) at PU < 60
  - Layer 2-4: unrecoverable SEUs accumulate over a fill
  - some channels were consistently masked but **no clear pattern on the geometry**

- **~10% of Layer 1 was masked** **in fills with PU ~60 and L1 trigger rate ~100-110 kHz**

- **Data quality remained good** but needed to reduce downtime in order not to loose many data

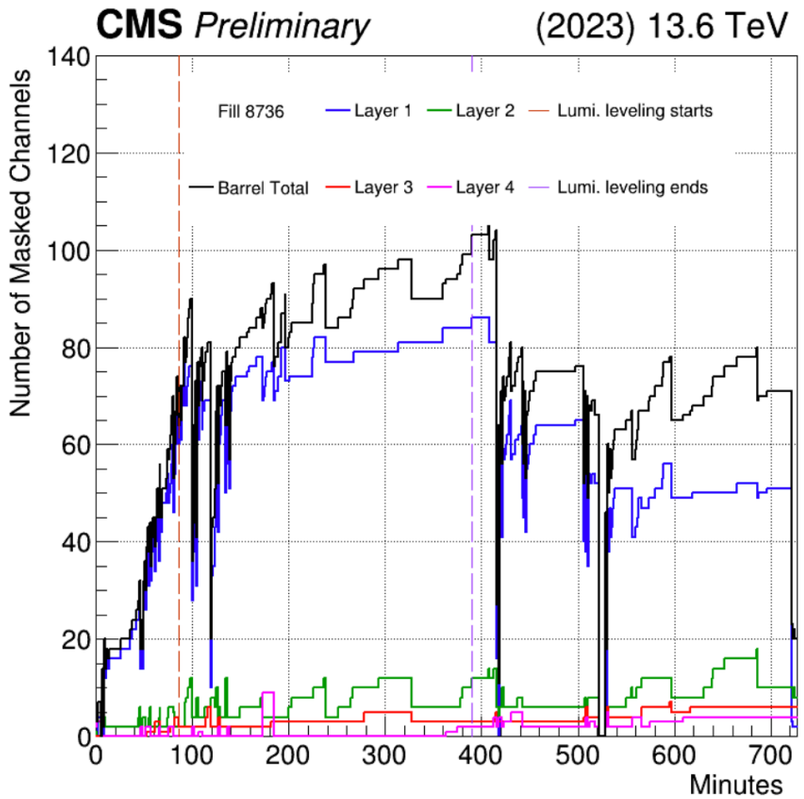
SEU = Single Event Upset



Mitigation changes

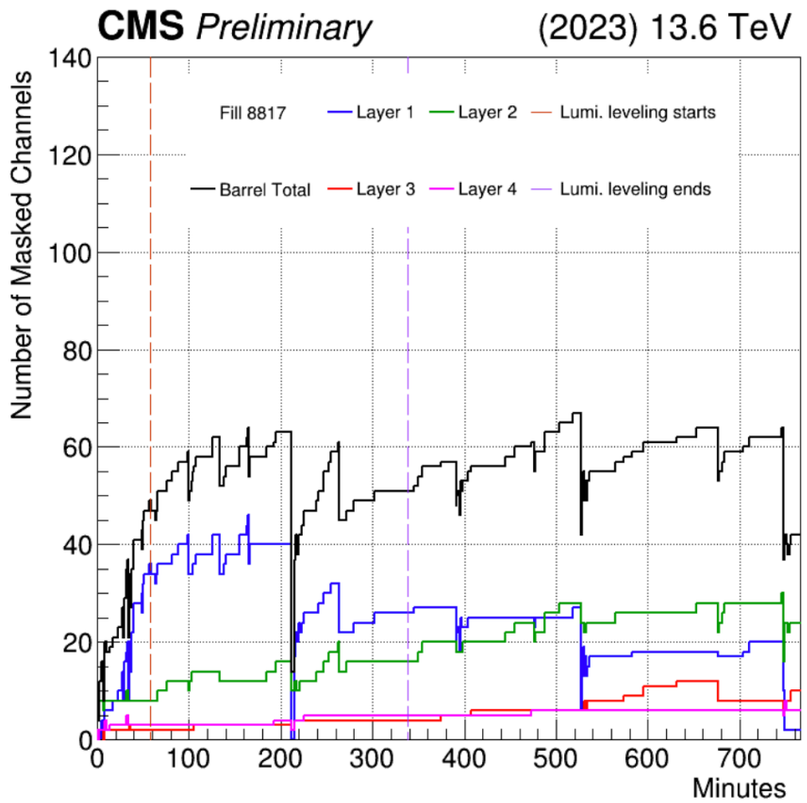
- **Situation better after increasing number of allowed readout errors** required to auto-mask a channel

- **Big improvement after adjusting phases of the 400MHz data transmission** (relative phase of readout chip and TBM)
  - calibrations do not not always predict a good setting for high rate data transfer



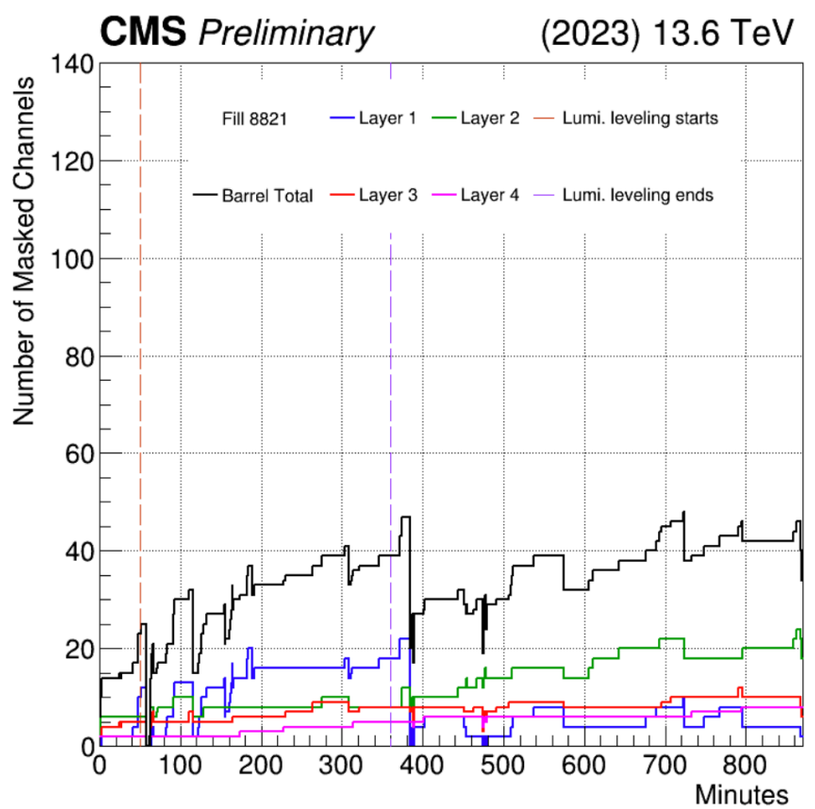
~10% of Layer 1 auto-masked

new conditions to auto-mask channels



~5% of Layer 1 auto-masked

phases adjustment



~2% of Layer 1 auto-masked

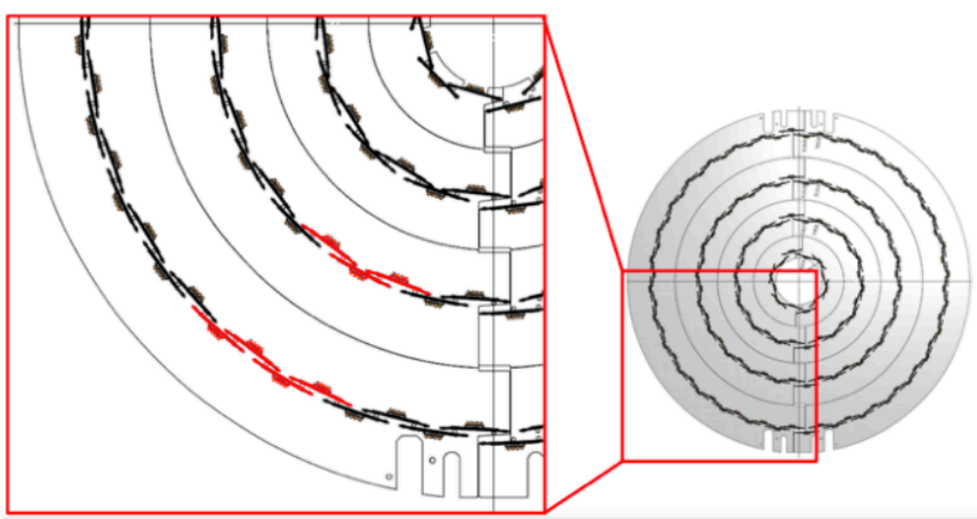
- **Auto-masking of Layer 1 modules now very low** even at high PU (~63), **usually 1% of channels**

Small “hole” in BPix

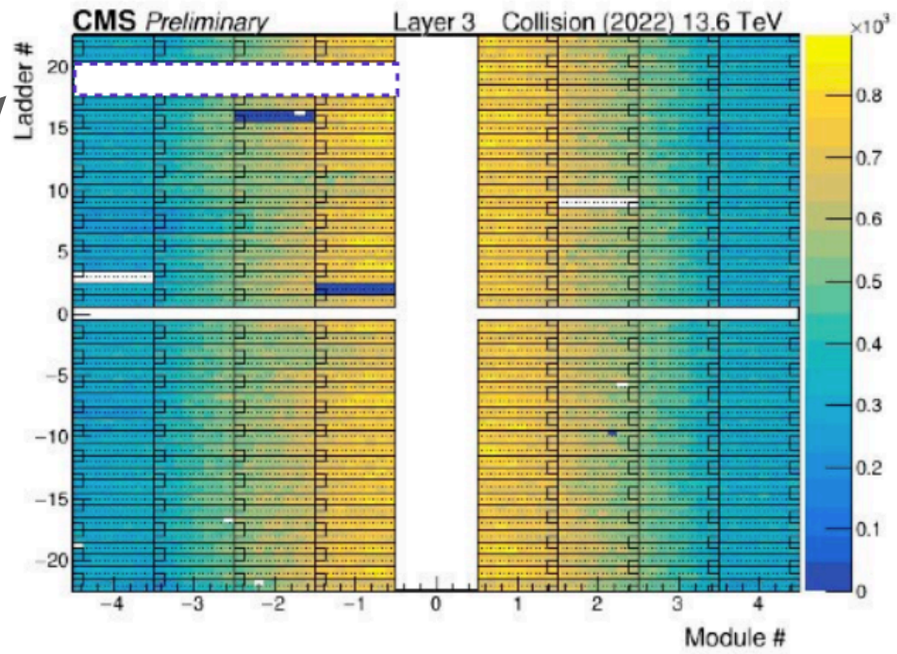
PLL = Phase-Locked-Loop
QPLL = Quartz supported PLL

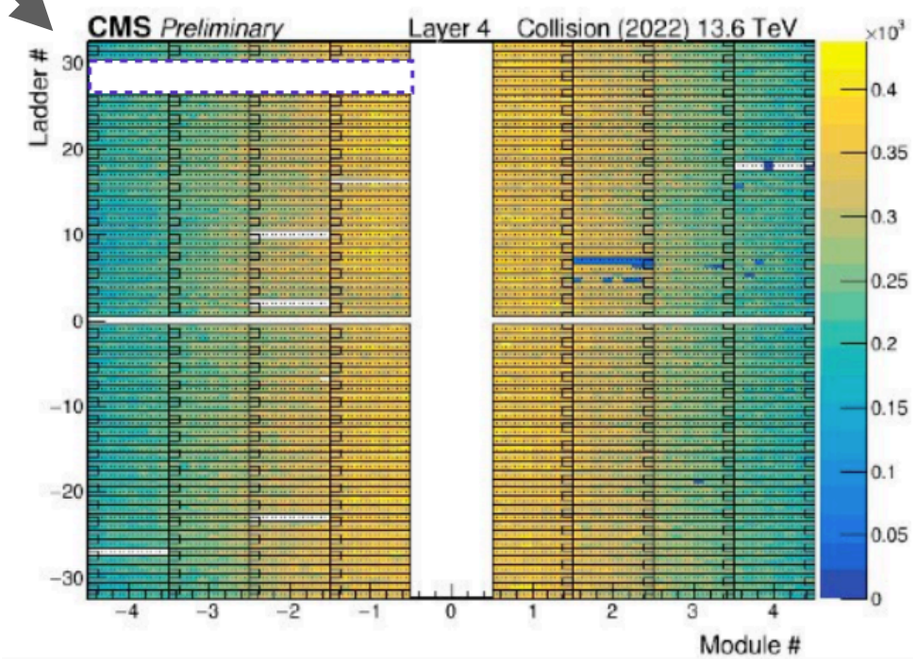
- **Part of BPix could not configure after TS1 in June 2023**
- **After investigation, discovered that QPLL circuit does not lock to LHC clock**
- **Layers 3 and 4 of one sector of BPix affected**
- **Modules are not currently read out**
  - fixing the issue would require extracting and reinstalling pixel detector, risking to create more issues while fixing this one

… sometimes problems can’t be fixed…



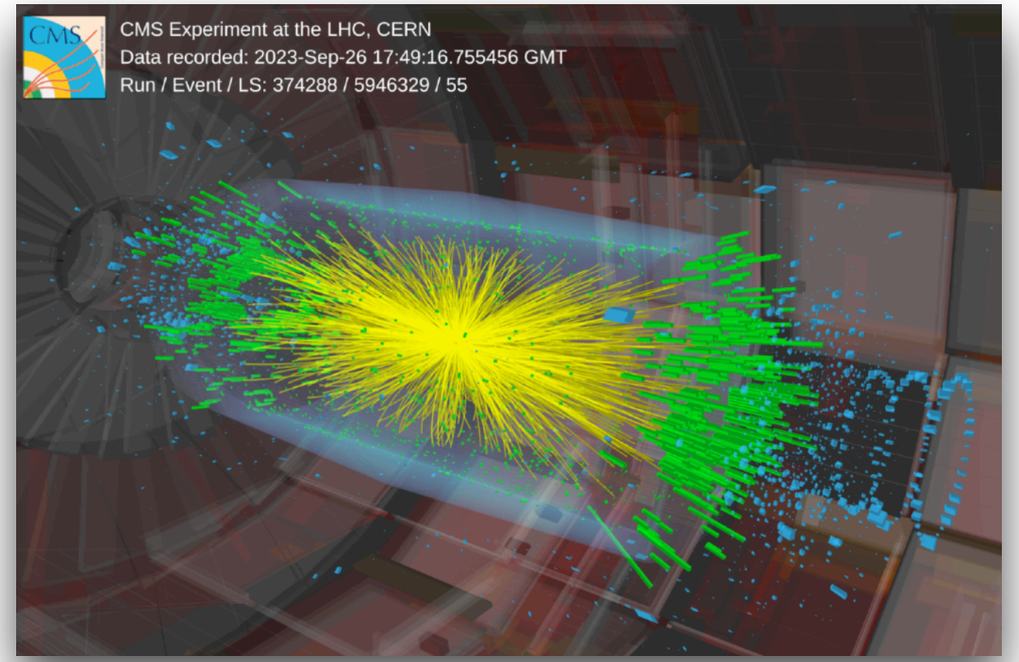
BPix ~ 96.2%

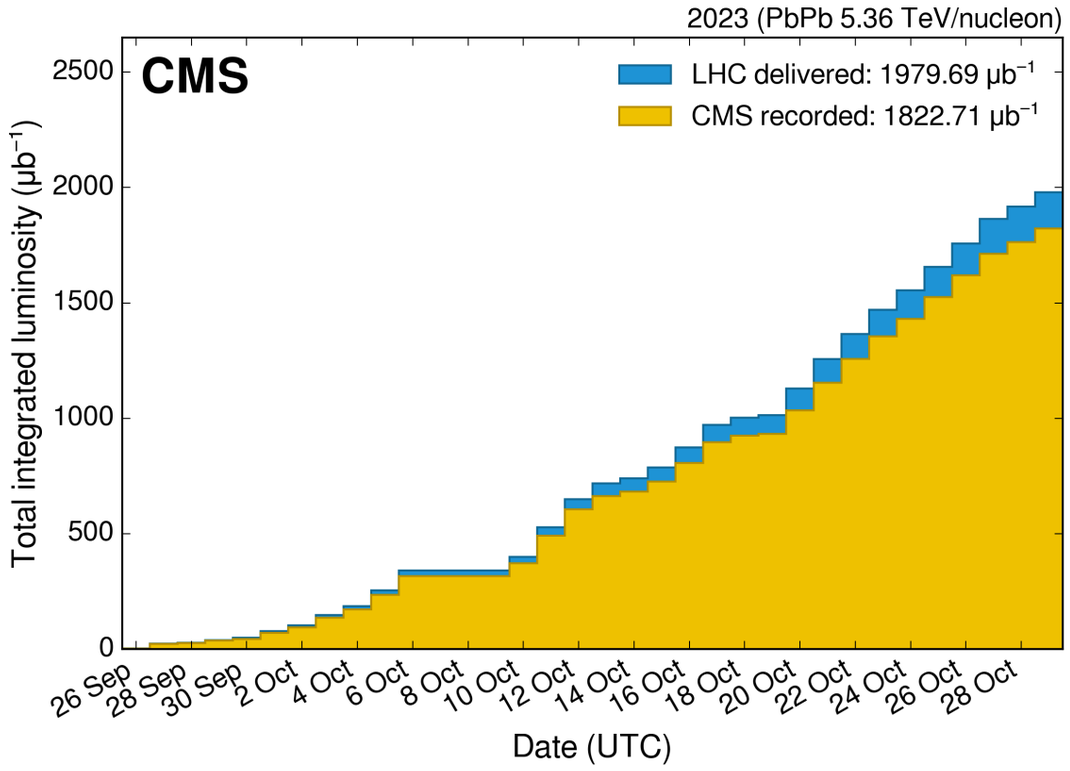


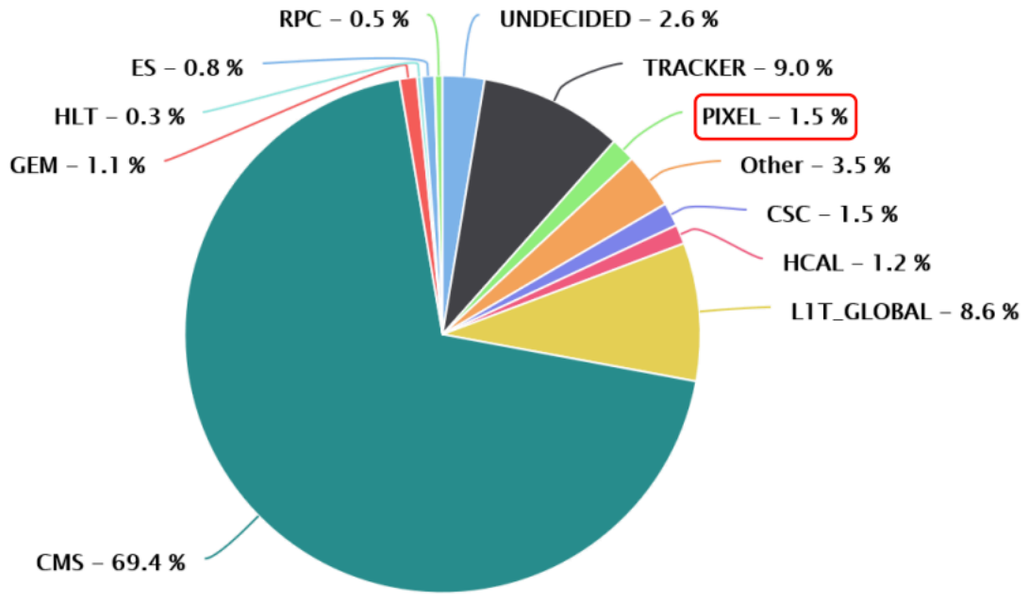


Heavy Ion

- **Pixel performed well during heavy ion collisions**
  - buffers increased to allow for larger event sizes in readout
  - low luminosity leads to virtually no SEUs
- **Very low downtime during this period**

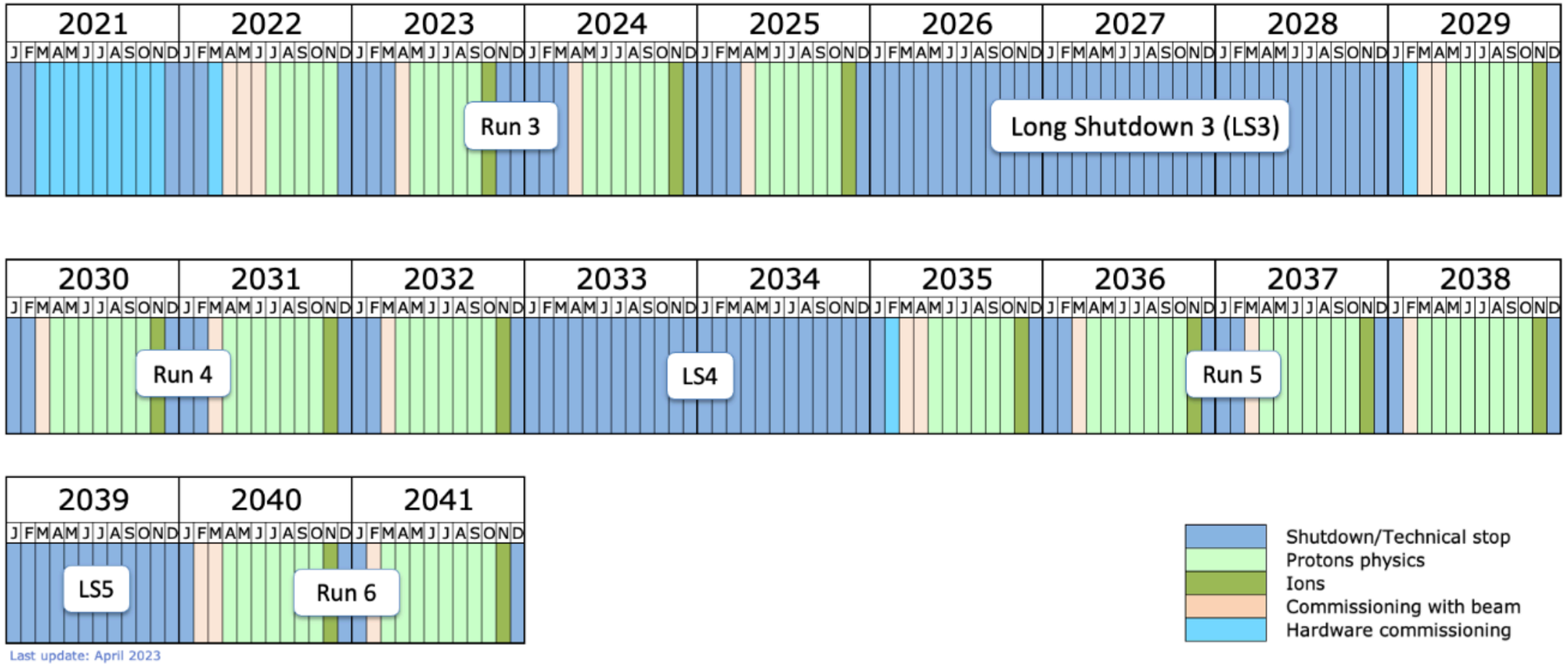






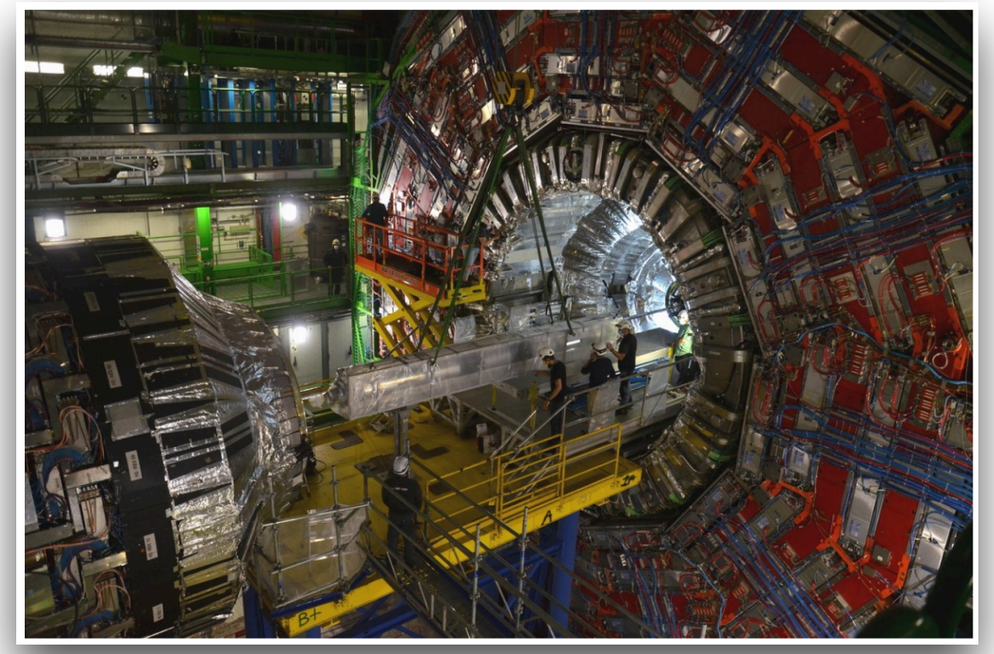
What about the future?

- **Run 3 will last until the end of 2025**
- **Tracker detector will be replaced during LS3**
- **A lot of work ahead for both Operations and Upgrade groups** = *a lot of opportunities to learn more details about the detector and to contribute to a successful data-taking !*

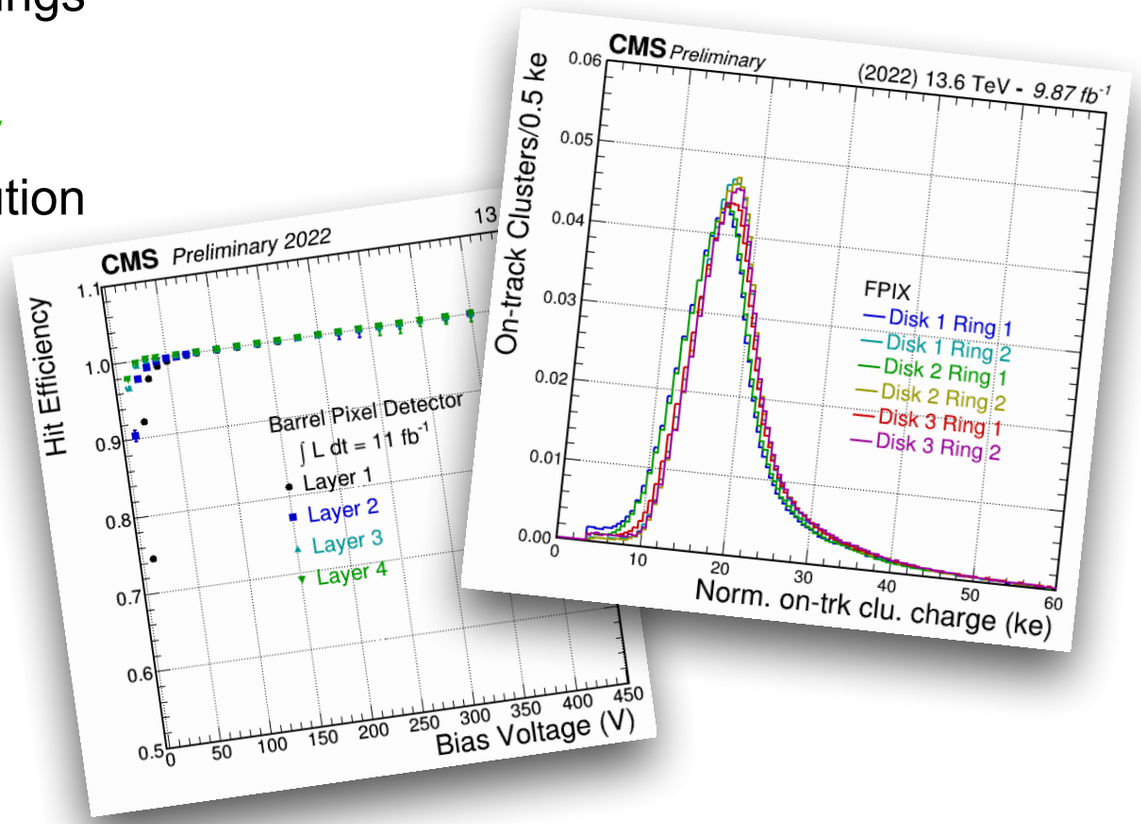


Summary

- **Pixel refurbished during the Long Shutdown 2**
- **Smooth installation in summer 2021**
- **Detector commissioned in 2021 and 2022**
  - no new problems observed after installation
  - detector in good shape and ready for Run 3



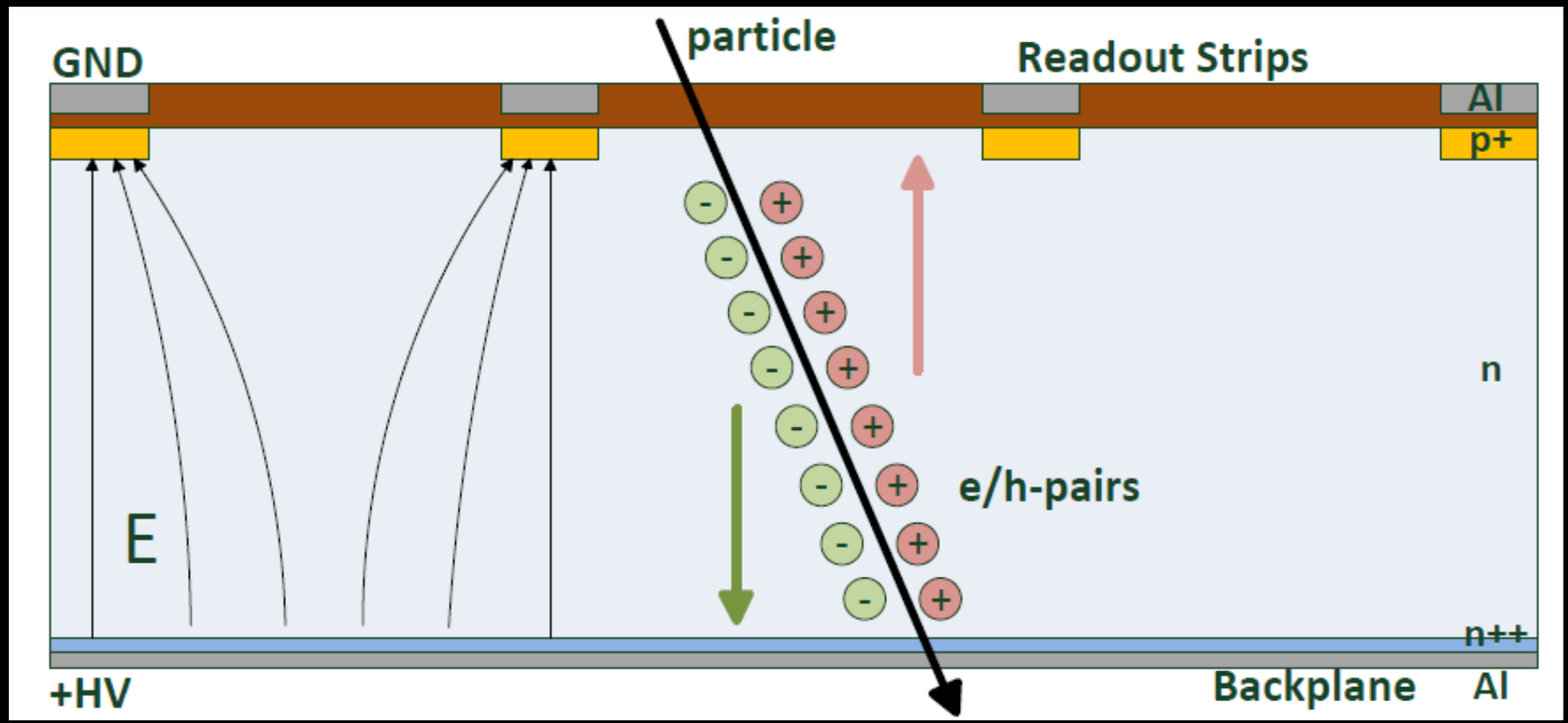
- **Successfully participated in first stable beams at 13.6 TeV**
  - performed bias and timing scans to find optimal settings
- **Successful Run 3 data-taking with good data quality**
  - good cluster properties and excellent position resolution
  - performance comparable to Run 2
  - few operational challenges (irradiation of Layer 1, auto-masked channels) under control
  - need to live with BPix hole for the time being
- **A lot of work ahead to keep ensuring good operations !**



BACKUP

Working principle of silicon sensors

- Electron-hole-pairs generated by ionizing particles traversing the silicon are separated by E-field and ‘drift’ to the electrodes



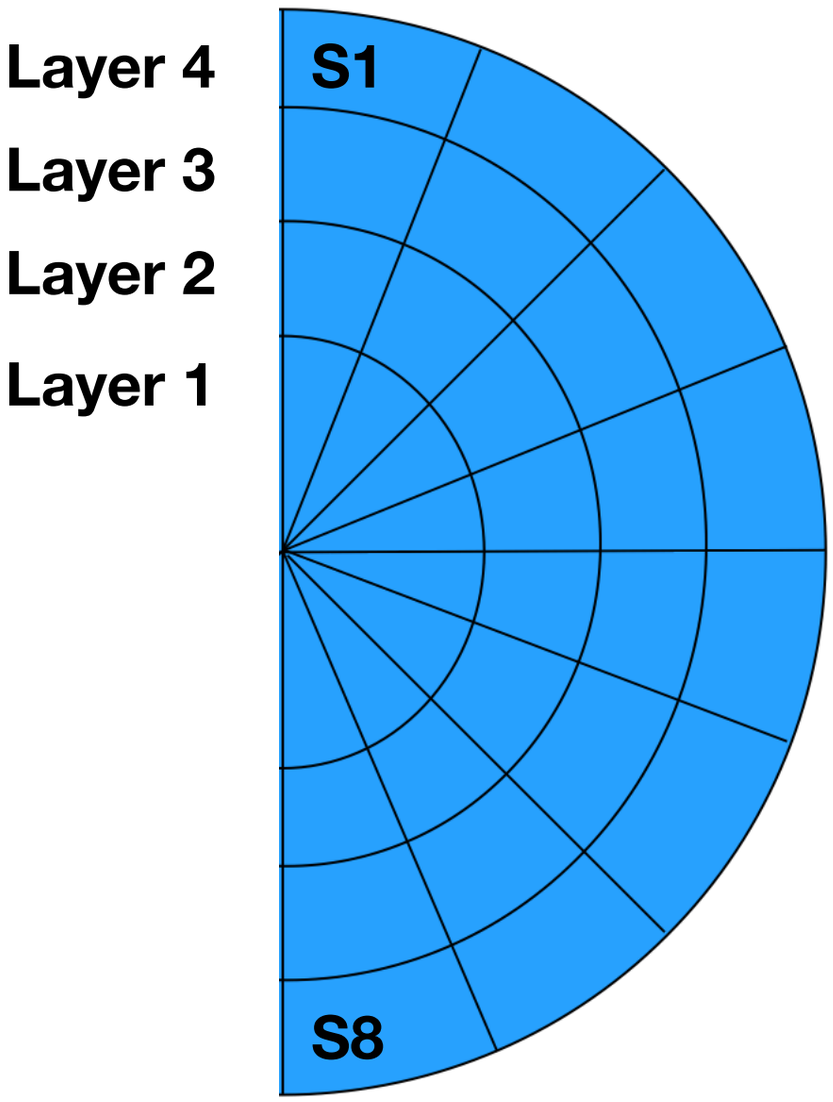
Basically the same for pixels and strips

- Strips ‘collect’ holes
- Pixels ‘collect’ electrons

} Depends on ‘polarity’ of implants

R. Eber, E L ECTRIC F I E LDS AND CHARGE CARRI ER DRI F T IN HIGHLY IRRADIAT ED S I L ICON PART ICL E DE T ECTORS, PhD, IEKP, KIT, 2013

BPix modules names

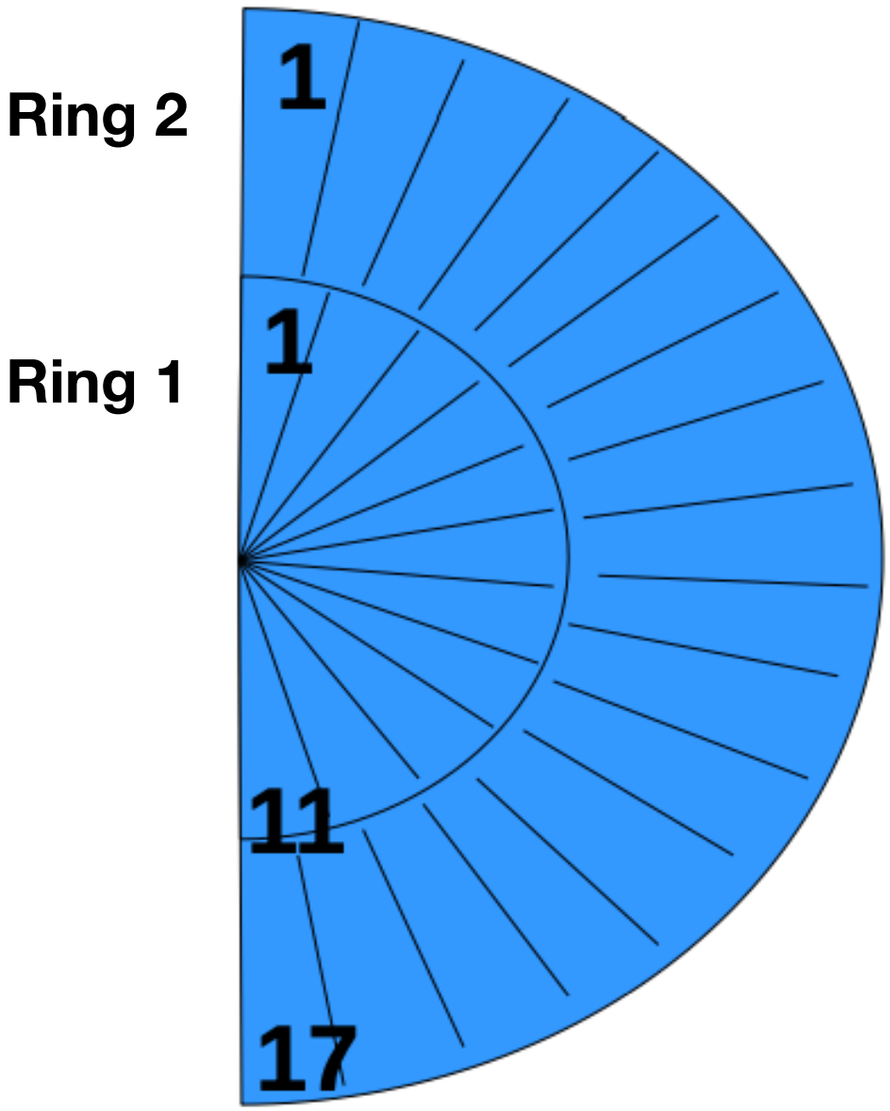


BPix_BpO_SEC8_LYR3_LDR22F_MOD3

Half-cylinder:	BmO, BmI, BpO, BpI
Sector:	1…8
Layer:	1…4
Ladder:	1…6 [in layer 1]
	6…14 [in layer 2]
	14…22 [in layer 3]
	22…32 [in layer 4]
Module:	1…4 [1 is the most central]

Layer1 modules, with 2 TBMs, use letter “F” (full) and “H” (half) - from Phase 0 nomenclature - in ladder name:
F has rocs 0-3, 11-15
H has rocs 4-10

FPix modules names



FPix_BpO_D3_BLD8_PNL1_RNG2

Half-cylinder:	BmO, BmI, BpO, BpI
Disk:	1…3
Blade:	1…11 [in ring 1]
	1…17 [in ring 2]
Panel:	1…2 [side of the blade]

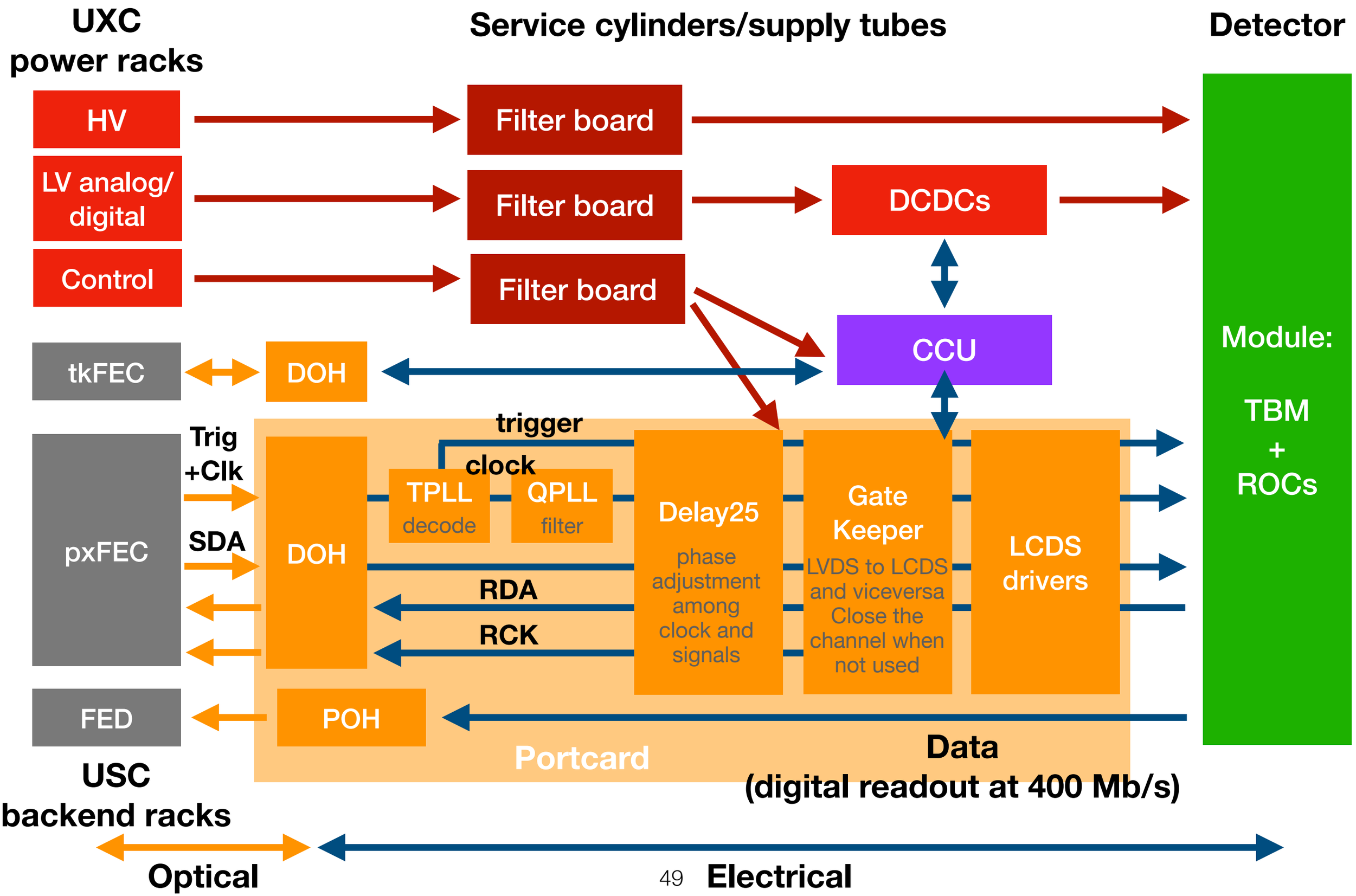
Quiz: which is a valid module name ?

a) FPix_BmO_D3_BLD11_PNL1_RNG2

b) FPix_BpI_D4_BLD8_PNL2_RNG1

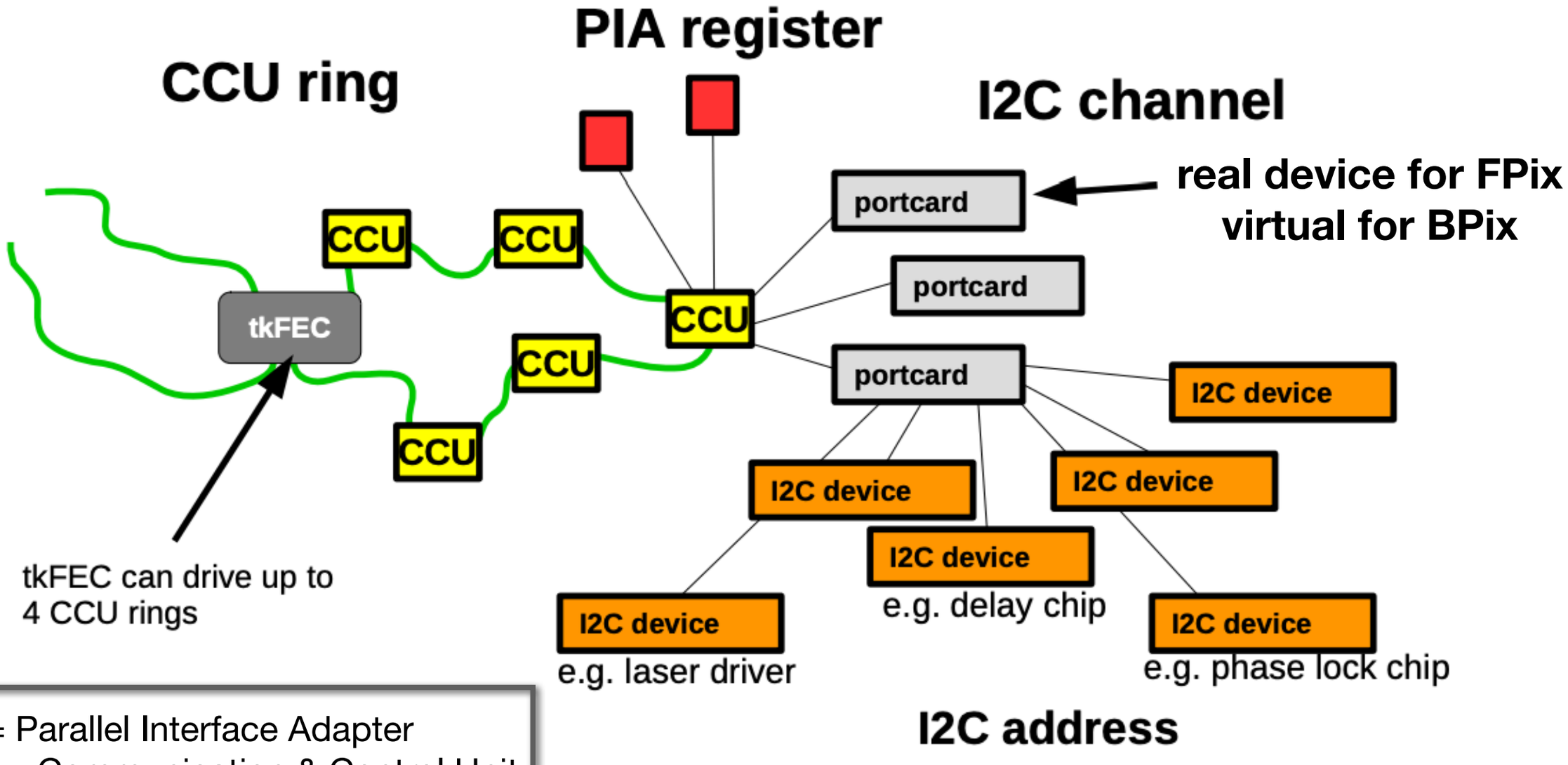
c) FPix_BpO_D1_BLD13_PNL1_RNG1

Hardware connections



Control of Auxiliary Hardware

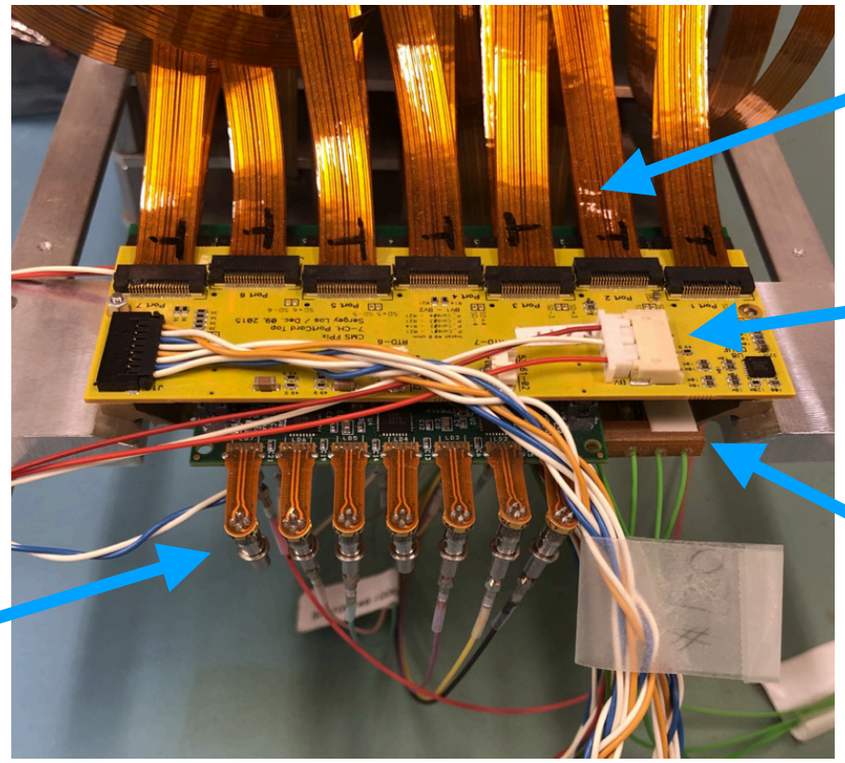
- For each CCU:
  - two **I2C channels used to program the readout electronics** on the service half-cylinders
  - up to 16 **PIA registers used to enable/disable the DCDC converters and to generate reset signals for the readout electronics** on the service half-cylinders and the detector modules



PIA = Parallel Interface Adapter
CCU = Communication & Control Unit

DOH = Digital Opto-Hybrid
POH = Pixel Opto-Hybrid

DOH and POH

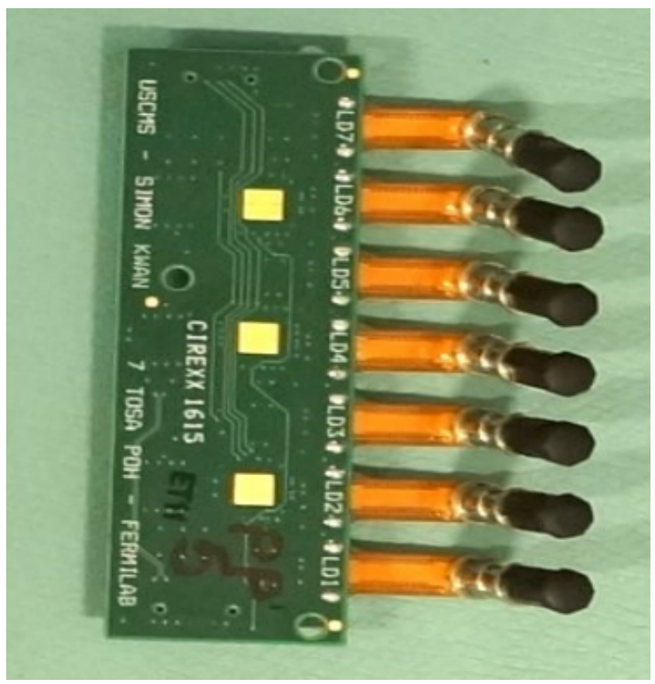


Module cables

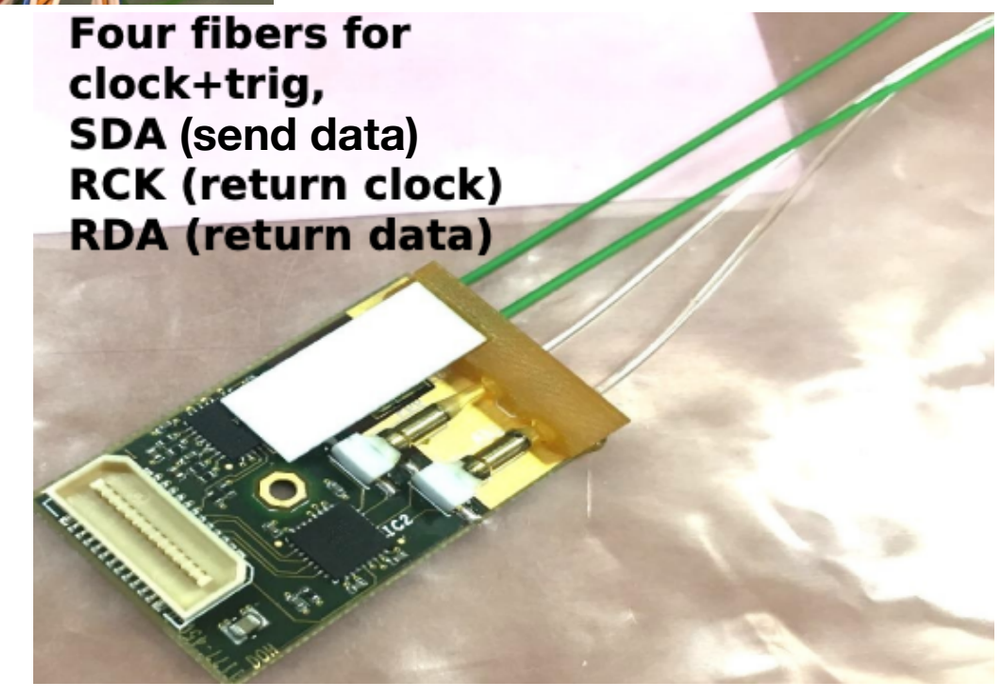
FPix portcard

POH

DOH



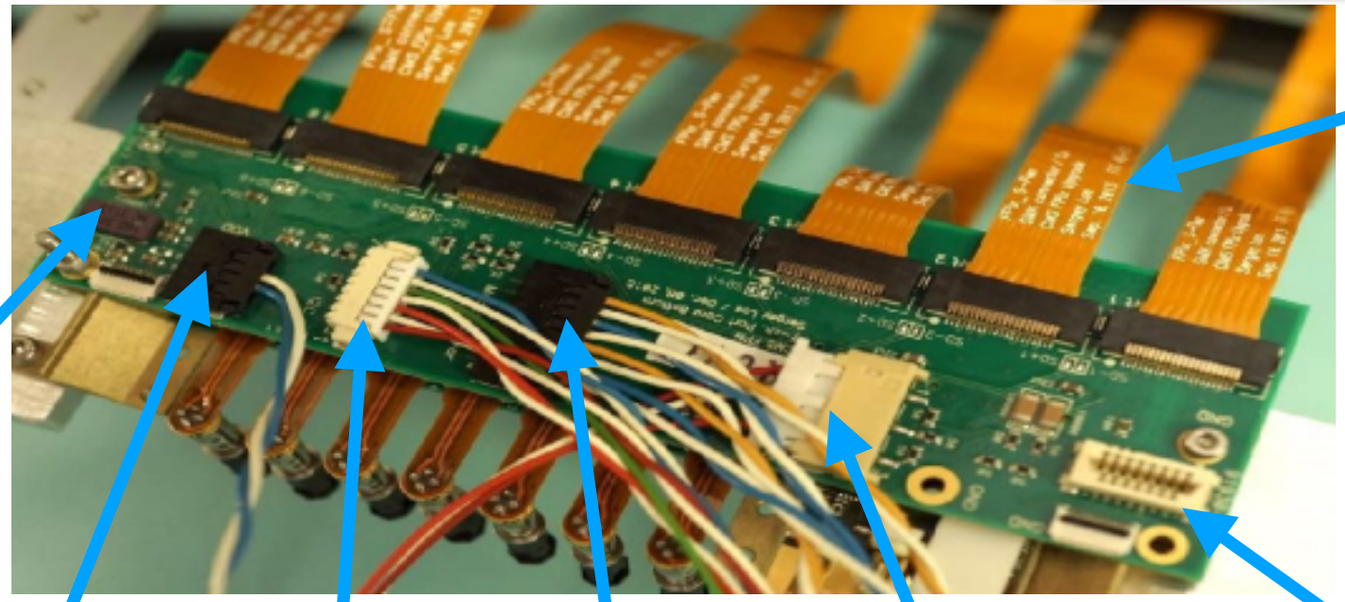
Daughter boards attached to FPix portcard



FPix Port card

PLL = Phase-Locked-Loop
TPLL = Tracker PLL
QPLL = Quartz supported PLL
DCU = Detector Control Unit
LCDS = Low-Current Differential Signal

Top layer



Module cables

Quartz oscillator of QPLL

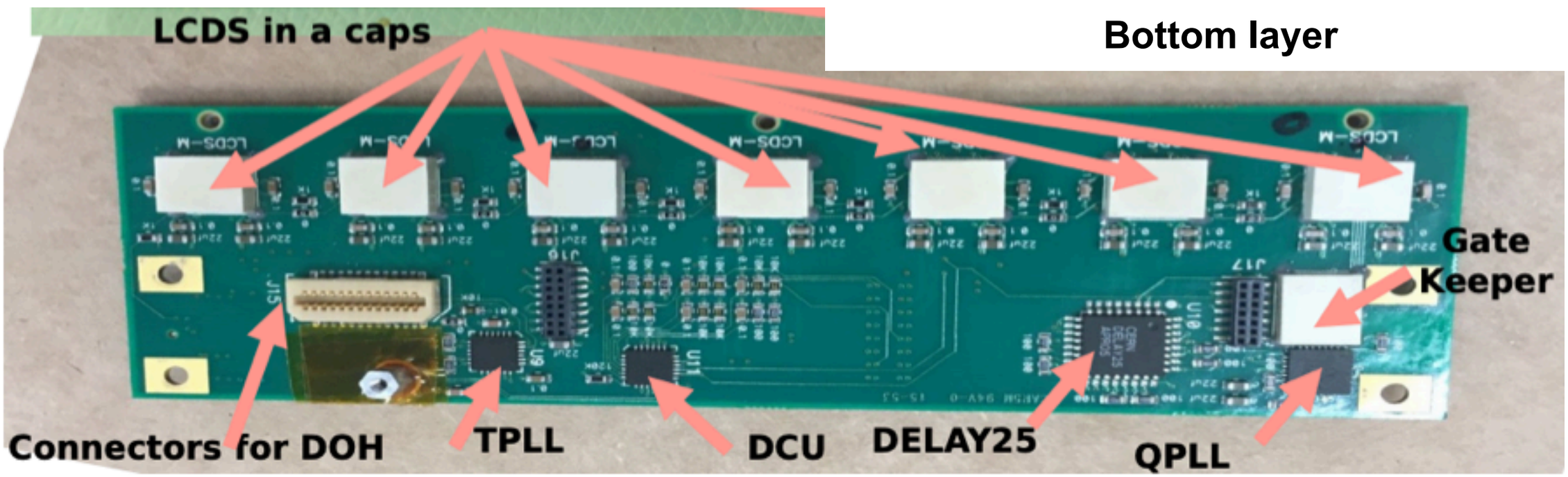
Power port card

Control port card

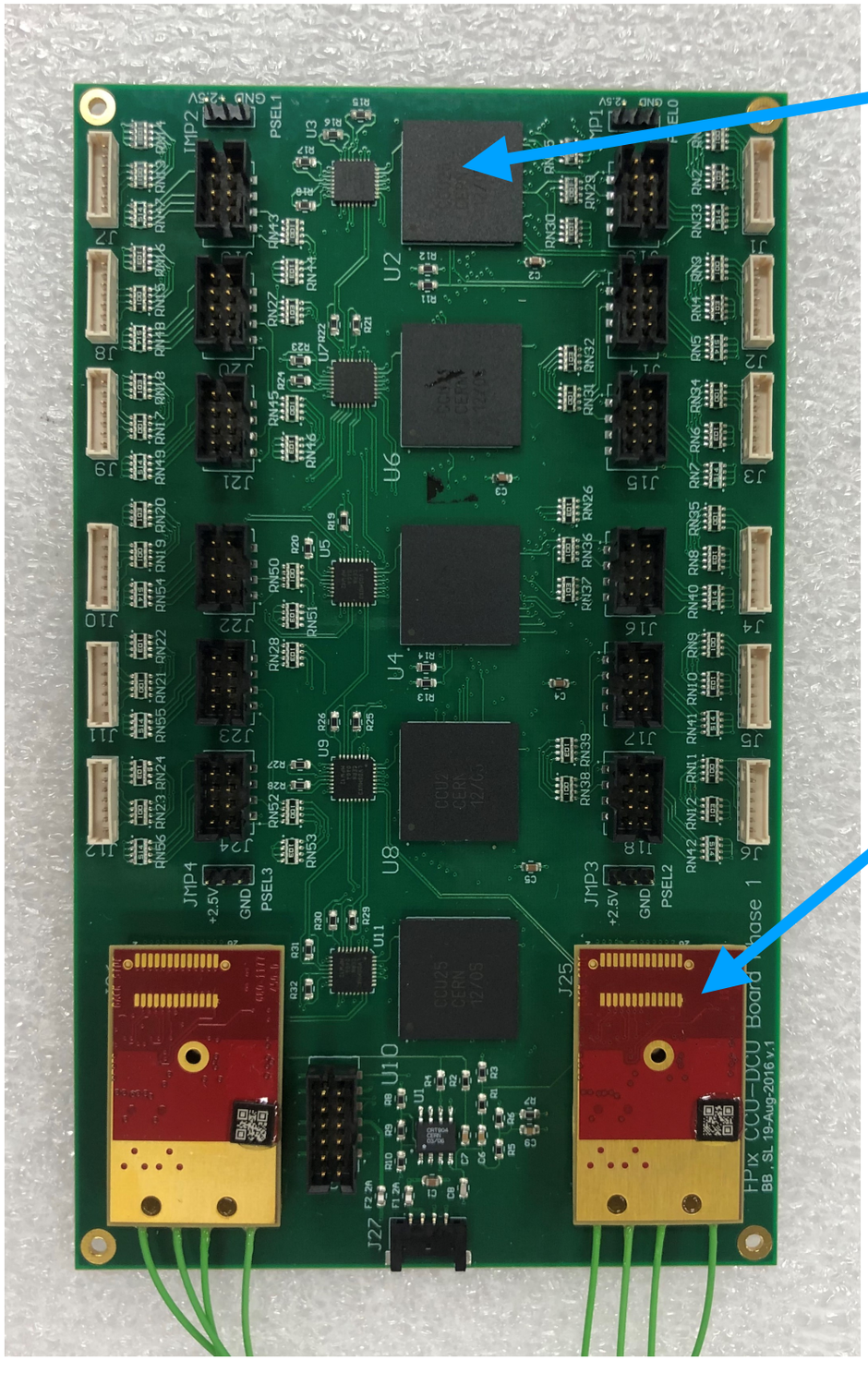
LV for modules

HV for modules

Connector for second layer



FPix CCU board

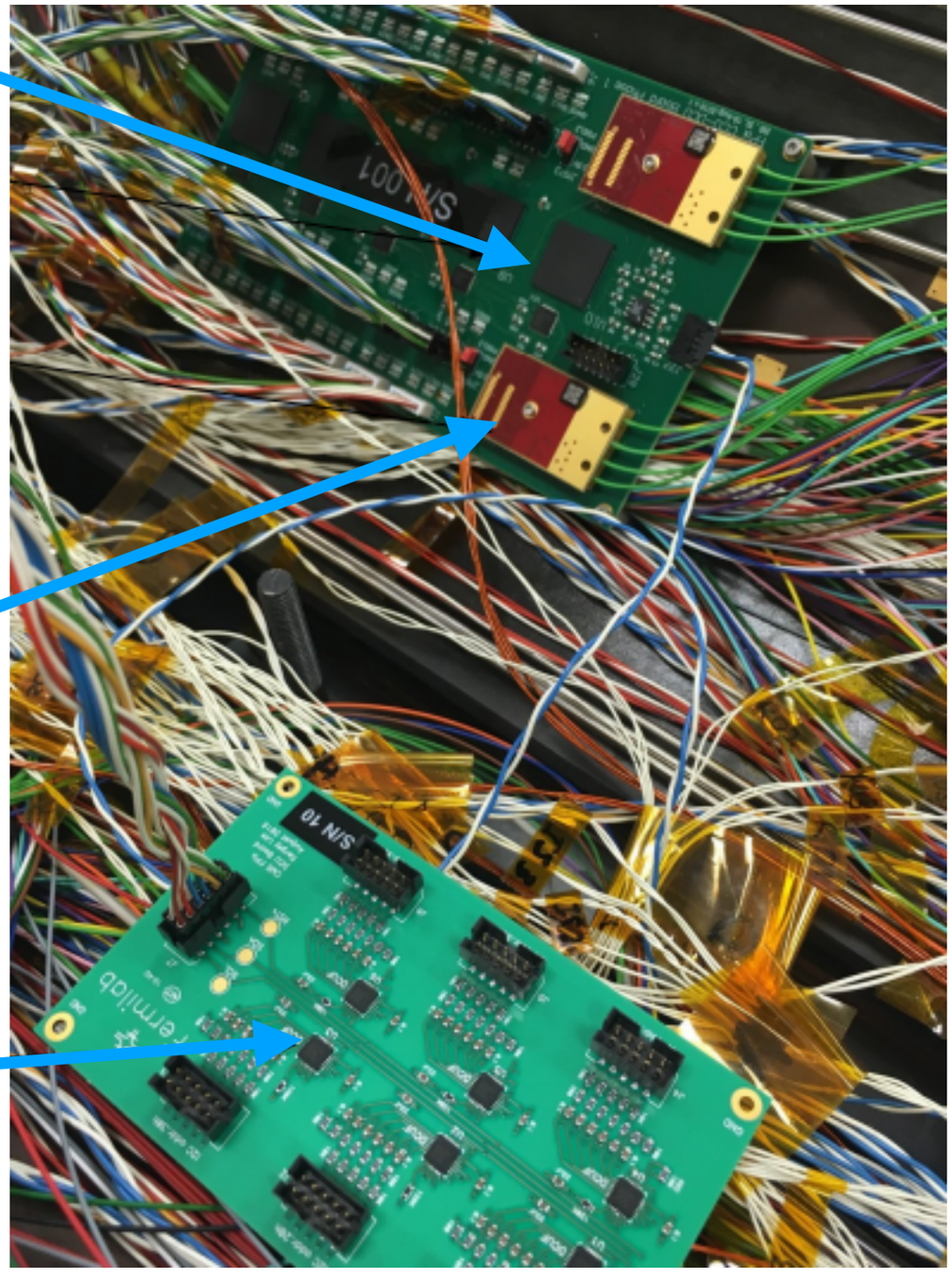


CCU

1 CCU board,
with 4 CCUs + 1
(for redundancy),
in each FPIX
service half-cylinder

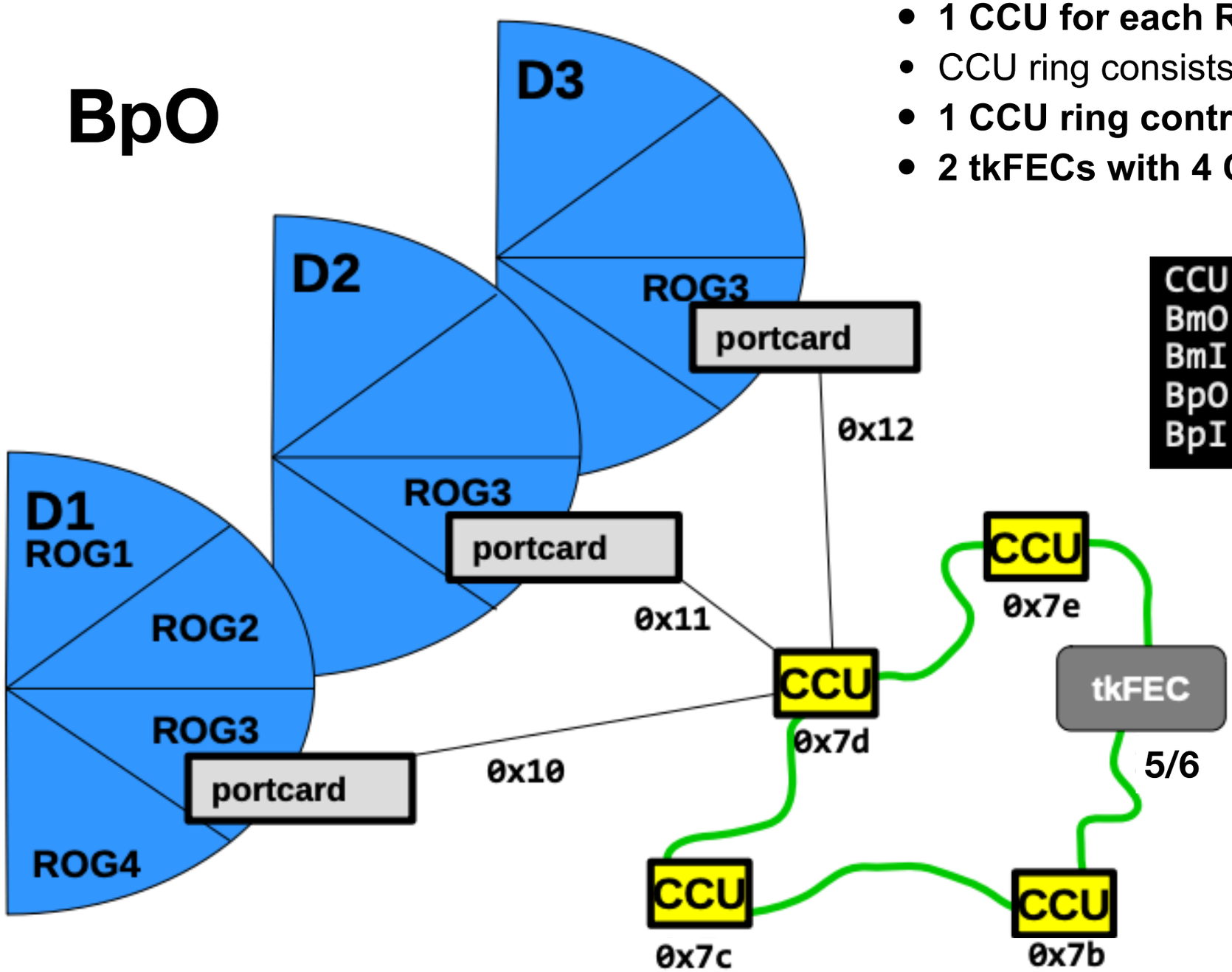
DOH

DCU



FPix CCUs & Read Out Groups

- Portcard = read out group (ROG)
- **1 CCU for each ROG of the 3 disks**
- CCU ring consists of 4 (+1 for redundancy) CCUs
- **1 CCU ring controls 1 half cylinder**
- **2 tkFECs with 4 CCU rings for full FPix**



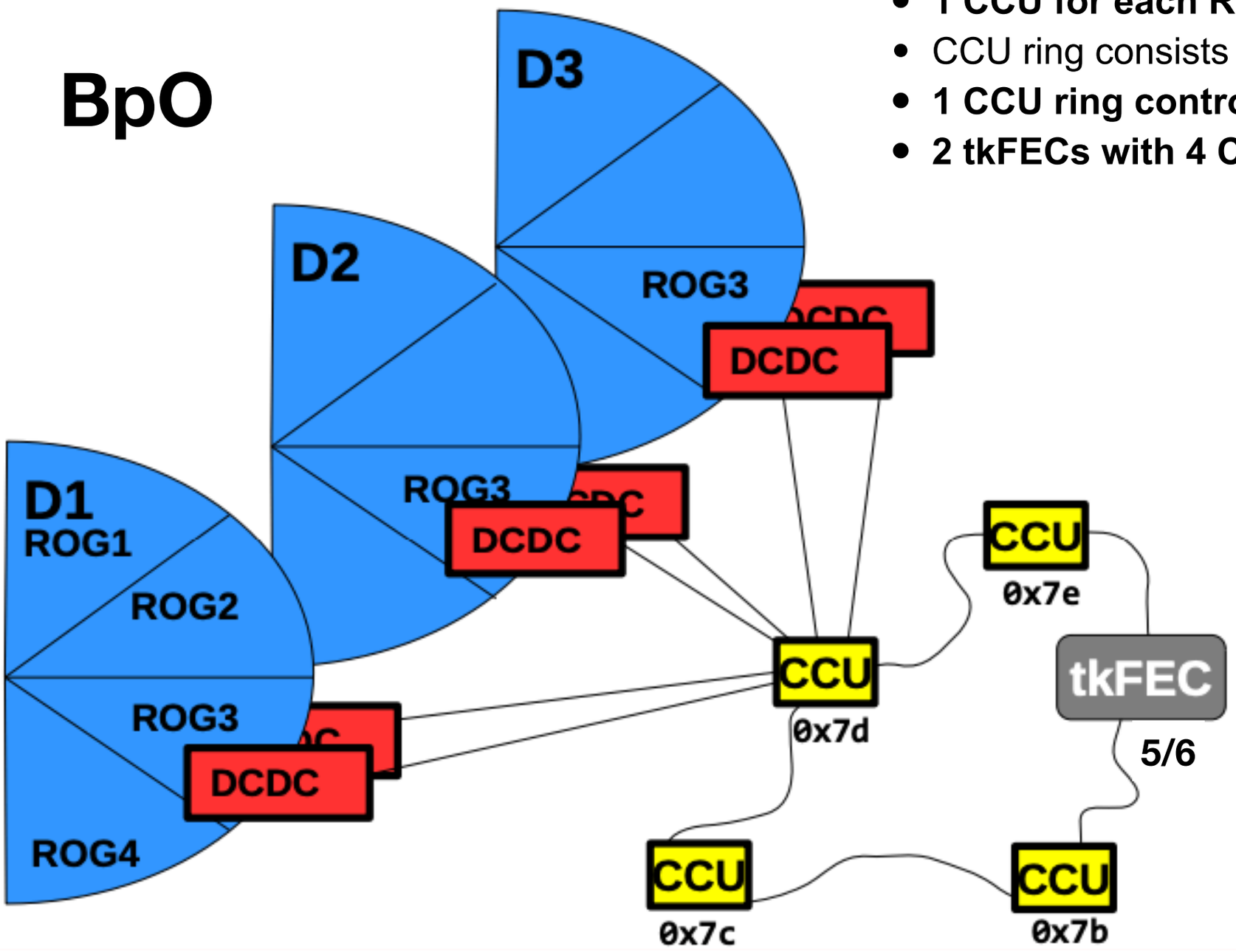

```
CCU ring
BmO: 0 (tkFEC 6)
BmI: 1 (tkFEC 6)
BpO: 2 (tkFEC 5)
BpI: 3 (tkFEC 5)
```

```
CCU addresses
ROG1: 0x7b
ROG2: 0x7c
ROG3: 0x7d
ROG4: 0x7e
```

```
I2C channels
D1: 0x10
D2: 0x11
D3: 0x12
```

FPix Power Groups

BpO

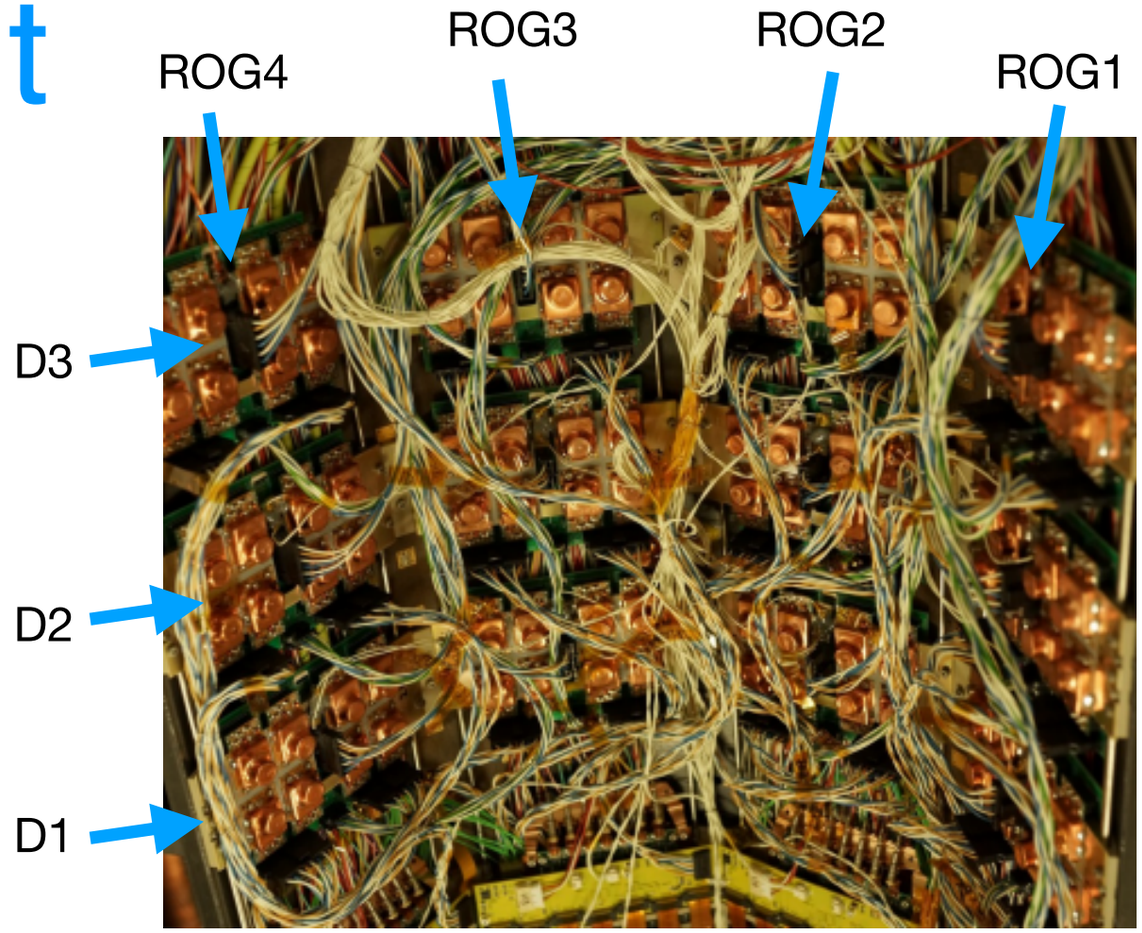


- Portcard = read out group (ROG)
- **1 CCU for each ROG of the 3 disks**
- CCU ring consists of 4 (+1 for redundancy) CCUs
- **1 CCU ring controls 1 half cylinder**
- **2 tkFECs with 4 CCU rings for full FPix**

Each converter group consist of 2 analog and 2 digital converters

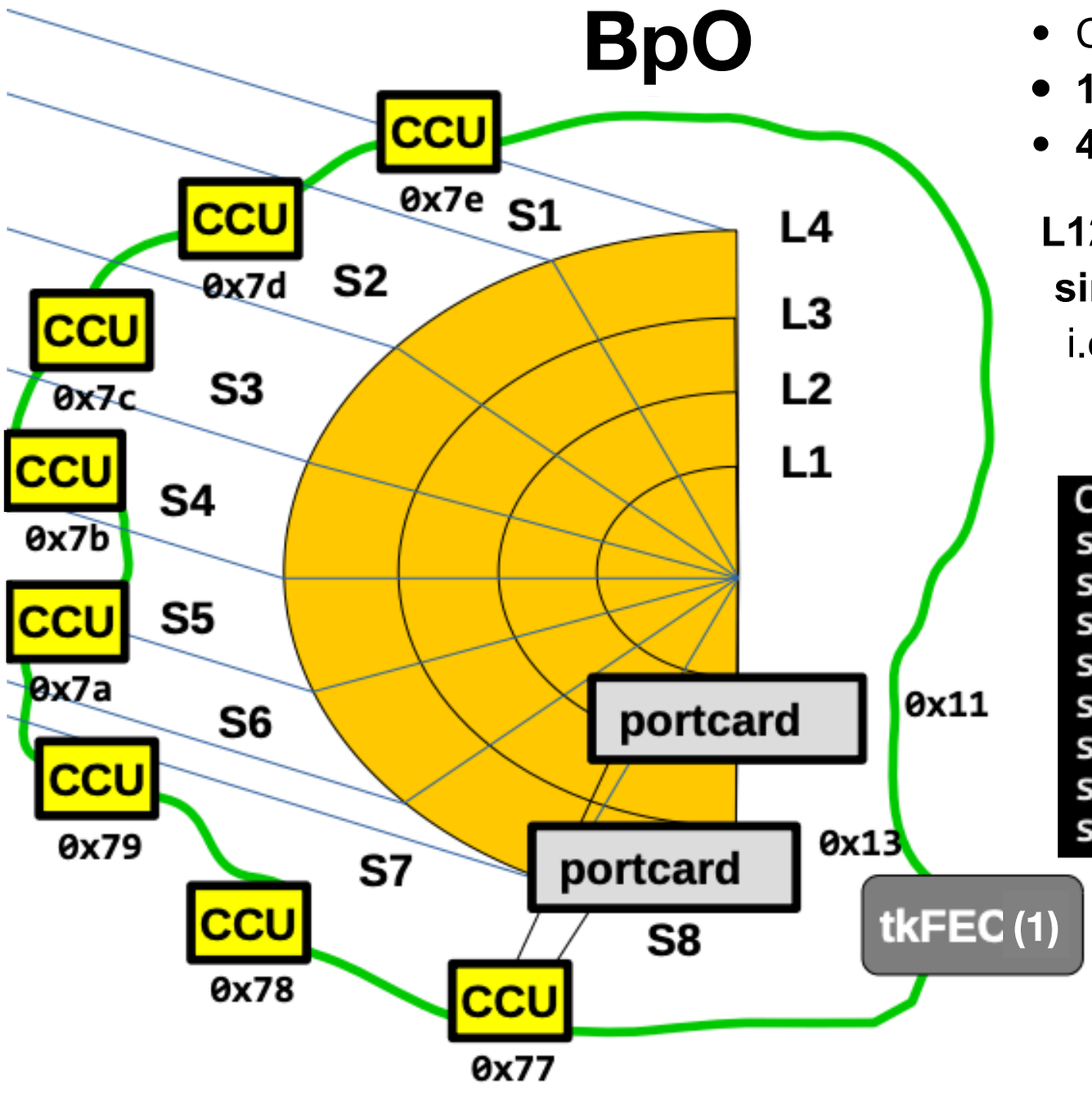
FPix DCDC layout

- DCDC pairs 1+2 and 3+4 are controlled as 2 power groups, each with 4 DCDCs in total (2 analog and 2 digital)
- 4 DCDC converter pairs (1+2+3+4) are mounted on 1 DCDC motherboard
- in each service half-cylinder:
  - 24 power groups
  - 12 motherboards



	BpO															
	ROG4				ROG3				ROG2				ROG1			
D3	A4	A3	A2	A1	A4	A3	A2	A1	A4	A3	A2	A1	A4	A3	A2	A1
	D4	D3	D2	D1	D4	D3	D2	D1	D4	D3	D2	D1	D4	D3	D2	D1
	ROG4				ROG3				ROG2				ROG1			
D2	A4	A3	A2	A1	A4	A3	A2	A1	A4	A3	A2	A1	A4	A3	A2	A1
	D4	D3	D2	D1	D4	D3	D2	D1	D4	D3	D2	D1	D4	D3	D2	D1
	ROG4				ROG3				ROG2				ROG1			
D1	A4	A3	A2	A1	A4	A3	A2	A1	A4	A3	A2	A1	A4	A3	A2	A1
	D4	D3	D2	D1	D4	D3	D2	D1	D4	D3	D2	D1	D4	D3	D2	D1

BPix CCUs & Read Out Groups



- **1 CCU for each sector**
- CCU ring consists of 8 (+1 for redundancy) CCUs
- **1 CCU ring controls 1 half cylinder**
- **4 tkFEC with 4 CCU rings for full BPix**

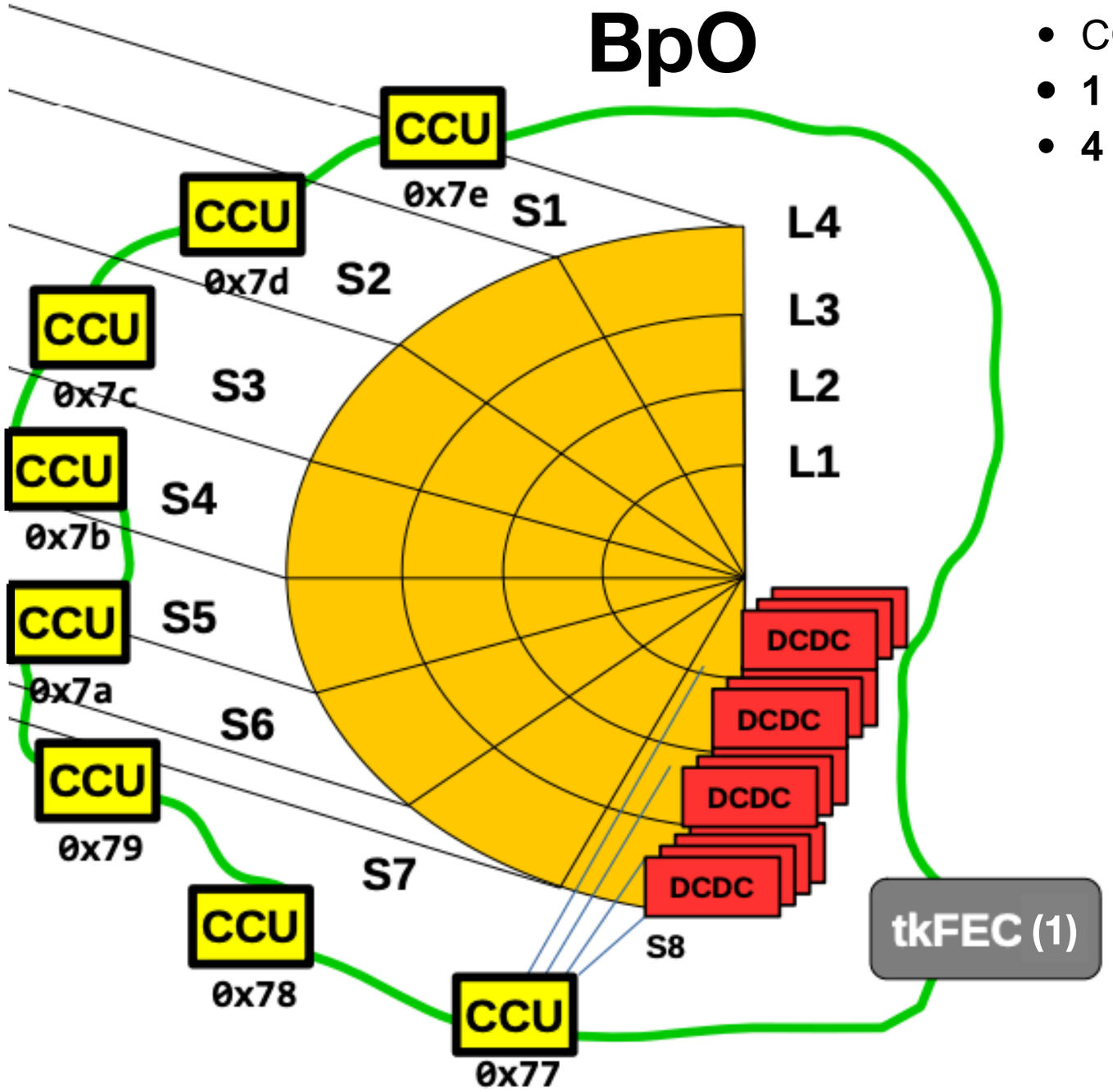
L12 and L34 behave like single readout groups, i.e. 1 “portcard” for L12 and 1 for L34

```
CCU ring
BmO: 1 (tkFEC 3)
BmI: 4 (tkFEC 4)
BpO: 2 (tkFEC 1)
BpI: 3 (tkFEC 2)
```

```
CCU addresses
sector 1: 0x77 (BmO/BpI), 0x7e (BmI/BpO)
sector 2: 0x78 (BmO/BpI), 0x7d (BmI/BpO)
sector 3: 0x79 (BmO/BpI), 0x7c (BmI/BpO)
sector 4: 0x7a (BmO/BpI), 0x7b (BmI/BpO)
sector 5: 0x7b (BmO/BpI), 0x7a (BmI/BpO)
sector 6: 0x7c (BmO/BpI), 0x79 (BmI/BpO)
sector 7: 0x7d (BmO/BpI), 0x78 (BmI/BpO)
sector 8: 0x7e (BmO/BpI), 0x77 (BmI/BpO)
```

```
I2C channels
L12: 0x11
L34: 0x13
```

BPix Power Groups

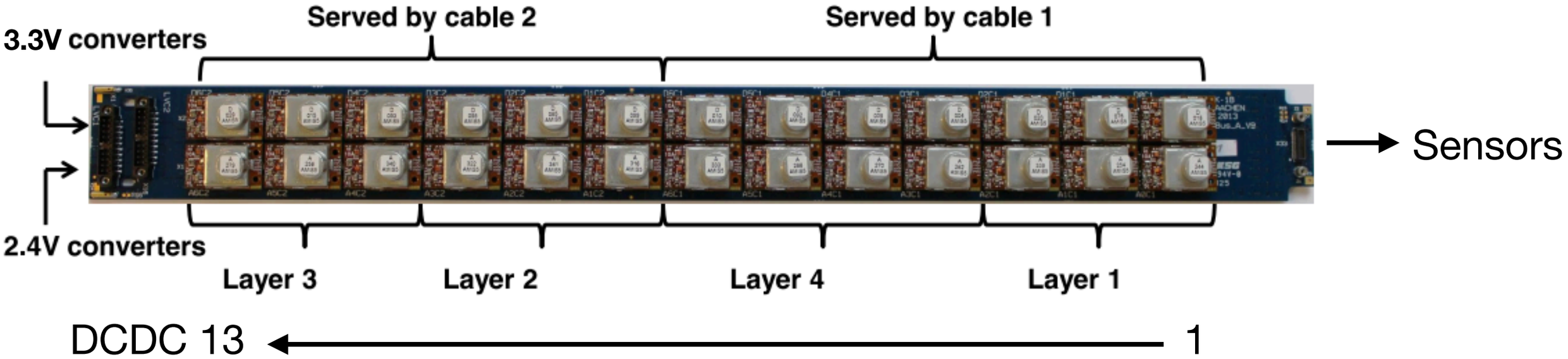


- **1 CCU for each sector**
- CCU ring consists of 8 (+1 for redundancy) CCUs
- **1 CCU ring controls 1 half cylinder**
- **4 tkFEC with 4 CCU rings for full BPix**

Each converter group consists of 1 analog and 1 digital converters

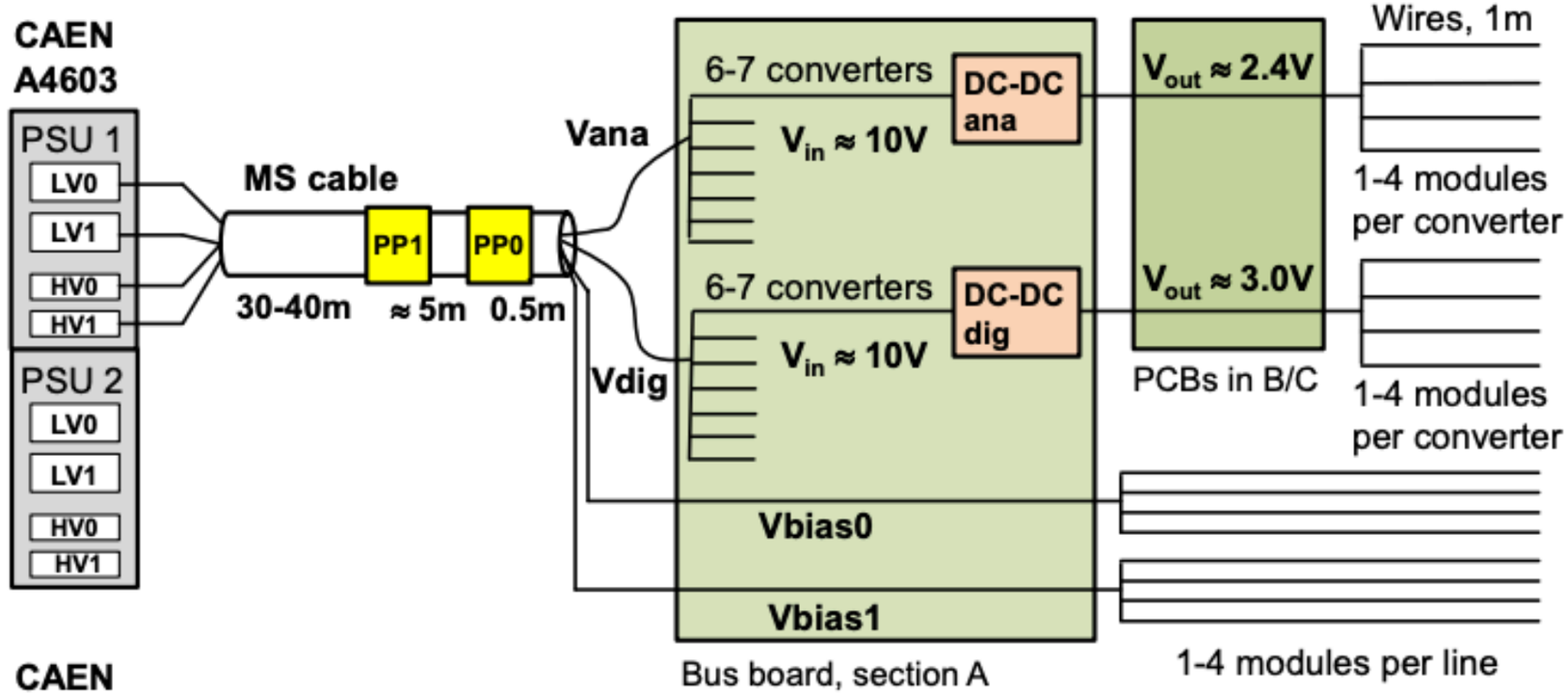
LYR	PG	DCDC
1	1	1
1	1	2
1	1	3
4	1	4
4	1	5
4	1	6
4	1	7
2	2	8
2	2	9
2	2	10
3	2	11
3	2	12

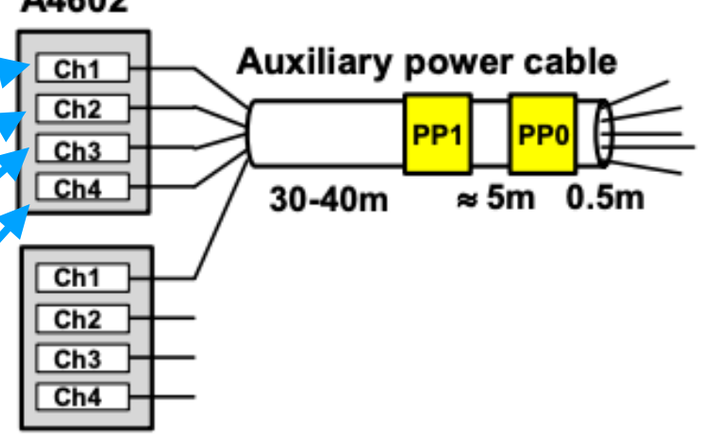
BPix DCDC layout



- Layer14 and Layer23 are each 1 power group
- 13 pairs of DC-DC converters are mounted on 1 bus-board
- 8 bus-boards for each service half-cylinder

Power system



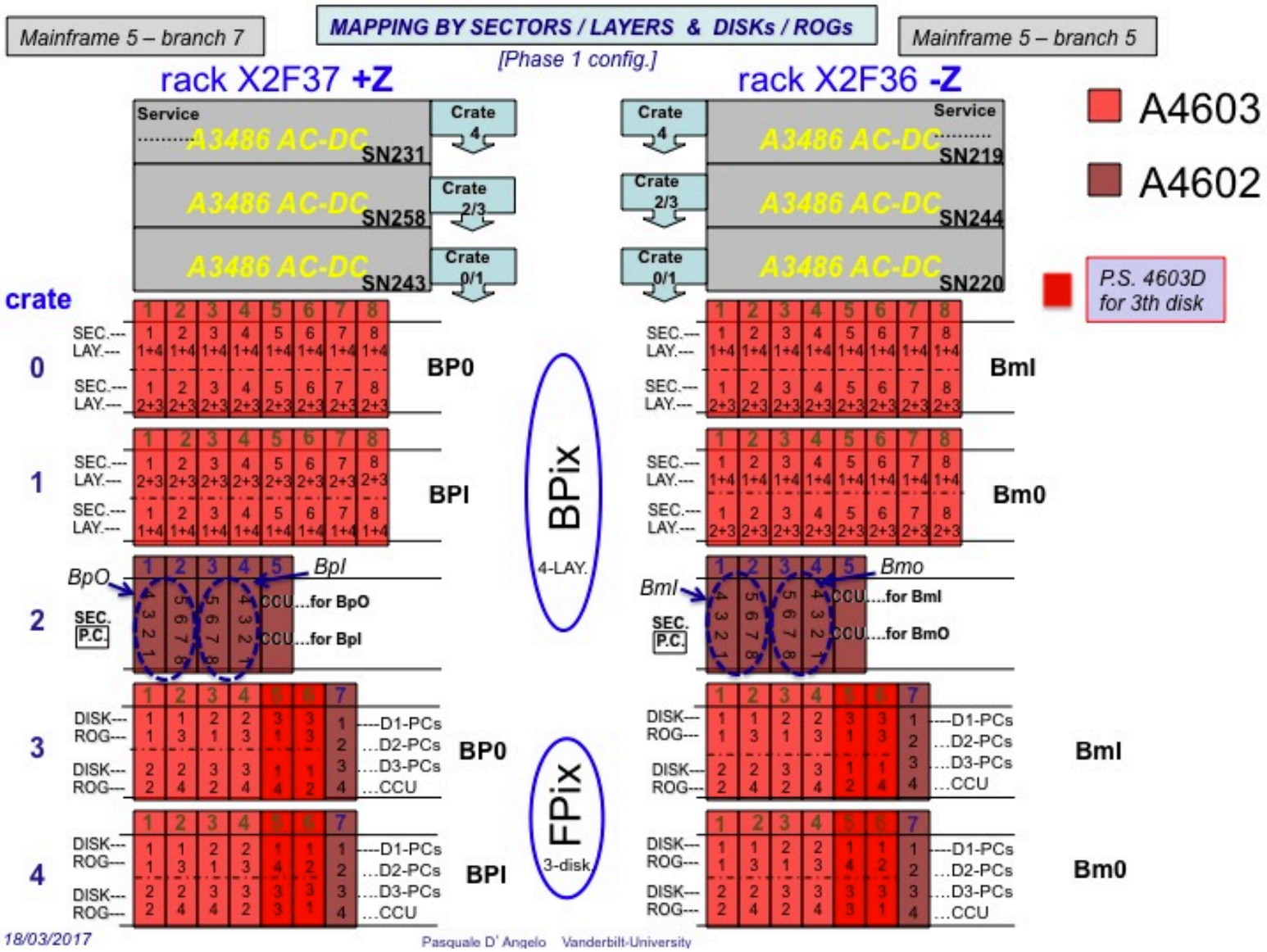


5 x power to POHs etc.
of one readout slot,
or to CCUs of one control ring

Different Power requirements

- Low Voltage: Analog and Digital module power
- High Voltage: Sensor power
- Control Voltage: Auxiliary electronics power

Front-end racks



UXC side

Rack location: X2 F 37

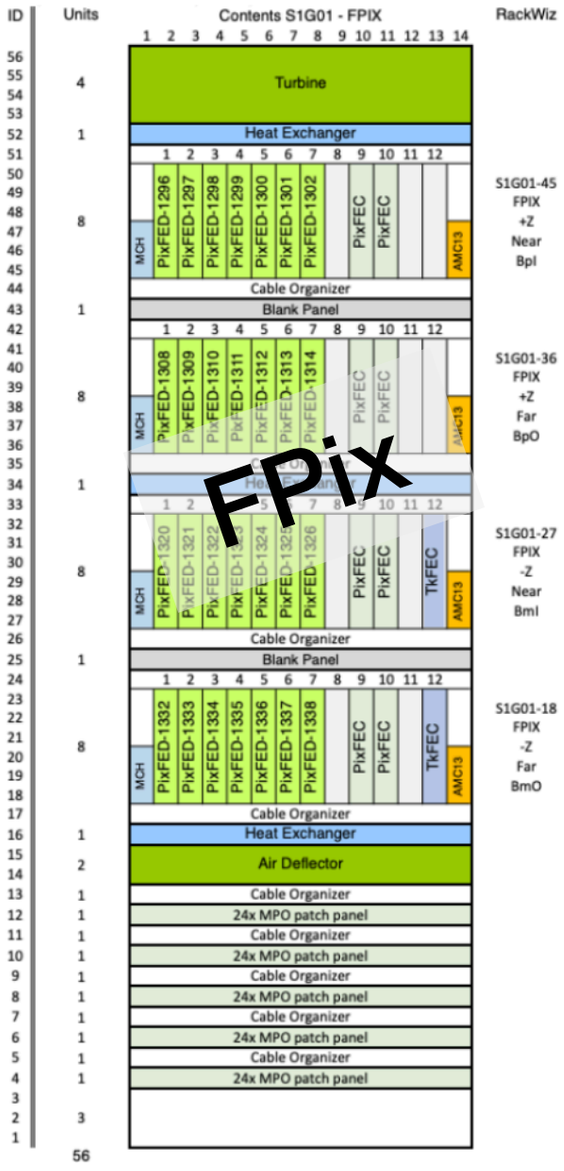
UXC floor rack

X2F37 for +Z end

X2F36 for -Z end

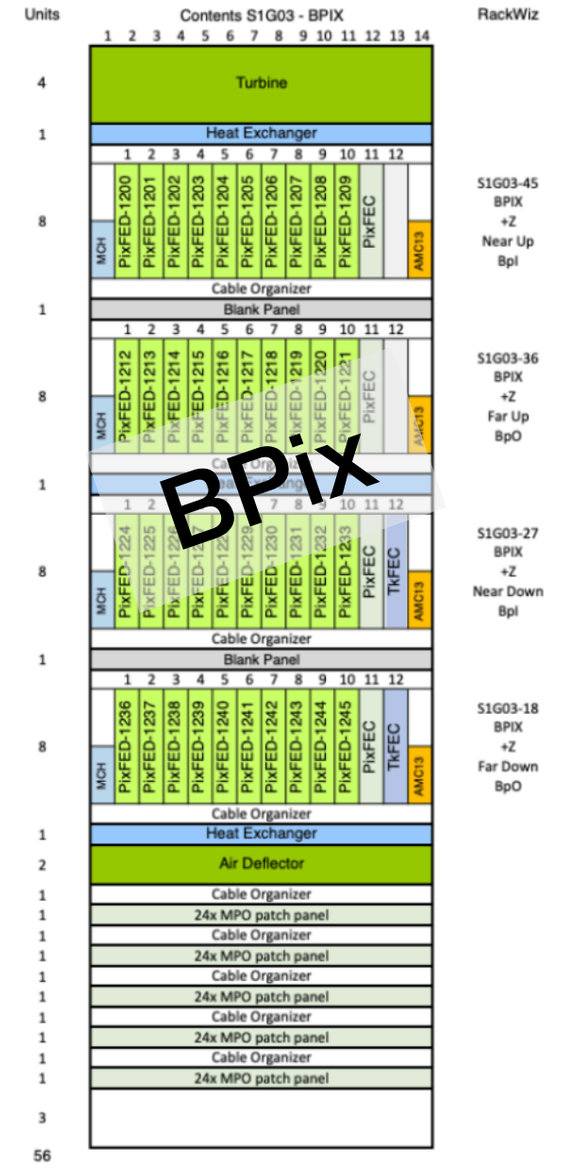
Back-end racks

S1G01

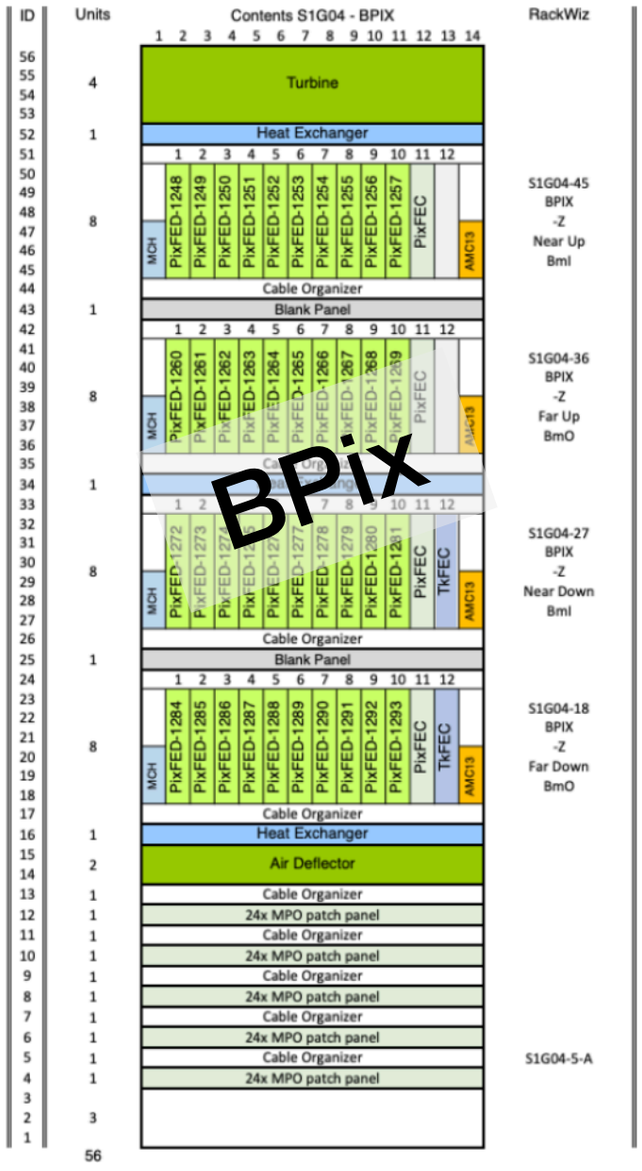


S1G02

S1G03



S1G04



Rack location: S1 G 01

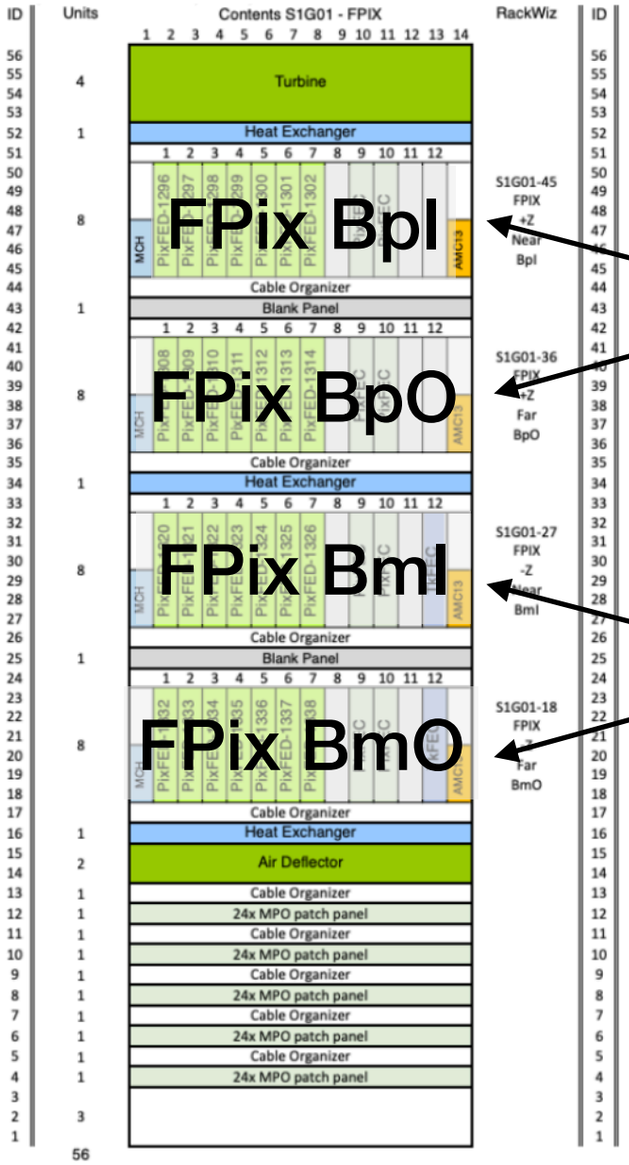
room row rack

Crate location: S1G01-45

hight in standard units

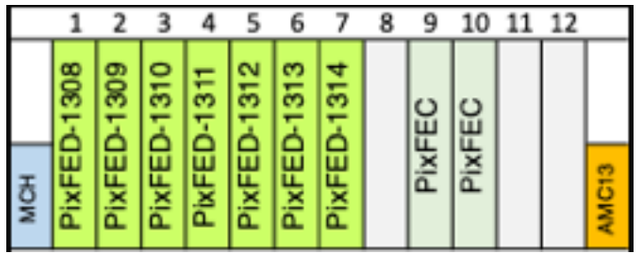
Back-end racks layout: FPix

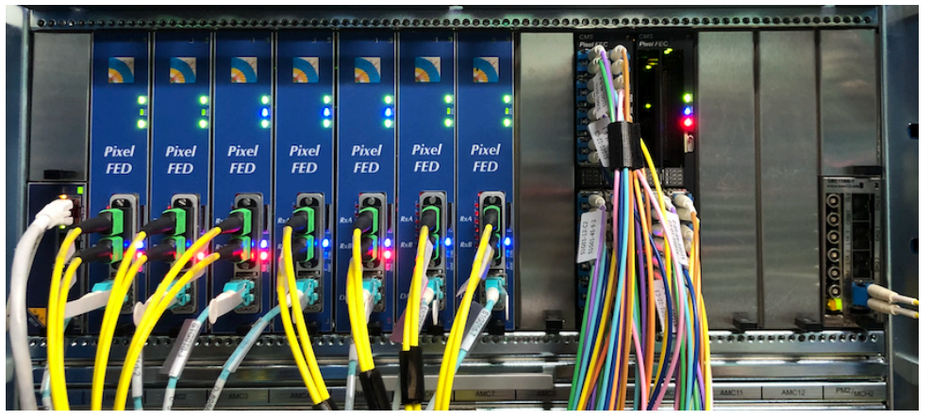
S1G01



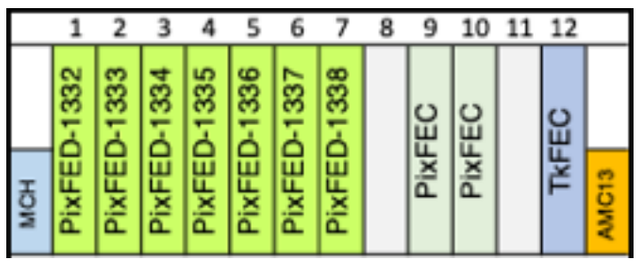
4 FPix crates
1 crate = 1 half cylinder

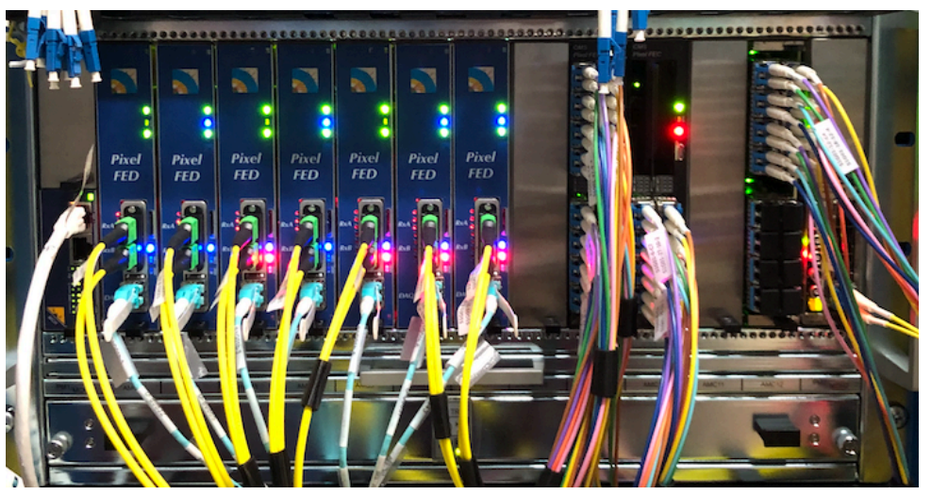
7 FEDs
2 PixFECs



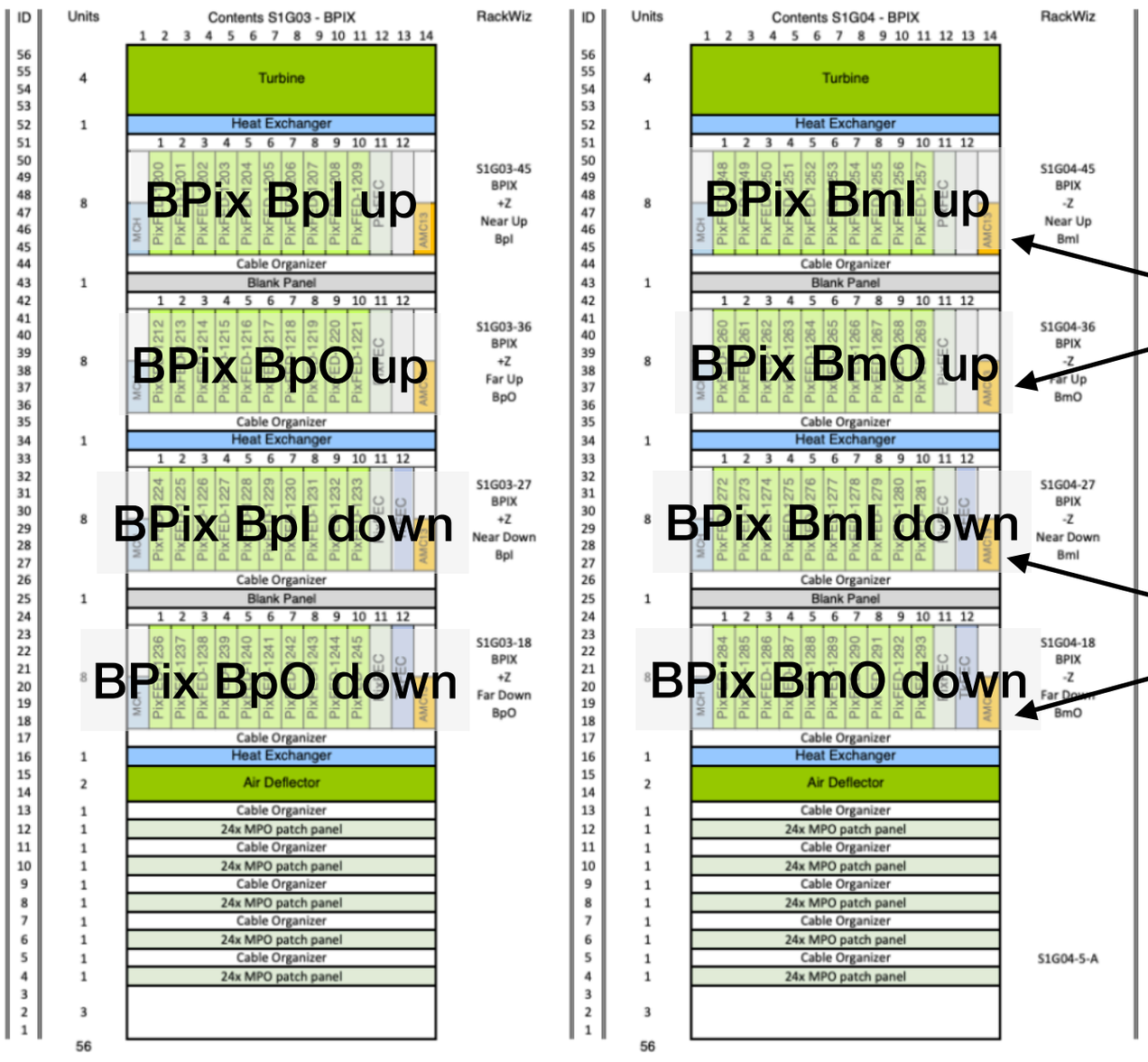


7 FEDs
2 PixFECs
1 TkFEC





Back-end racks layout: BPix



10 FEDs
1 PixFEC

10 FEDs
1 PixFEC
1 TkFEC

8 BPix crates
1 crate = 1/2 half cylinder

Layer 1 module overview

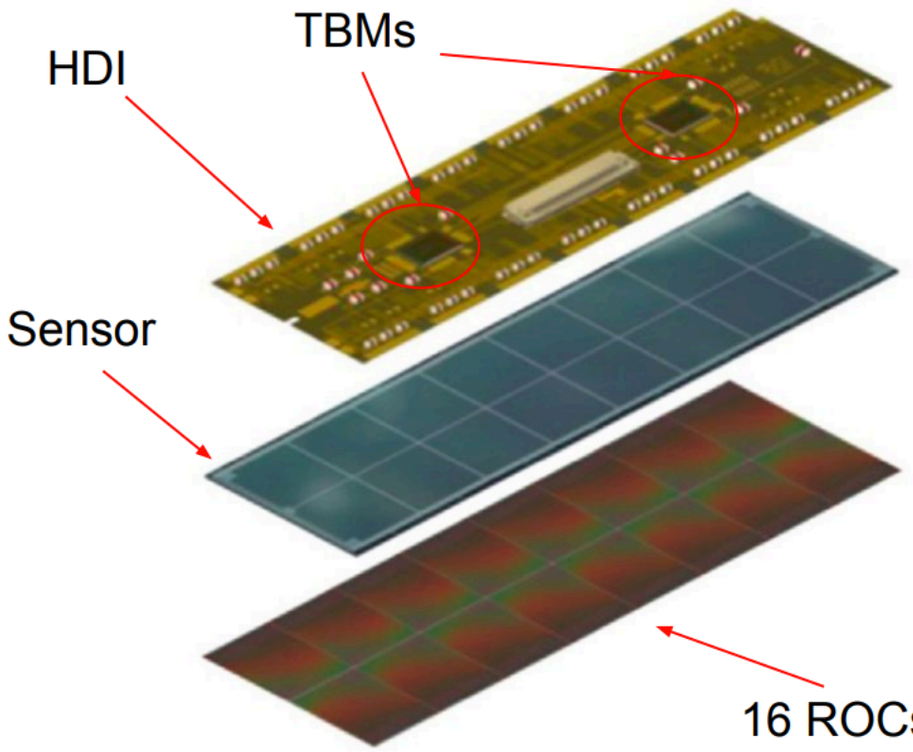
- **High-density interconnect (HDI10d)**
  - glued on top of the sensor and wire-bonded to readout chips (ROCs)
  - routes control and data signals between ROCs and token bit manager chips (TMBs)
  - routes high-voltage to the sensor

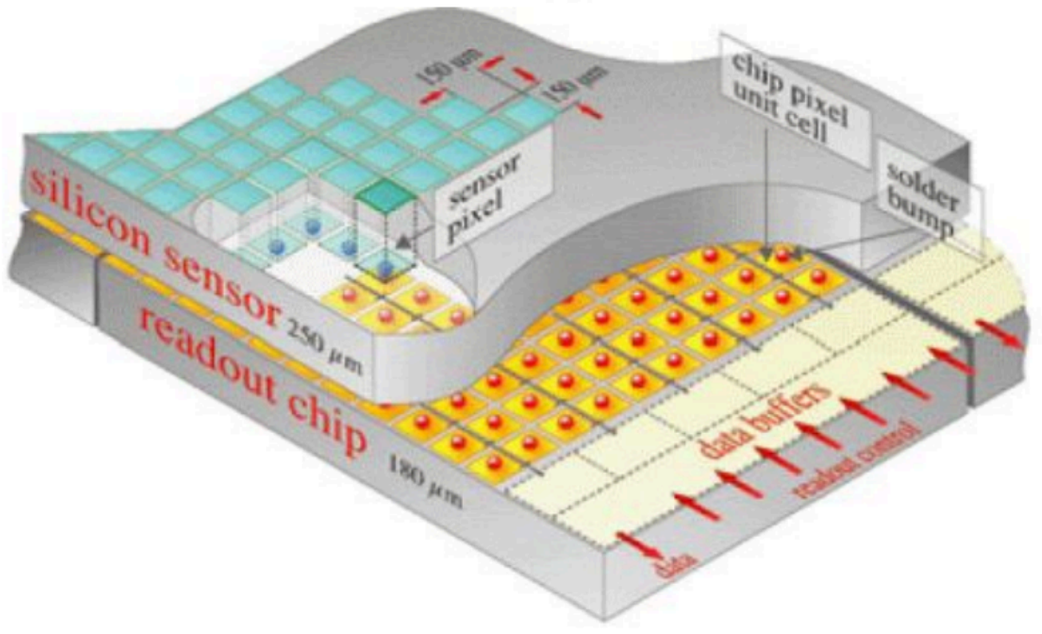
- **Silicon sensor**
  - “sandwiched” between HDI and ROCs
  - connected with ROCs through bump-bonds

- **Read out chips (PROC600 v4)**
  - 16 chips at the bottom of the modules
  - read signals from sensor, process them and send them to TBM

- After testing campaign, modules were ranked based on their quality and accordingly assigned to appropriate locations on Layer 1 (highest quality modules in the center)

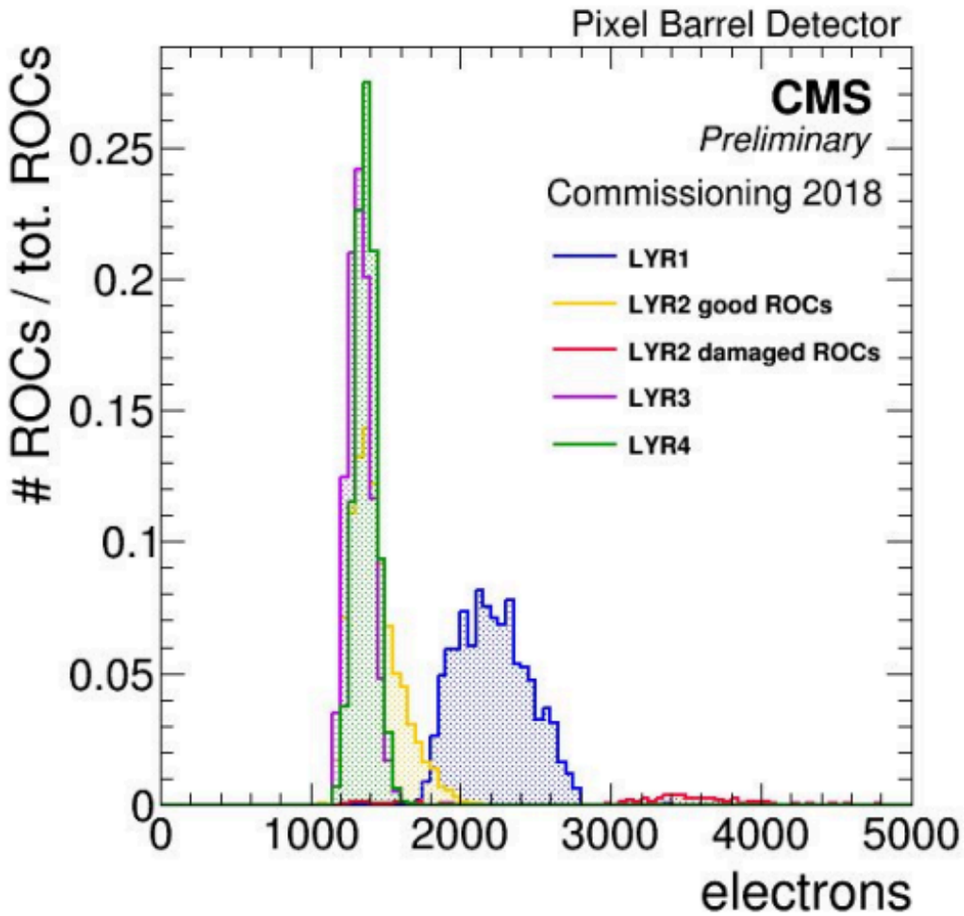
- The entire readout of a module in Layer 1 is designed to cope with a particle hit rate of up to 600 MHz/cm²





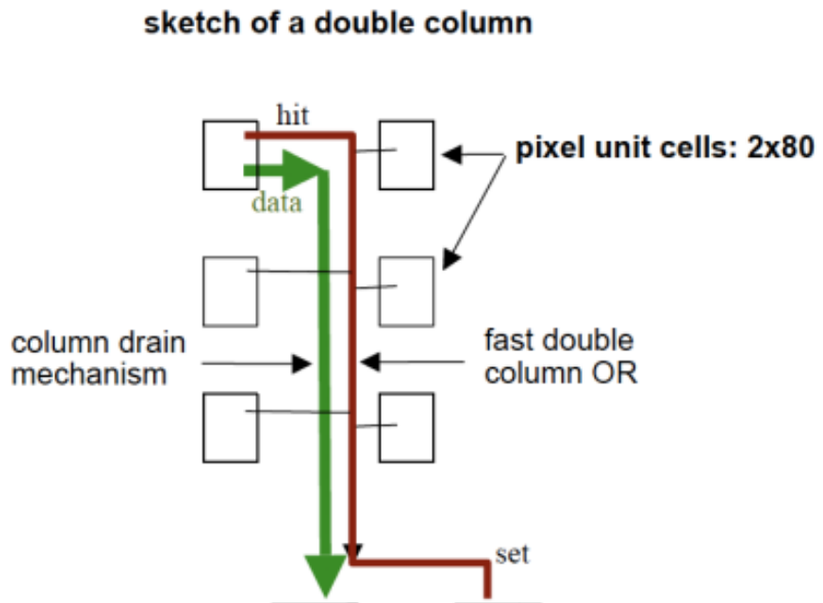
Operation challenges in Run 2

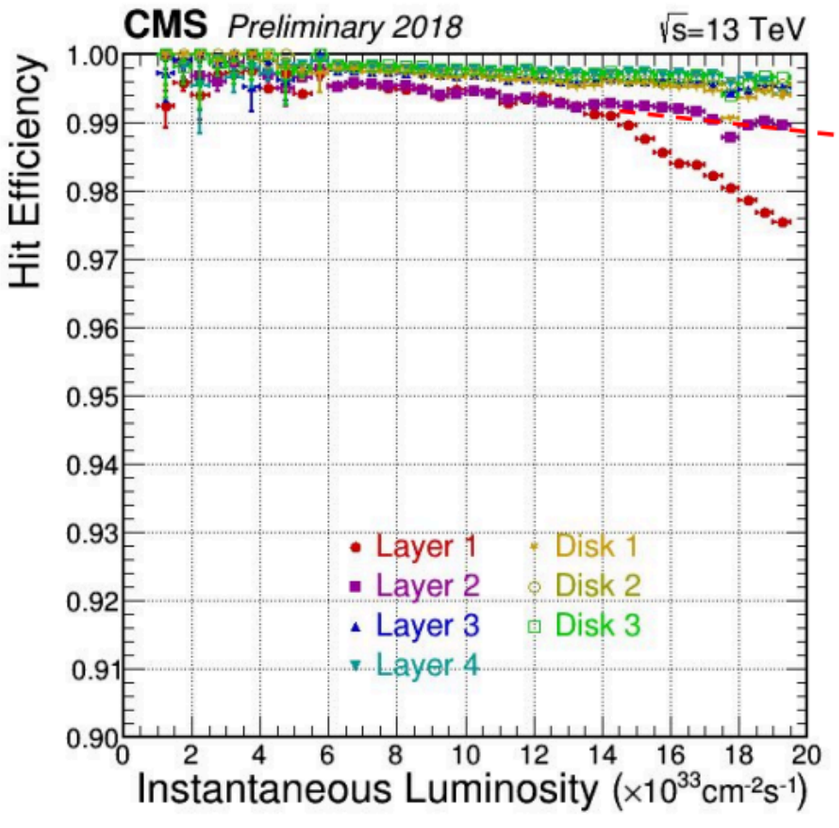
- **Crosstalk**
  - Layer 1 has higher threshold than expected, mainly due to electronics crosstalk
  - the injection capacitor was too close to the trim lines of the pixel
  - the source could be mitigated via “programming”, but a layout change solved the problem
  - **problem addressed in new version of PROC600v4**



Operation challenges in Run 2

- **Dynamic Inefficiency**
  - hits are stored in chip periphery (double column drain architecture)
    - timestamp - timestamp buffer
    - data - data buffer
  - due to a glitch we lose synchronization between data and time, leading to loss of data
  - **problem addressed in new PROC600v4**



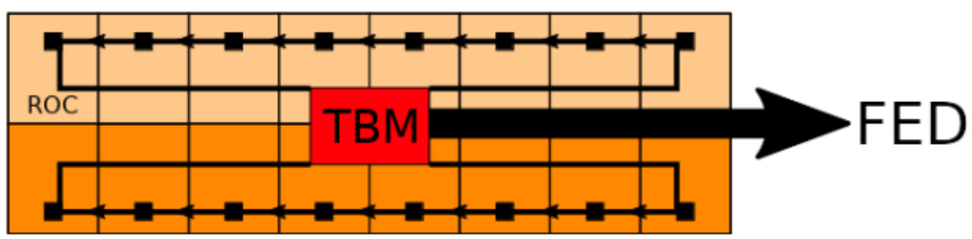


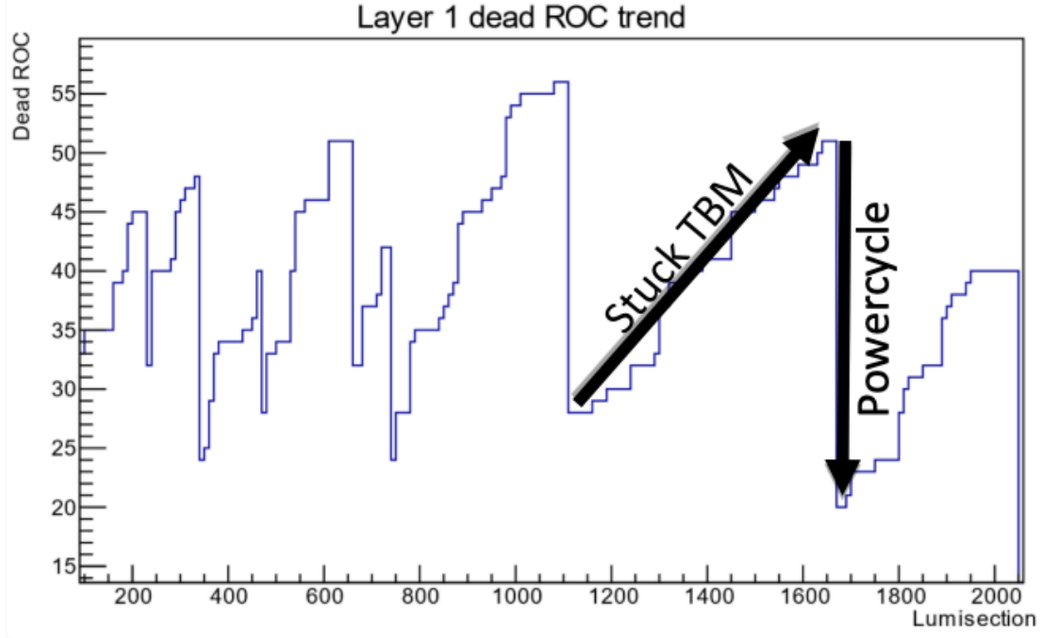
Expected for new Layer 1

Overall excellent efficiency from Phase-1 Pixel detector already in Run 2
but now we have a new Layer 1 which will improve performance substantially

Operation challenges in Run 2

- **Stuck TBMs**
  - when a L1 trigger is received, the TBM collects data from all readout chips and sends them to a FED
  - this process is affected by Single Event Upset (SEU): TBM can get stuck in one state, leading to loss of data
  - the only way to recover is through a **power cycle**
  - new TBM for Layer 1 (TBM10d) solves this problem
    - **reset of TBM is possible in new version**

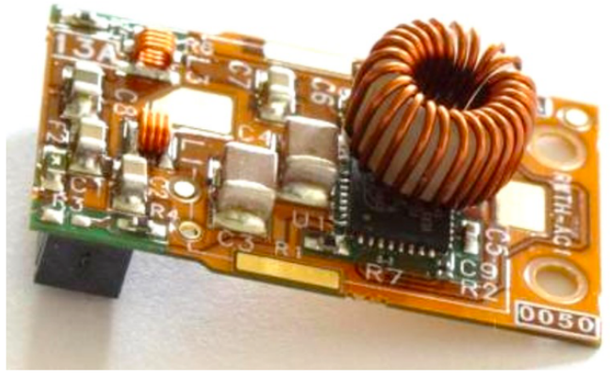




SEU rate during 2018: ~ 30/fb-1

Operation challenges in Run 2

- **DCDC converters failure**
  - resulted from a fault in the FEAST chip design
  - when a DCDC is disabled, a charge builds up on the circuit due to irradiation (>10kGy) causing the DCDC to break
  - impact on operations (2018):
    - converters not used to power cycle modules
    - power cycling needed for stuck TBMs - stuck TBMs accumulated
    - reduced supply voltage to 9V
    - power supplies (CAEN) used to power cycle modules between beams
    - high current trips in power groups with higher share of modules
    - raised trip limits, programmed to reduce start up current in power groups
    - disabled a few DCDC converters to prevent trips while power cycling/ turning on detector -> **no broken DCDCs in 2018** (active fraction ~94.5%)

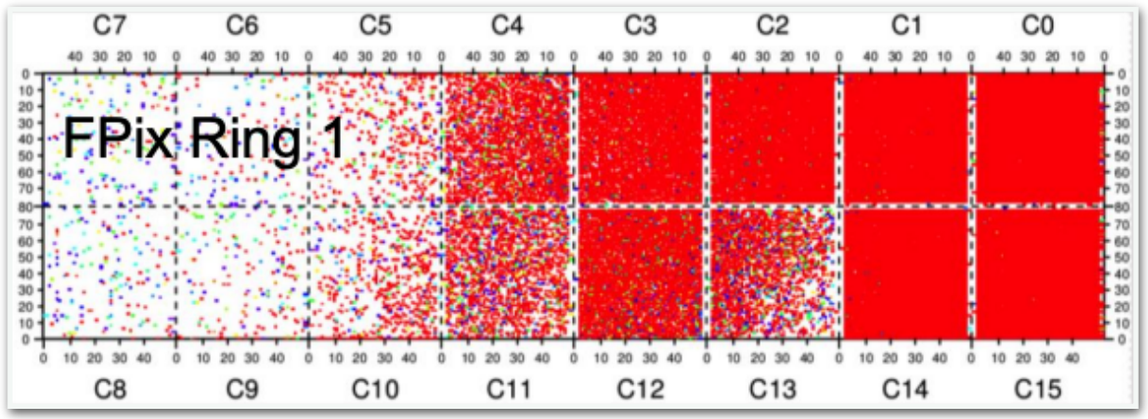


Mar. 2017	5th Oct. 2017	Dec. 2017	YETS 2017/2018	May 2018
Phase-1 upgrade done, Started data taking with 95.6% active detector	1st DCDC Converter Broke	5% converters not working, 11% detector not active	Detector Extracted, Replaced all DCDC with bigger fuse, problem not yet understood	Problem reproduced in the lab (IRAD,X-ray), reason understood

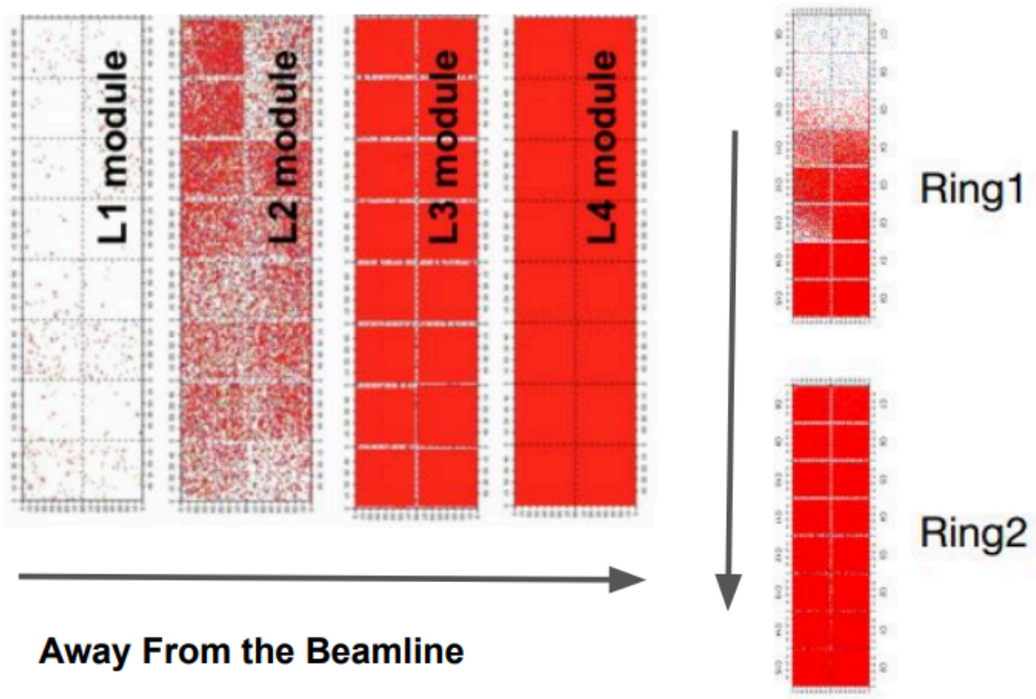
New production of DCDC converters with new version of FEAST chips for Run 3 solves the problem

Operation challenges in Run 2

- **DCDC damaged modules**
  - DCDC damaged modules were not correctly powered
  - sensor leakage current cannot be drained efficiently if the ROC is not powered
  - bias voltage (HV) ON and module power (LV) OFF leads to bad grounding
  - the leakage current is drained through the pre-amplifier, damaging the pre-amplifier and the module
  - the damage seems to accumulate with radiation and distance from beamline
  - 6 (accessible) Layer 1 modules replaced during 2017-18 YETS out of total 8 damaged modules in Layer 1
  - accessible DCDC-damaged modules in Layer 2 were replaced during LS2



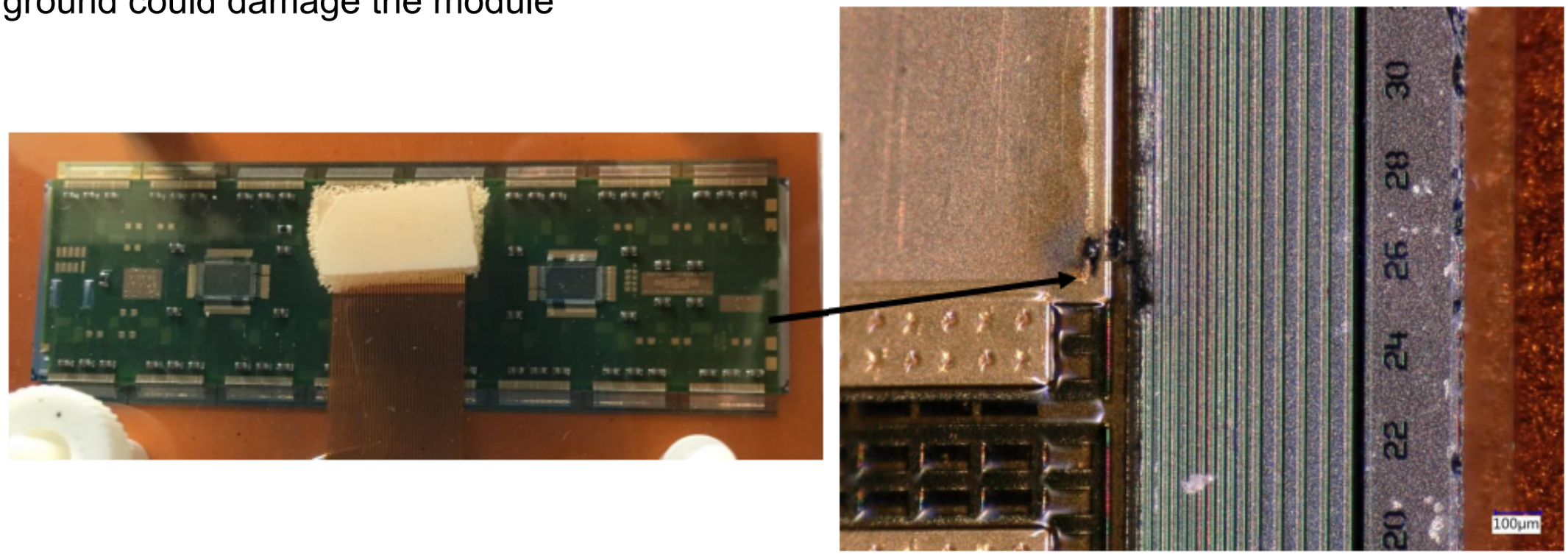
Damages due to HV on and LV off



HV problems in Run 2

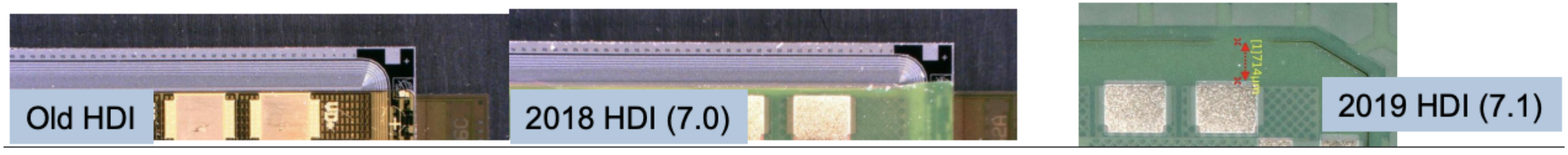
Problem:

- the edge of the Layer 1 HDI was not covering the sensor enough, so a HV spark to pad ground could damage the module

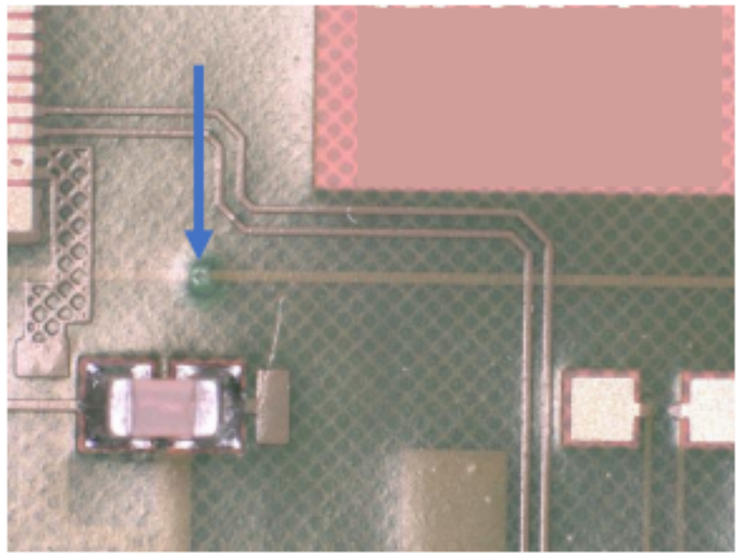


Solution:

- for the new Layer 1 the HDI boarder was increased to cover the guard rings completely

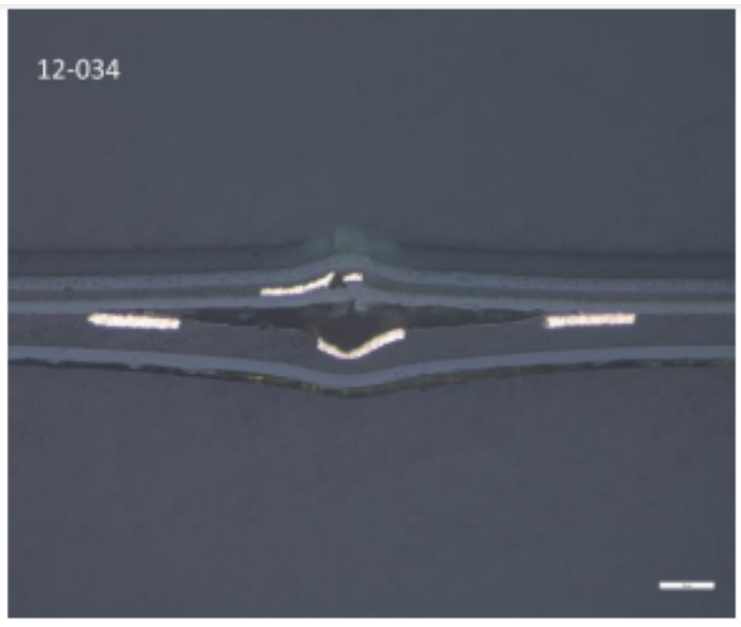


HV problems in Run 2



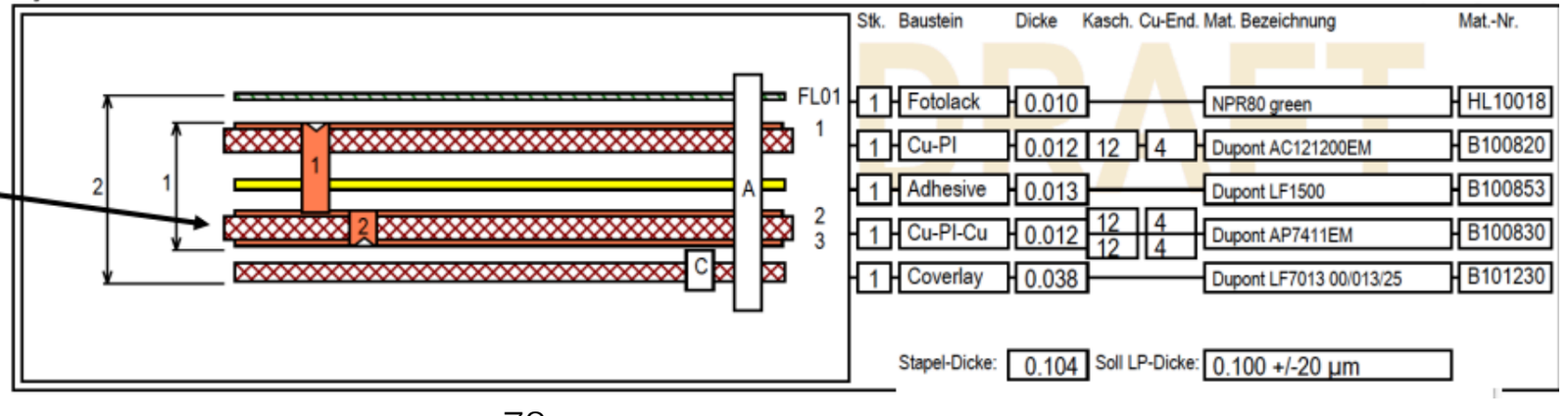
- While testing the new HDIs at 1100V (800V maximum in the detector, originally designed for 600V) a short occurred

- Further test showed that it's not so difficult to break an HDI
  - humidity probably has an effect (or opening the test box)



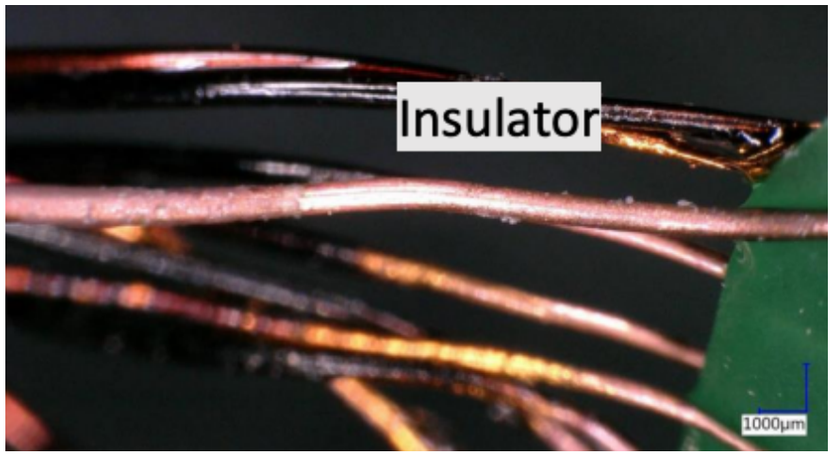
- New HDI without a ground grid around the HV line
  - no problems observed for long testing at 1100V

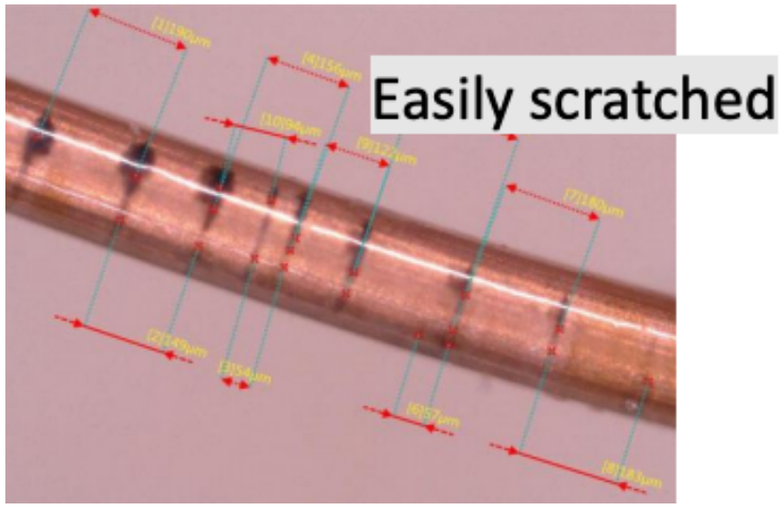
Insulator should hold 3kV

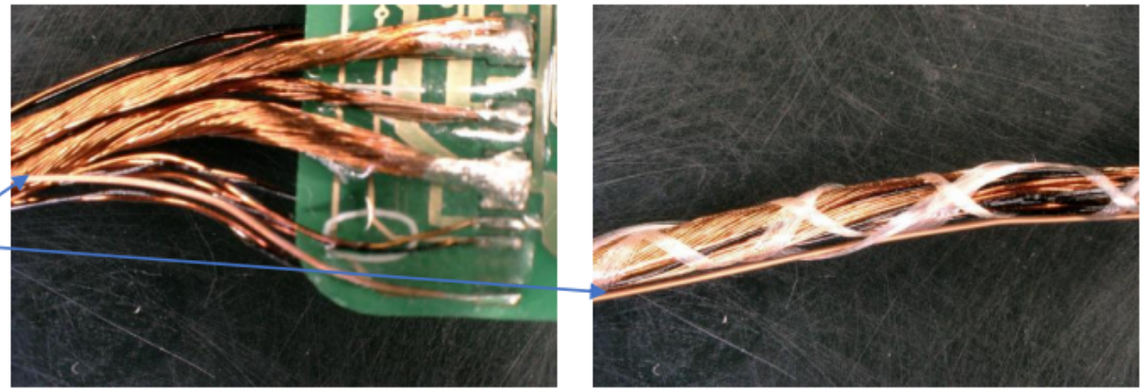


HV problems in Run 2

- New module cables showed HV problems:
  - insulator was stripped too far back
  - PEEK insulation was too susceptible for mechanical damage







- New thicker PEEK insulation solved both issues

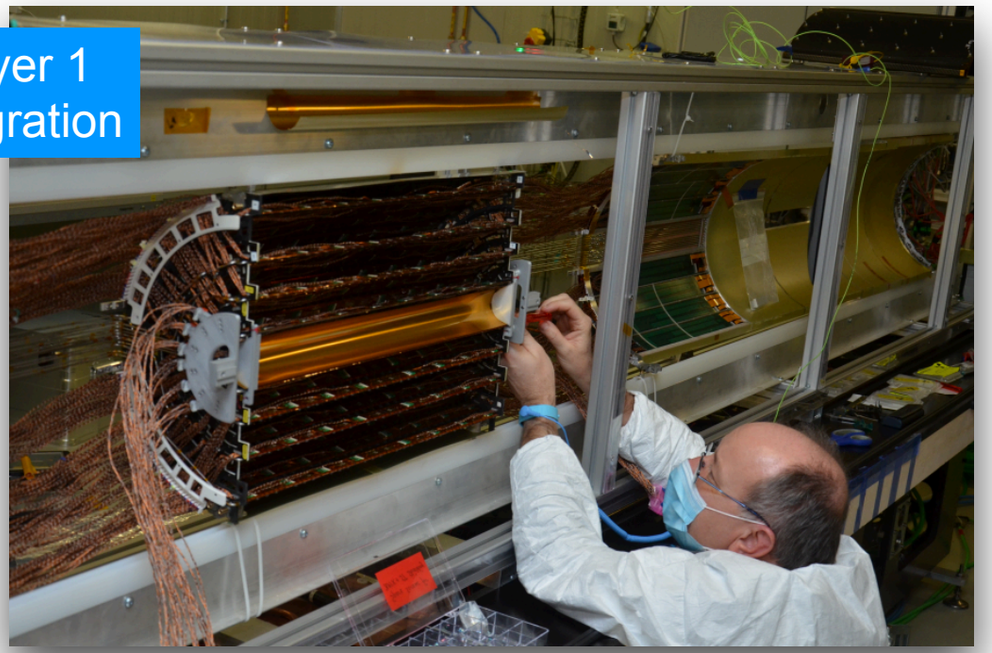
Layer 1 and 2 work

- **Installed new Layer 1 modules:**
  - delivered to CERN at the end of October 2020, after work at PSI
  - tested after unpacking (post-transportation) at beginning of 2021
    - overall ~6 weeks of delay w.r.t. the original plan due to the Covid situation
  - integrated with all cabling and cooling connections
- **Replaced 8 (out of 10) modules in Layer 2 damaged by HV ON / LV OFF condition**
  - 2 not accessible (facing outwards)

Final work at PSI

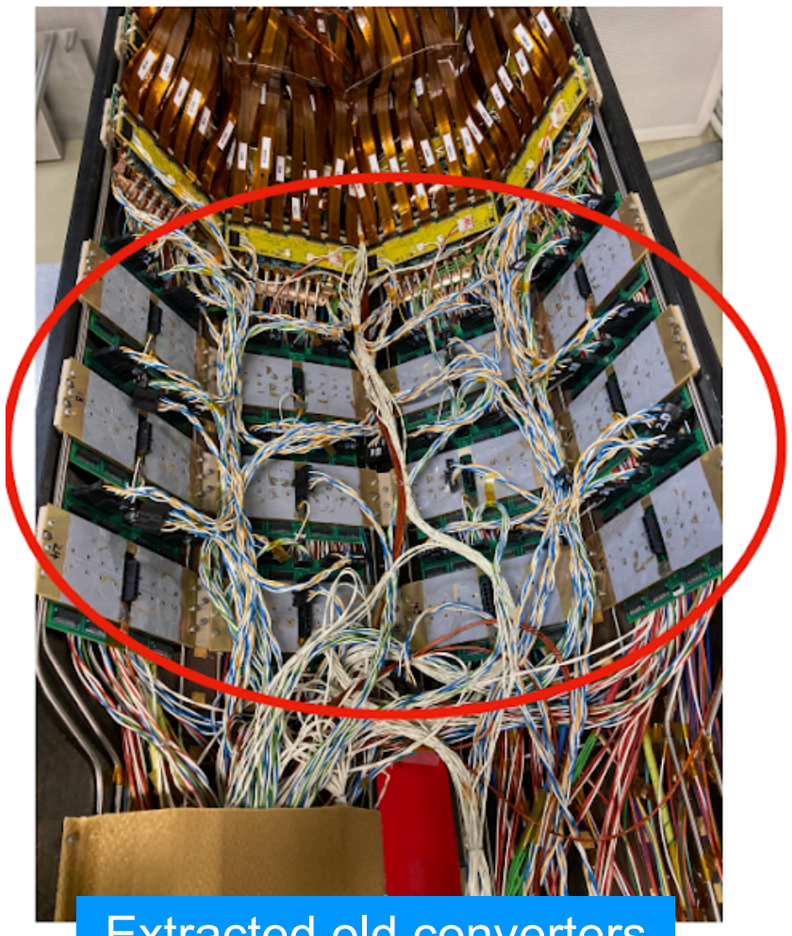
Delivery to P5

Layer 1 integration

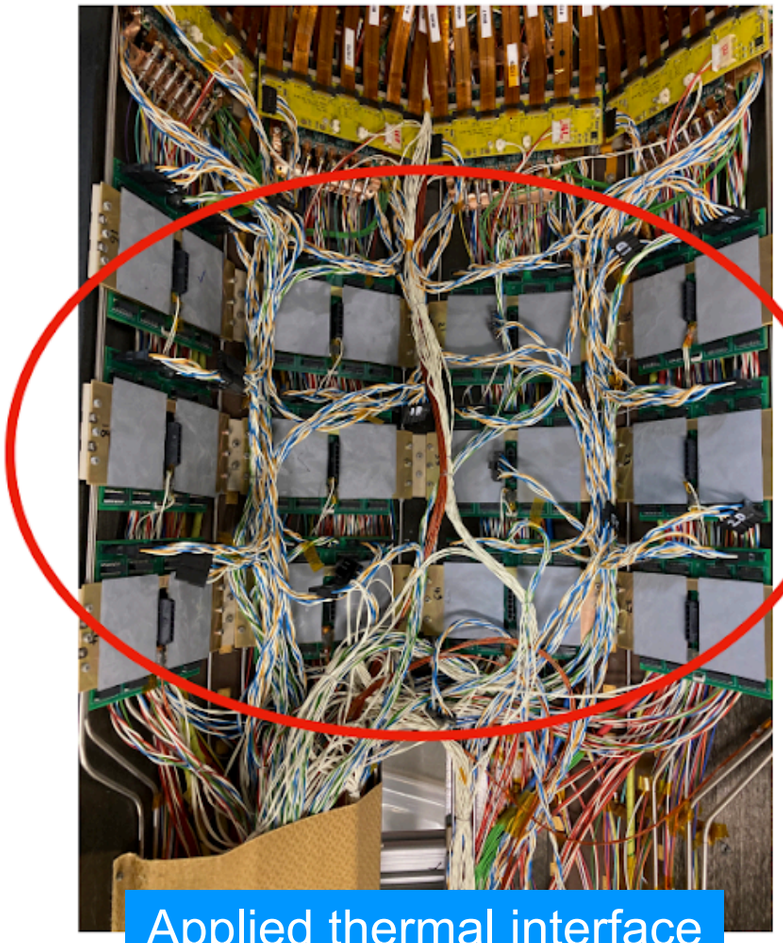


Layer 1 cabling

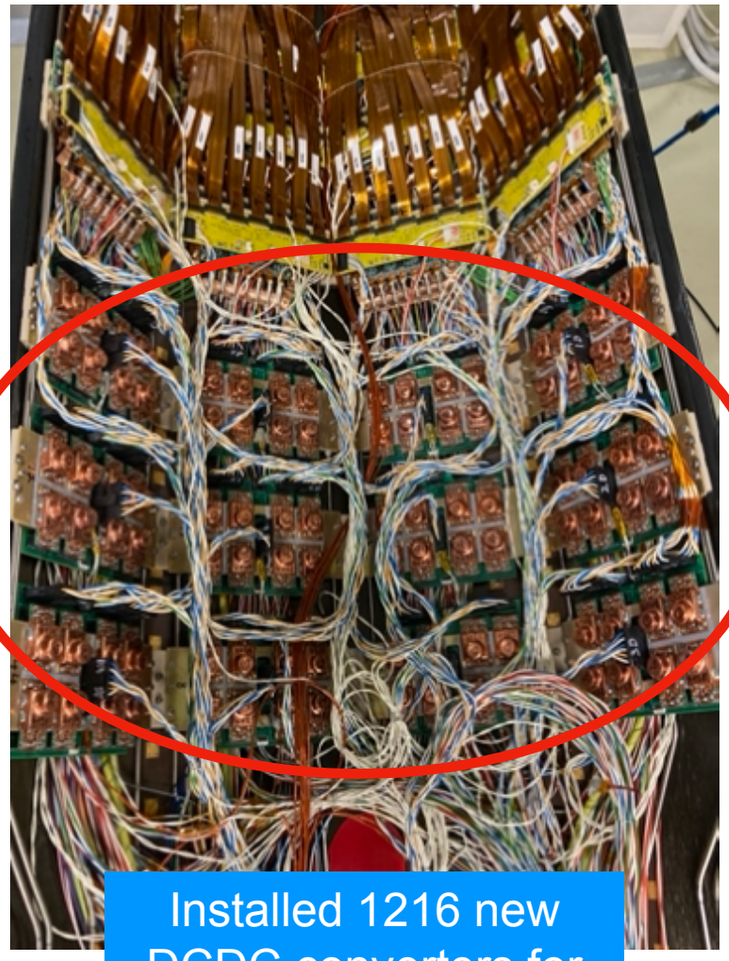
DCDCs replacement



Extracted old converters



Applied thermal interface film for better contact



Installed 1216 new DCDC converters for Run 3 detector

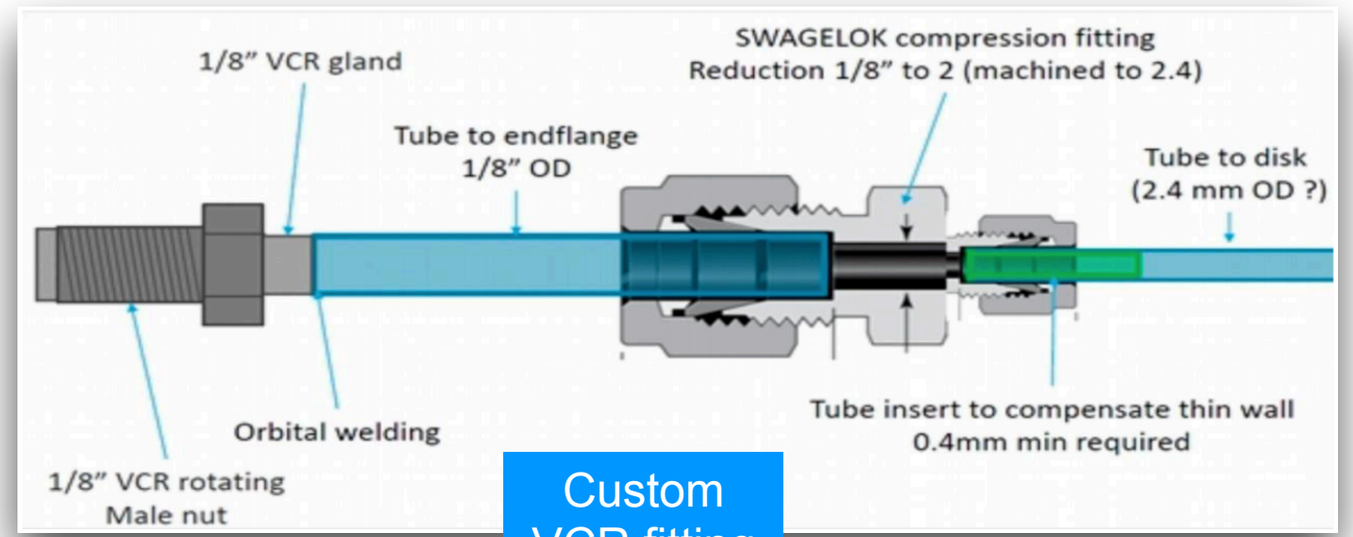
All DCDC converters have been replaced with the new production:
revised ASIC (FEAST v2.3) to fix failure mechanism in disabled state

Type	Required
2.4 V (= Analog)	608
3.3 V (=Digital, BPix)	320
3.5 V (=Digital, FPix & BPix L2)	288

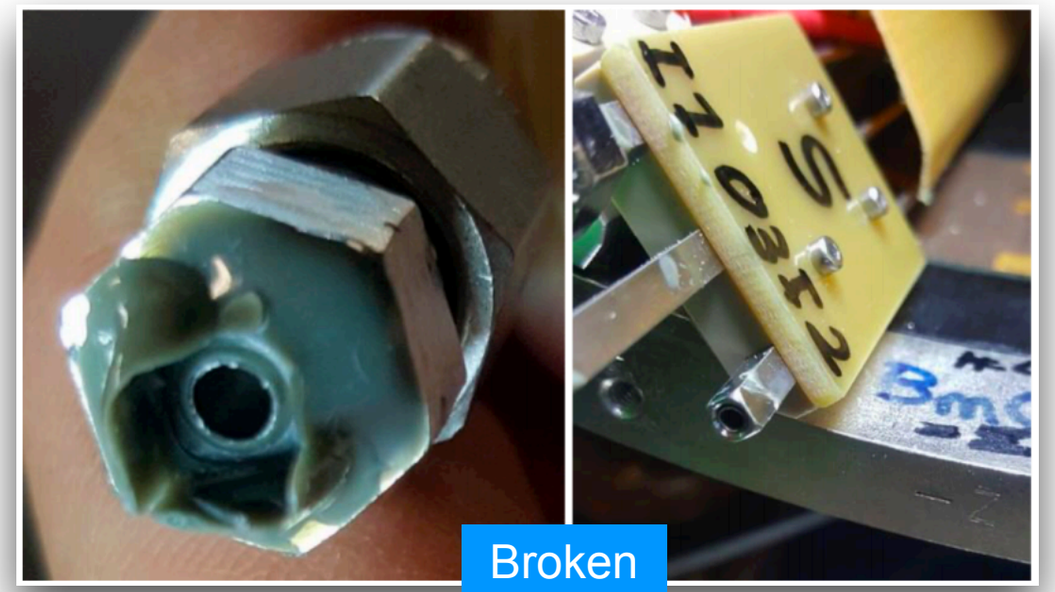
FPix cooling connections

- **Inlets with fixed nut directly welded to cooling pipes**
  - glue meant to reduce mechanical stress
  - minimal mechanical torque needed to break off the nut
- **High risk to damage the 24 connections during handling**
  - one broke during lab checkout
- **To ensure operational stability, introduced rotating nut and custom VCR fitting**

CO_2 cooling inlets

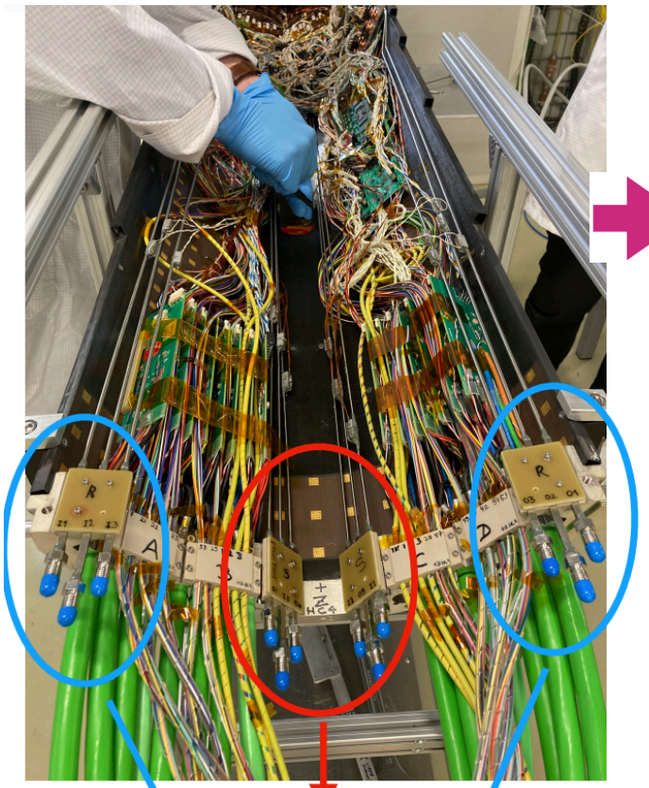


Custom VCR fitting solution



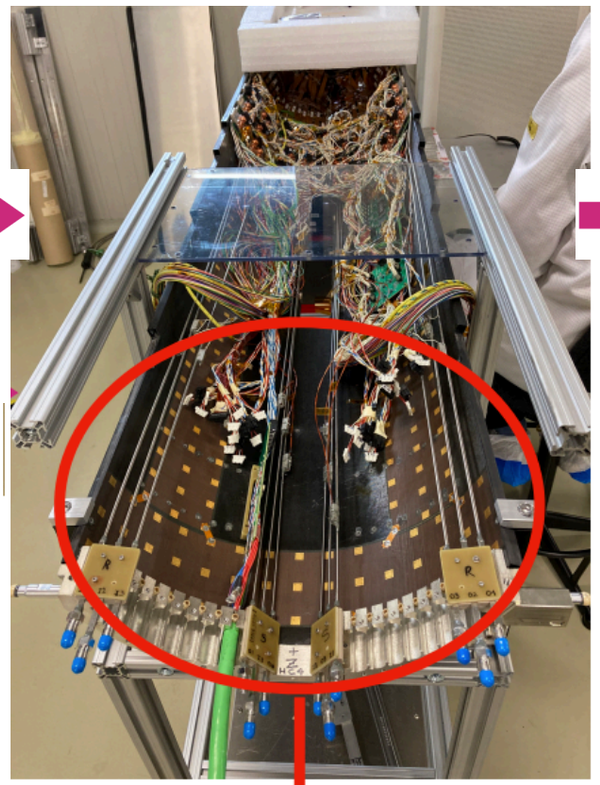
Broken inlet

FPix cooling pipe repair

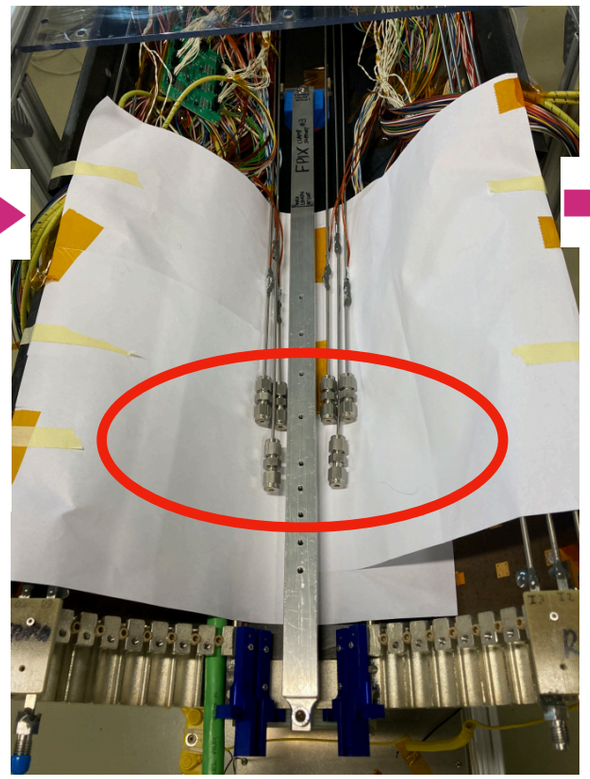


Cooling Inlets

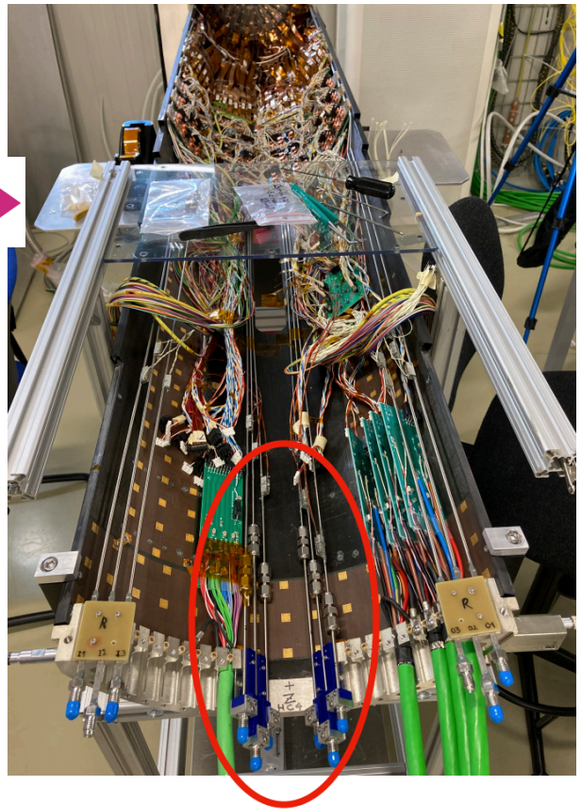
Cooling Outlets



removed old filter boards to clear area for cooling repair



cooling repair in progress with custom VCR fittings



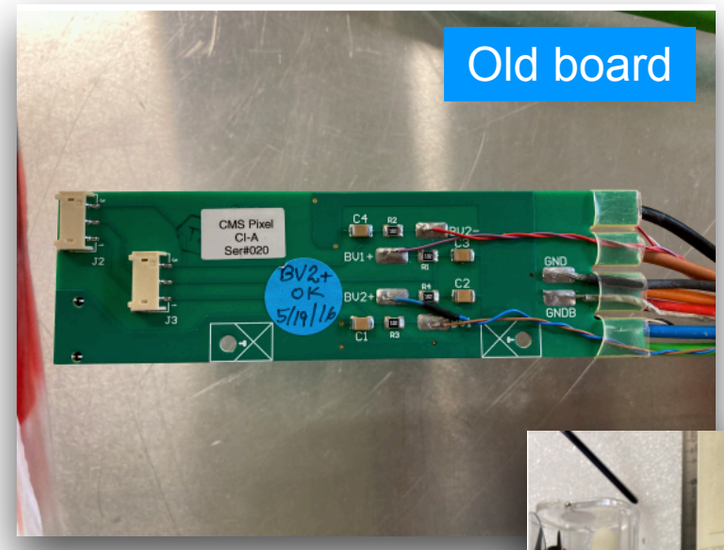
repair done with newly installed supply inlets with redesigned mounts

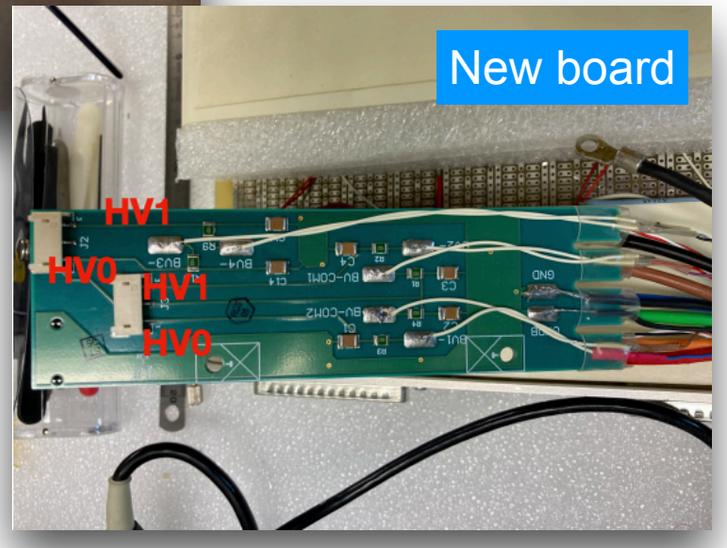
All cooling inlets have been refitted with custom Swagelok fitting and new mounts for the supply lines with rotating nut for strain relief

FPix filter board replacement

- **New filter boards have 4 independent HV lines (instead of 2) per power group to improve HV granularity**

- Tested 4 HV lines up to 800 V and common ground

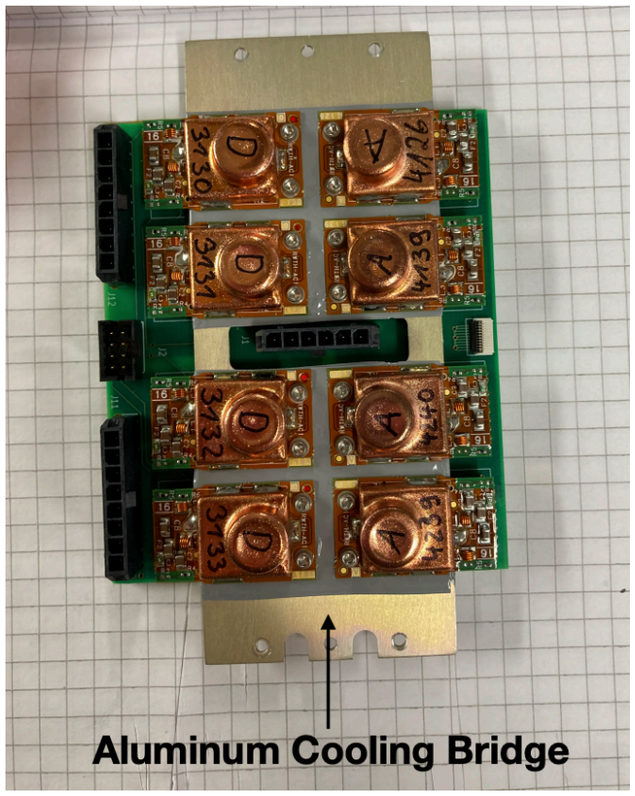


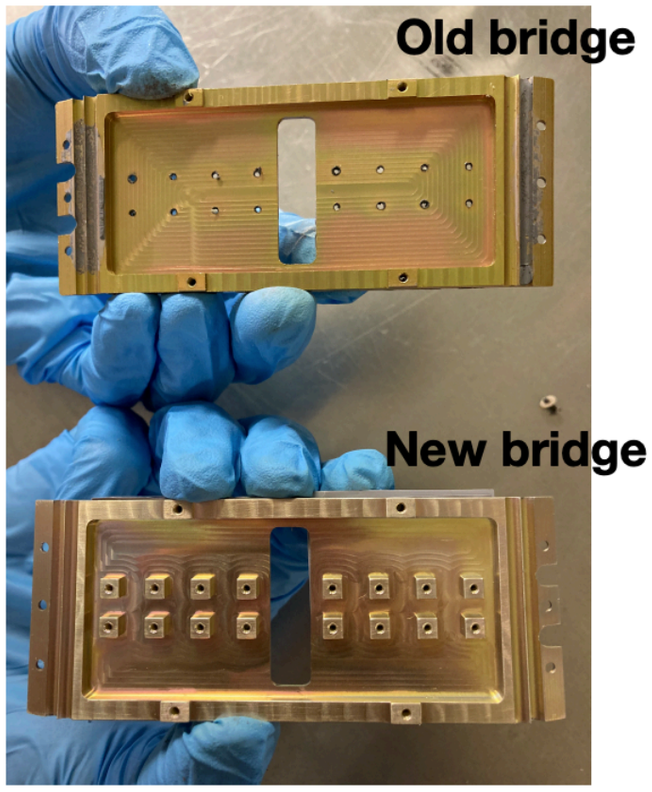


12 module power filter boards per 1/4 FPix

Other FPix refurbishment

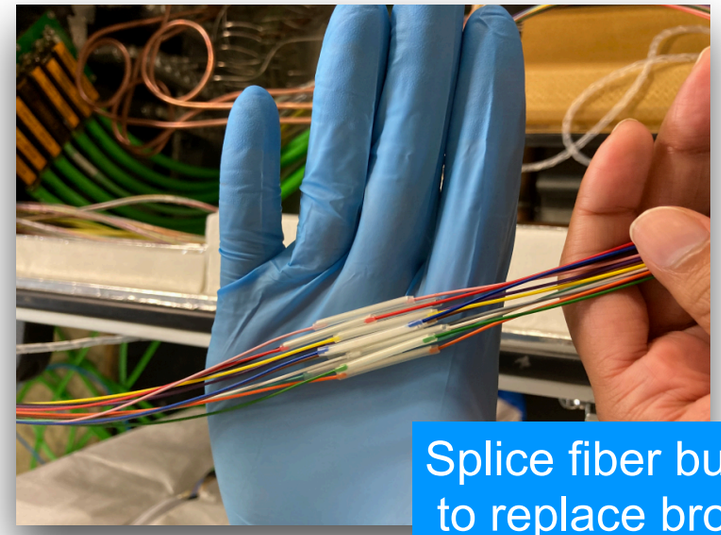
- **Repaired broken FED fiber bundle (MTP) connector**
- **Replaced DCDC cooling bridges for better thermal contact** - DONE only when deemed necessary





Better thread better thermal contact between DCDC and cooling bridge

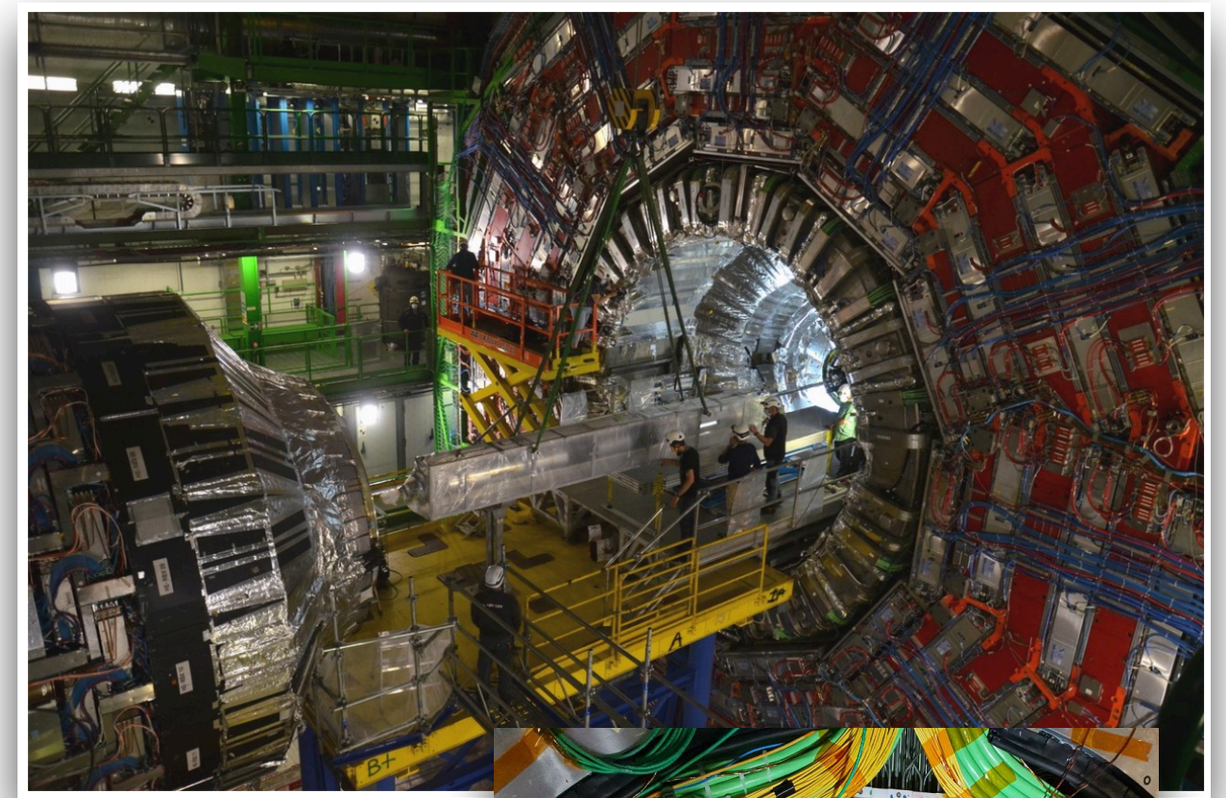
Broken FED bundle connector



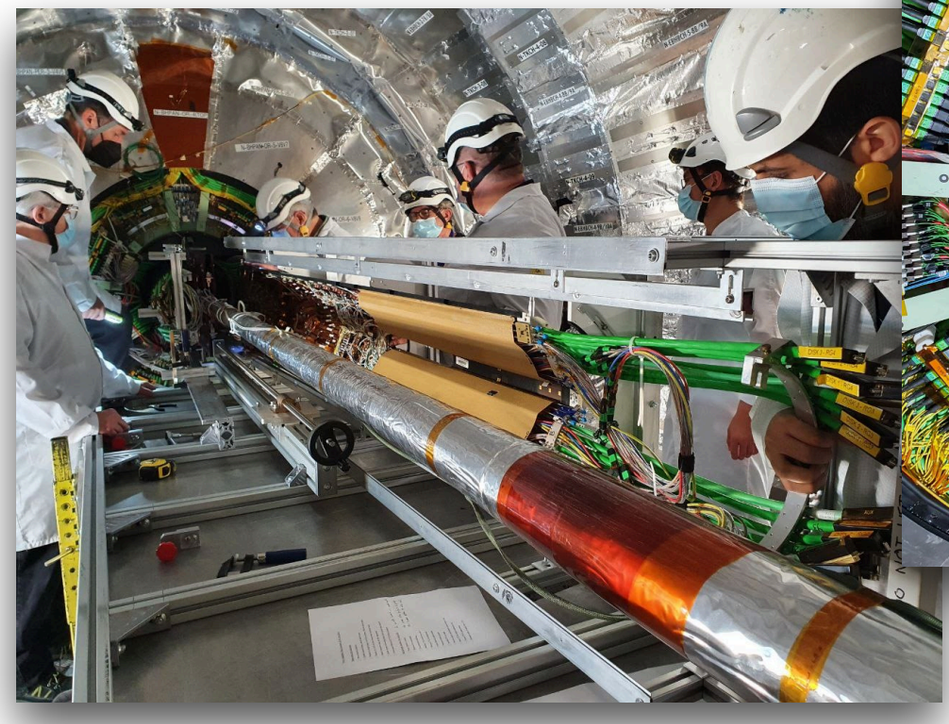
Splice fiber bundle to replace broken MTP connector

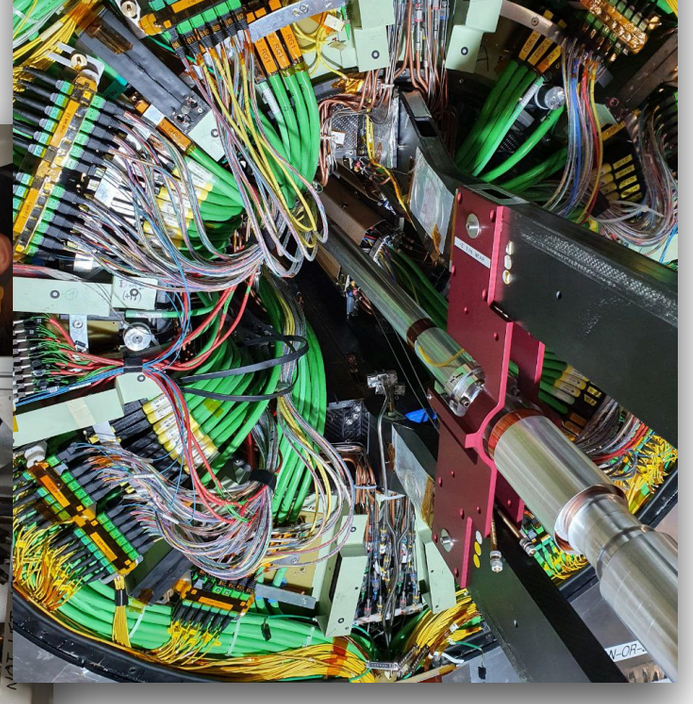
Pixel installation

- **BPix installed on 21st June 2021**
  - by PSI team with support of local crew
- **FPix installed on 28th (BmI/BmO) and 29th (BpI/BpO) June 2021**
  - by US experts with support of local crew
- **Cooling connection and leak test done**
  - also pressure (overnight) test for new L1 lines
- **Power and readout connections done**
- **CO2 flow established at +17 degC**



Very smooth installation





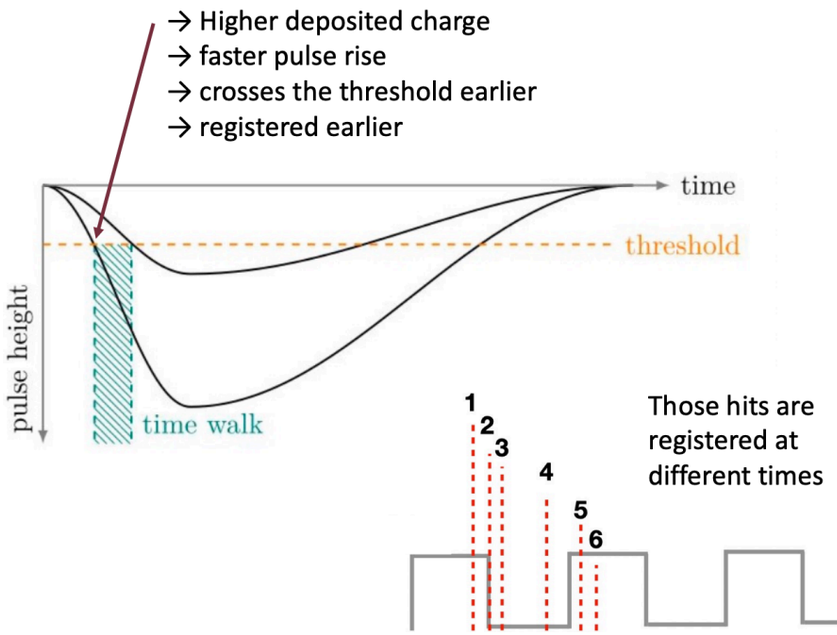
HV bias and timing scans

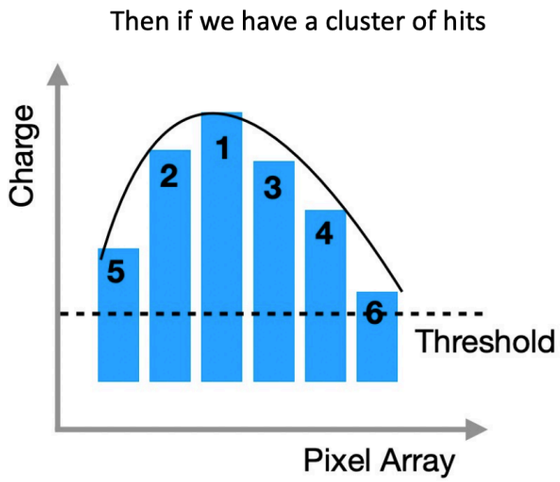
- **Two types of HV bias scan**:
  - **full scan**: on a full layer/disk - performed in special runs because bad data quality
  - **mini scan**: on a few non-overlapping modules (1 power group for each layer/ring on BPix/ FPix) - performed during the data taking with negligible effect on the data quality
- The applied bias voltage is increased from zero to the operational/higher voltage and the changes in the hit efficiency and average normalized on-track cluster charge are followed
- **Hit efficiency** = probability to find any cluster within 1mm around an expected hit independent of the cluster quality (less affected by charge collection efficiency)
- The effect of radiation damage is visible in the shift of the plateau in different scans
- The complex evolution of the hit efficiencies with irradiation is understood to come from multiple effects some of which are the inversion of the charge carrier type in the silicon sensor and the annealing during the periods with no data-taking

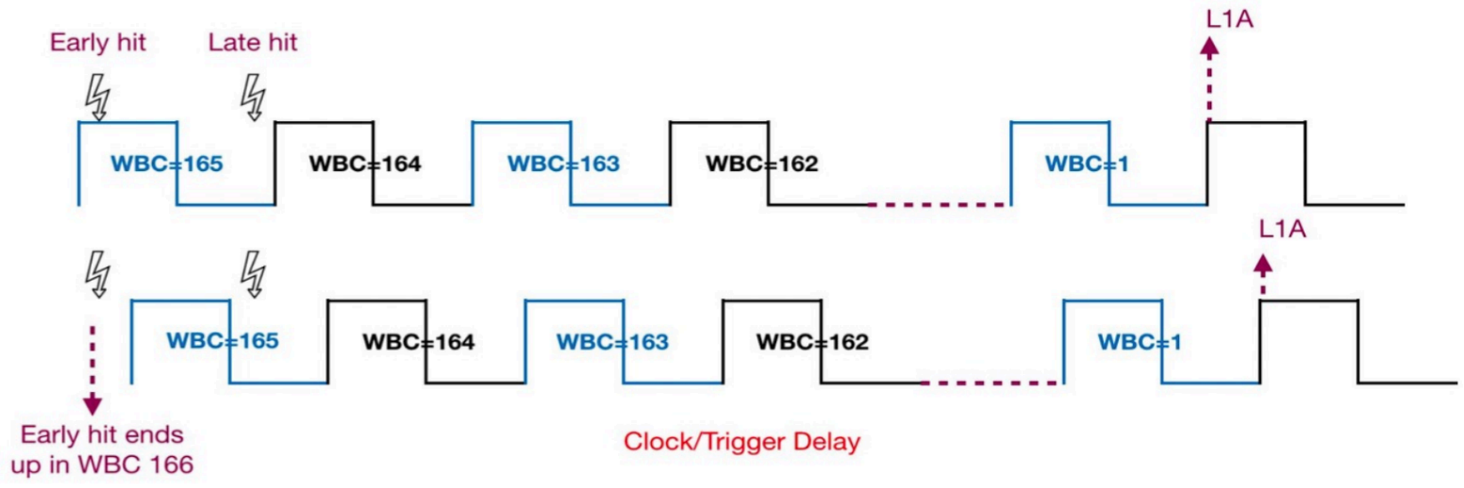
- **Timing scan** over different values of (globalDelay25 and WBC) settings to find a delay that maximize cluster properties and hit efficiency
  - the timings of all layers are changed at the same time: if one layer is inefficient, the measurements of the cluster properties are affected by the missing layer and have large systematic uncertainty (intervals indicated by the shaded bands)
  - L1 is not displayed because it is needed for track seeding so the quantity proportional to hit efficiency is not well defined for L1

Timing scans

- The pixel detector is read out on receipt of a Level-1 Accept (L1A) signal
- **Trigger delay** = delay between the bunch-crossings and when the L1A arrives at the pixel ROCs
- **Sources of delay**:
  - dominant: Global trigger latency
  - other: fiber length, electronic response along the path
    - critical: not knowable exactly and vary among different readout groups
- **Time-walk effect** = hits that deposit low charge in the sensor are registered later than hits that deposit higher charge i.e. the registration time of hits is dependent on deposited charge







Residuals

Hit residuals measurement: Triplet method

- BPix:
  - pT > 12 GeV tracks with hits in 3 layers are selected and refitted using hits in two of three layers
  - trajectory extrapolated to remaining layer
  - triplets considered for Layer 3, propagated from hits on Layer 2 and 4
- FPix:
  - pT > 4 GeV tracks with hits in 3 disks are selected and refitted using hits in Disks 1 and 3
  - trajectory extrapolated to Disk 2
- residuals with the actual hit are calculated and residual distribution fitted with the Student-t function

Reconstruction

- Positions are reconstructed with two algorithms:
  - **Generic**: a simple algorithm based on track position and angle; used in our High Level Triggers (HLT) and early track iterations offline
  - **Template**: an algorithm based on detailed cluster shape simulations predicted by PixelAv; used in the final fit of each track in the offline reconstruction
- Observed residual distribution is the sum of the intrinsic detector resolution and a track extrapolation error (larger for lower pT tracks)
- The performance of the Template algorithm is seen to be better than the Generic algorithm

Soft error recoveries (SERs)

- SER = procedure triggered to recover high number of auto-masked channels
  - 8 L1 central channels OR 12 L1 channels OR 20 total channels
- Auto-masked channel = channel with 63 OOS/min
- Out-Of-Sync (OOS) = 255 FED errors
- FED errors = TimeOut errors, EventNumberErrors, …
- Blacklisted channel = auto-masked channel not recovered after a few SERs
- RunningDegraded = 100 total blacklisted channels OR 12% of Layer 1 blacklisted

Mitigation changes

- **~10% of Layer 1 was masked in fills with PU ~60 and L1 trigger rate ~100-110 kHz**
  - **data still good**

- **Changed criteria to go into RunningDegraded:**
  - triggered only when there are (60 -> 80 ->) **100 total blacklisted channels or 12% of Layer 1** channels are blacklisted
  - **indication that data quality could become bad**

- **Uploaded new pxFEC firmware: no more FEC programming errors**

- **Changed conditions required to auto-mask a channel:**
  - 30 OOS/min -> 63 OOS/min: **10% -> 6% of Layer 1 masked**
  - 63 OOS/min -> 63 OOS/30 s: **6% -> 5% of Layer 1 masked**

- **Changed TBM phases for most frequent auto-masked channels:**
  - a lot of settings (POH bias, POH gain, tbm pkam, trimming, masking, VcThr, …) were changed only on a few modules to check their effect
  - only TBMPLL settings were effective: **5% -> 2% of Layer 1 masked**

Limits at high PU

- **No particular hardware/software limits at PU~70**

- **Problems will come with higher luminosities:**
  - L1 input links will saturate at a lumi of 3*10^34 and L1A rate of 100kHz (PU ~ 85)
  - limits for the FED before backpressure should be around 3.73 GBs at 100 kHz, which we shouldn’t reach before a lumi of 3*10^34, where the worse FEDs will output 3.4Gbs

- **However, substantial impact on BPix Layer 1 efficiency already at PU = 65**