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SALSA: a new versatile front-end ASIC for MPGDs

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RD51 meeting WG5

06/12/2023

Introduction

SALSA project and specifications

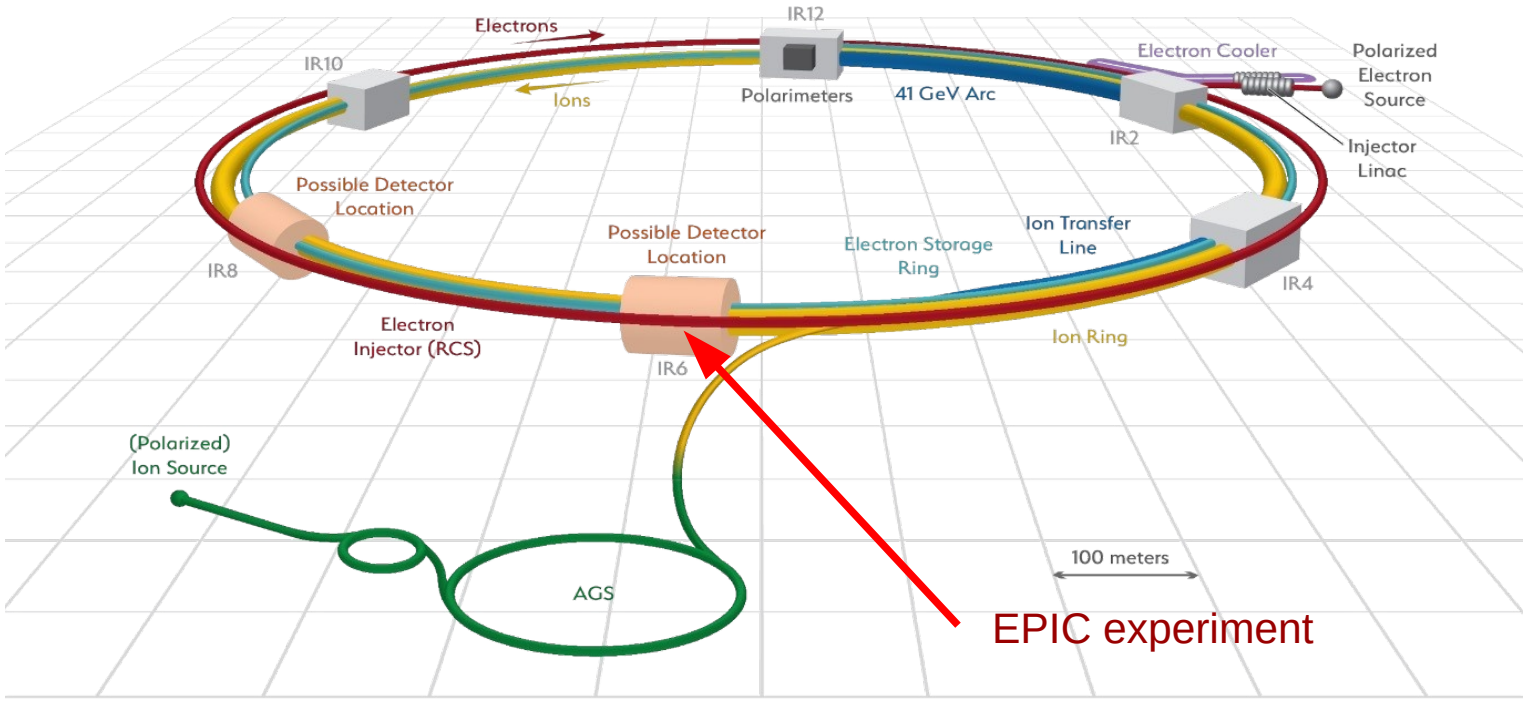
First prototype results

Prospects

THE EIC PROJECT

EIC collider

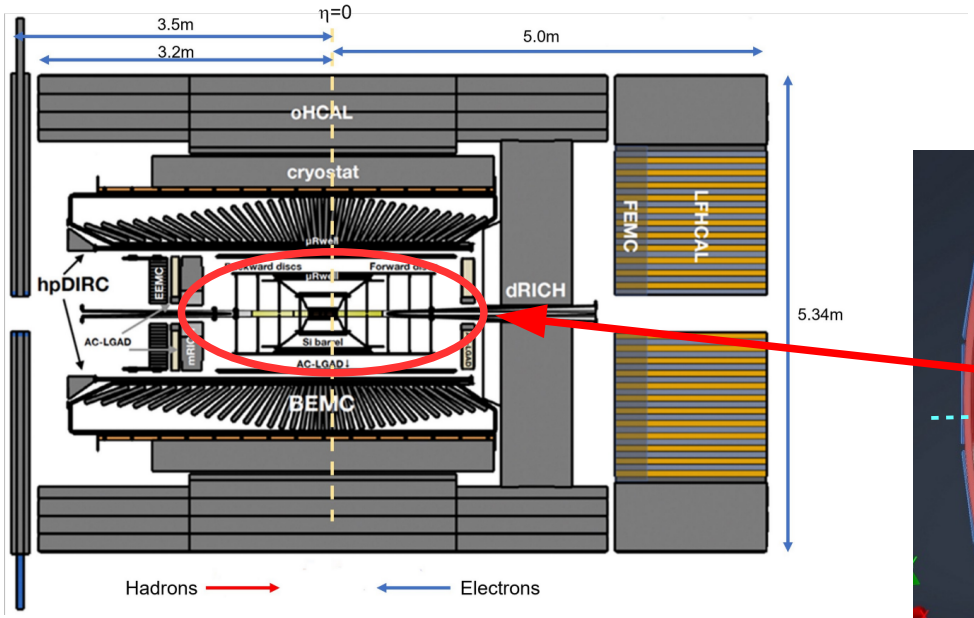
- Hadron physics: nucleon structure, quarks and gluons spins, gluon saturation, etc...
- High luminosity electron-ion collider (all nuclei from p to U) at BNL (USA), also with polarized beams: e, p, d, ^{3}He
- 5-18 GeV e^- vs 40-275 GeV p, 20-100 GeV in CoM
- First beam ~ 2031
- 2 experiments: EPIC (already financed) and "Detector 2"



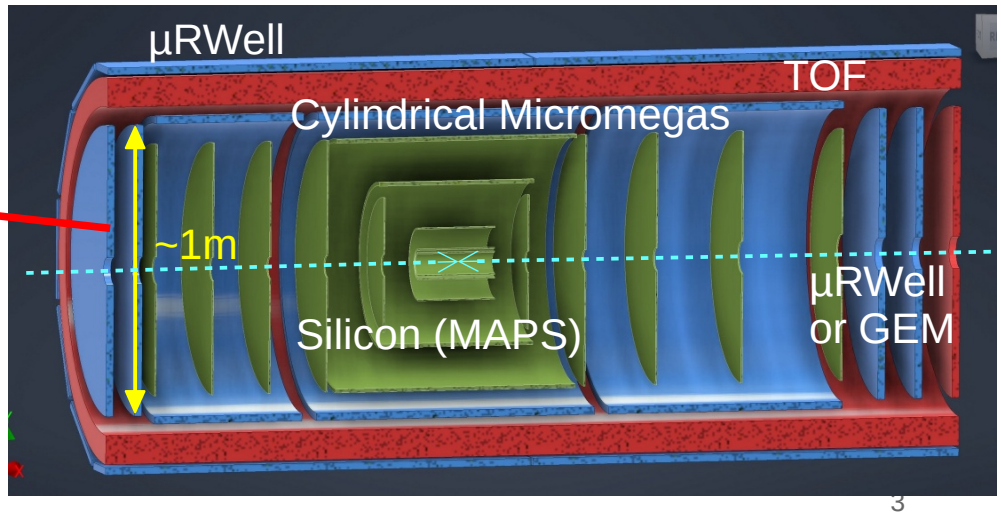
THE EPIC EXPERIMENT

EPIC detector

- 1.7 T solenoid with trackers, particle ID, calorimetry, far-forward/backward detectors
- Tracking: Silicon, MPGDs
- pID: hpDIRC, RICH, TOF (AC-LGAD 30 ps resolution)
- Tracker expected resolution: 150 µm, 10-20 ns
- MPGD trackers: cylindrical Micromegas + µRWell endcap disks (or GEM) + flat µRwell outside of TOF barrel
- DAQ with triggerless streaming readout
- SALSA ASIC: foreseen for readout of all MPGDs



EPIC tracker



SALSA : VERSATILE READOUT CHIP FOR MPGD

Motivations of the project

- To develop a new versatile multi-channel readout chip in the framework of the EIC project and beyond
  - adapted to streaming readout DAQs
  - for MPGD trackers but not only, also TPC, photon detectors,...
  - with possible future developments for other kinds of detectors (calorimeters, non-MPGD photon detectors) and/or specific constraints (ps-level time resolutions ?)
- Integrated per-channel ADC and digital processing
- Large ranges in term of signal amplitudes, electrode capacitances, peaking times, signal rates
- TSMC 65nm technology for improved performances and sustainability

Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Sao Paulo University (USP) + associated institutes designed the SAMPA chip (ALICE TPC), experts in on-chip ADC and digital processing
- IRFU developed several MPGD front-end chips (AFTER, AGET, DREAM,...) and other kinds of chips (SAMPIC and HGCROC TDC,..), experts in low-noise radiation-hard generic front-ends
- Large amount of complementary competences to collaborate on a common versatile front-end chip including digitization and digital processing
- Blocks developed by CERN in TSMC 65nm technology are also reused

SALSA CHIP DESIRED SPECIFICATIONS

Versatile front-end characteristics

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large gain ranges: 0-50 to 0-5000 fC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (EPIC is limited to 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

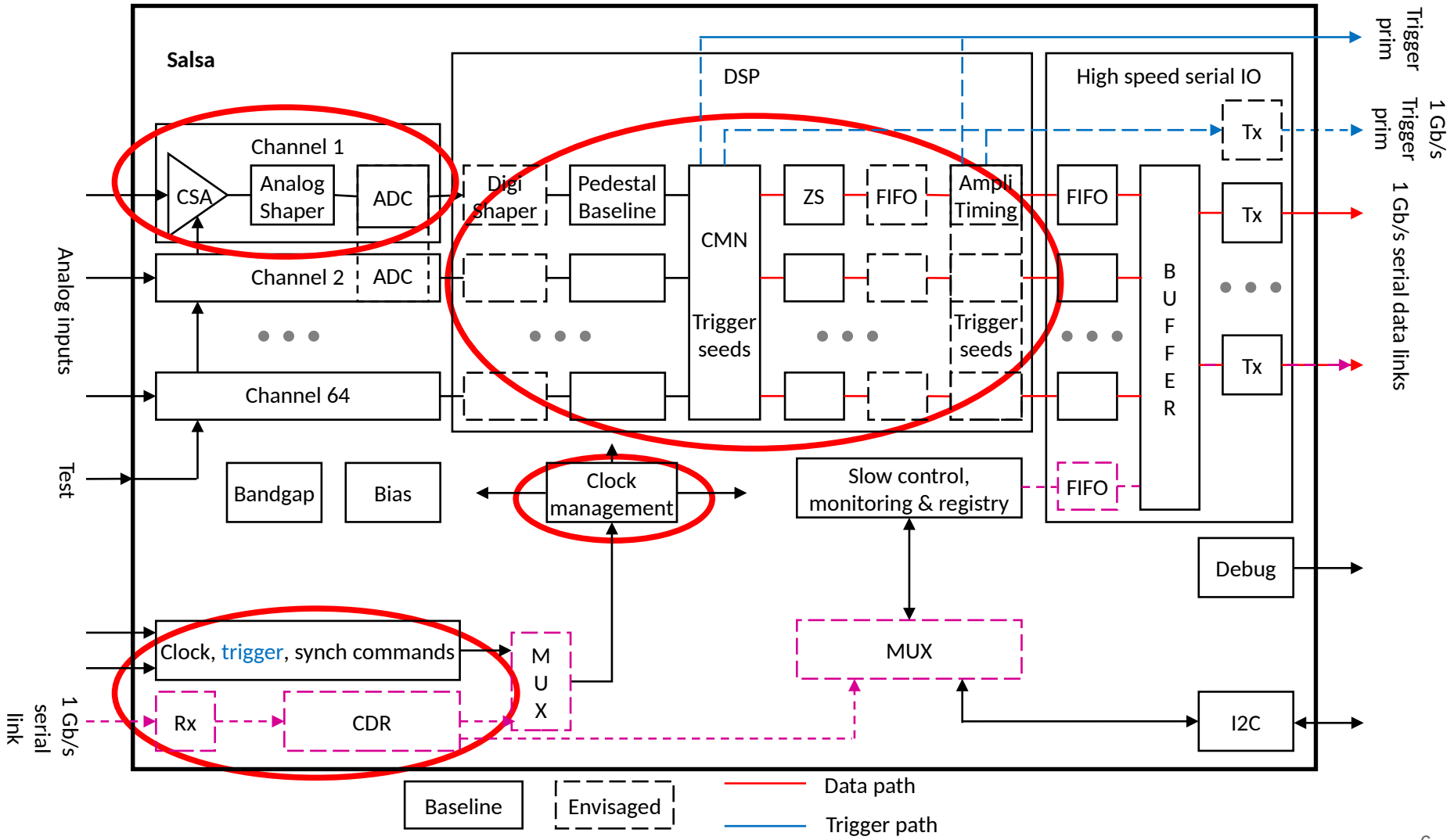
Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- Input clock, fast commands and slow control fed with unique CDR signal, as well as standard separated ones
- ~1 cm^2 die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID), working at 2T magnetic field

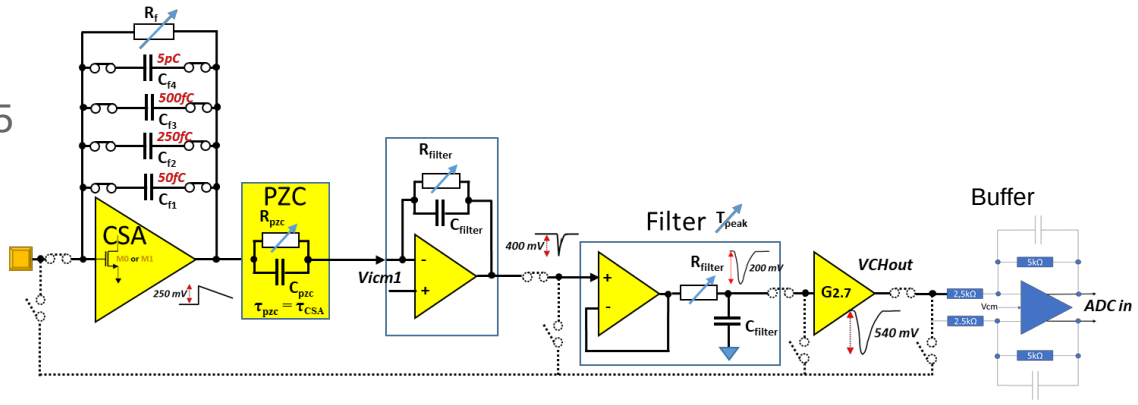
Preliminary design of SALSA



SIGNAL AMPLIFICATION AND DIGITIZATION

Front-end stage

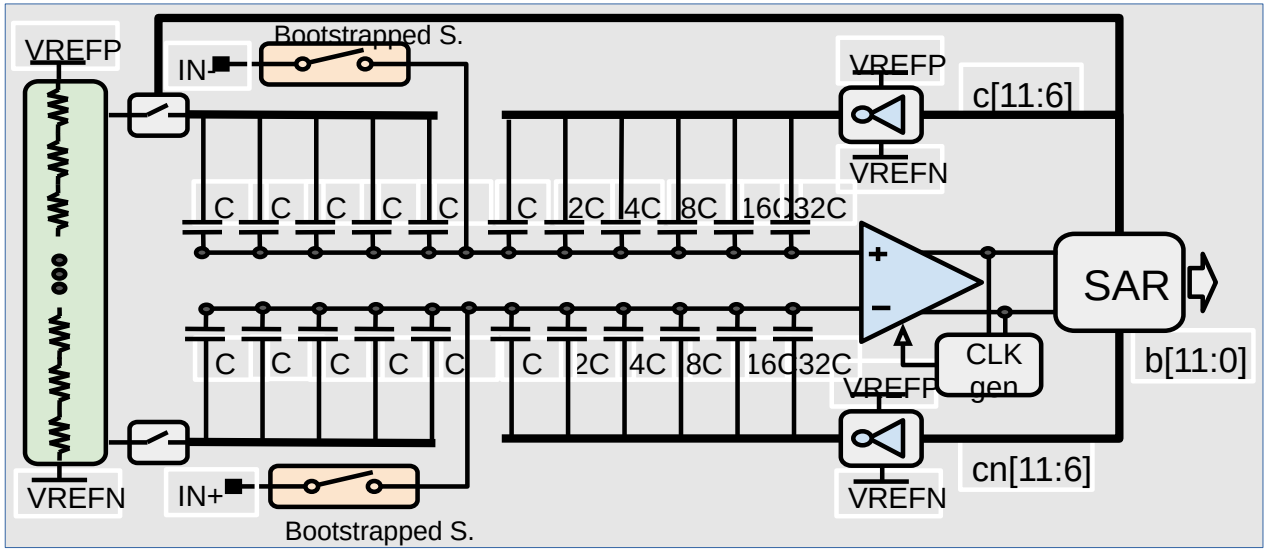
- Charge Sensitive Amplifier + Pole-Zero Cancellation + shaper
- 4 gain ranges from 0-50 fC to 0-5 pC
- 8 peaking times 50 to 500ns
- 2 input transistor sizes
- 2 polarities
- Integrated anti-saturation circuit
- Integrated test pulses



Scheme from P. Baron

ADC block

- 12 bits 5-50 MS/s SAR ADC
- Expected 10-11 ENOB bits



Scheme from H. Hernandez

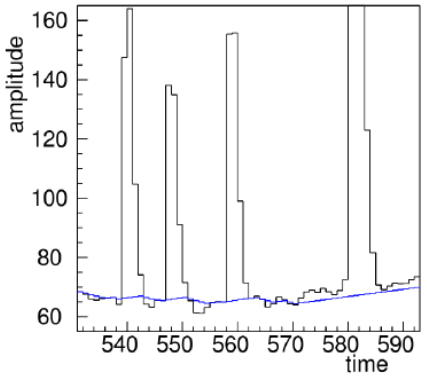
DSP DATA PROCESSING, PRELIMINARY VERSION

General remarks

- Data processing, reduction and formatting from ADC values to output links
- Each process can be deactivated individually by user
- Process parameters through ASIC registers
- Part of codes from SAMPA chip
- Considered processes still under study, suggestions welcome !

Baseline corrections

- Pedestal subtraction with fixed value per channel
- Common mode correction to reduce common noise impact
- Baseline slope following algorithm



Plot from SAMPA doc

Digital shaping

- Cancellation of signal tail if necessary

Zero suppression

- Keeping samples above fixed thresholds, possibly neighbor ones
- Different data format between ZS and non-ZS samples

DSP DATA PROCESSING

Feature reconstruction

- To further reduce data flux
- For instance peak finding algorithm: amplitude + time + TOT extraction

Trigger management

- Samples selected to be extracted when trigger signals received
- Trigger primitives generation when samples above threshold
- Nature of trigger primitives to be defined (logic signal, data on specific fast link, etc...)

Data monitoring and calibration

- Specific fast commands to generate calibration data (non-ZS, with test pulses, etc...)
- Software scaler per channel for occupancy evaluation

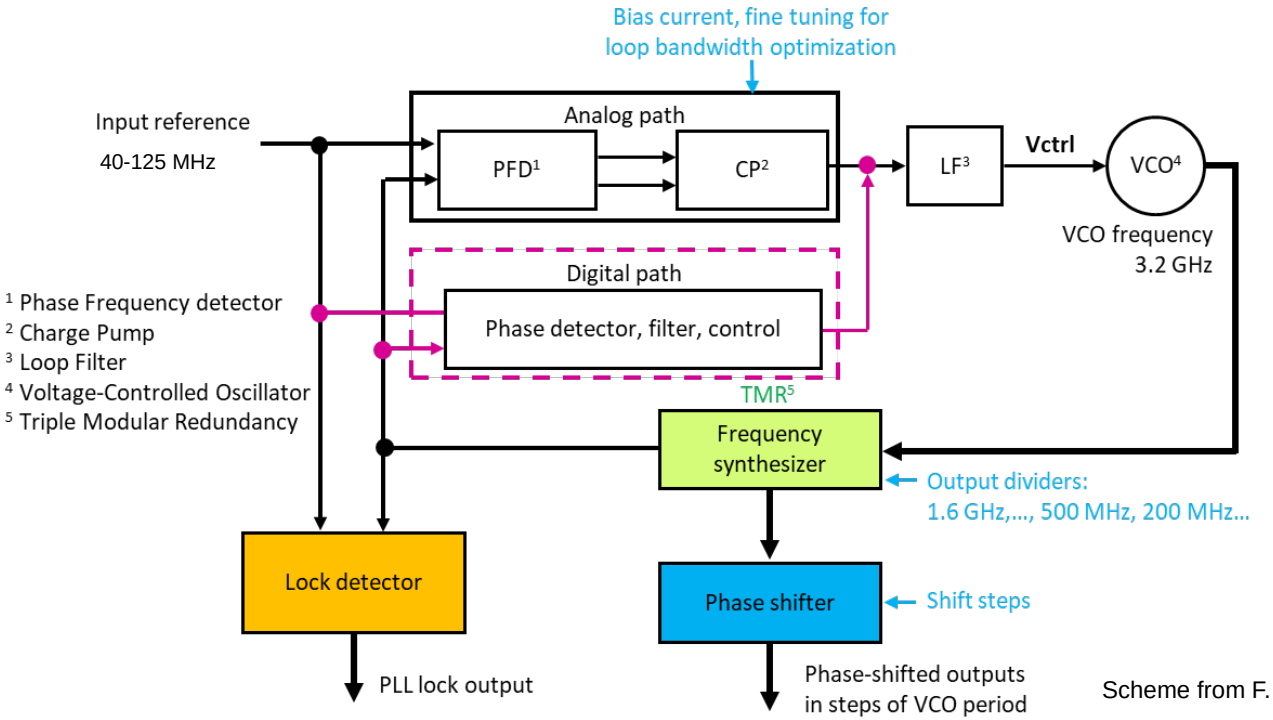
Data formatting and buffering

- Formats for ZS and non-ZS sample data, featured data, monitoring data
- Output data flux segmented in packets which will contain all kinds of data
- Packet identification by numbering and timestamps
- Packet buffering and transmission over 1 or several Gbit/s links
- Generation of error packets in case of troubles

SALSA CLOCK MANAGEMENT

Development of the "PRISME" 65nm PLL IP block

- No existing PLL block fitting our requirements in TSMC 65nm technology
- Large frequency ranges for input (40-125 MHz) and outputs (up to 1.6 GHz)
- Low power and radiation hardness capability
- Hybrid PLL mixing analog and digital paths, with 3.2 GHz VCO frequency
- Very low internal time jitter: ~3 ps RMS up to 1 GHz
- 4 clock outputs each with programmable frequency and phase
- This block will be available for HEP community

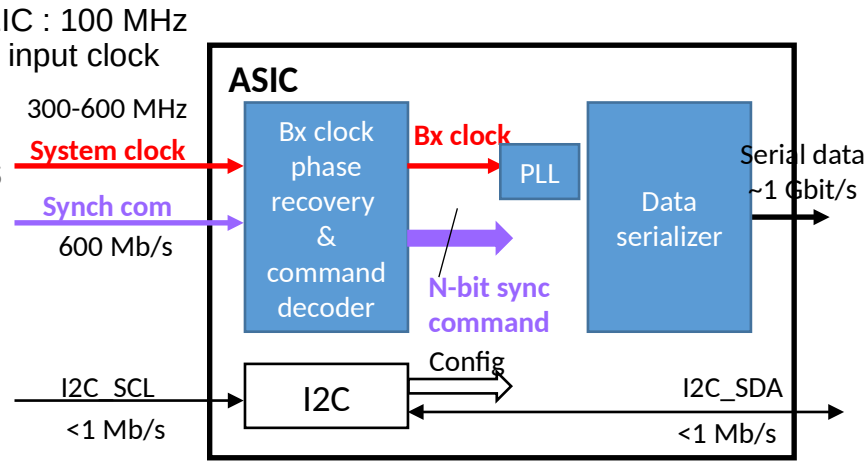


Scheme from F. Bouyjou

CLOCK, FAST COMMAND AND SLOW CONTROL INPUTS

Traditional way

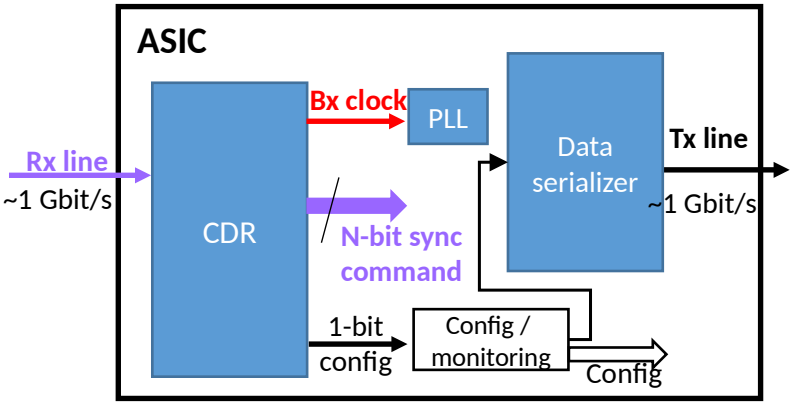
- 1 differential input for clock
- 1 differential input for fast commands: T_0 synchronization, calibration triggers, event triggers (non-streaming readout mode), etc...
- 1 SDA + SDC I2C input for slow control and configurations
- Will be implemented in SALSA

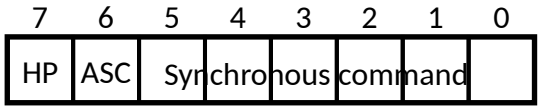


Schemes from I. Mandjavidze

Single encoded line grouping all inputs

- High speed 1Gb/s differential input which carry clock + fast commands + slow-control
- Internal CDR in SALSA to extract the different parts
- 8 bits every 10 ns (EIC): 6 bits for fast command ID, 1 bit for slow-control, 1 parity bit
- Slow control output through data output line
- Simplify connectivity: 1 diff input for everything instead of 4
- Possibility to implement this in SALSA in parallel with the traditional way
- May be proposed to some other readout ASICs in EIC as well





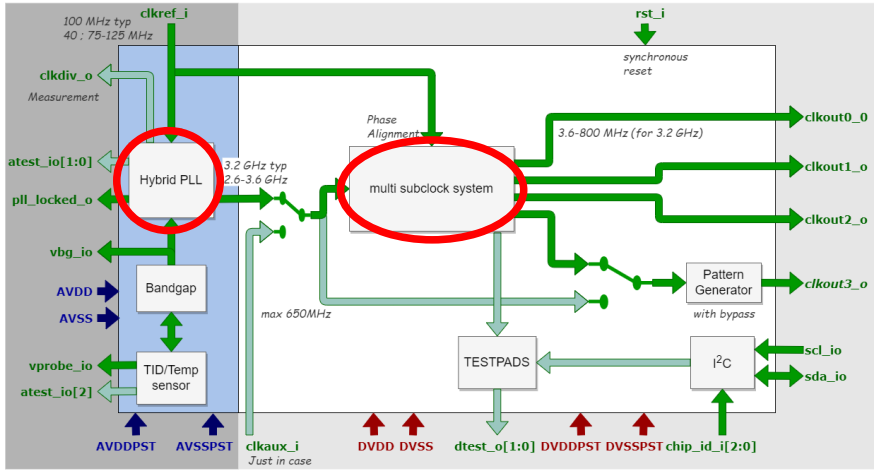
Structure of the SALSA project

- Split in different tasks
  - Front-end (IRFU)
  - ADC (USP)
  - DSP (USP + IRFU for algorithms and architecture)
  - General services (clock, slow-control, analog biases, high speed links) + architecture (IRFU with help of USP, some CERN blocks reused)
- Parallel development of the different tasks, with constant interactions between groups for common issues, in particular interfaces between tasks
- Design, production and tests of several prototypes foreseen to complete the project

PRISME side project

- Specific budget from EIC R&D project support
- PRISME prototype to test PLL block + service blocks (bandgap, biases, I2C, I/O links,...), partly from CERN
- 4 programmable clock outputs with individual frequency and phase tuning
- Prototype submitted in July 2023, just arrived, in packaging process

Design of the PRISME prototype

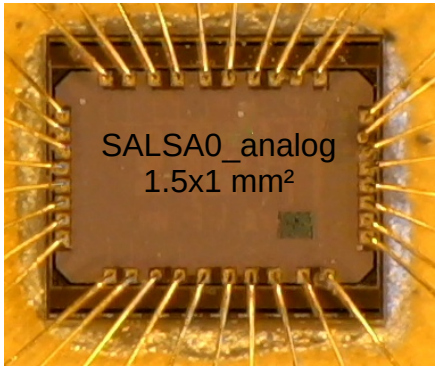


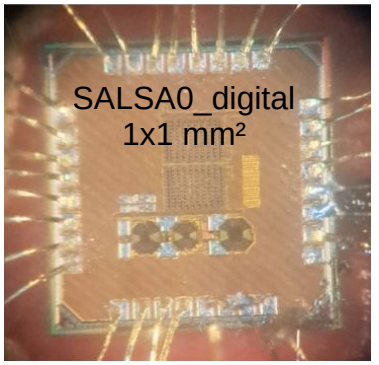
Scheme from C. Flouzat

TIMELINE OF THE PROJECT

The different steps

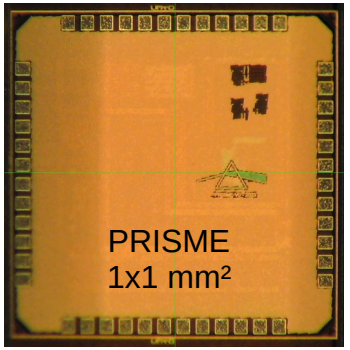
- 2020-22: Discussions and reflections on the project
- 2022-23: SALSA0 prototypes to study first designs
  - SALSA0_analog featuring 4 front-end channels
  - SALSA0_digital featuring an ADC block
- 2023: PRISME prototype for PLL block + first version of general services
- 2023-24: SALSA1 prototype to test full front-end + ADC chains
- 2023-25: SALSA2 prototype to test fully featured ASIC including DSP, but with ~32 channels
- 2025-26: SALSAf as pre-serial prototype with nominal number of channels





Status of prototypes

- SALSA0 prototypes submitted in November 2022 and January 2023, tests of analog proto in progress, tests of digital ones started
- PRISME prototype received in December 2023, under packaging, tests to be started this month or beginning of January
- SALSA1 design ongoing, submission foreseen 1st trimester of 2024
- Reflections on SALSA2 architecture and DSP data processing ongoing, submission foreseen beginning of 2025



Pictures from P. Baron, B. Sanches and F. Bouyjou

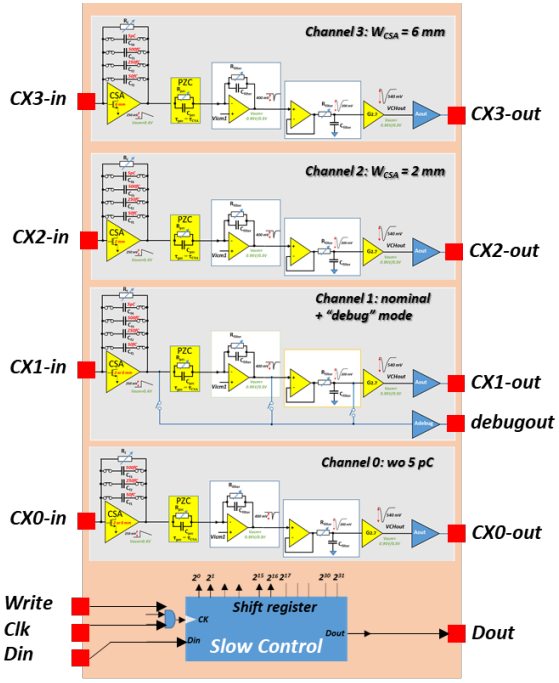
TESTS ON FRONT-END STAGE

SALSA0_analog prototype

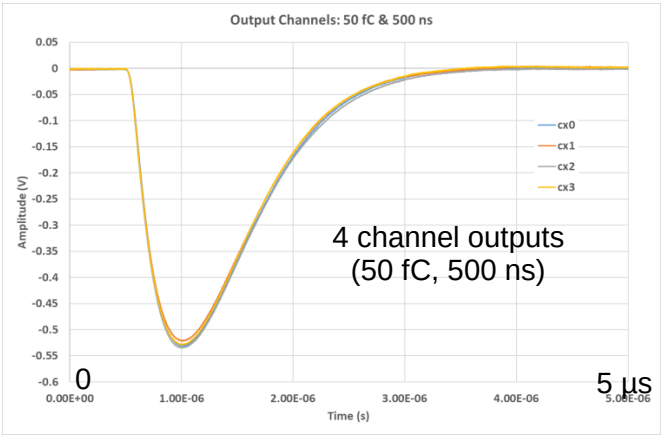
- 4 front-end channels with slight differences between them
- CX1 channel with debug output for monitoring
- CX0-2-3 with different input transistors, CX0 without 5 pC gain range

Preliminary results

- Test-bench with selectable input capacitance, input signal generation with configurable amplitude and rate, programmable oscilloscope, etc...
- Almost all configuration parameters (gains, peaking times, anti-saturation,...) were tested and work well
- Measurements in agreement with simulations: bias currents, power consumption, DC values, etc...
- Some discrepancies concerning transfer functions and noise levels especially at 50 fC gain range
- Origin due to parasitic resistances in the chip. Now understood and reproduced in simulations. Already corrected in the CSA design for SALSA1
- Further tests in progress, in particular vs temperature

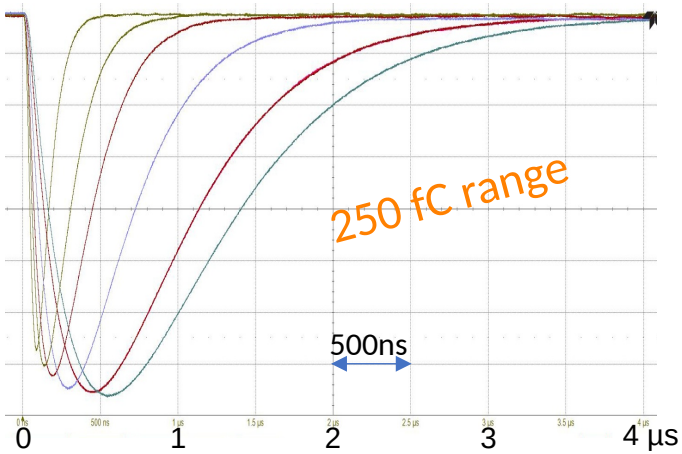


Scheme from P. Baron

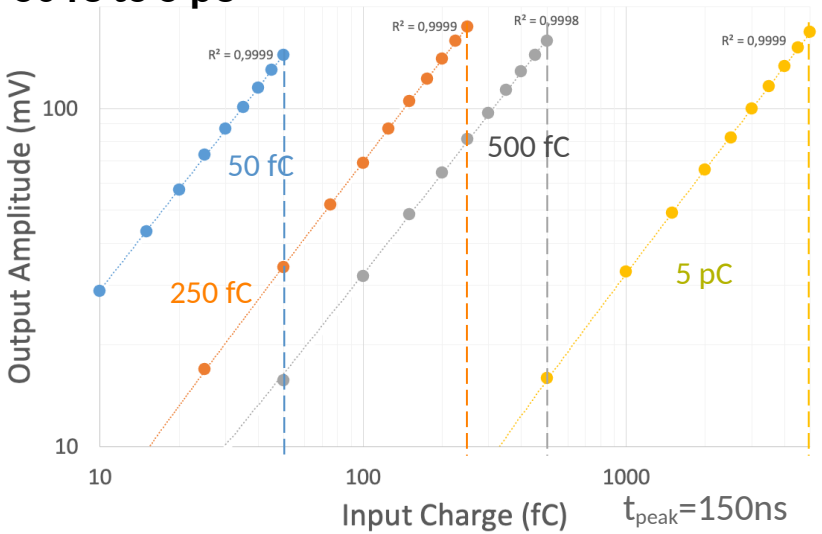


MAIN RESULTS WITH 120 PF INPUT CAPACITANCE

Peaking time programmable from **50 ns to 500 ns** with no tail

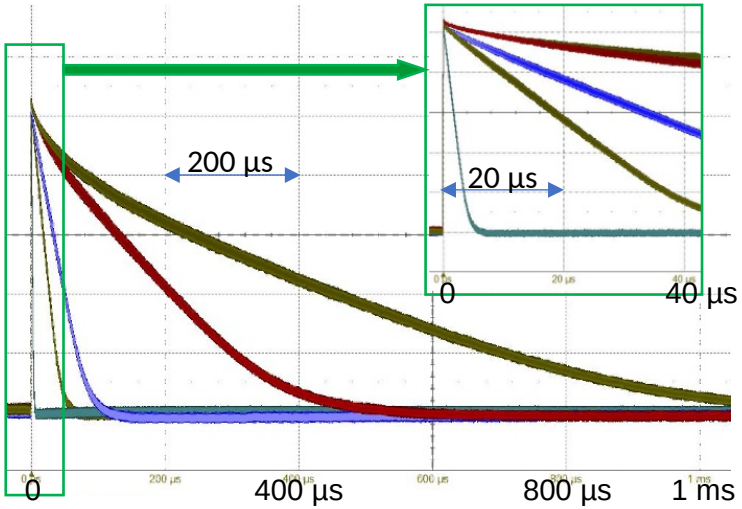


Gain programmable => dynamic range from **50 fC to 5 pC**

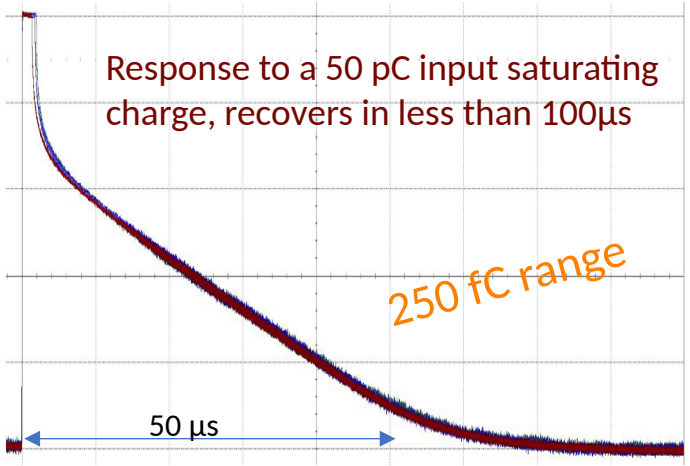


Preliminary

T_{fall} CSA programmable from 5 µs for high rate to 1 ms for low noise



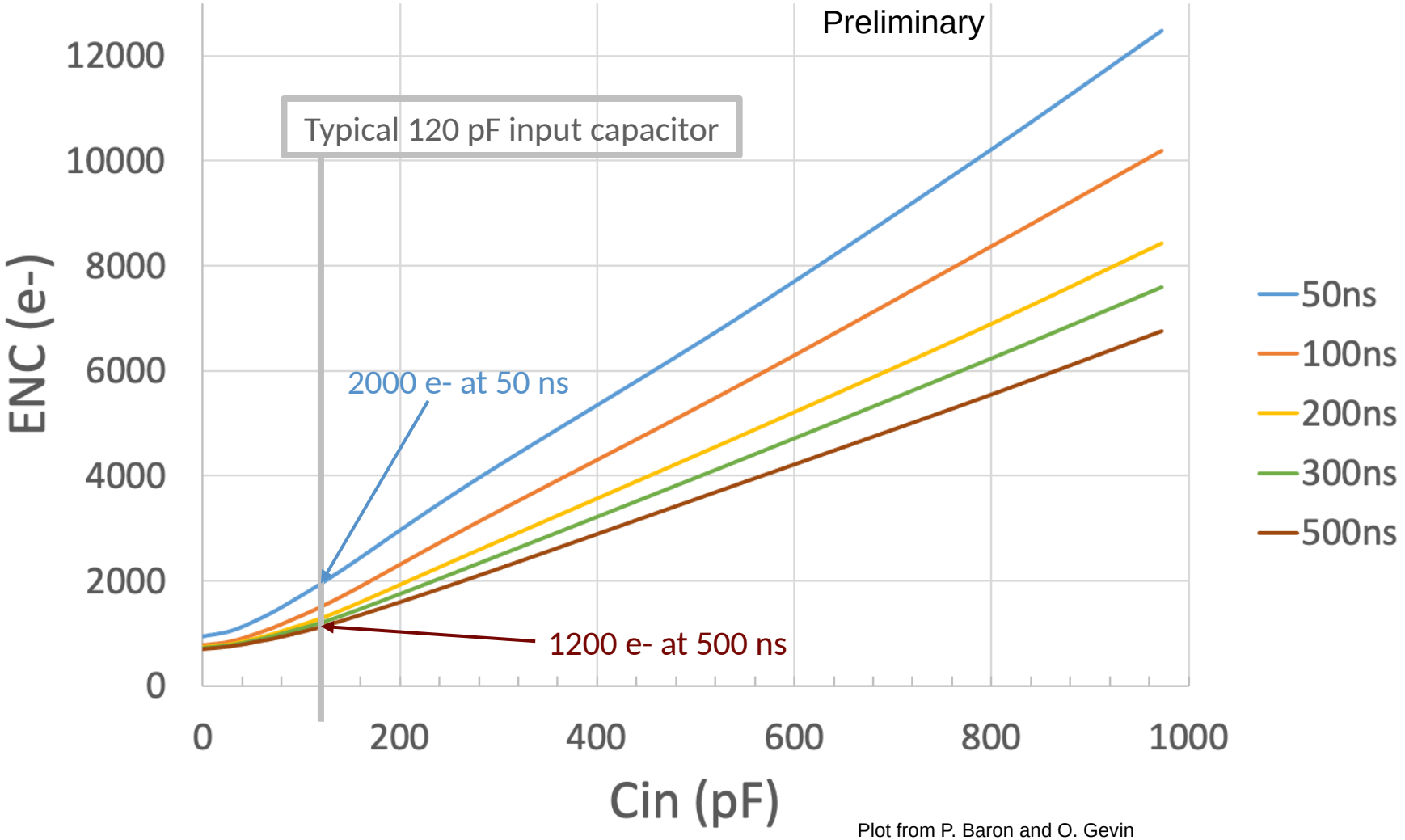
CSA anti-saturation circuit => **fast recovering**



Plots from P. Baron and O. Gevin

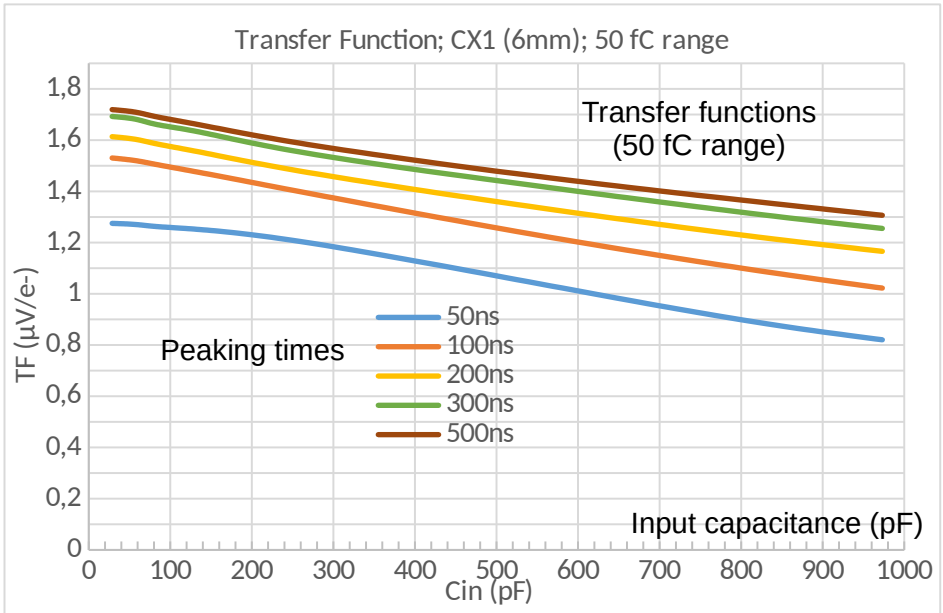
MAIN NOISE RESULTS: TYPICAL CASE

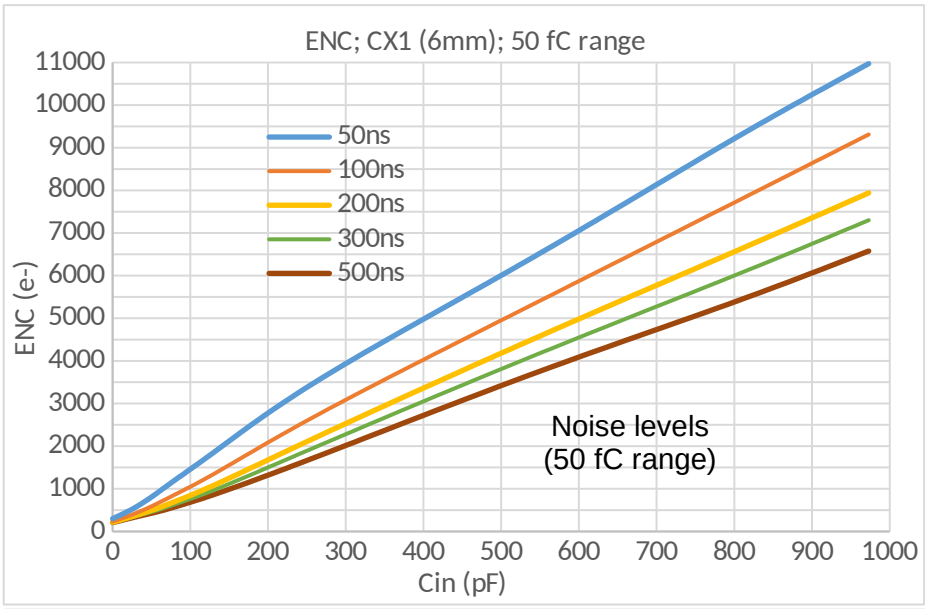
Equivalent Noise Charge in the **250 fC range** at different peaking times



Plot from P. Baron and O. Gevin

TRANSFER FUNCTIONS AND ENC FOR EXTREME GAIN RANGES





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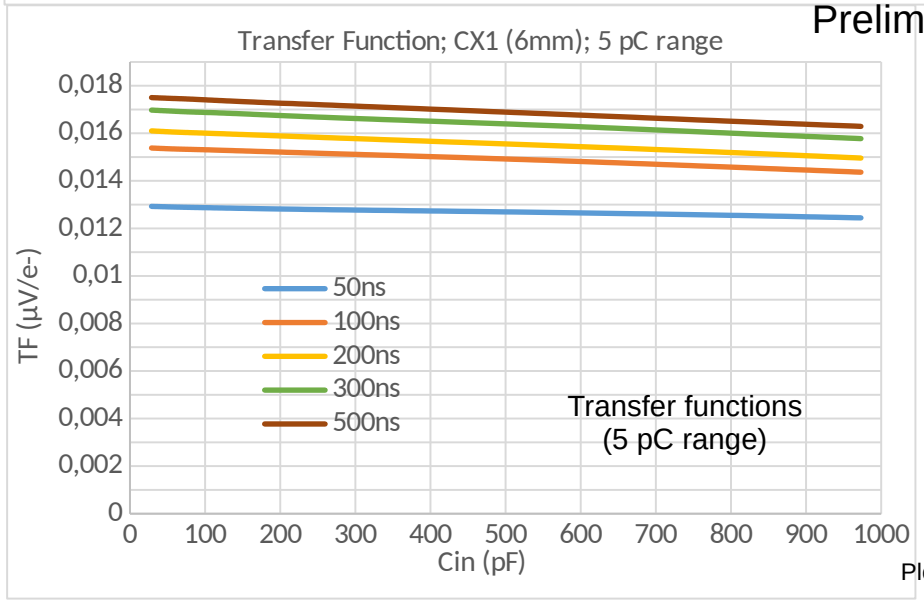
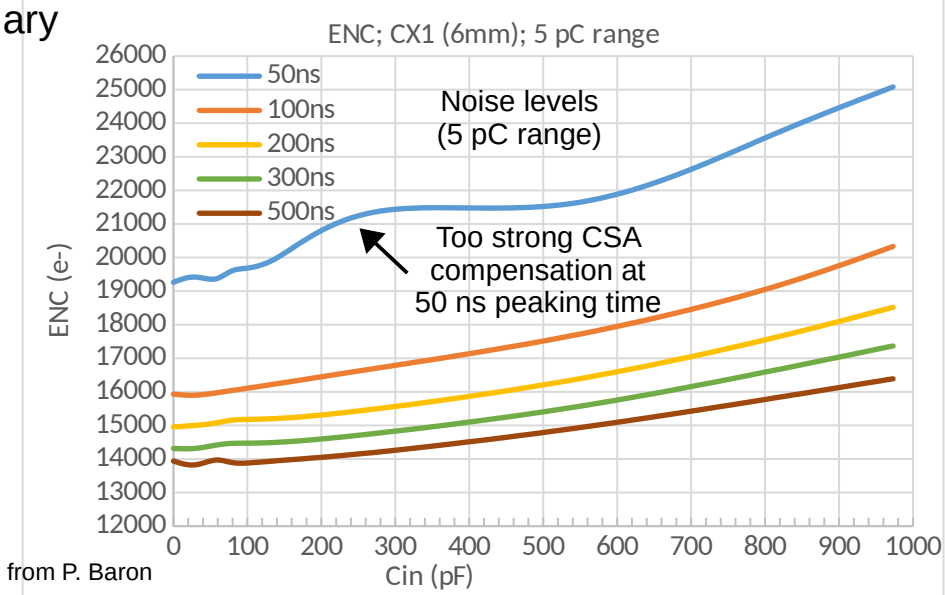




Plots from P. Baron

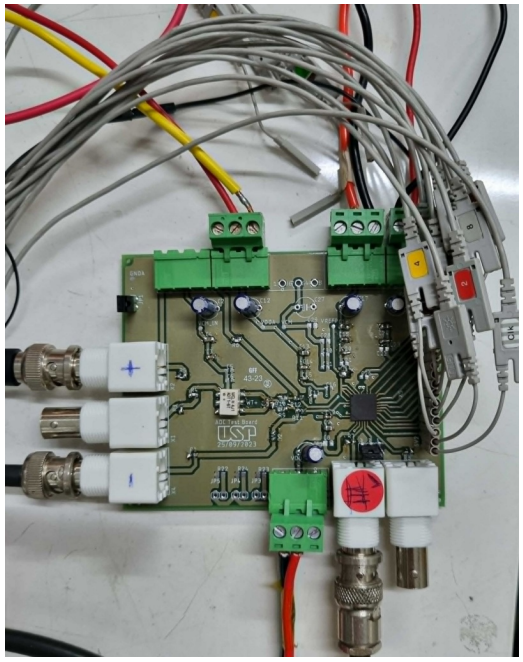
TESTS ON ADC BLOCK

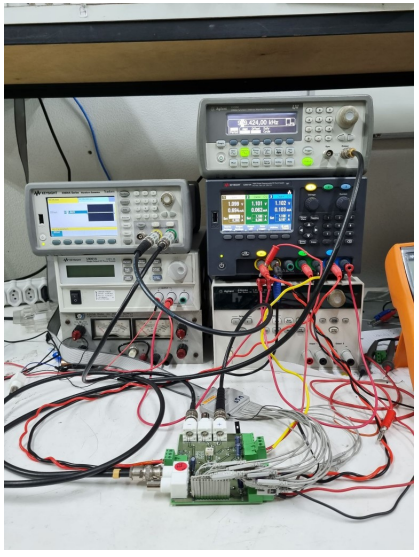
SALSA0_digital prototype

- 1 ADC block
- Test board to feed LV and clocks (sampling and conversion)
- Digital analyzer to read ADC output
- Tests started after mid-November

Very preliminary outcomes

- Problems of bonding with some of the prototypes
- Power consumption lower than foreseen in simulation (factor > 2)
- Unexpected offset for the 0 digital value, investigation ongoing on test board and in simulation
- ADC prototype under study, no result yet





Pictures from
B. Sanches

PRESENT STATUS AND PROSPECTS

Present status

- Performance specifications finalized, could be adapted in function of chip block study results. Still open to suggestions !
- Tests ongoing on SALSA0 prototypes, helpful to fix bugs, verify simulations, and evaluate performances
- Design of SALSA1 prototype (front-end + ADC) in progress
- Studies ongoing on logic architecture and DSP data processing for SALSA2 prototype
- Grant from EIC eRD109 R&D program
- Grant from French and Brazilian research agencies to be requested in 2024

Next steps

- Completion of tests on SALSA0 and PRISME prototypes beginning of 2024
- Production and tests of SALSA1 in 2024
- Production and tests of SALSA2 in 2025
- Design of SALSAf pre-serial ASIC in 2025, production and tests in 2026
- Compatible with the EIC project timeline