AGH University of Science and Technology

ASICs for Calorimeters

Marek Idzik

RD51 WG5 meeting, CERN 6 December 2023

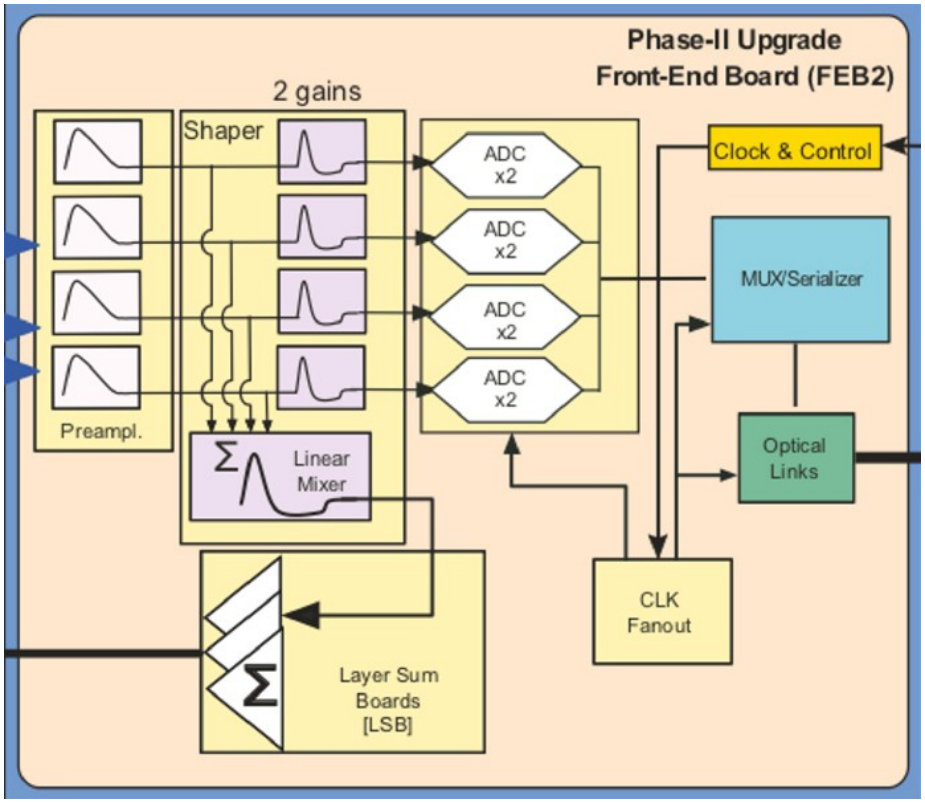
Outline

- Introduction
- Examples of readout ASICs for Calorimetry in LHC Upgrades
  - Comparison of key parameters
  - ASIC R&D in DRD6 (Calorimetry)
- Past – Present ASIC comparison
  - S-ALTRO, FLAME
  - Power and Technology limits
- DRD7 vs DRD1, wish-list, ...

Introduction
ASICs for Calorimetry vs other detectors

- Readout ASICs for calorimetry have many common specs/requirements/challenges with other detectors:
  - Energy deposition (Amplitude) measurement
  - Precise timing – 4D calorimetry - becomes an important requirement
  - High speed data links – lower granularity (not always) but more bits per channel
  - Complexity leading to System on Chip (SoC) architecture
  - Very low power per channel, particularly for multi-channel ASICs in high granularity detectors
- Specific requirement due to large input dynamic range:
  - Amplitude measurement with resolution 10-15 bits

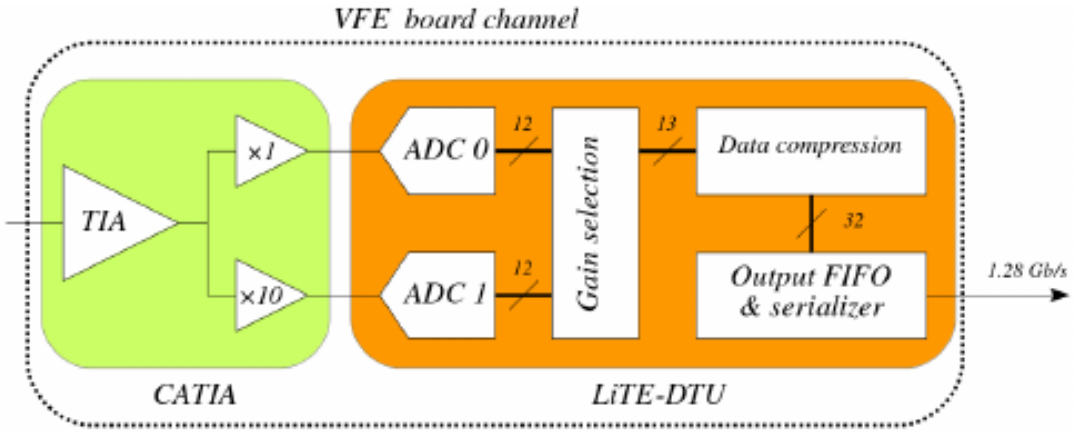
ALFE2+COLUTA readout ASICs for ATLAS Phase-2 LAr Calorimeter Upgrade



- 2 ASICs in 2 CMOS processes
- Only 4/8 channels
- No TDC (time measurement from pulse shape)
- High power consumption

- PA/S ALFE2 ASIC
  - CMOS 130nm
  - 4 channels x 2 gains
  - Bipolar shaping, Tpeak~15ns
  - Power ~150mW/chan
- COLUTA
  - CMOS 65nm
  - 8 channels
  - Sampling 40 MHz
  - Amplitude measurement
    - 15-bit hybrid SAR ADC
    - ENOB ~11.5 bit
    - Power 140mW
  - 10 x 640Mbps link

CATIA+LiTE-DTU readout ASICs for CMS Phase-2 Barrel Calorimer Upgrade

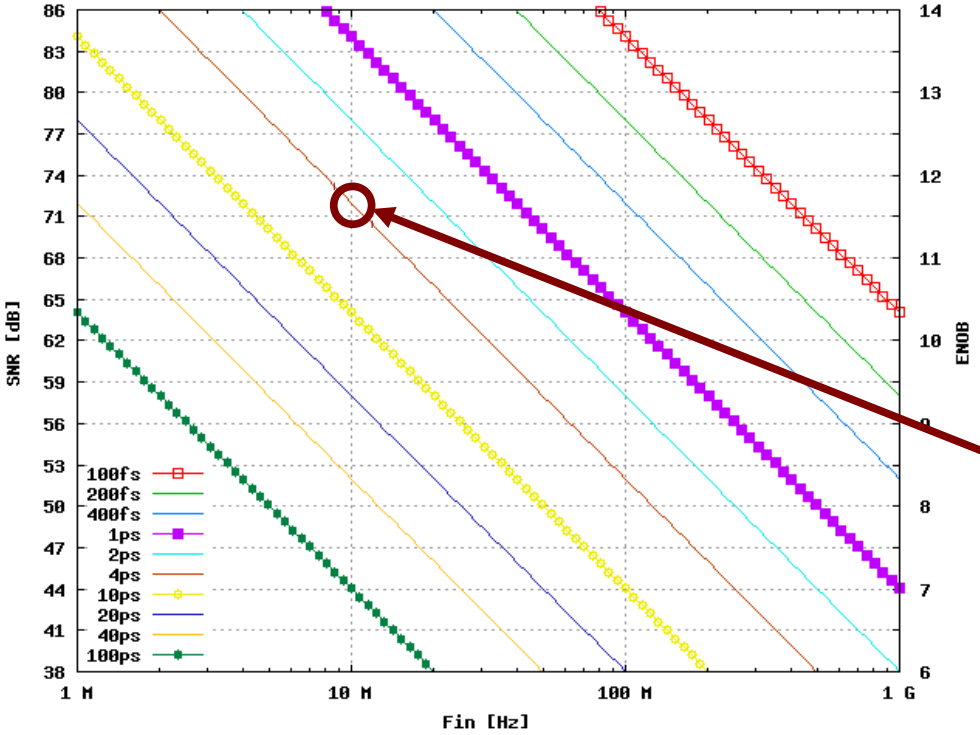


- CATIA ASIC
  - CMOS 130nm
  - Transimpedance amplifier with 2 gain stages
- LiTE-DTU
  - CMOS 65nm
  - 2 channels
  - Sampling 160 MHz
  - Amplitude measurement
    - 12-bit SAR ADC
    - ENOB ~10.7
    - Power ~10mW
  - Data compression and High speed link 1.28Gbps

- 2 ASICs in 2 CMOS processes
- Only 1/2 channels
- No TDC, very fast sampling (160MSps) to get timing info

Sampling fast signals at high resolution
Reminder on ADC aperture error

Resolution vs aperture jitter



$$SNR[dB] = 20\log\left(\frac{1}{2\pi f_{in} t_{Jitter}}\right)$$

$$ENOB \equiv \frac{SNR[dB] - 1.76}{6.02}$$

For f_{in}=10MHz and sampling jitter t_{jitter}=4ps it is NOT possible to get ENOB>11.7

Jitter od sampling clock degrades the ADC ENOB even for “perfect” ADC

HGCROC readout ASIC for CMS Phase-2 Calorimeter Endcap Upgrade

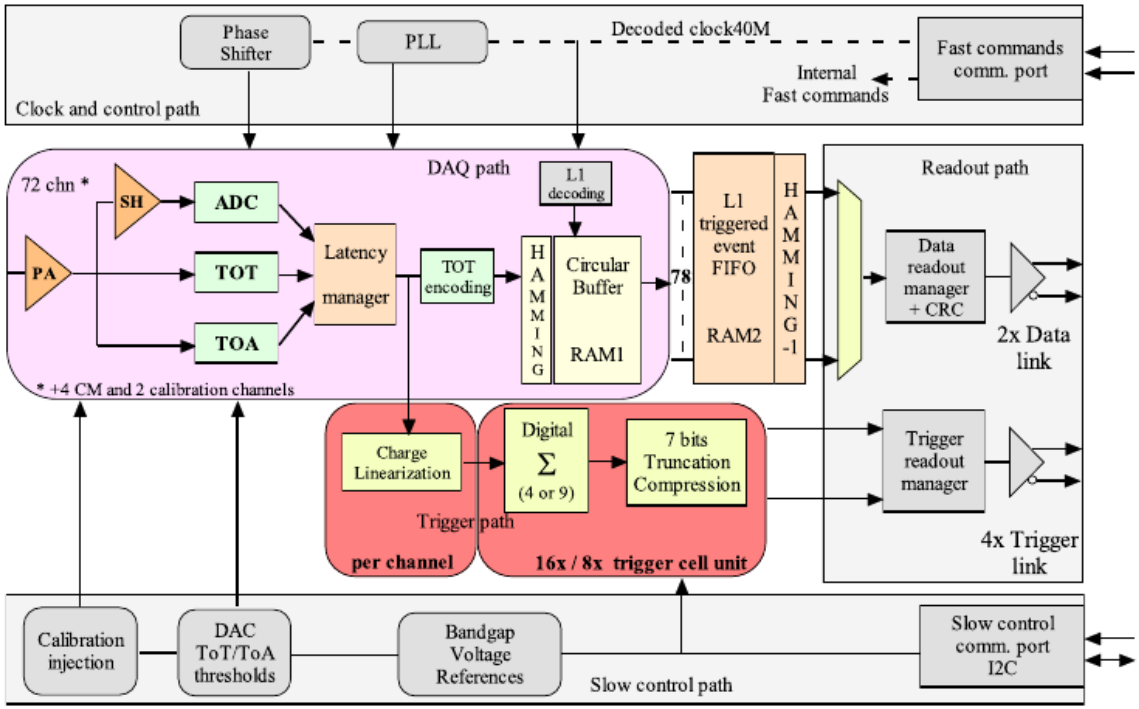


Figure 1. HGCROC3 block diagram with 72 regular channels divided in two paths: data acquisition with memorisation (DAQ) and trigger path.

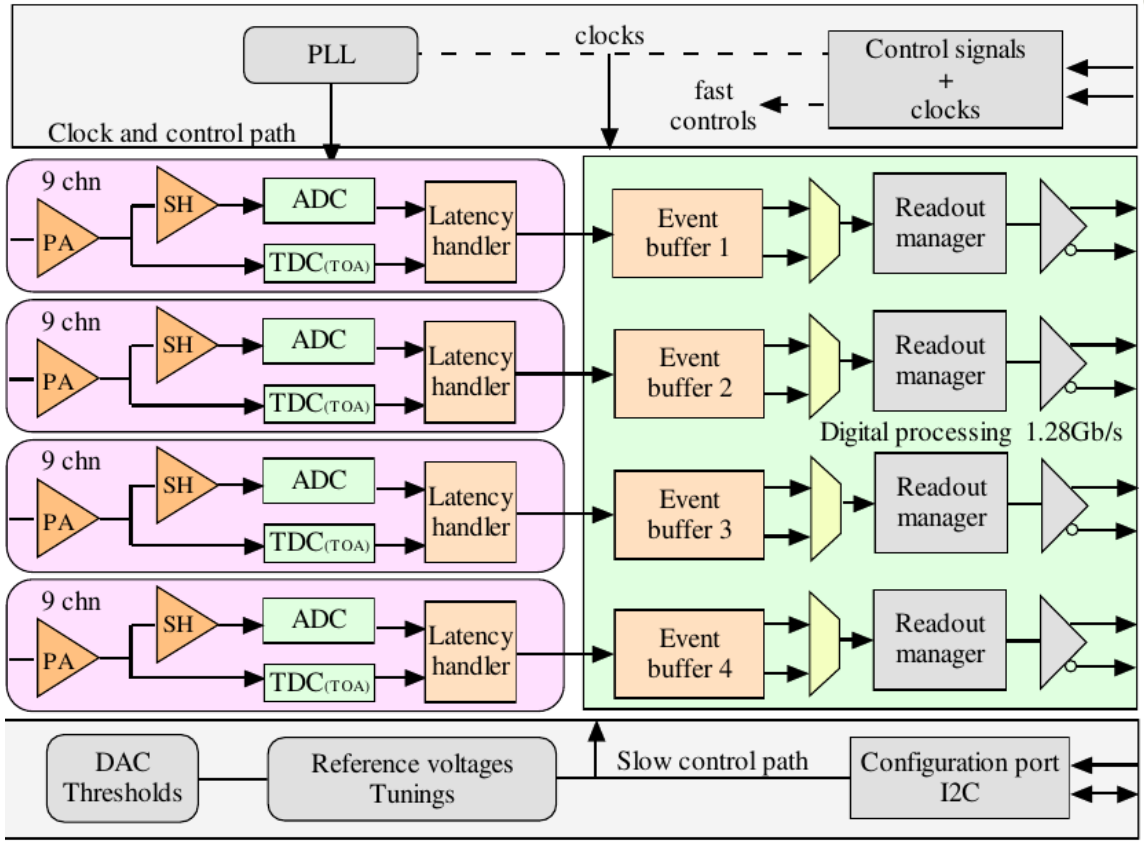
CMOS 130nm
72 channels
Sampling 40 MHz
Time measurement
- 10-bit TDC 25ps bin

Amplitude measurement
- 10-bit SAR ADC (linear range)
- ToT 12-bit TDC 50ps bin (saturation)

High speed links 1.28Gbps
Power <15mW/channel
- FE ~5.5mW
- 10-bit 40MSps ADC ~0.7mW
- 12-bit ToT TDC ~0.5mW@10%
- 10-bit ToA TDC ~0.5mW@10%

- One SoC-type ASIC including FE+ADC+TDC in each channel
- Multi-channel (72) ASIC
- Low power consumption

HKROC ASIC for PMs in Hyper-Kamiokande (derived from HGCROC)



- CMOS 130nm
- 36 channels
- Waveform digitizer (40MHz) with auto-trigger
- Hit rate 400-1000 kHz/chan average
- Time measurement
  - 10-bit TDC 25ps bin
- Amplitude measurement
  - 10-bit SAR ADC
- High speed links 1.28Gbps
- Power ~10mW/channel
  - FE ~5.5mW
  - 10-bit 40MSps ADC ~0.7mW
  - 10-bit ToA TDC ~0.5mW@10%

Key features similar to HGCROC but working as waveform digitizer with auto-trigger

Calorimetry - State of the Art
ASICs under development

Chip(s)	Experiment /Detector	CMOS nm	No. Chan.	ADC Fsample / N-bit / power	TDC
HGCROC	CMS/HGCAL ALICE/FoCal-E	130	72	40MHz / 10-bit / 0.7mW + TOT for large signal	Yes, 25ps bin
ALFE2 COLUTA	ATLAS/LArCalo	130 65	4 8	40MHz / 15-bit / 140mW	No, 200ps - ns (OFC)
CATIA + LiTE-DTU	CMS/ECAL	130 65	1 2	160MHz / 12-bit / 10mW	No, precise timing from ADC samples

Several other projects for LHC Upgrades are in less advanced stage ...

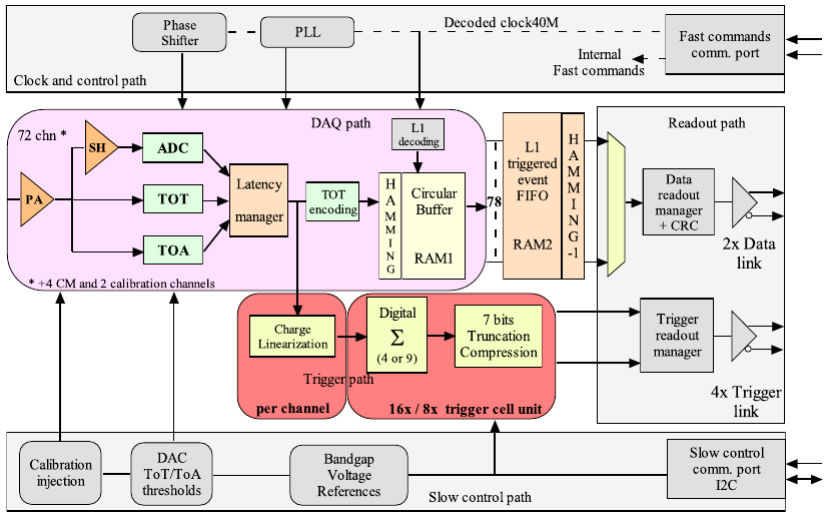
The idea of signal measurement

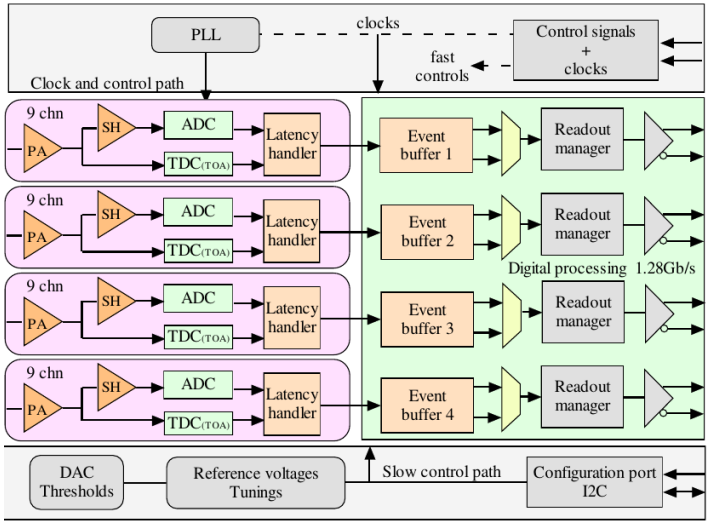
- Fast ultra-low power ADC&TDC in each channel
- Fast high-precision ADC and time measurement from pulse shape
- Very fast ADC and timing info inferred from ADC samples

Other considerations:

- SoC multi-channel ASIC (HGCROC) vs FE&ADC few-channel ASICs (ALFE+COLUTA, CATIA+LiTE-DTU)
- Usage of commercial blocks (ADC in LiTE-DTU)
- CMOS 130/65nm used presently

DRD6 proposal: Common readout ASICs for calorimeter prototypes (OMEGA + AGH + CEA Saclay)

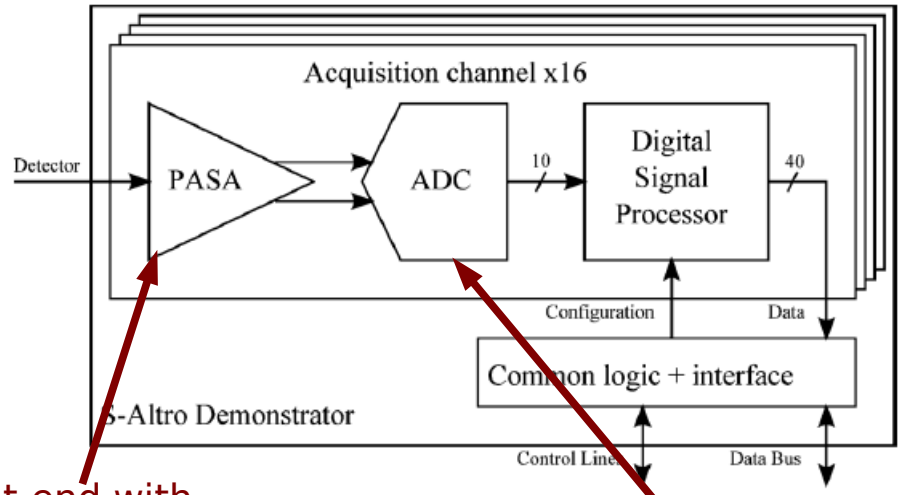




The idea is to start from HGCROC/HKROC ASICs:

- Main objective is to reduce power from ~15mW to few mW per channel
- Allow better granularity
- Improve performance in Preamp, Shaper, ADC, TDC, DSP
- Variants for Si, SiPM, LAr
- Implementation of cryogenic operation

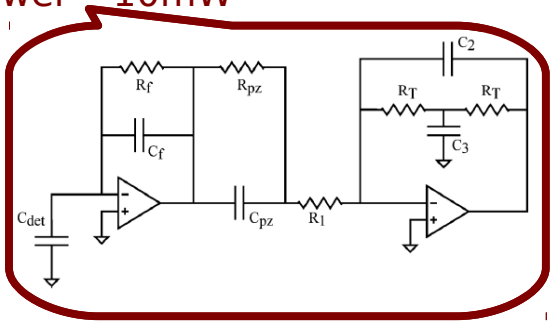
S-ALTRO ASIC in CMOS 130nm
State of the Art of SoC ASIC – 10 years ago!

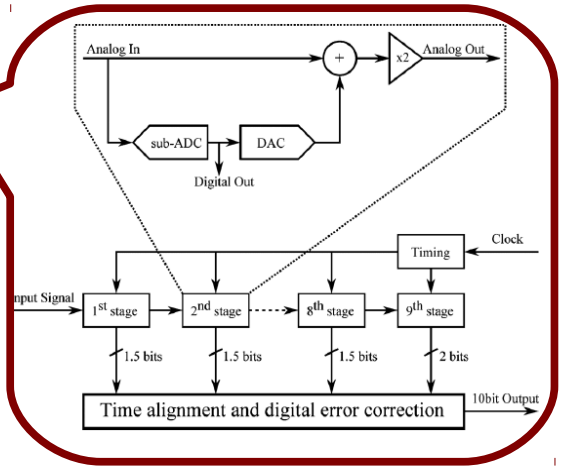


Supply voltage	1.5 V core, 2.5 V pads
Programmable gain	12, 15, 19 or 27 mV/fC
Programmable peaking time	30, 60, 90 or 120 ns
Shaper type	CR-(RC)^4
Programmable signal polarity	Positive or negative
Linearity	±5% up to 150 fC
Detector capacitance	4-20 pF
ENC	<1000 e$^-$ @ 12 pF
Cross-talk	<1%
Number of bits	10
Sampling frequency	10-40 MHz
Readout frequency	max 80 MHz
Power consumption	<50 mW/channel
Area	<4 mm^2/channel

Front-end with
semi-gaussian shaper
Power ~10mW

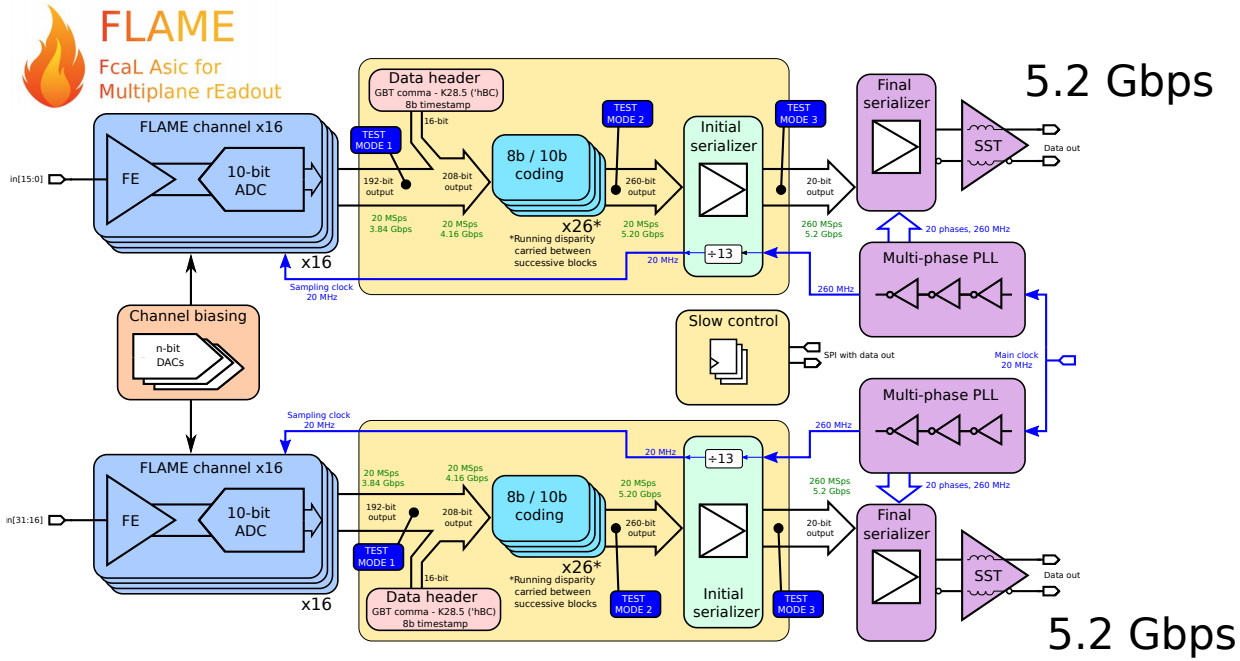
10-bit pipeline ADC
ADC consumes ~33 mW !!

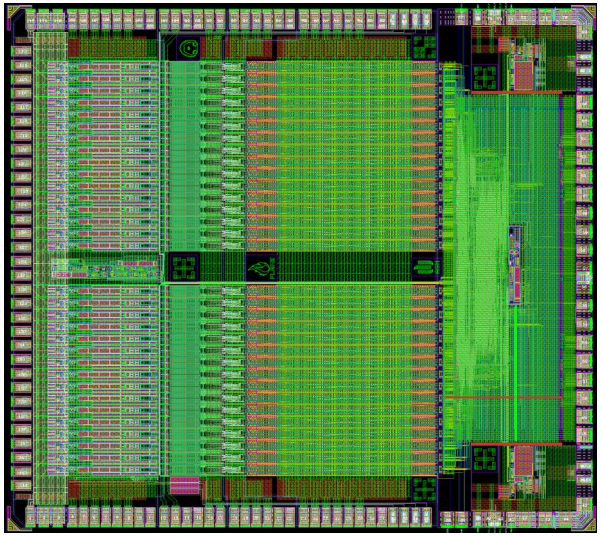




P. Aspell, M.De Gaspari, H. Franca, E. Garcia, L. Musa "A Super-Altro 16: A Front-End System on Chip for DSP Based Readout of Gasous Detectors", IEEE Trans. On Nucl. Science vol. 60, April 2013 pp. 1289-1295

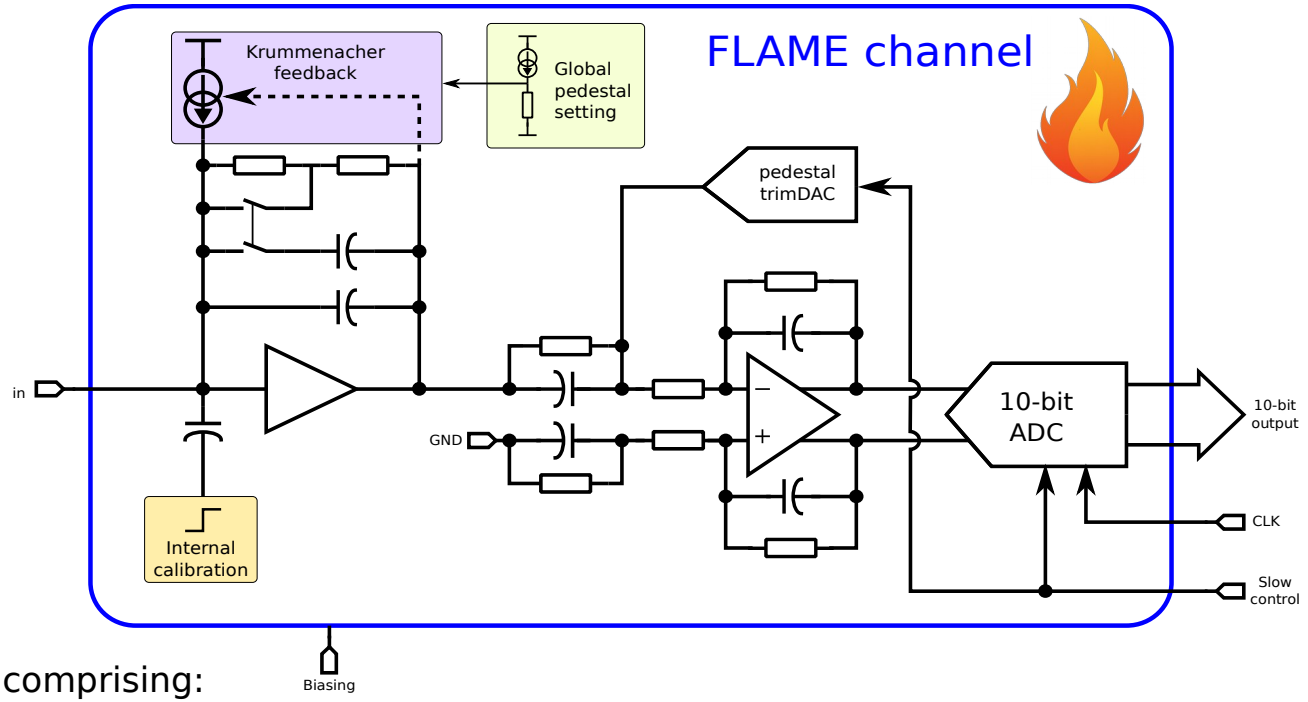
FLAME Readout ASIC in CMOS 130nm for forward calorimetry





FLAME is a 32-channel ASIC in CMOS 130nm with analog front-end (T_{peak}~50ns, switched gain), and 10-bit ADC (f_{sample}=20MHz) in each channel, followed by two fast (5.2Gbps) serialisers and data transmitters

FLAME ASIC in CMOS 130nm
Single channel



- Analog front-end comprising:
  - Charge sensitive preamplifier with variable gain:
    - High gain – for MIP sensitivity (up to ~200fC)
    - Low gain – for shower measurement (up to ~6pC)
  - Detector capacitance ~20-40pF
  - Differential CR-RC shaper with ~50ns peaking time – for amplitude and time measurement using deconvolution
  - Krummenacher feedback
  - Internal calibration and pedestal trimDAC
  - Power consumption ~1.2mW

- 10-bit SAR ADC in each channel
  - Default sampling rate 20MSps (max. up to 50MSps)
  - DNL, INL < 0.5 LSB
  - ENOB > 9.5
  - Ultra low power consumption (~0.7 mW/channel@40 MSps ~0.35mW/channel@20MSps)

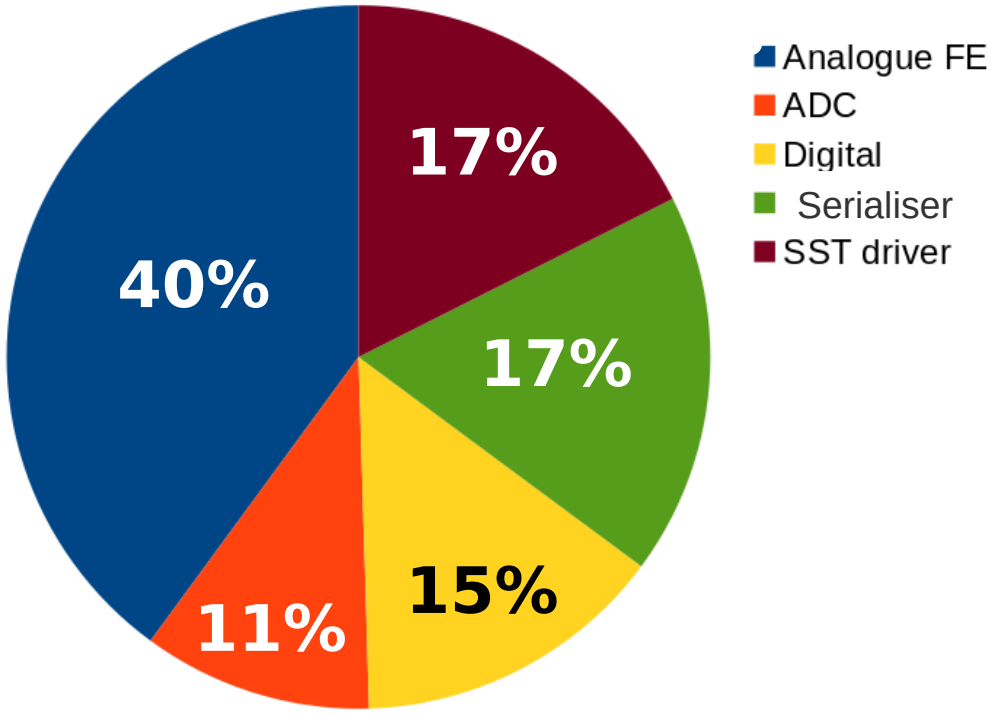
FLAME ASIC in CMOS 130nm
Power consumption and contributions

Average power consumption:
3.13 mW / channel

- Analogue FE : 1.25 mW/chan
- ADC : 0.33 mW/chan
- Digital : 0.45 mW/chan
- Serialiser : 0.55 mW/chan
- SST driver : 0.55 mW/chan

Total ASIC consumption (32 channels)

- Analogue FE : 40.0 mW
- ADC : 10.6 mW
- Digital : 14.4 mW
- Serialiser : 2x 8.8 mW
- SST driver : 2x 8.8 mW
- **Total : 100 mW**



In last decade huge decrease of power consumption, for ADC almost 2 orders of magnitude – mainly due to architecture

Power&Speed vs CMOS process 130/65/28 nm
Comparison of fast 10-bit SAR ADCs

CMOS [nm]	Verification	Power@40MHz [uW]	Max fsample [MHz]	Applications in ASICs
130	Fabricated ASIC M. Firlej et al. JINST 18 P11013	680	50	FLAME, HGCROC, HKROC, TOFHIR
65	Fabricated ASIC J. Moroń TWEPP 2019	440	50-60	
65	Fabricated ASIC J. Moroń TWEPP 2019	~550	80-90	lpGBT (analog part)
28	Post-layout simulation	~150 ?	~200 ?	

- 65nm consumes less and is faster than 130nm, but there is not much difference
- if post-layout simulations are reliable (???) there is a big advantage of 28nm, both in power and speed

Cooperation between DRD7 and other DRDs… DRD1 wish-list ?

- DRD7 – R&D on Electronics and Data processing should interact and cooperate with other detector DRDs
  - Using this opportunity and being one of DRD7.3 conveners
    - mostly focused on DRD7.3 – “High Performance TDC and ADC blocks at ultra-low power”

I’d be glad to know your thoughts on possible cooperation and to know the DRD1 wish-list to DRD7.3

If not here you can always contact me by email.

Thank you for attention

Back-up

Timing Detectors - State of the Art
ASICs under development

Chip	Experiment /Detector	CMOS nm	No. Chan.	TDC / Total power per channel
TOFHIR	CMS/BTL	130	32	TAC+ADC10-bit40MHz, 20ps bin (~30ps) / ~17mW TOT amplitude measurement
ETROC	CMS/ETL	65	16x16	TOA+TOT, ~20ps bin (<50ps) / ~3mW
FastRICH	LHCb/RICH	65	16	CFD, 25ps bin (30-40ps) / ~6mW
ALTIROC	ATLAS/HGTD	130	15x15	TOA+TOT, 20ps bin (~35ps) / ~5mW TDC ~0.5mW@10% occupancy

NOT to be compared! – numbers very approximate, different operation scenarios – only to show order of magnitude

- Different techniques - CFD, TOA+TOT, TAC+ADC - are used for precise time measurement
- Time precision is strongly affected by sensor contribution
- CMOS 65nm or 130nm preferred

Fast sampling - State of the Art
Multi-channel ASICs already completed (only <= 130nm considered)

Chip	Experiment /Detector	CMOS nm	No. chan.	ADC Fsamp. / N-bit / power	TDC
SAMPA	ALICE/TPC	130	32	10MHz / 10-bit / 1.5mW	-
PACIFIC	LHCb/SciFi	130	64	40MHz / 2-bit	-
SALT	LHCb/UT	130	128	40MHz / 6-bit / 0.5mW	-

SoC type ASICs including: analog FE, DSP, high speed links, etc…

The first complex multi-channel ASICs with sampling rates up to 40 MSps – LHC collision frequency 40MHz – are already operational or are being installed in LHC experiments. This has become possible thanks to the technology scaling and architecture development, in particular squeezing the ADC power to a level below the power of the analog front-end.