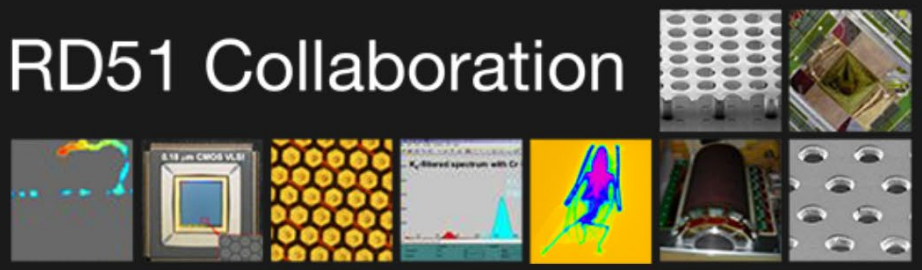

RD51 Collaboration → DRD1 Collaboration

Prospects for VMM4

for Applications in the DRD1 Collaboration

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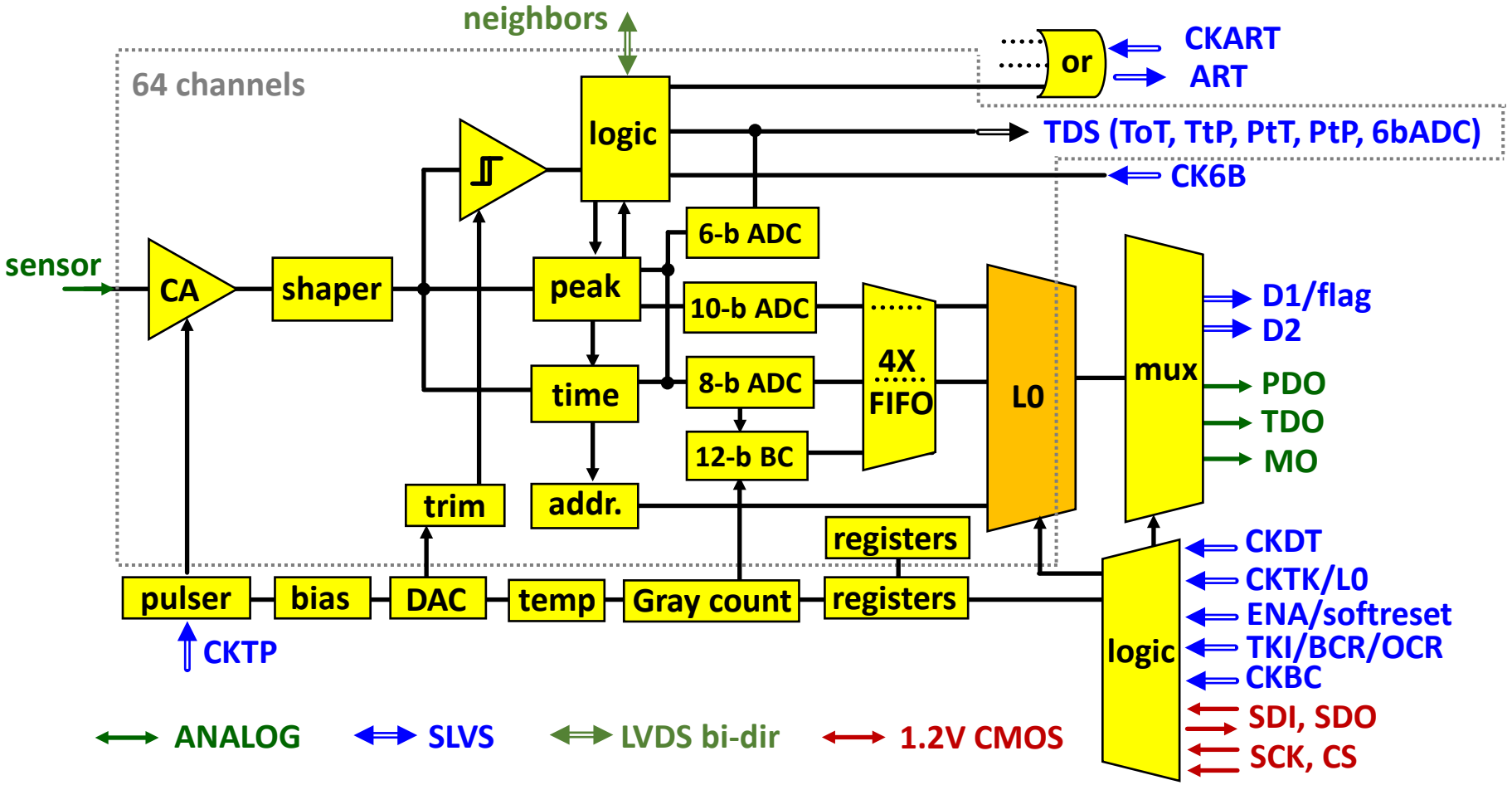
RD51 Collaboration Meeting, December 4-8 2023

Outline

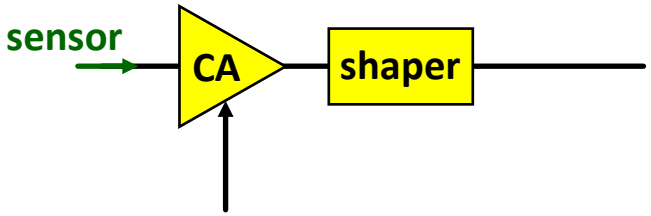
- **VMM3a**: architecture, performance, limitations
- Prospects for **VMM4**

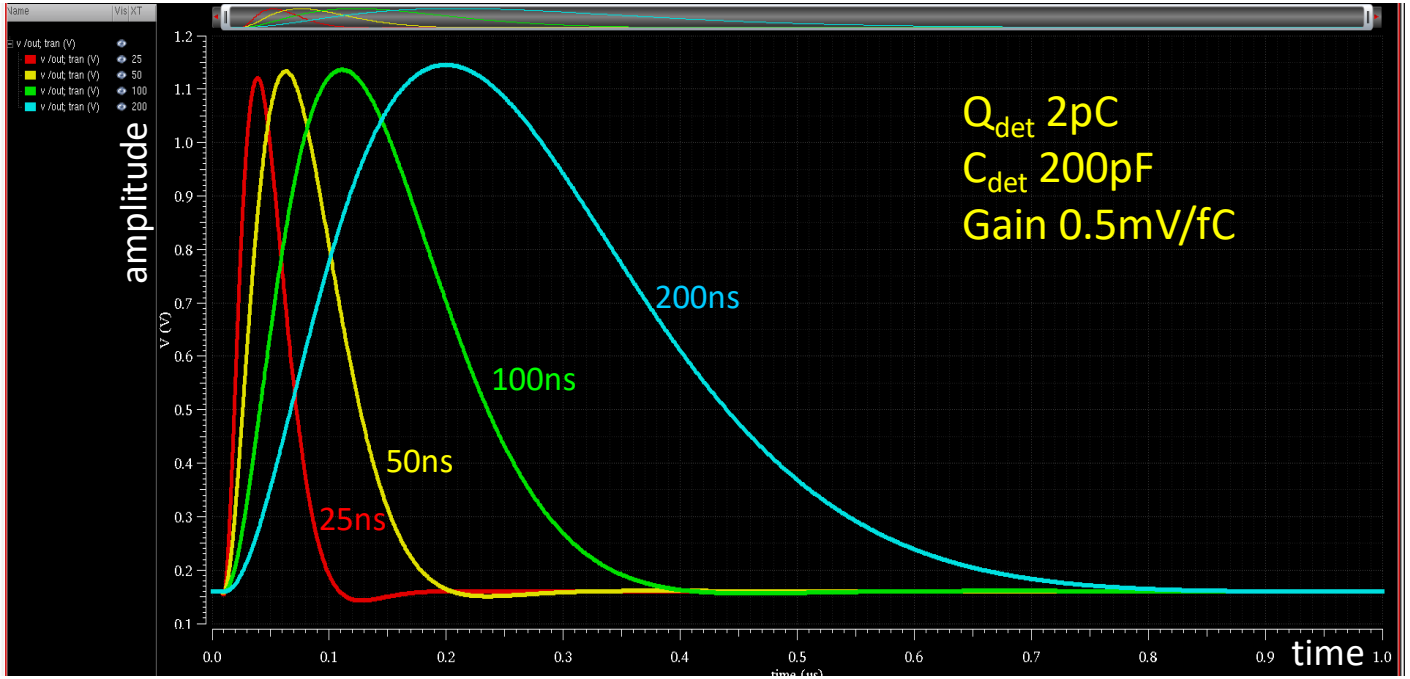
VMM3a Architecture



- high-functionality and high-programmability front-end ASIC
- designed for multiple NSW detectors, also adopted outside ATLAS
- efficient charge and timing measurements with high throughput

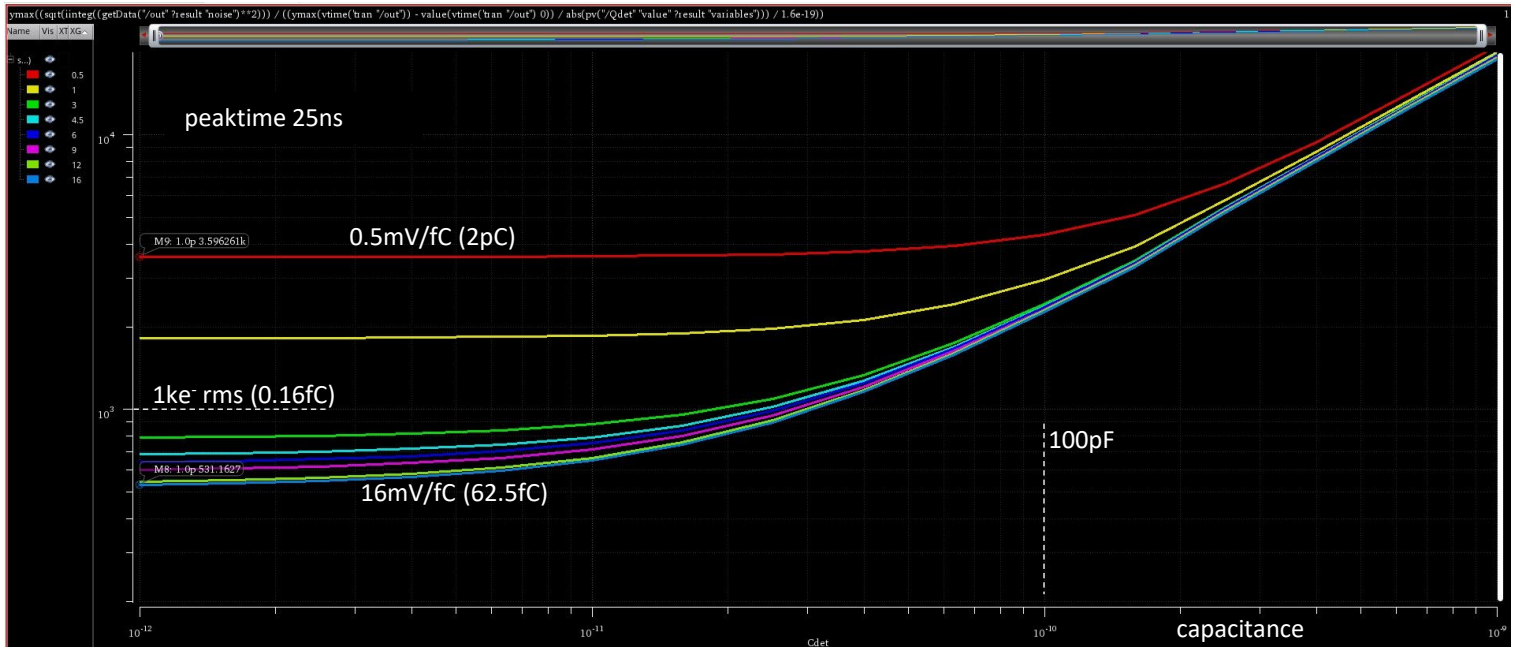
Analog Front-End

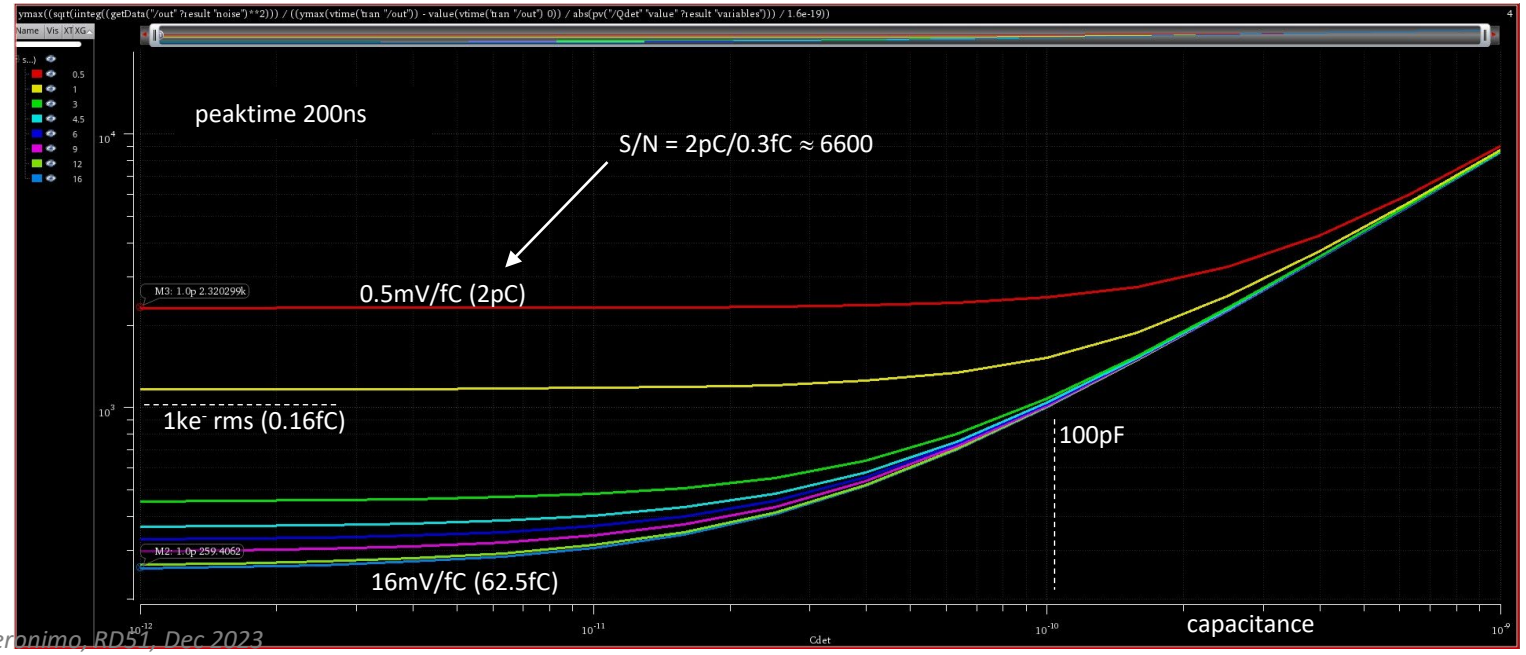




- input transistor: PMOS 180nm x 20mm, 2mA
- input capacitance: optimized for 200pF, can operate from **sub-pF to several nF**
- adjustable charge polarity: **positive, negative**
- adjustable gain**: 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC**
- maximum charge: linear up to **2pC**, fast recovery from **50pC**
- adjustable peaking time: **25, 50, 100, 200 ns**
- ion **tail compensation**: off, mild, strong
- leakage-adaptive, high-leakage modes, DDF low-noise shaper, BGR-stabilized baseline, test capacitor, mask, ...

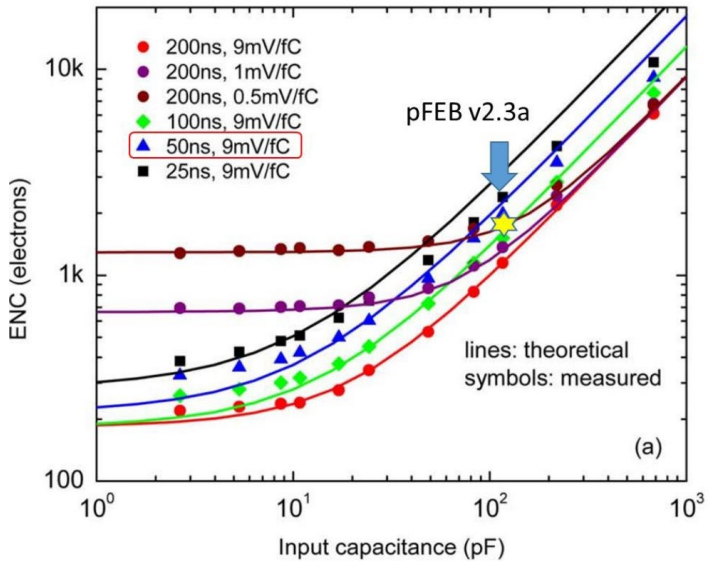
Equivalent Noise Charge

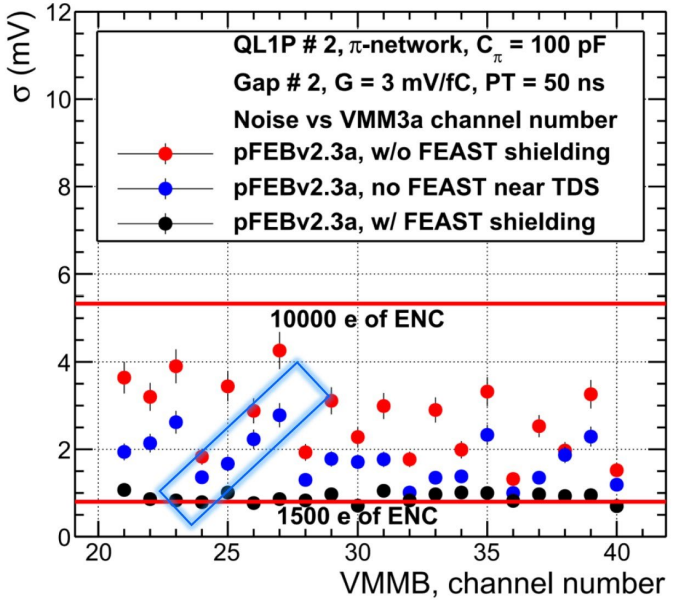




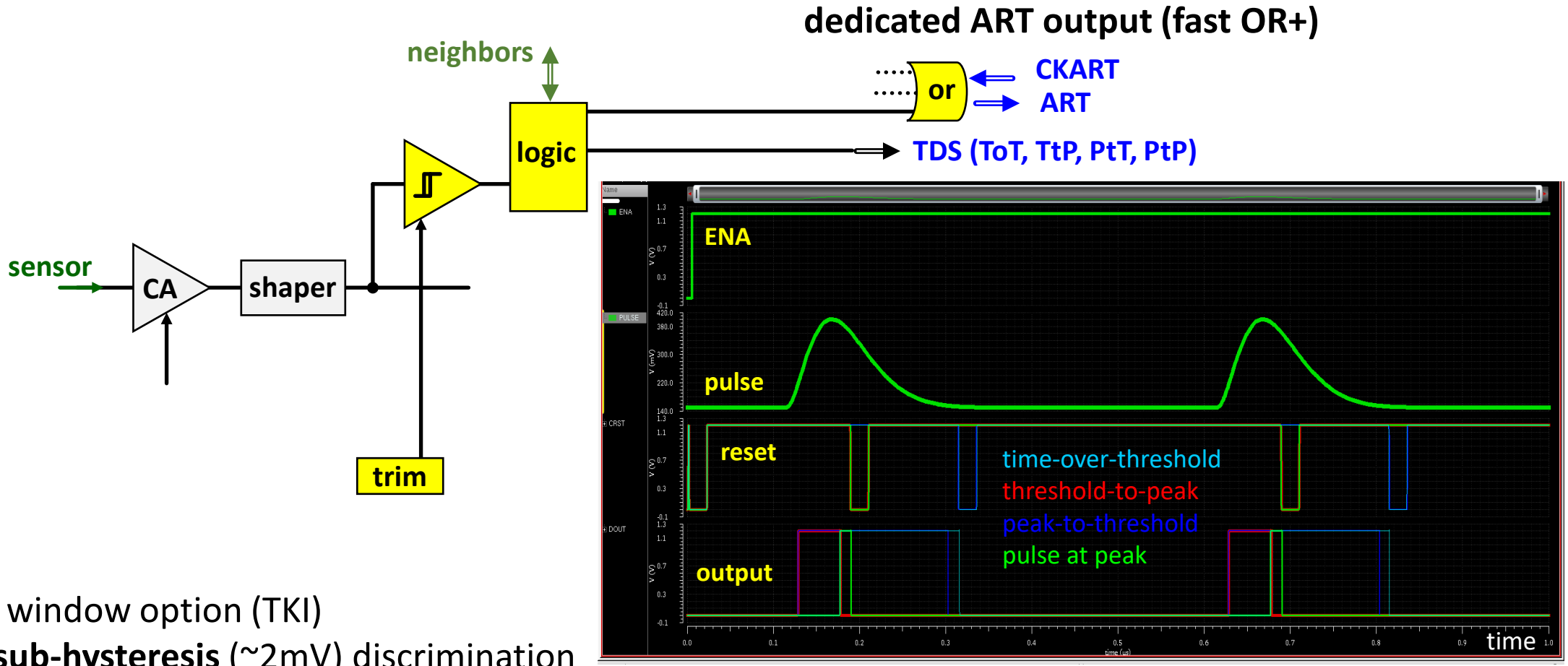
simulations (user reference)

example measurements (environment-dependent)



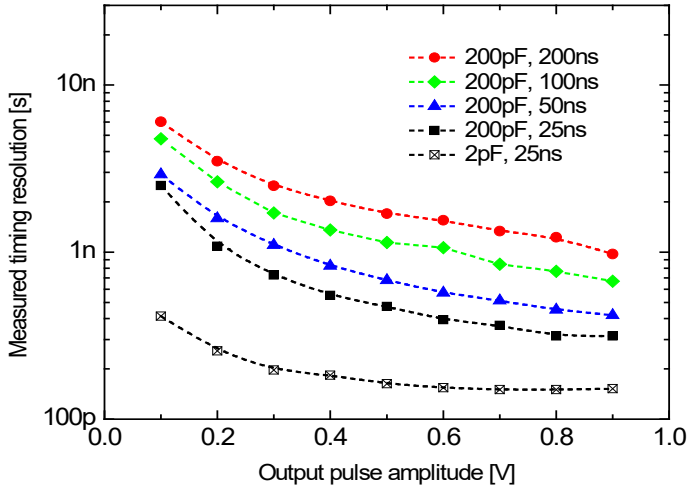


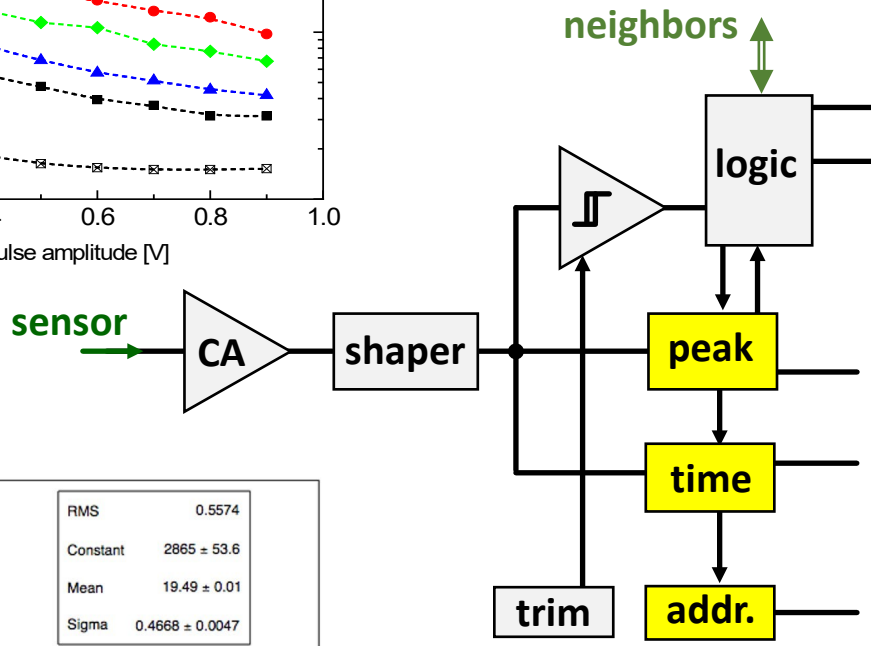
Discrimination, Direct Outputs, Address in Real Time (ART)

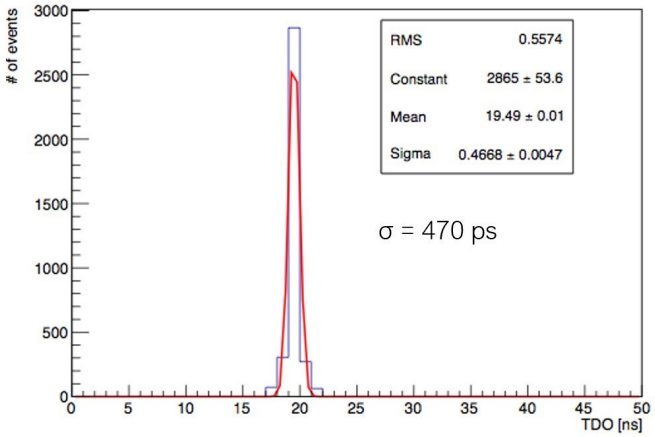


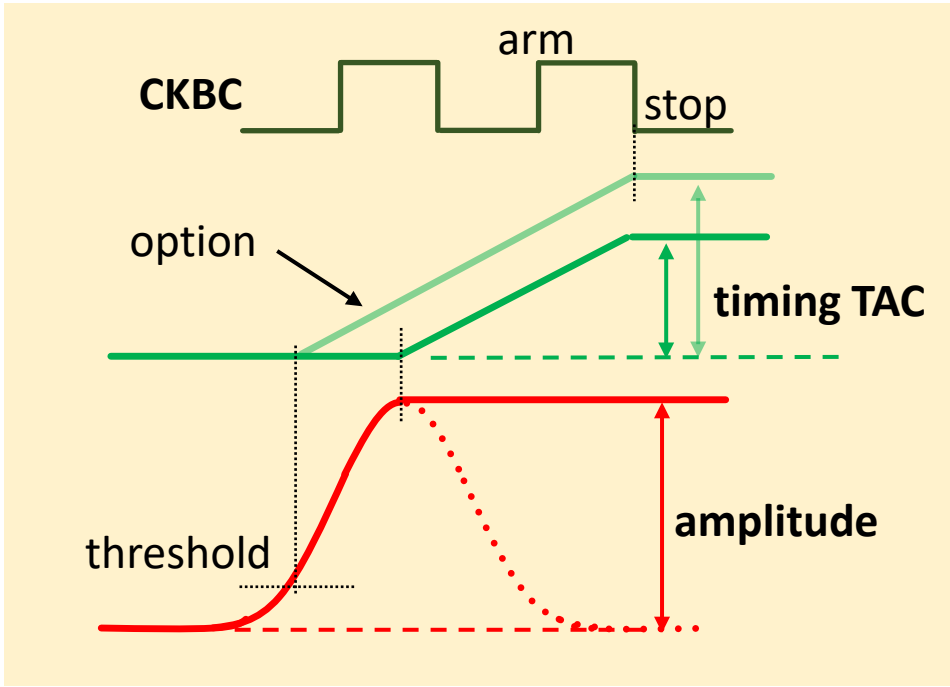
- acceptance window option (TKI)
- trimmable **sub-hysteresis** (~2mV) discrimination
- neighbor channels acquisition: **sub-threshold neighbors** with **inter-chip communication**
- flag with serialized **first address in real time** (ART) with dedicated output, **DDR option**, sync option
- **direct SLVS output per channel** with programmable measurements:
  - **time-over-threshold** ToT, **threshold-to-peak** TtP, **peak-to-threshold** PtT, **pulse-at-peak** PtP

Peak and Time Detection



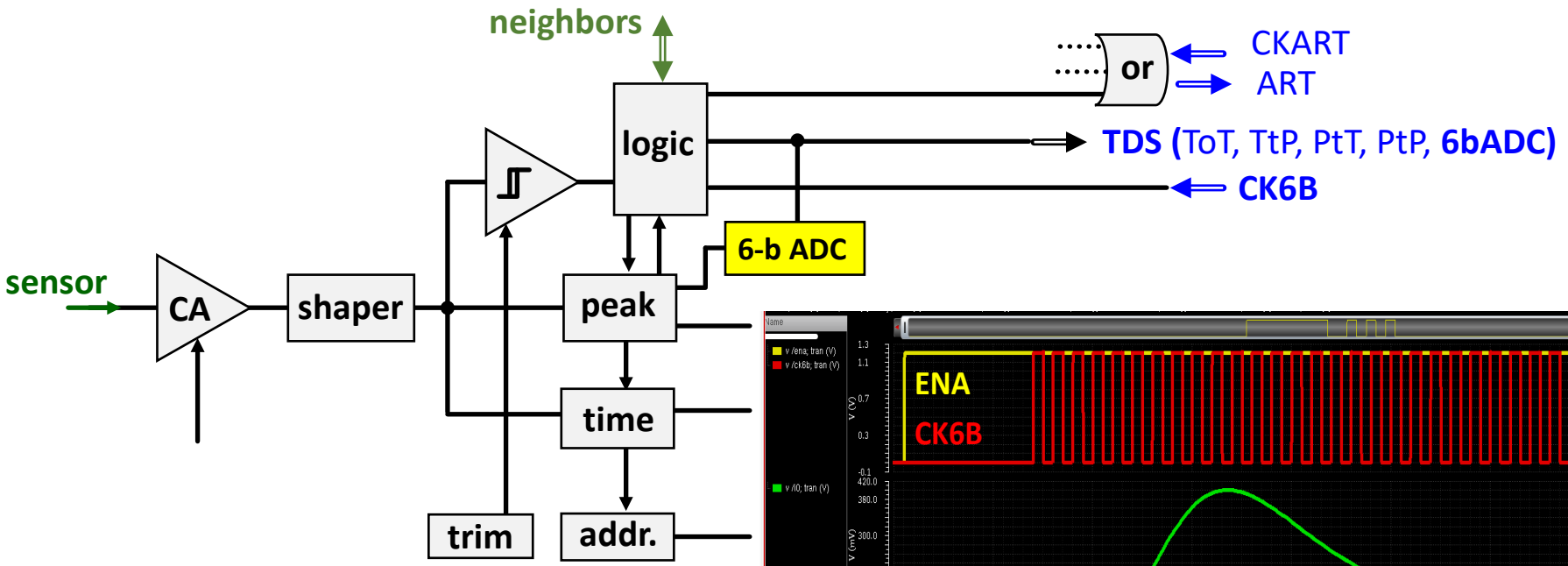


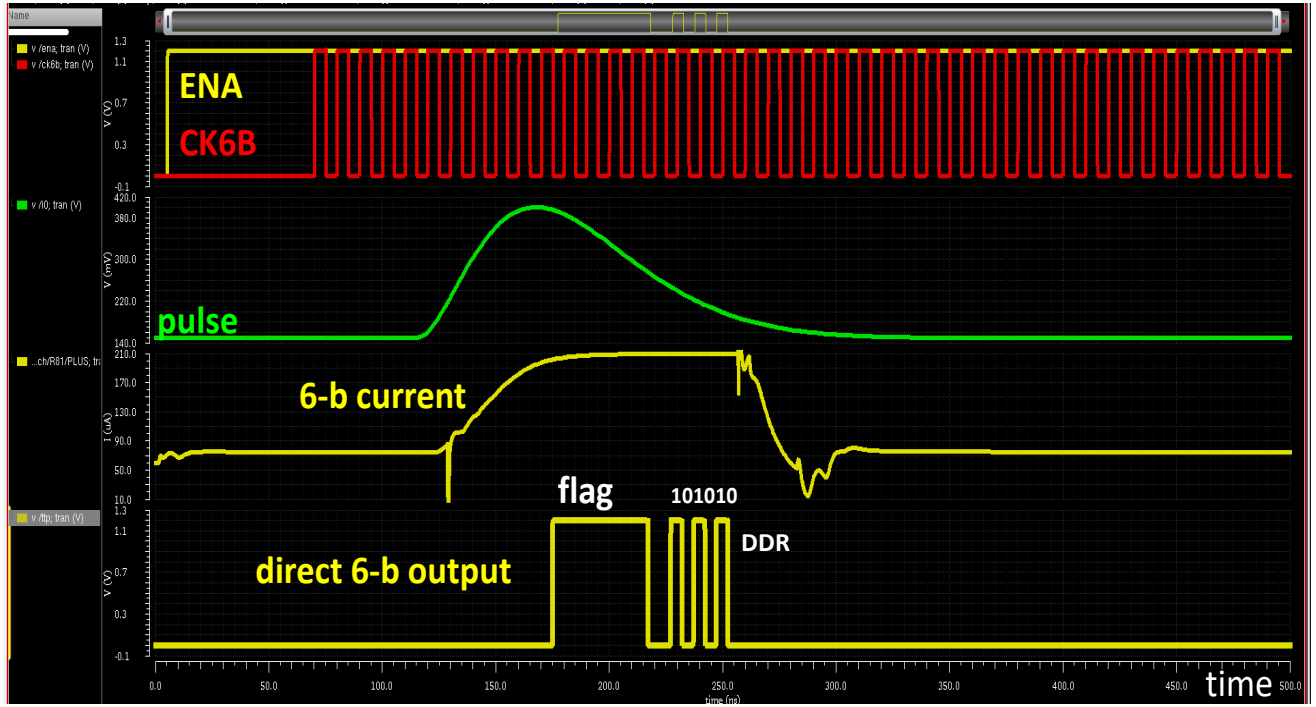




- peak detection: measurement of peak amplitude (charge) and storage in analog memory
- time detection: measurement of **peak timing** (**sub-200ps, low time-walk**), TAC and storage in analog memory
- optional **timing at threshold**, adjustable time-to-amplitude conversion (**TAC**): 60, 100, 350, 650 ns

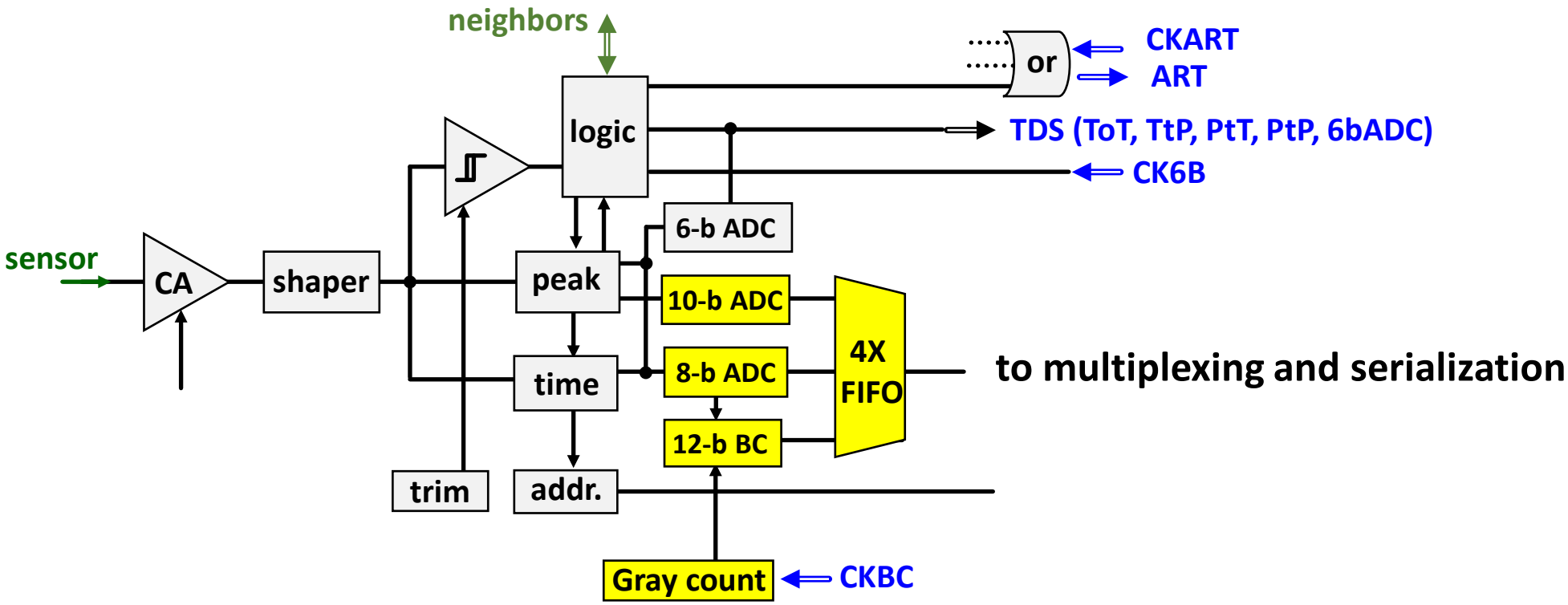
Lower-Resolution Direct 6-bit ADC Outputs





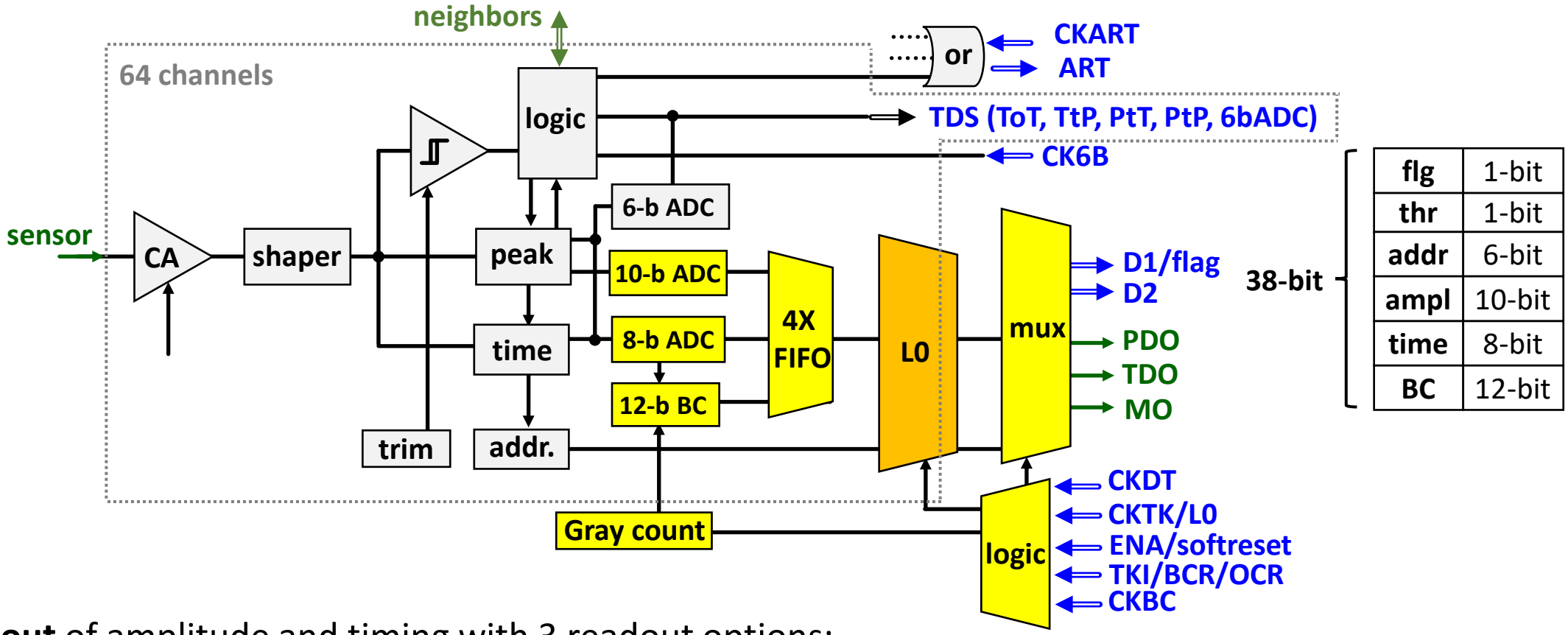
- direct 6-bit ADC output per channel
- event **flag at peak** followed by **serialized address**
- completes **conversion within 25 ns from peak**
- adjustable conversion time and offset
- **continuous** autoreset operation, **DDR option**

Higher Resolution 10- and 8-bit ADCs, Timestamp, Local FIFO



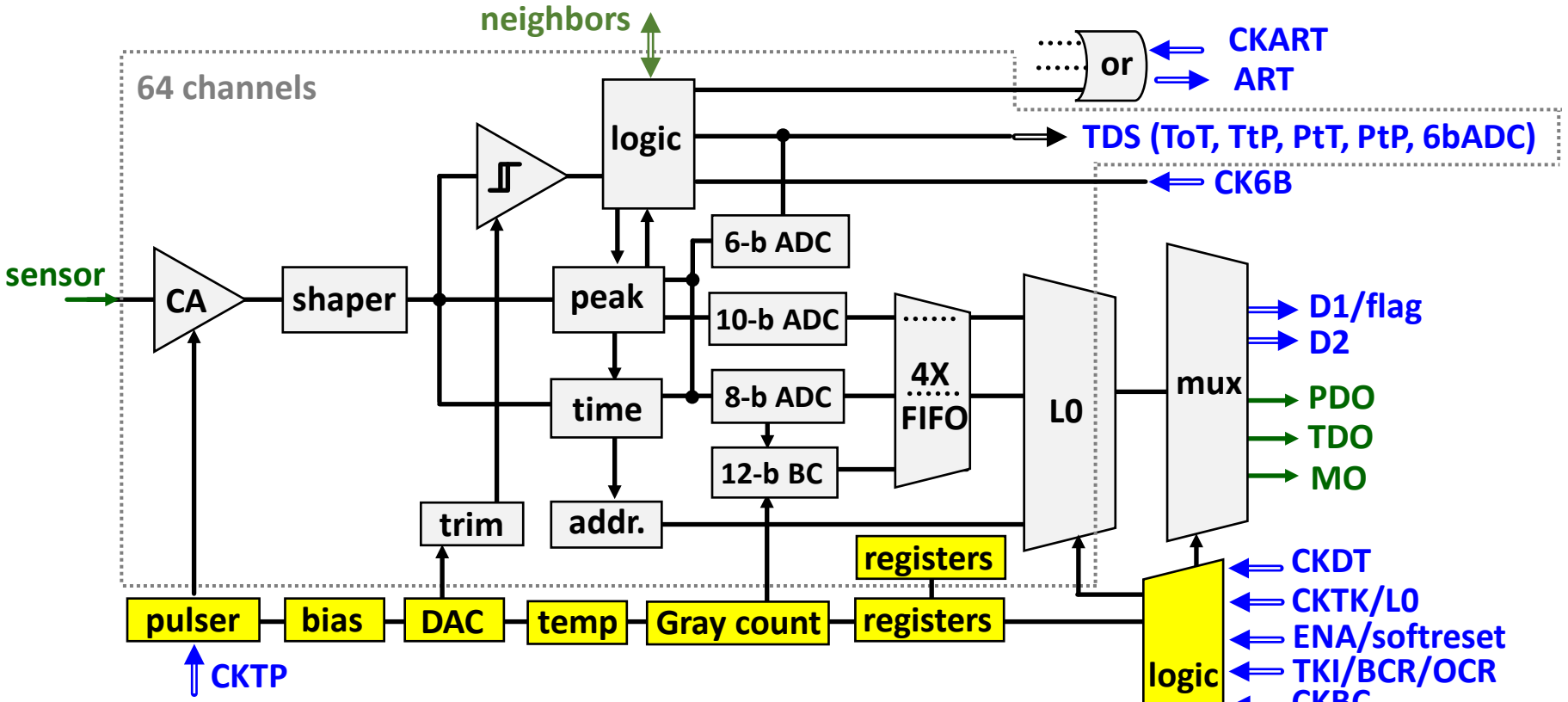
- **10-bit 200ns** peak **amplitude** conversion
- **8-bit 100ns fine timing** conversion of the TAC
- **12-bit coarse timestamp** from shared Gray-code counter
- full **timing** information: **20-bit** (~100µs worth) with sub-ns resolution
- local **4-deep FIFO** to provide derandomization

Readout Modes and Level-0 Processor



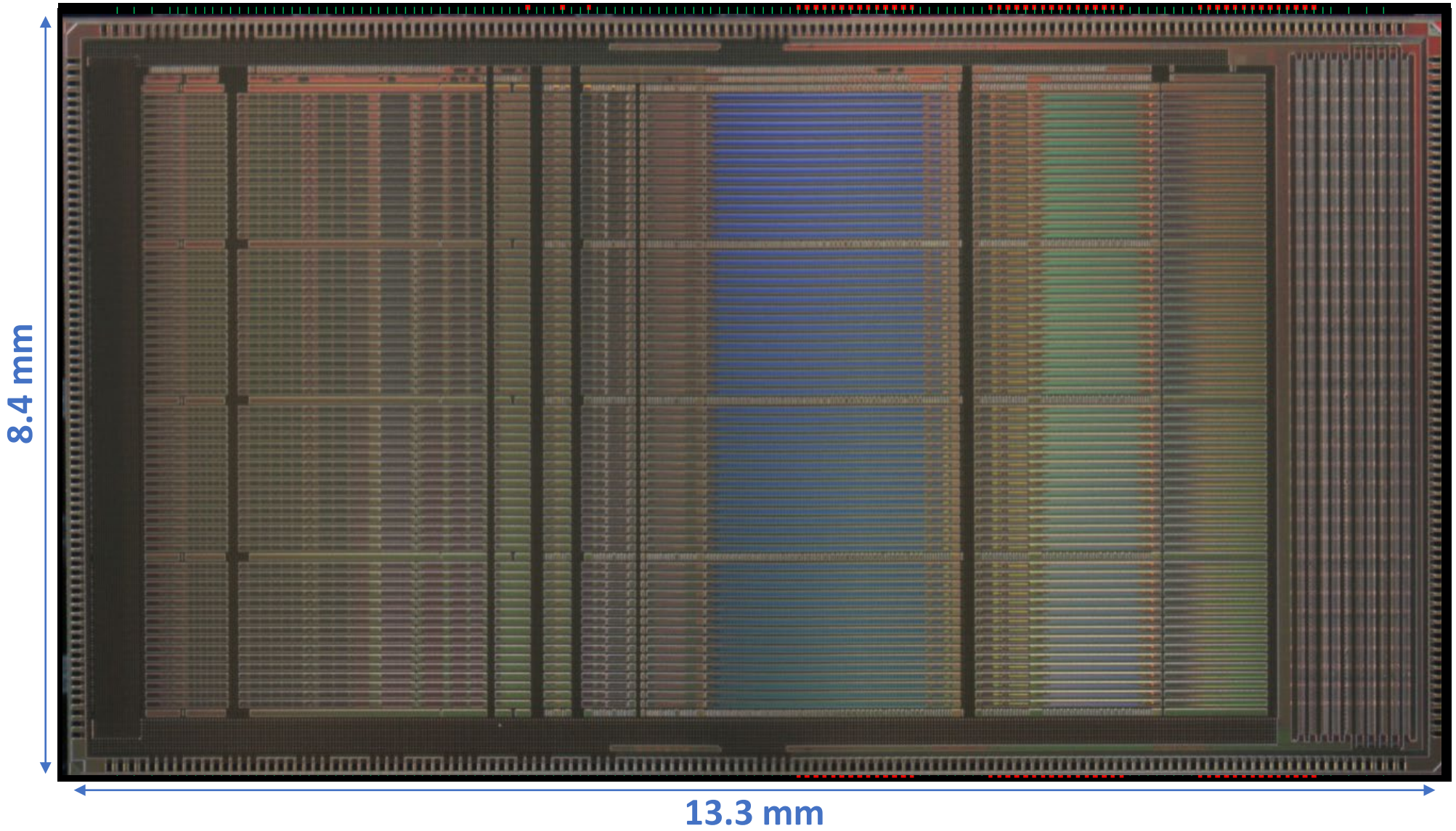
- **sparse readout** of amplitude and timing with 3 readout options:
  a) mixed-signal **2-phase**: analog peak and timing at PDO,TDO and serialized address
  b) digital **continuous**: 38-bit event data at **D1,D2**, **DDR** option (>1Gb/s)
  c) **level-0** processor (from Sorin Martoiu): NSW-specific, 64-deep latency FIFO, programmable acceptance windows, event builder, serializer, ...

Additional Functions and Shared Circuits



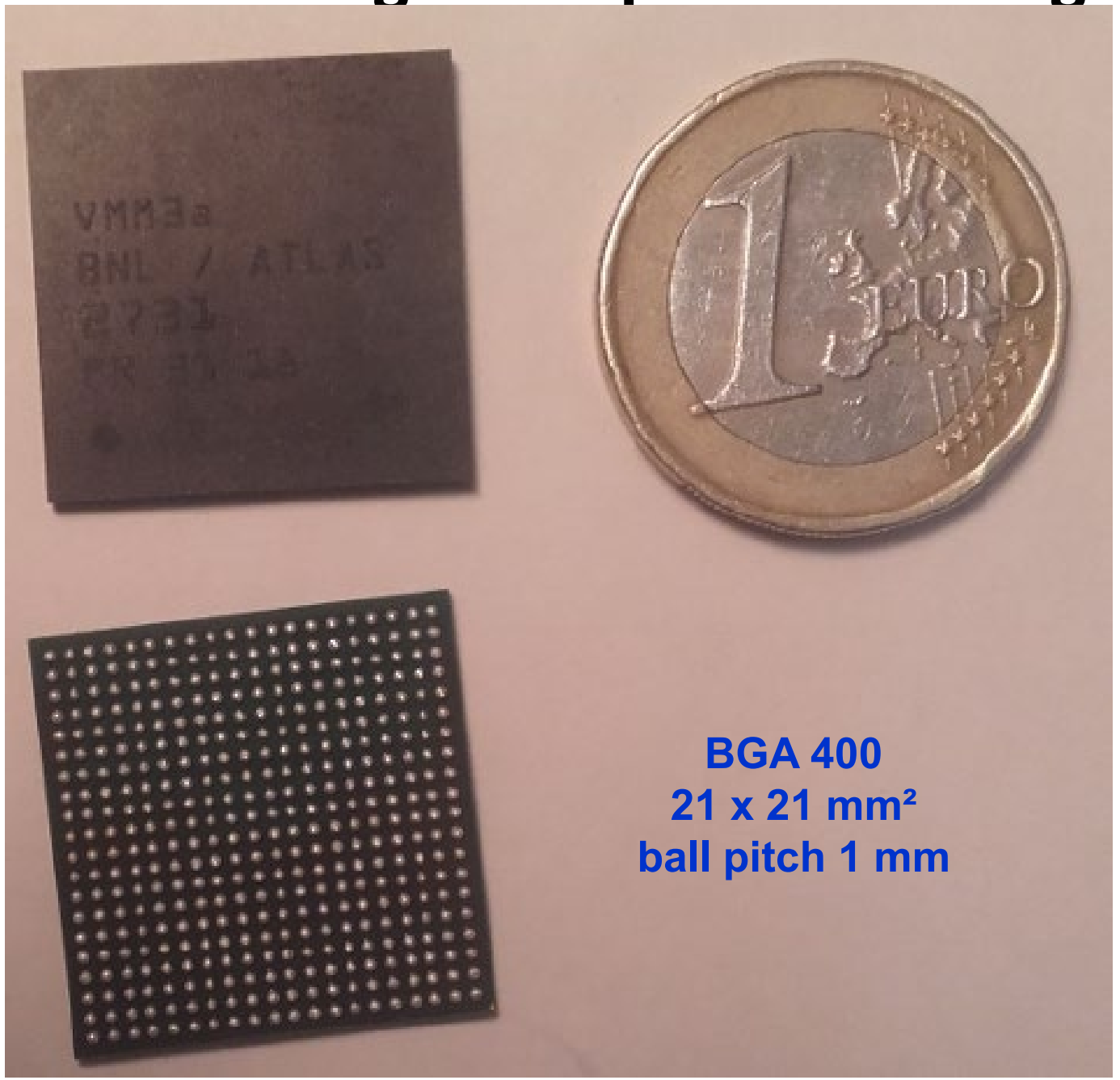
- **test pulse** generator 10-bit adjustable
- coarse **threshold** generator DAC 10-bit adjustable
- **temperature** sensor: ~ 725 mV - 1.85 mV/°C
- **analog monitor**: analog signal, trimmed threshold, DACs, temperature
- configuration **registers**: 96-bit + 24-bit / channel
- **SEU** and **TID** tolerant circuits

Physical Layout, Pinout, Fabrication



GD CMOS 130nm, power dissipation ~8-12 mW/channel (config. dependent), 10M MOSFETs

Wire Bonding and Optional Packaging



Vddp preamp +1.2V

Vdd analog +1.2V

Vss analog 0V

V ddad ADC +1.2V

V ssad ADC 0V

Vddd digital +1.2V

Vssd digital 0V

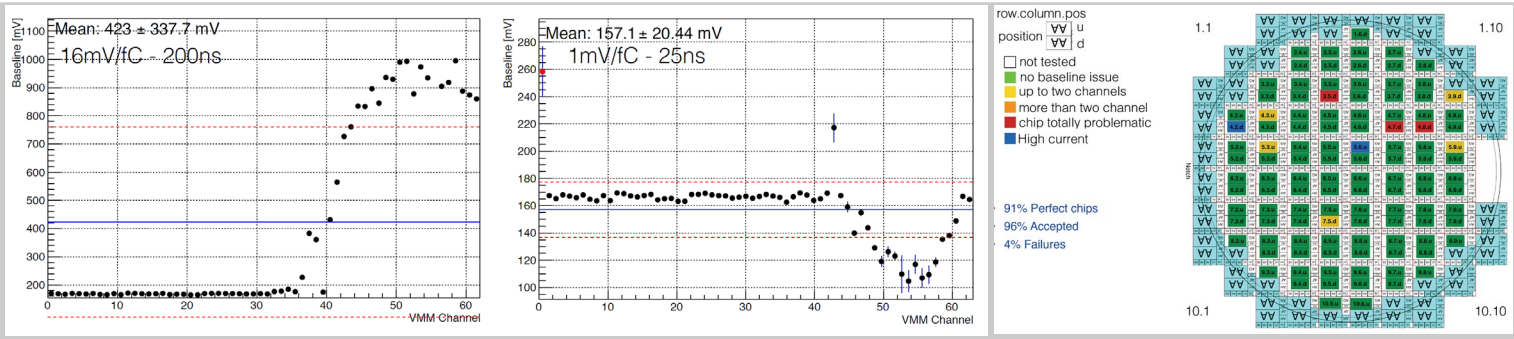
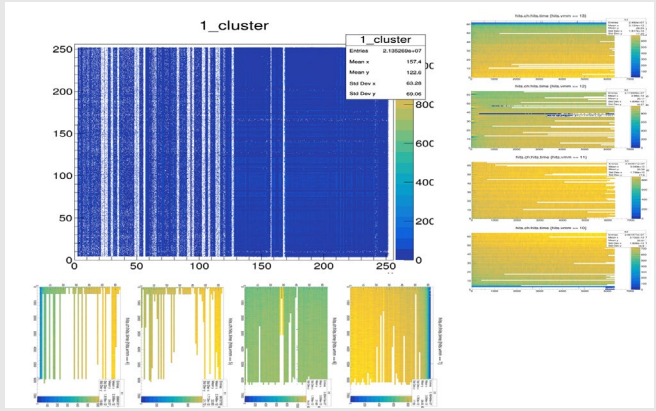
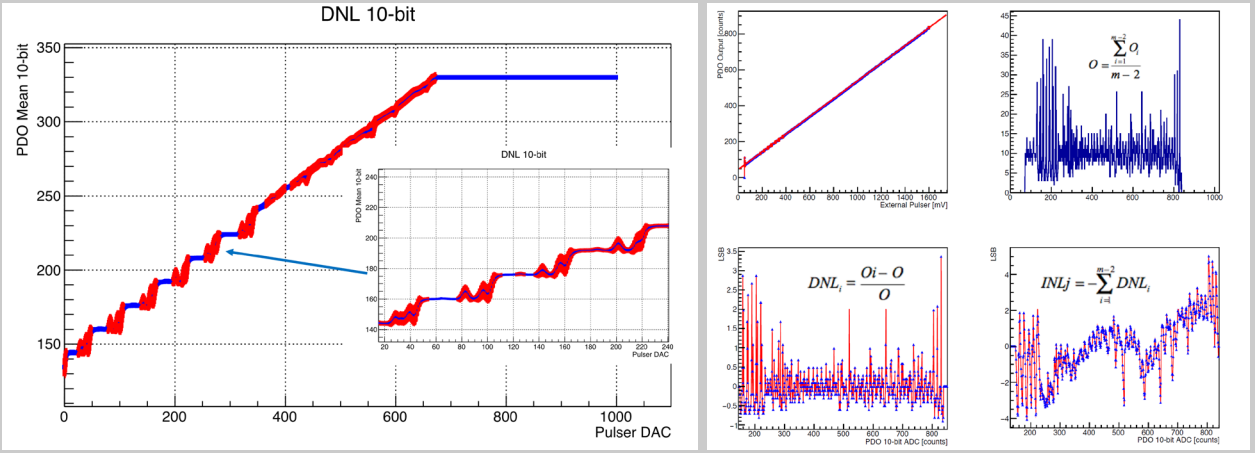
analog in

analog out

digital SE **IO**

+ xxx - SLVS IO

Issues in VMM3a

Item	Detail	Notes
Yield	• channel loss from abnormal gate leakage due to manufacturing problems, confirmed by GF in private communications • results in ~65% yield at 100% functionality • very localized issue, well understood and resolvable at design level	
Event loss	• first reported by Dorothea Pfeiffer @ ESS • present when operating in timing-at-threshold due to logic bug • results in channel loss or lock, depending on configuration • very localized, well understood and resolvable with design fix	 Occurring in ramp-at-threshold (SRAT=1). A time window opens from when the pulse crosses the threshold to when the peak is found. If the rising edge of CKBC doesn't occur within this time window, the stop signal doesn't get generated and the channel locks. Can be partially resolved by enabling auto-reset mode (STCR=1) plus 200ns peaktime and 650ns TAC slope. With any other peaktime or TAC setting channel loss may occur.
ADC linearity	• present in 8-bit and 10-bit ADCs, shows as • accumulations due to missing redundancy • results in effective ~7-bit resolution • can be resolved by adding redundancy or by upgrading to other ADC architectures	

Prospects for VMM4

concurrent

Item	Detail	Notes
Yield fix	localized MOSFET modification	
Event-loss fix	localized logic fix	re-enable local FIFO
ADCs upgrade	redundancy or upgraded ADCs	reduce deadtime, increase rate
Migration to TSMC 65nm	same 1.2V core voltage, additional metal layer	benefits: modeling, speed, noise, uniformity, power dissipation, rad. tolerance, fab. time
On-demand upgrades to support DRD1 detectors	▪ **optimized front-end and/or mixed-signal processing** ▪ **high-resolution modes (charge and/or timing)** ▪ **low-power modes** ▪ **higher rate capability** ▪ **L0-core revision or other dedicated DSP** ▪ **stronger ESD protections** ▪ **optimized digital interface** ▪ **additional functionality/programmability** ▪ **...** ▪ **multiple VMM4 versions, shared fabrication**	▪ adjust/extend peaktime and/or gain ranges ▪ achieve sub-100e^- and/or sub-10ps resolution ▪ add static/dynamic power-down options ▪ fast/parallel processing, upgraded Gb/s links ▪ multiple ad-hoc digital processing cores ▪ tailored low-parasitic configurations ▪ I2C access, multi-function IOs ▪ two VMM versions can fit one fab reticle cell

When targeting an ASIC common to all detectors, beware of unavoidable trade-offs!

Conclusions

- VMM3a
  - versatile design with high-functionality and high-programmability
  - designed for NSW, adopted by several research groups outside ATLAS
  - affected by few understood, localized and fixable issues
  - design modularity makes it suitable for revisions and upgrades

⬇

- **VMM4**
  - fixes (yield, timing-at-threshold, ADCs)
  - design migration to TSMC 65nm
  - on-demand upgrades to support DRD1 detectors
  - multiple VMM4 versions as needed

Acknowledgment

Hans Muller, Jochen Kaminski

George Iakovidis, Venetios Polychronakos, Sorin Martoiu