DRAFT

Wishlist future ASIC

Ad-hoc draft for suggestions

towards a common ASIC for gas detectors

Please send suggestions **before** the Wednesday 6 Dec   WG5 meeting

Task	Performance goal	Comments	Possible deliverables next 3-5 y
(Muon systems) New front end electronics	- 1 fC threshold - Geometrical avalanche quenching - High sensitivity electronics and new detector structures to achieve stable and efficient operation (rate, occupancy) up to O(MHz/cm2)	- Study of the integration of the FE electronics in the detector Faraday cage - Study of the integration of electronics and readout PCB	- Conceptual electronics design based on gas detector simulation and experimental measurements - Development and test of a front-end prototype
(Large-volume drift chambers) Front-end ASIC for cluster counting	- High bandwidth - High gain - Low power - Low mass	achieve efficient cluster counting and cluster timing performances	full design, construction and test of a first prototype of the front-end ASIC for cluster counting
(Straw chamber) Electronic readout, ASIC	- Time readout with sub-ns precision - Leading edge and trailing edge time readout	- Dedicated R&D on ASIC	- ASIC - Readout system
(Time Projection Chambers) Low-power FEE	•< 5 mW/ch for >1e6 pad TPC - ASIC development in 65 nm CMOS	•continuous vs. pulsed	- Present stable operation of a multi-channel TPC prototype with a low-power ASIC
(Gaseous photon detectors) FEE	- High input C - Low noise - large dynamic range	•	- present an ASIC concept/prototype
(Gaseous timing detectors) Low-noise FEE	- High input C - large dynamic range - Fast rise time - sensitivity to small charge - Low noise	•	Define an ASIC

Higher dynamic range

Vcc =1.2V

C_f = 1/gain

Q_{in}

U_{out} = Q_{in}/C_f
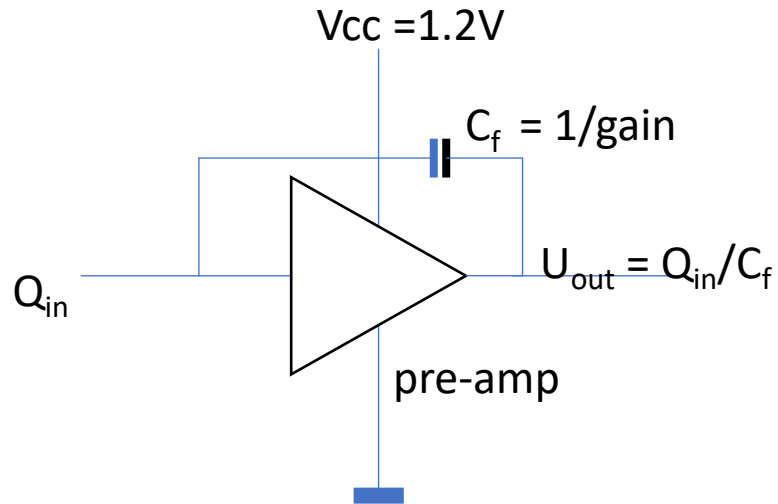
pre-amp

$Q_{in\ max}$ = Vcc[V] / gain

=> 62 fC @ 16mV/fC

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=> 1 pC @ 1mV/fC
=> 2 pC @ 0.5mV/fC

increase V_{cc} for preamps ?

dual gain: Qin -> 2 channels with gain1/gain2 = 4, 8, 16

logarithmic or dual-slope preamp

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Higher rates, less deadtime

interleaved SAR ADC blocks 10 or 12 bit ?

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Higher spark immunity

add integrated TVS to inputs

use newer input MOS technologies

add fast common-mode stabilizer to preamp inputs

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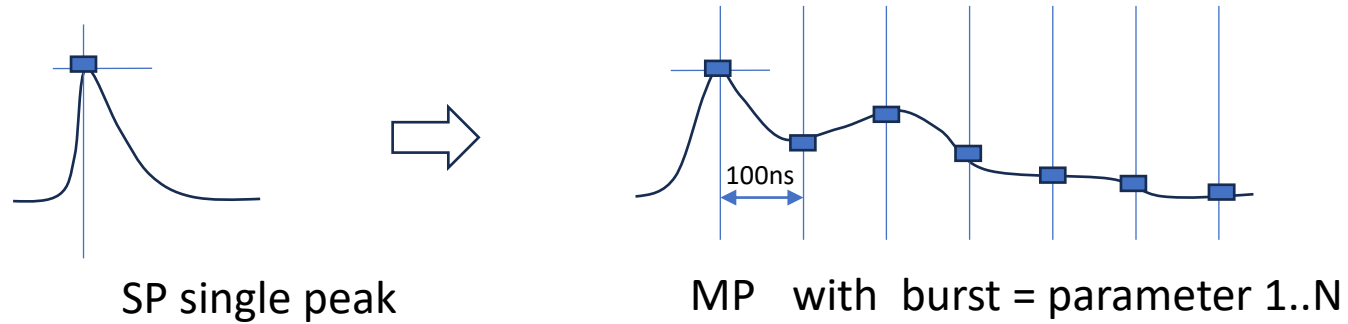## More flexible ASIC parameter Controls

add selective I2C register access

Faster and slower peaking times

16 ns …   400ns

picoSeC Ion tail cutter

auto-reset CSA at 1st peak

Enhance peakfinder-only mode by adding 10-MHz trailing samples

SP single peak

100ns

MP   with burst = parameter 1..N

Add simple Fast OR (threshold) output

32ch or 16 ch   ?

Preamp gain settings

settable per channel

power of 2   increase