SRS_e extended readout architectures

From “SRS classic” to $SRS_{extended}$

Hans Muller

From “SRS classic” to SRSe

More than 50 WG5 meetings with status on SRS classic since 2009

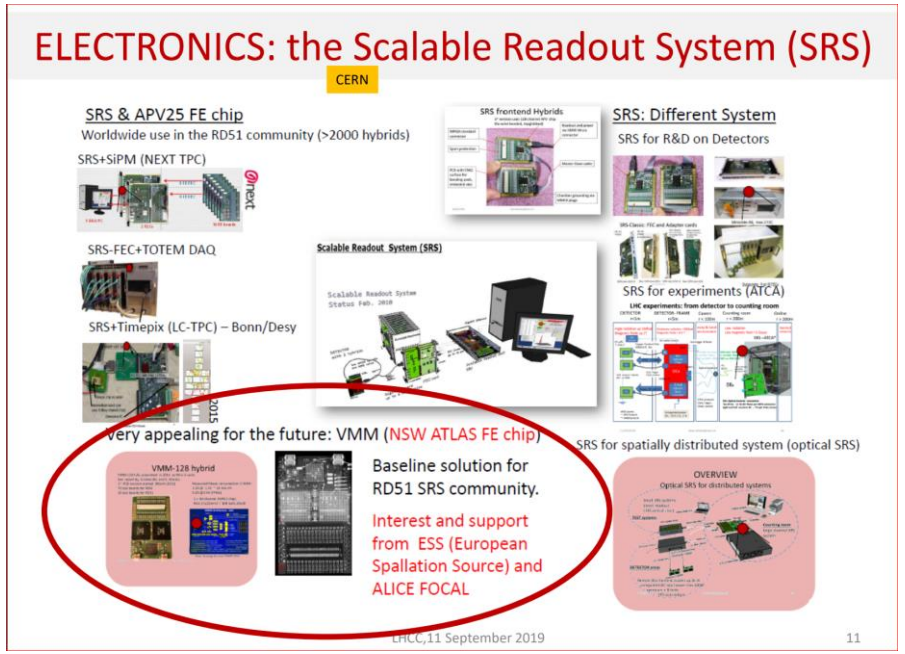
1st presentations SRS in Sept 2009

…….follow Indico over 14 years ….

Last SRS classic status report 2023

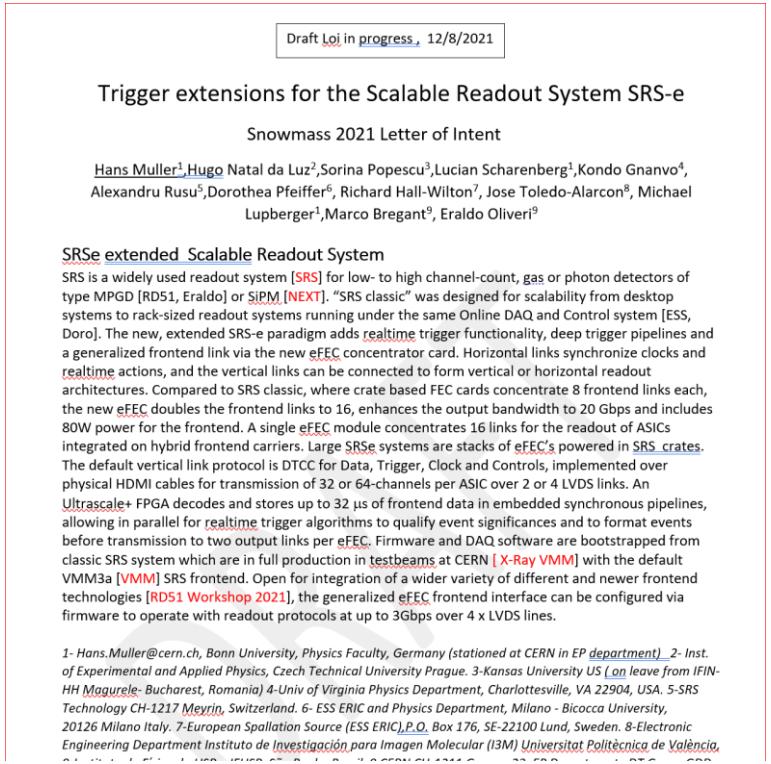
Today very last WG5 meeting :

going further with SRS$_e$



Revised and open for DRD1 teams

- Signatories 2021
  Snowmass LoI for SRSe



Draft LoI in progress , 12/8/2021

Trigger extensions for the Scalable Readout System SRS-e

Snowmass 2021 Letter of Intent

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SRSe extended Scalable Readout System

SRS is a widely used readout system [SRS] for low- to high channel-count, gas or photon detectors of type MPGD [RD51, Eraldo] or SiPM [NEXT]. "SRS classic" was designed for scalability from desktop systems to rack-sized readout systems running under the same Online DAQ and Control system [ESS, Doro]. The new, extended SRS-e paradigm adds realtime trigger functionality, deep trigger pipelines and a generalized frontend link via the new eFEC concentrator card. Horizontal links synchronize clocks and realtime actions, and the vertical links can be connected to form vertical or horizontal readout architectures. Compared to SRS classic, where crate based FEC cards concentrate 8 frontend links each, the new eFEC doubles the frontend links to 16, enhances the output bandwidth to 20 Gbps and includes 80W power for the frontend. A single eFEC module concentrates 16 links for the readout of ASICs integrated on hybrid frontend carriers. Large SRSe systems are stacks of eFEC's powered in SRS crates. The default vertical link protocol is DTCC for Data, Trigger, Clock and Controls, implemented over physical HDMI cables for transmission of 32 or 64-channels per ASIC over 2 or 4 LVDS links. An Ultrascale+ FPGA decodes and stores up to 32 µs of frontend data in embedded synchronous pipelines, allowing in parallel for realtime trigger algorithms to qualify event significances and to format events before transmission to two output links per eFEC. Firmware and DAQ software are bootstrapped from classic SRS system which are in full production in testbeams at CERN [X-Ray VMM] with the default VMM3a [VMM] SRS frontend. Open for integration of a wider variety of different and newer frontend technologies [RD51 Workshop 2021], the generalized eFEC frontend interface can be configured via firmware to operate with readout protocols at up to 3Gbps over 4 x LVDS lines.

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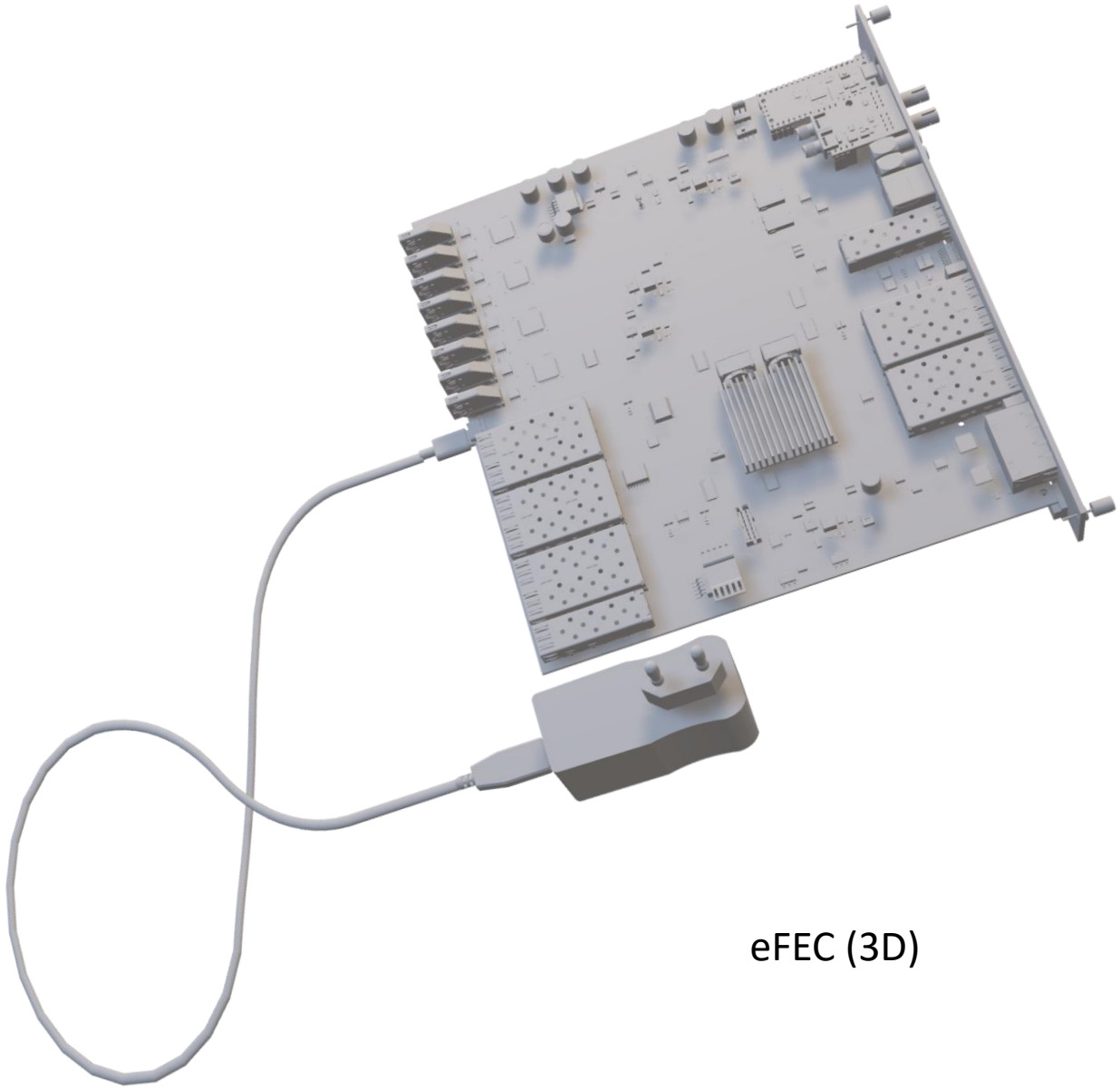
eFEC backend module

General
- same physical outlines as FEC + DVMM together 6U x 220mm
- housed and powered (USB-C) in classic SRS crates
- Ultrascale+ Zync FPGA

Connectors rear
- 8 x legacy, powered HDMI link ports to VMM frontend
- 6x frontend DTCCe link port SFP+ 1 /2.5/ 12.5 Gbps
- 1x 100Base Ethernet for Controls link
- USB-C power connector

Connectors front
- 4 x uplinks SFP+ to Online 10GBE/UDP
- 1 x uplink SFP+ vertical architecture summary link
- 2 coax Trigger Inputs and 2 coax trigger outputs (NIM)
- 1 CTF+ clock and trigger links (RG45)
- 1 x horizontal Xlink Rx Tx horizontal serial link (RG45)
- 1 x horixontal SYNCbus mixed analogue / digital

Plugin options
- 1 optical ST RX / TX link mezzanine (serial injector option)
- 32 bit SoC with USB debug port (Raspberry Pi pico)
- DDR4 plugin 64 GB (backside)



eFEC (3D)

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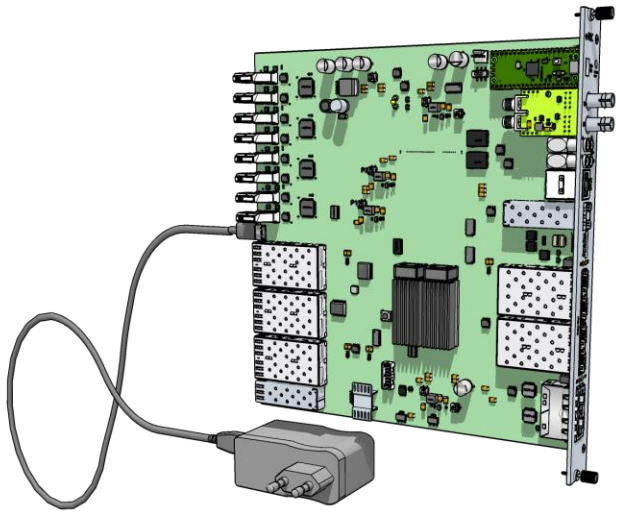
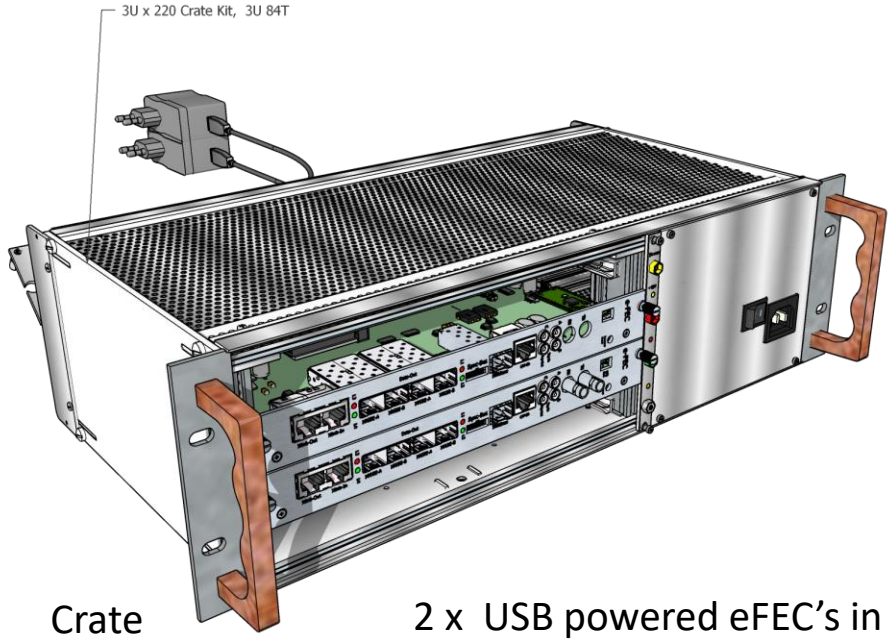
eFEC powered via USB-C (PD min 60 W)



Tabletop

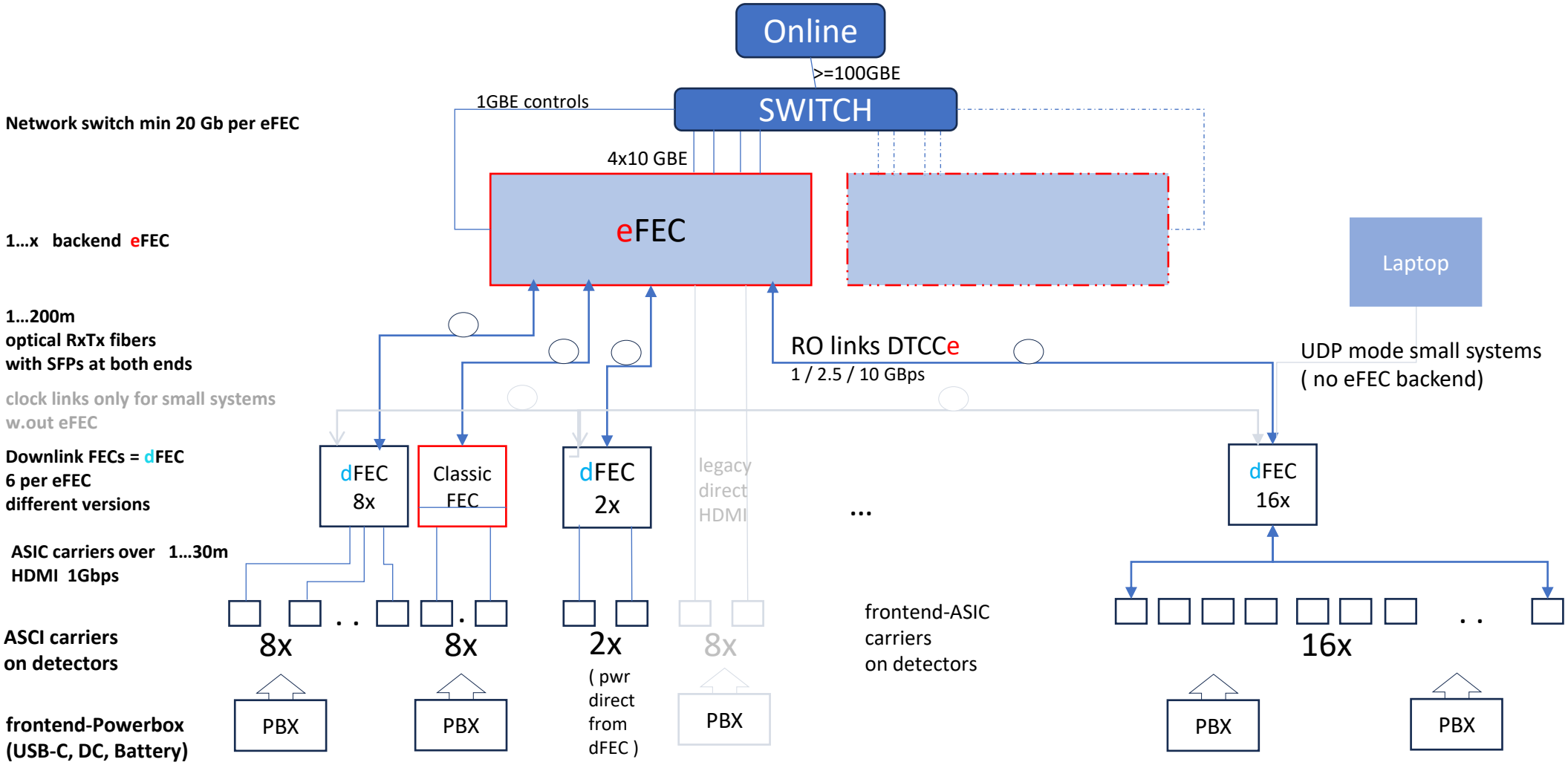


Crate

2 x USB powered eFEC's in Minicrate*

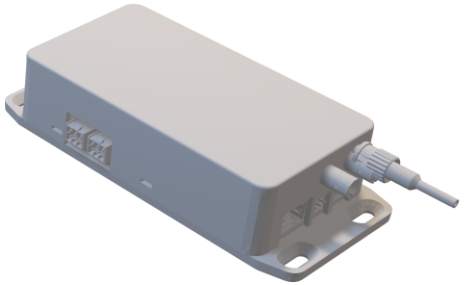
* no more ATX PS and ATX-power adapter required=> cheaper crates

Readout backend with eFECs



New: crateless dFECs

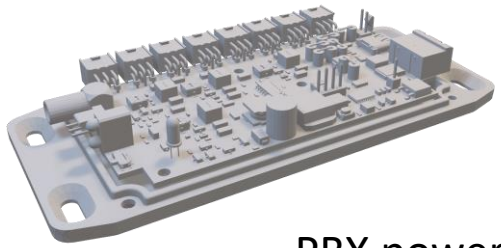
like the classic FEC , can also directly connect to DAQ on Laptop via ethernet



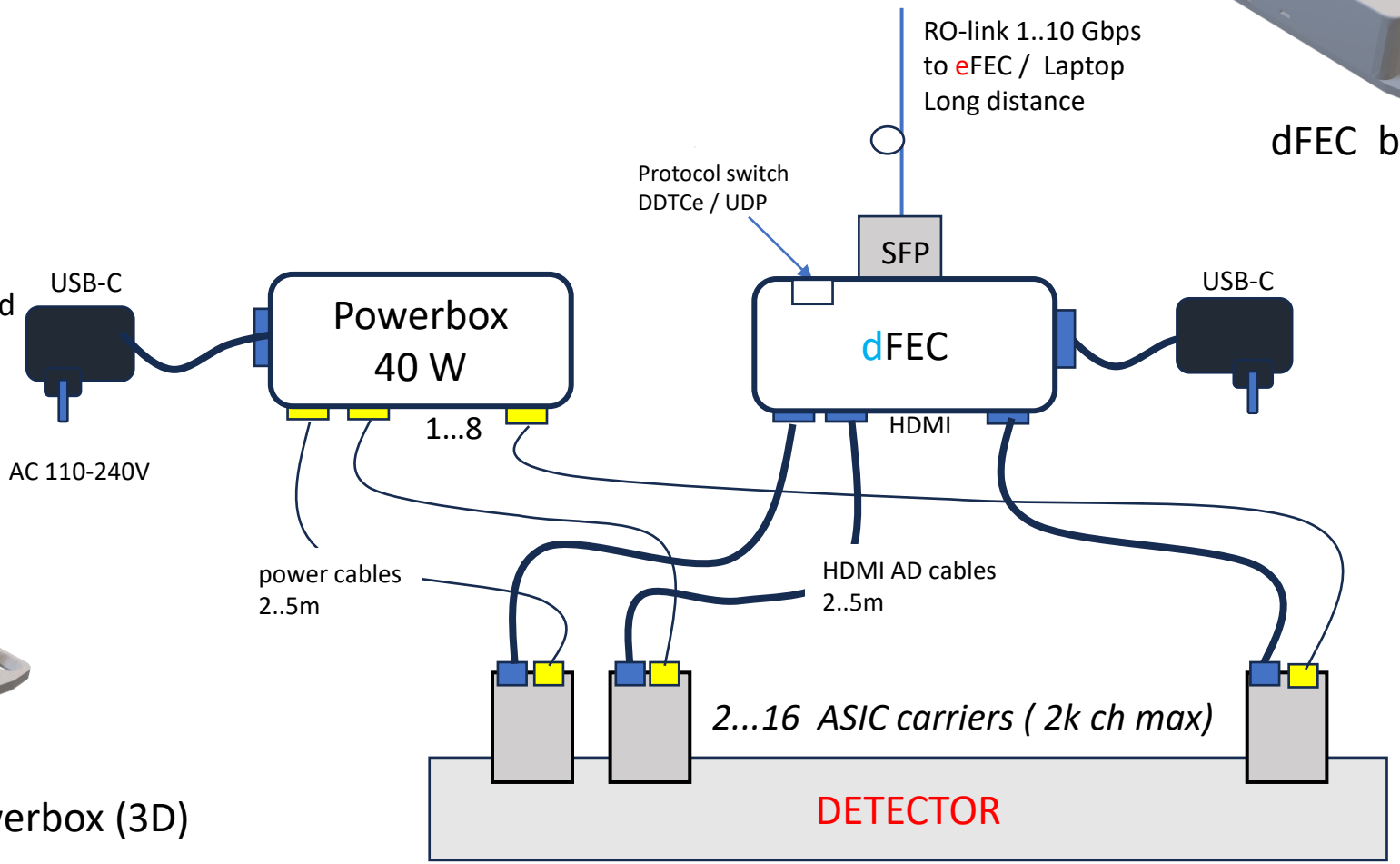
dFEC box (3D)

dFEC's

- portable / hand-sized boxes
- state of art FPGA logic
- 2 ..16 HDMI powered frontend ports
- max. 2k channels/ dFEC
- USB-C powered
- SFP for RO links copper or fiber
- switch for ethernet/DTCCe to backend
- ST optical clock link (plugin option)



PBX powerbox (3D)



FPGA resources eFEC

XCZU7CG (eFEC proto)

1728 DSP slices
=> Accumulator, Multiplier, XOR etc for very fast HW trigger logic

312 Block RAMs 36bit x 1k
configurable and cascadeable

=> 312 latency buffers (LB) for hit data

24 x GHT (16.3 Gb) transcievers
wordsize 16, 32, 64 bit

=> 6 x SFP input links 2.5/5/10 (from dFECs)
=> 4 x SFP link output 10GB to Online
=> 1 x SFP link output 10 GB (vertical archit.)

PHY block for DDR3 and DDR4 memory
=> plugin option for running Linux in RT core

4x 1GB MAC
=> 1 x SFP link output for 1GBE Controls link

proto final ?

Zynq UltraScale+ MPSoC: CG Device Feature Summary

Table 13: **Zynq UltraScale+ MPSoC: CG Device Feature Summary**

	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Application Processing Unit	Dual-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache						
Real-Time Processing Unit	Dual-core Arm Cortex-R5F with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM						
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC						
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters						
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII						
System Logic Cells	103,320	154,350	192,150	256,200	469,446	504,000	599,550
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080
Distributed RAM (Mb)						6.2	8.8
Block RAM Blocks						312	912
Block RAM (Mb)						11.0	32.1
UltraRAM Blocks						96	0
UltraRAM (Mb)						27.0	0
DSP Slices						1,728	2,520
CMTs						8	4
Max. HP I/O(1)						416	208
Max. HD I/O(2)						48	120
System Monitor						2	2
GTH Transceiver 16.3Gb/s(3)						24	24
GTY Transceivers 32.75Gb/s						0	0
Transceiver Fractional PLLs						12	12
PCIE4 (PCIe Gen3 x16)						2	0
150G Interlaken	0	0	0	0	0	0	0
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0

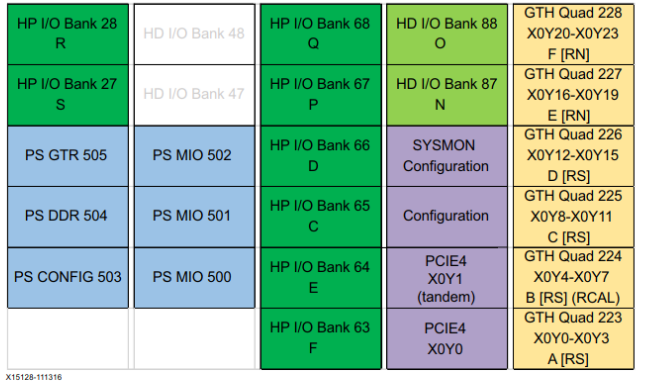
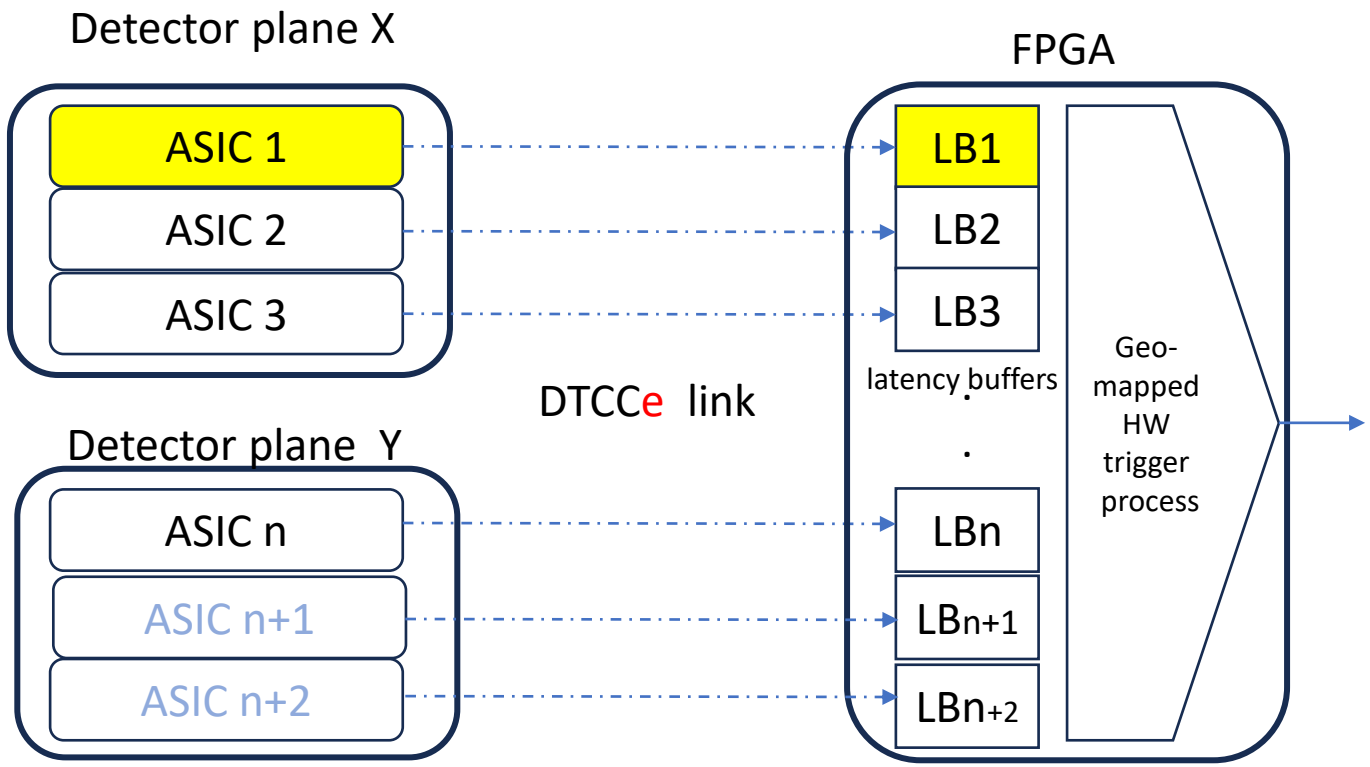


Figure 1-12: **XCZU7 Banks in FFVF1517 Package**

realtime triggers in eFEC

based on geometrically mapped, FPGA-embedded latency buffers (LBs)

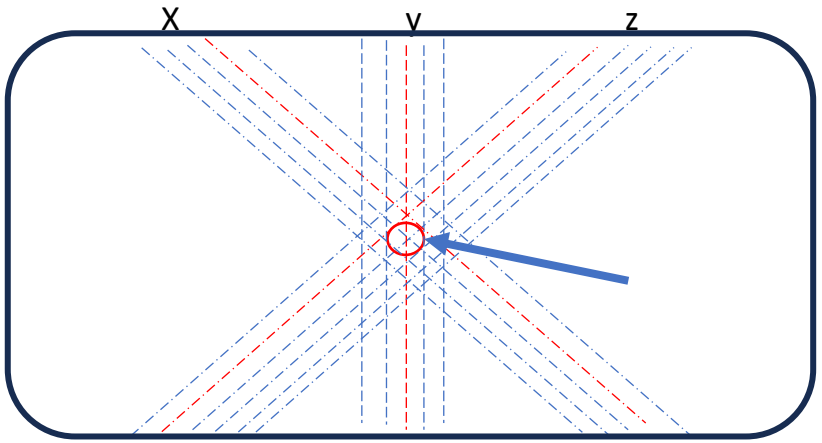
max 312 BRAMs = LB available in FPGA. 1 LB per ASIC, LB's indexed by L and ASIC Nr:
L = SPF in-link of eFEC Nr 1..6
Ax = ASIC Nr of link L, 1.32 transmitted from dFEC via new DTCCe link protocol.



Latency of single LB = 1024/(HitRate*Occupancy)
Example: 8MHz VMM3a hitrate @ 10% occupancy
(1024/8MHz)*0.1 = 12.8 us
Concatenate LBs for higher latency

312 LBs in Zu7GU (eFEC Proto)
912 LBs in Zu9GU

HW trigger example 1: remove hit redundancies



For 3 rotated detector planes, the channel indices x,y,z define a spacepoint as: $x + y + z =$ **const** $+/- \Delta$

eFEC HW point finder : combinatorial search for const with decreasing Δ

Example: 4 x 4 x 4 ASIC areas in 3 planes of 512 ch each.

Run XOR (DSP) for index comparison with "const +/- Δ "

Hit occupancy assume 20% , CR clock for DSP cycle ~ 150 MHz)

With $\Delta = 0$, 6.2 equiv. hit ch per ASIC, - 13.000 combinations

With $\Delta = +/-1$ reduced 4 equiv. hit ch ~ 4000 combinations

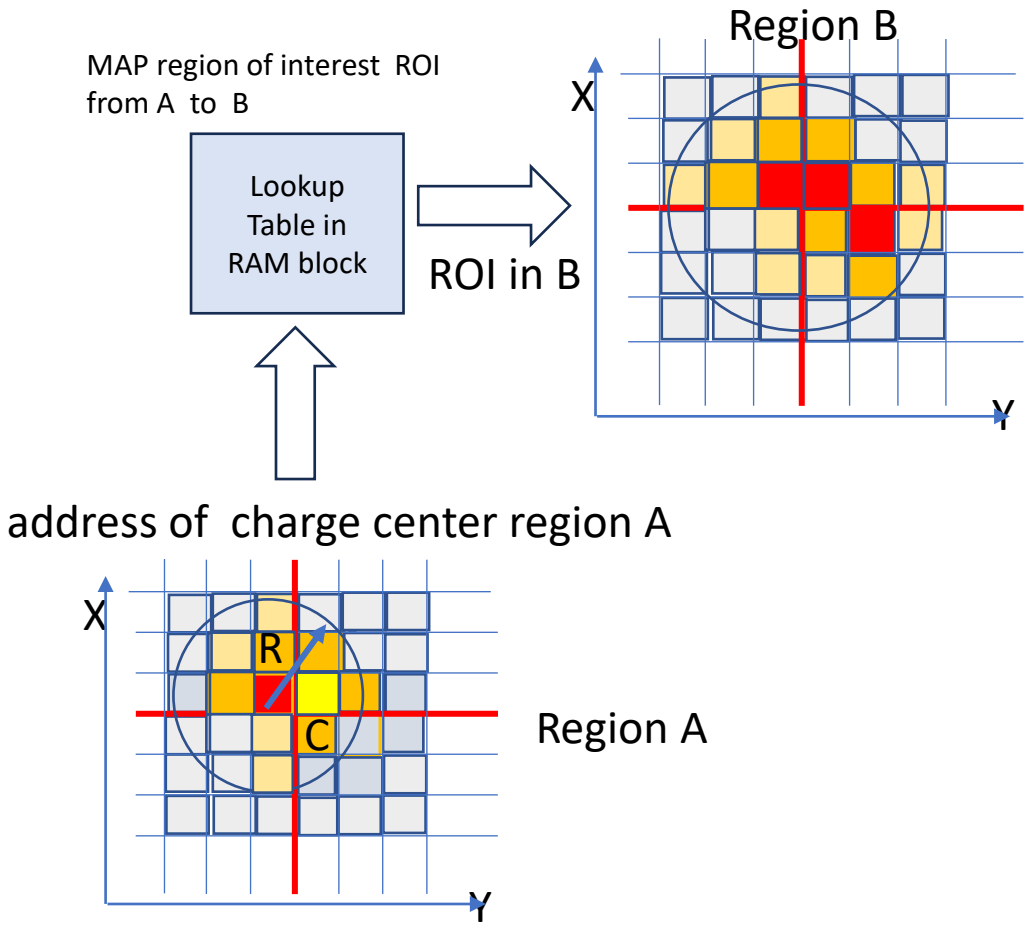
Process latency assume O(50-100us) -> Nr of concatenated LB's

Trigger result:

Clear hit entries without point match from LB output

HW trigger 2: ROI charge mapping

Example: parallel search in 2 detector regions of 2x 2 ASIC channels: combine search in geometrical ROI maps



Process sketch HW trigger with DSP slices

add/substract/compare,accumulate,shift, multiply @150 MHz

Region A search

- search radius around highest hit in region
- process sub-thresh neighbor hits
- add up charge
- Q_{min} = threshold for total charge sum trigger
- center of charge C becomes Lookup address

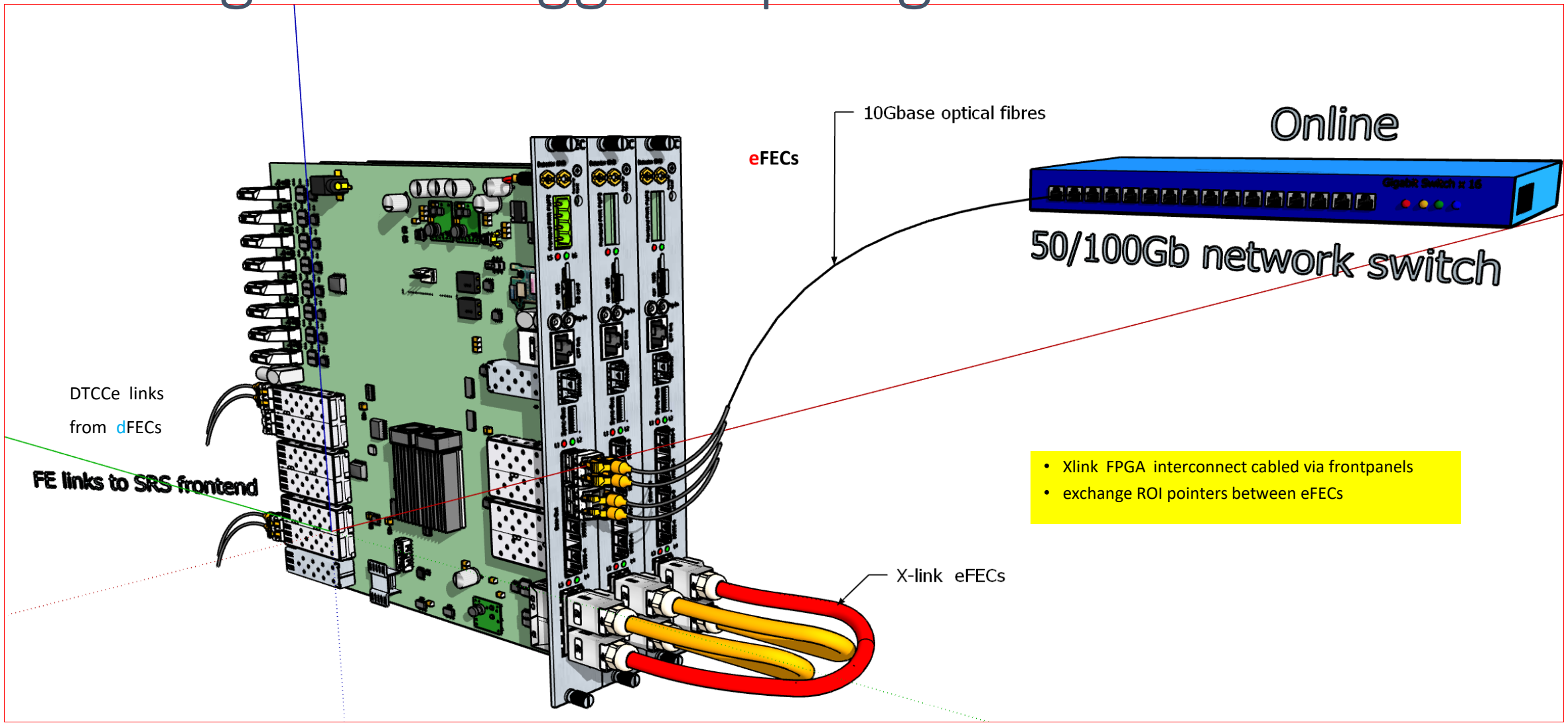
Region B search

- lookup table output defines ROI mask in region B
- search for charge clusters in B
- trigger if track match

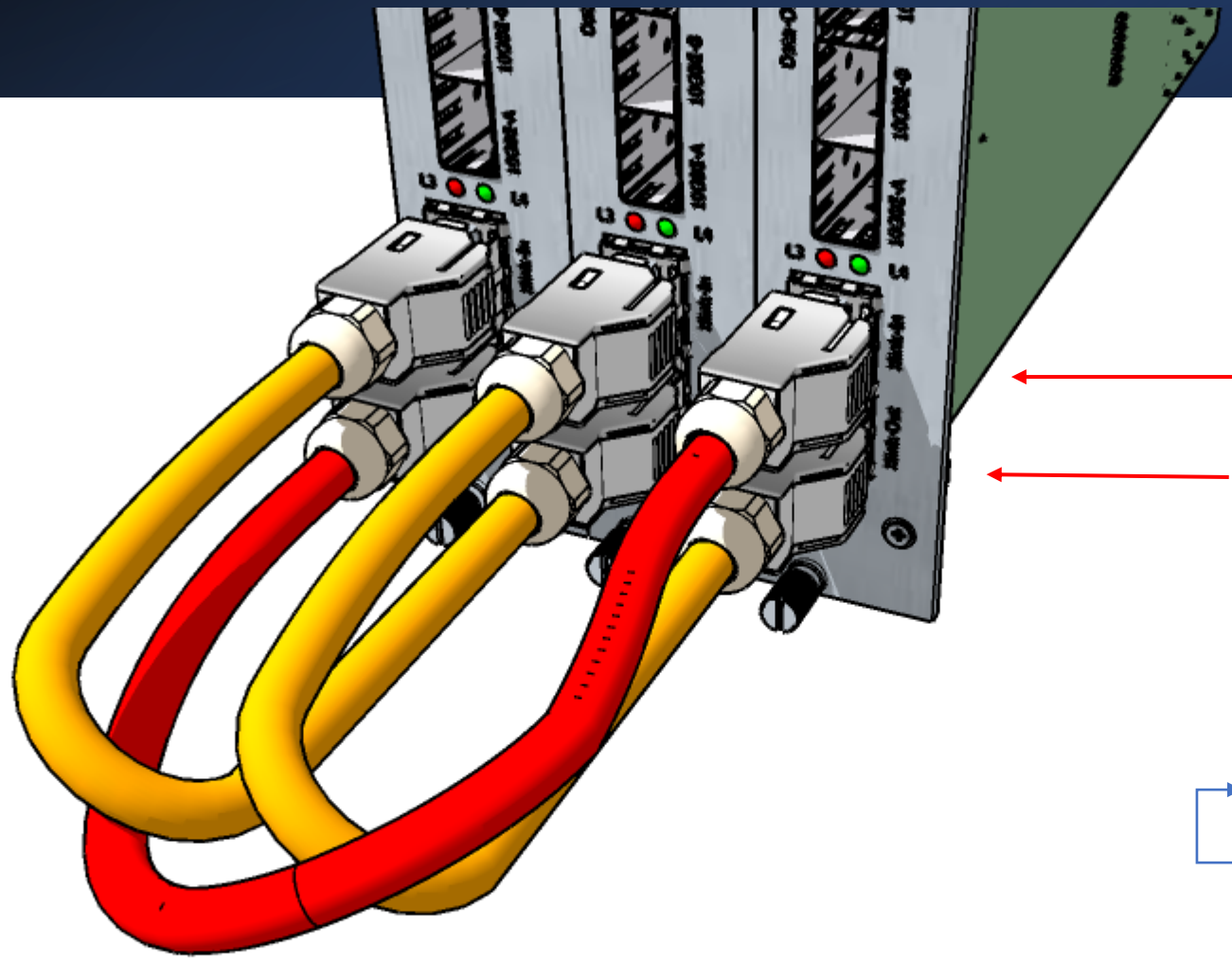
Trigger action

- add tracklet vector to output of LB buffer (user format)

Large area trigger topologies



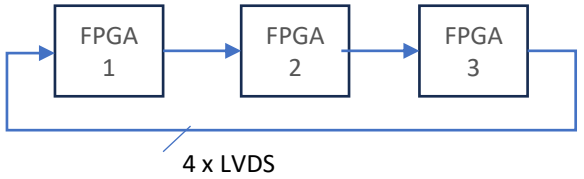
Xlink



Xlink-in

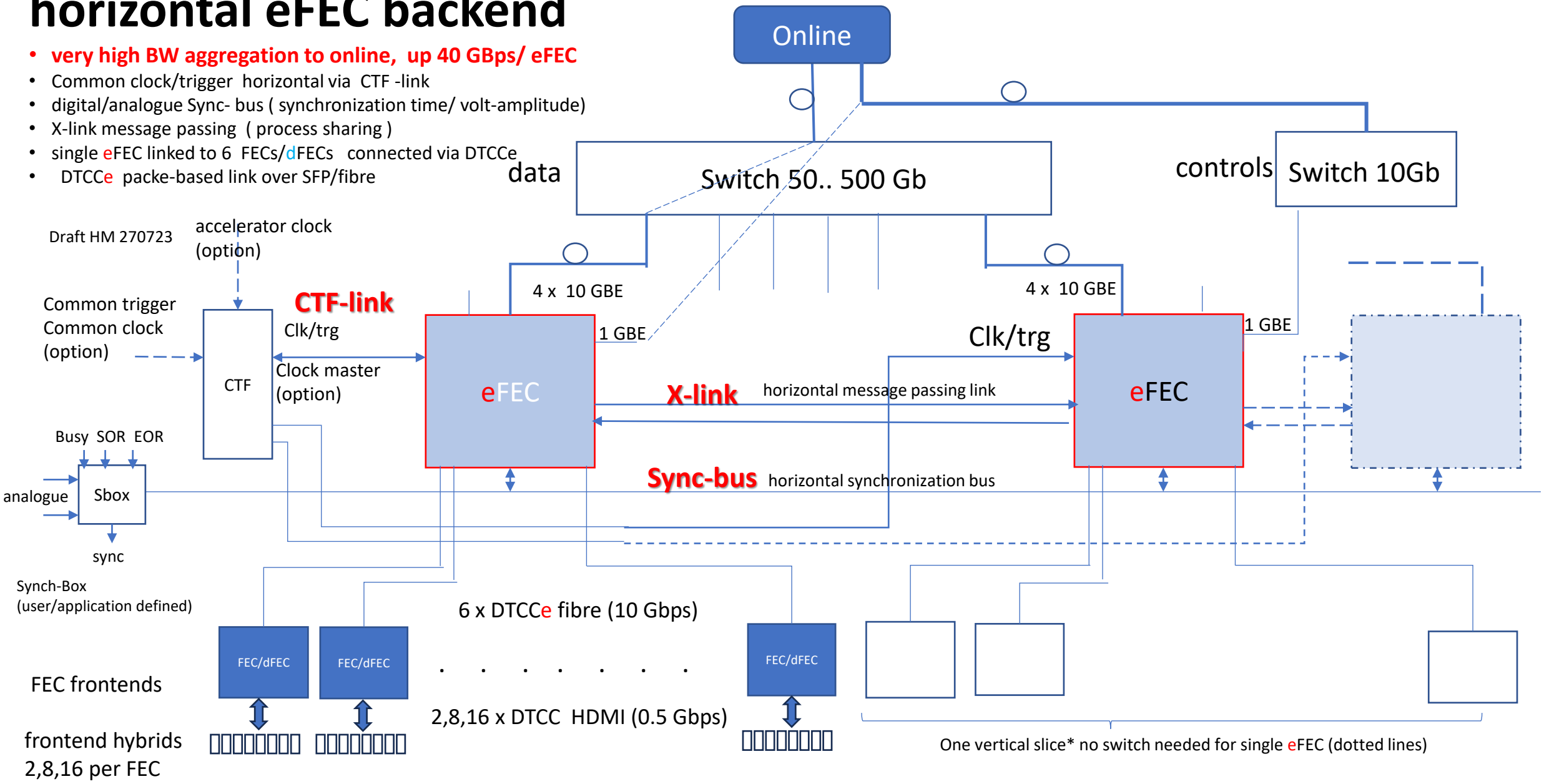
Xlink-out

share ROI's , pointers etc

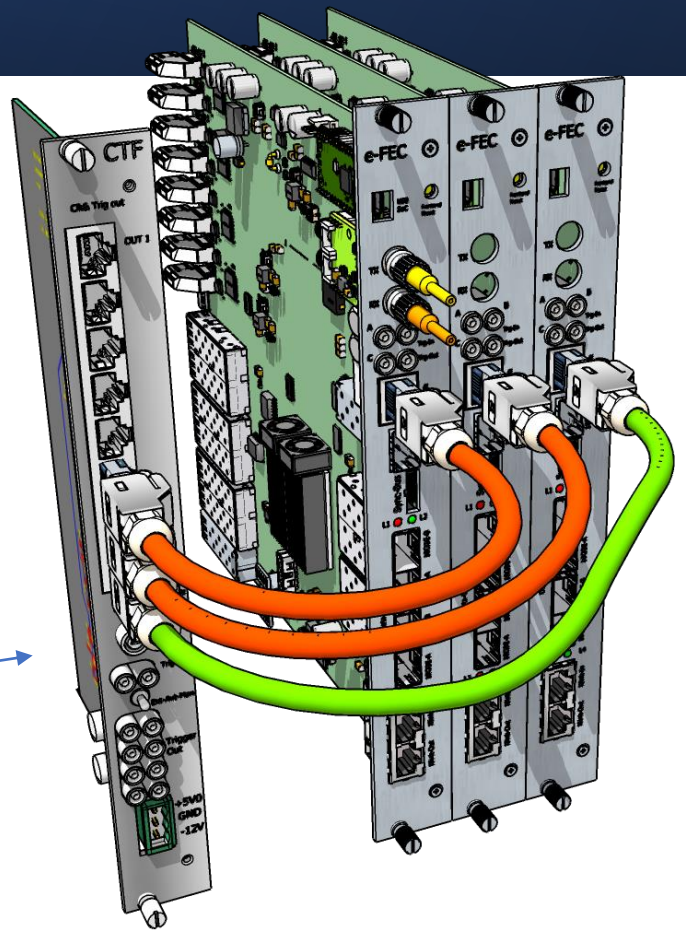


horizontal eFEC backend

- **very high BW aggregation to online, up 40 GBps/ eFEC**
- Common clock/trigger horizontal via CTF -link
- digital/analogue Sync- bus (synchronization time/ volt-amplitude)
- X-link message passing (process sharing)
- single eFEC linked to 6 FECs/dFECs connected via DTCCe
- DTCCe packe-based link over SFP/fibre



CTF-link: system clock from a single source clock and trigger fanout cables to eFECs



Single clock source

CTF+ clock and trigger distributor card

CTF⁺ pinout RG45

CLK-in P 1	TRG-in-P 3	CLK-out-P 5	TRG-out-P 7
CLK-in N 2	TRG_In-N 6	CLK-in-N 4	TRG-out-N 8

RJ45 connector CTF+ link for CAT6 cables

LVDS clock and trigger input and outputs

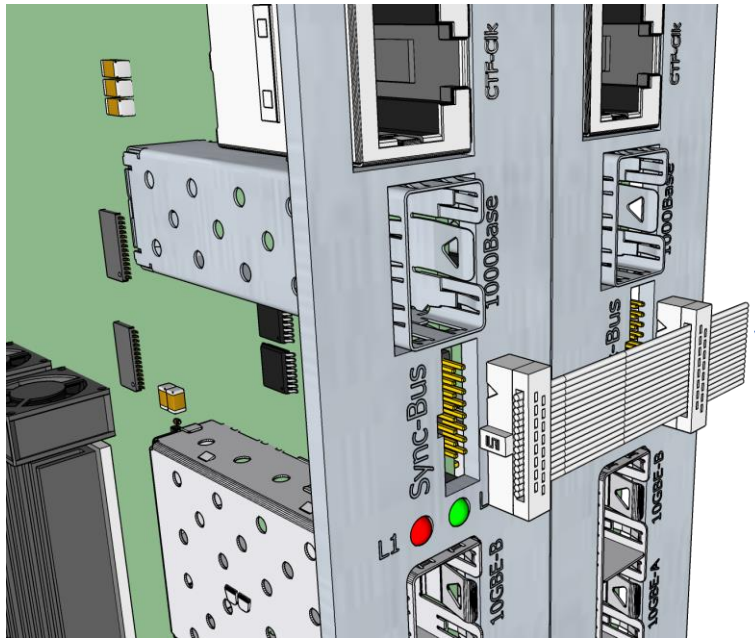
Backwards compatible with CTF (only inputs to eFEC)

New CTF⁺ allows 1 eFEC-generated clock become master clock

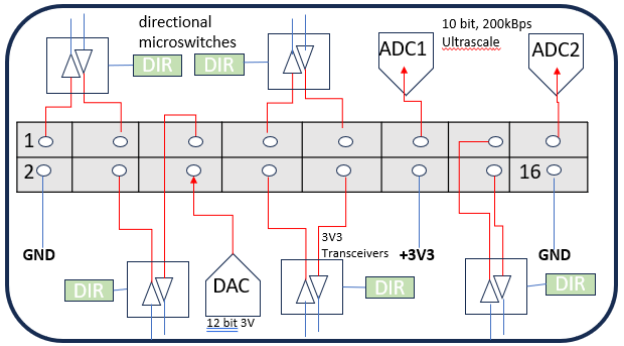
Common clock transmitted via DTCCe links to dFECs

Sync-Bus interface digital/analog for external signals

eFEC



FFSD 16- way IDC flat cable

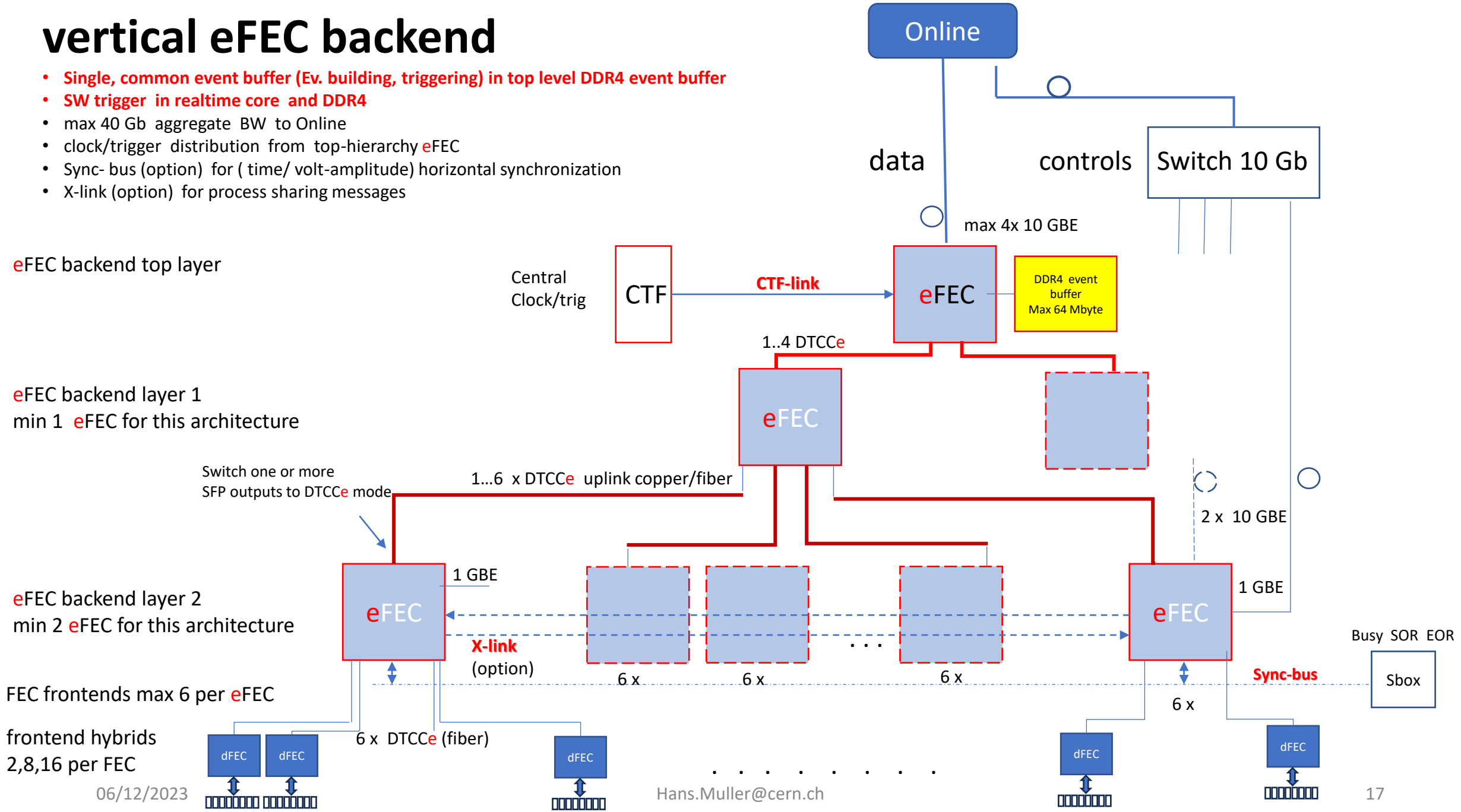


Synch Bus examples:

- common BUSY input
- BUSY output to common inputs
- B-field tracking via analogue ADC input
- HV ramping via analogue DAQ output

vertical eFEC backend

- **Single, common event buffer (Ev. building, triggering) in top level DDR4 event buffer**
- **SW trigger in realtime core and DDR4**
- max 40 Gb aggregate BW to Online
- clock/trigger distribution from top-hierarchy eFEC
- Sync- bus (option) for (time/ volt-amplitude) horizontal synchronization
- X-link (option) for process sharing messages



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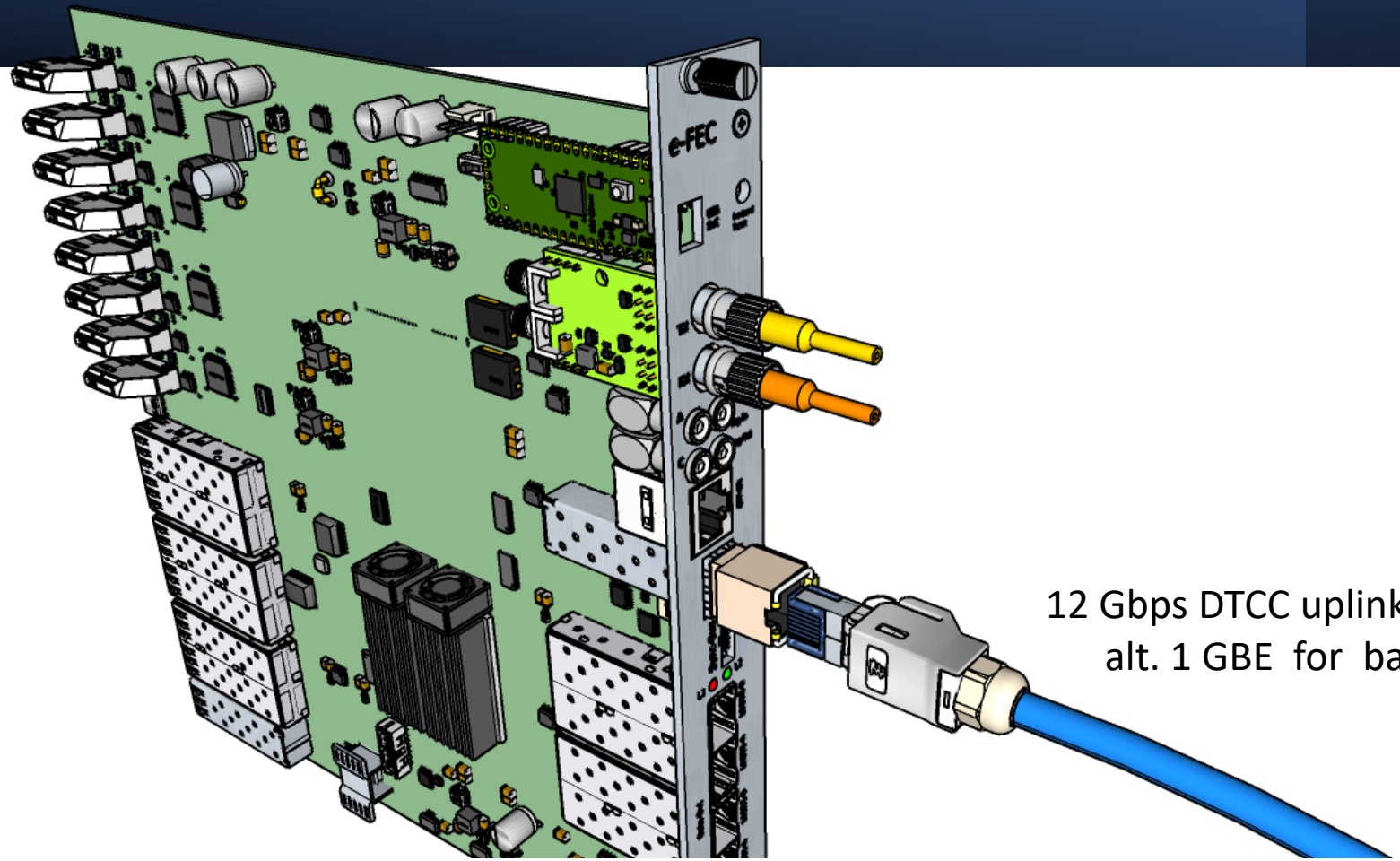
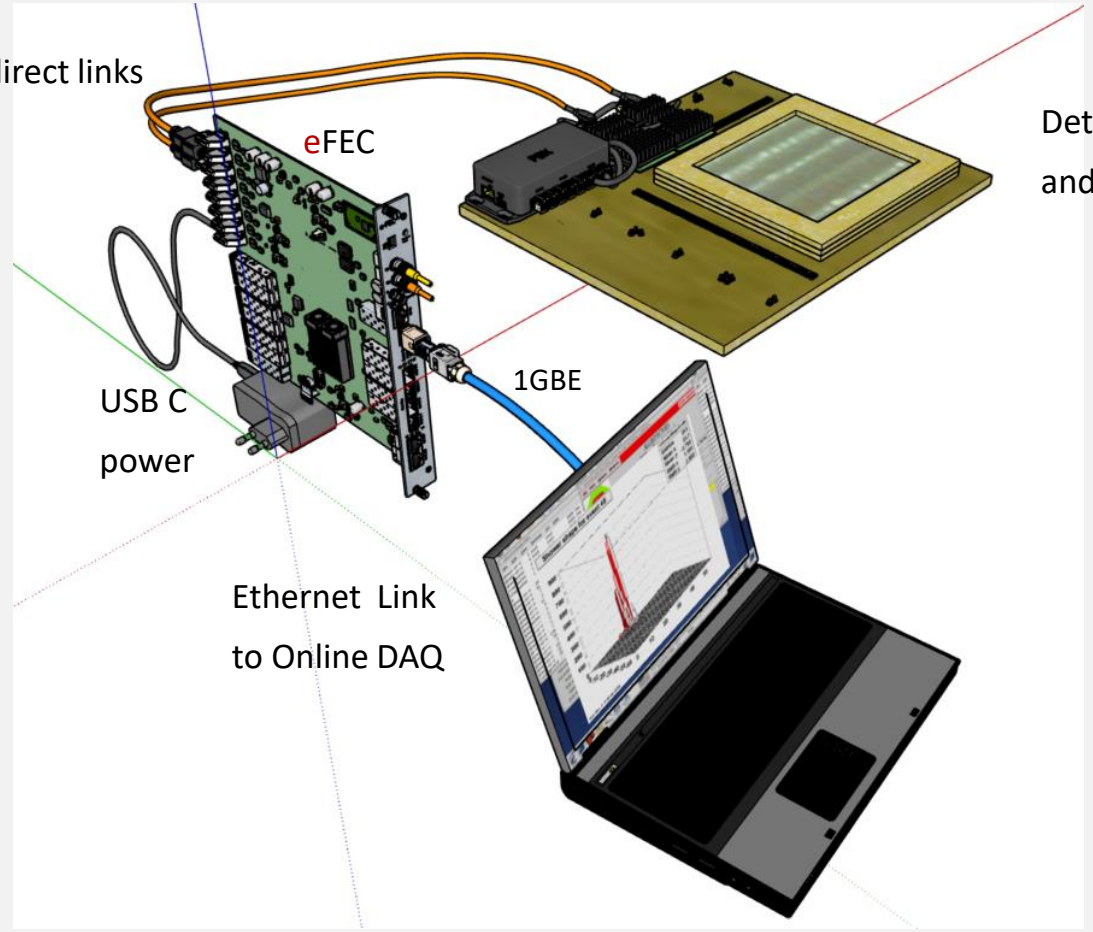
DTCCe Uplink vertical architecture



12 Gbps DTCC uplink for vertical backend architectures
alt. 1 GBE for backend-less DAQ

legacy HMDI ports for VMM3a frontends

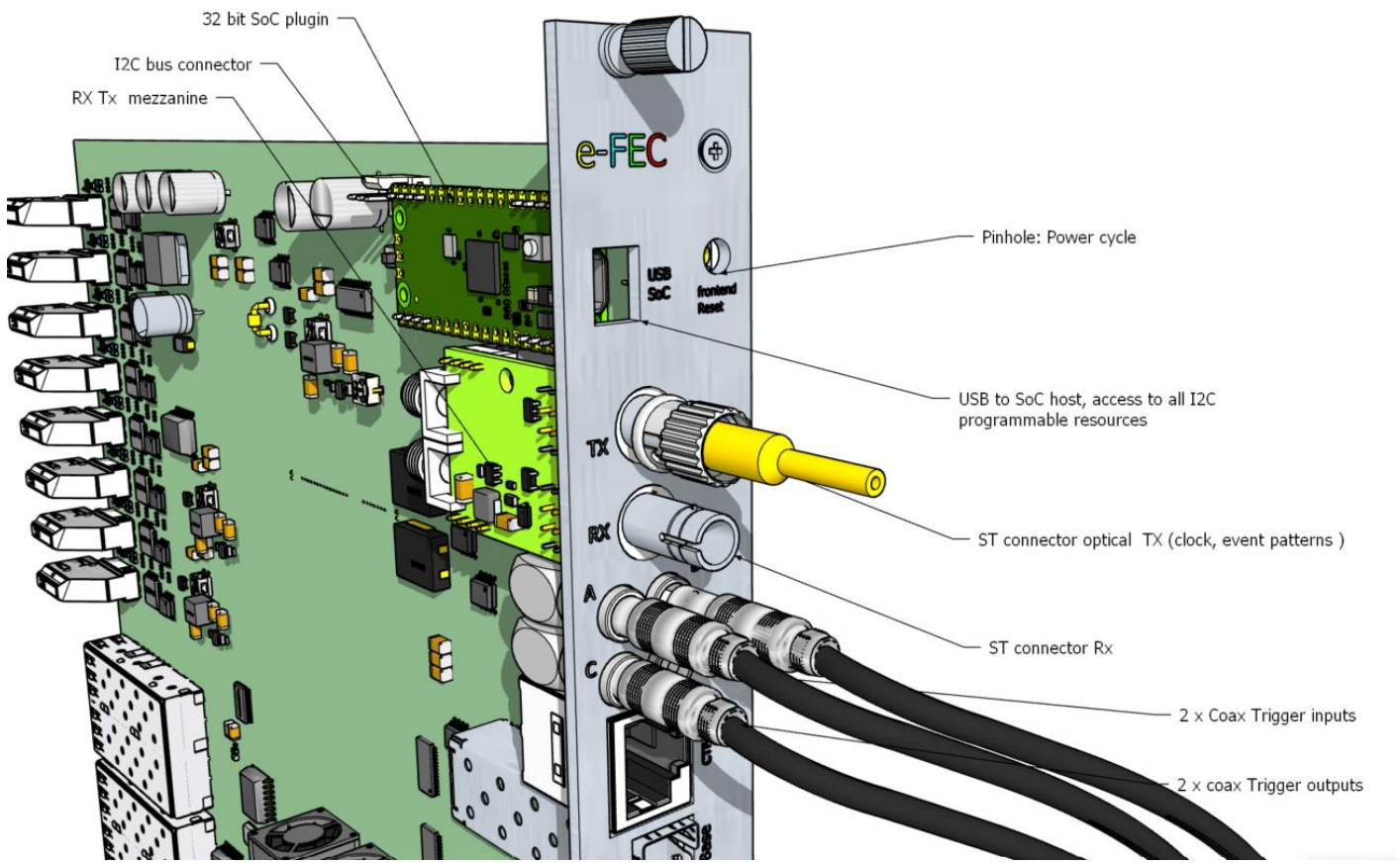


Detector with VMM hybrids
and powerbox

Example of a small, crateless
SRS readout system, short HDMI link and power
implemented with an eFEC

Alternatively, a 1k ch frontend can be powered
from a powerbox and VMM hybrids connected
via HDMI cables up to 20m.

eFEC utility plugins



<u>2 plugin cards accessible via frontpanel:</u>

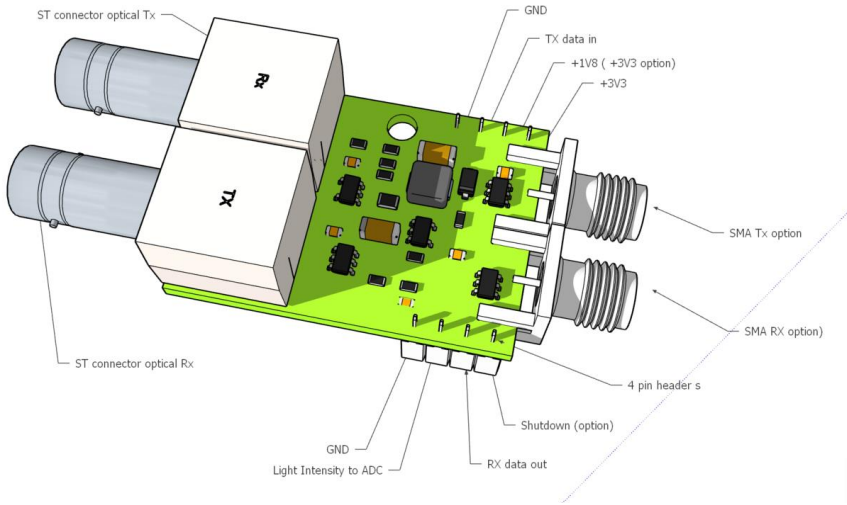
- 32 bit SoC (Raspberry Pi Pico) frontpanel access to USB debug and monitoring port

- optical RxTx tmezzanine 50 Mbaud for clock or patterns

RX-TX plugin mezzanine

- copper-to optical RxTx transceiver mezzanine for long-distance clock receiver/transmitters with ST connectors for up to 50 Mbaud.

- Tx : 820nm with 50/125 multimode fibers up to 900m.
- 62.5/125 fibers up to 2km.



Raspberry Pi Pico 32 bit SoC plugin for eFEC

RP2040 SoC 32 bit microcontroller

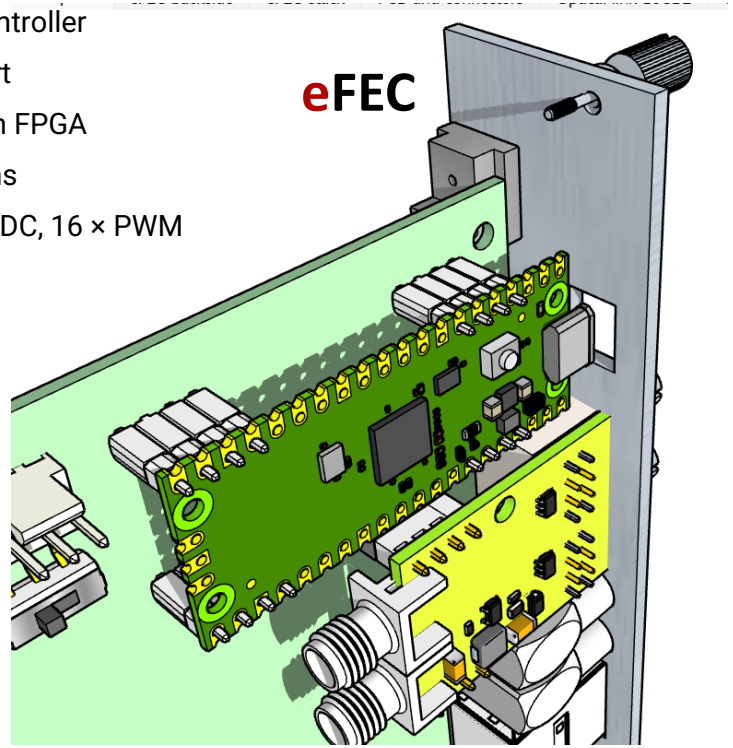
USB 1.1 program/debug port

Terminal port for RT Linux in FPGA

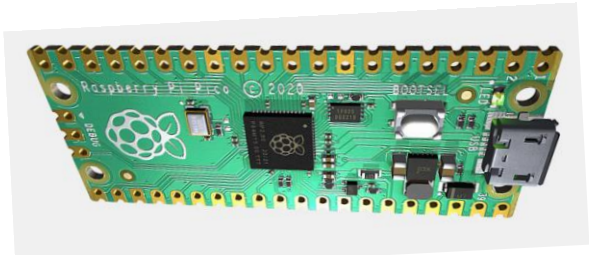
26 × multi-function GPIO pins

2 × SPI, 2 × I2C, 3 × 12-bit ADC, 16 × PWM

Temperature sensor

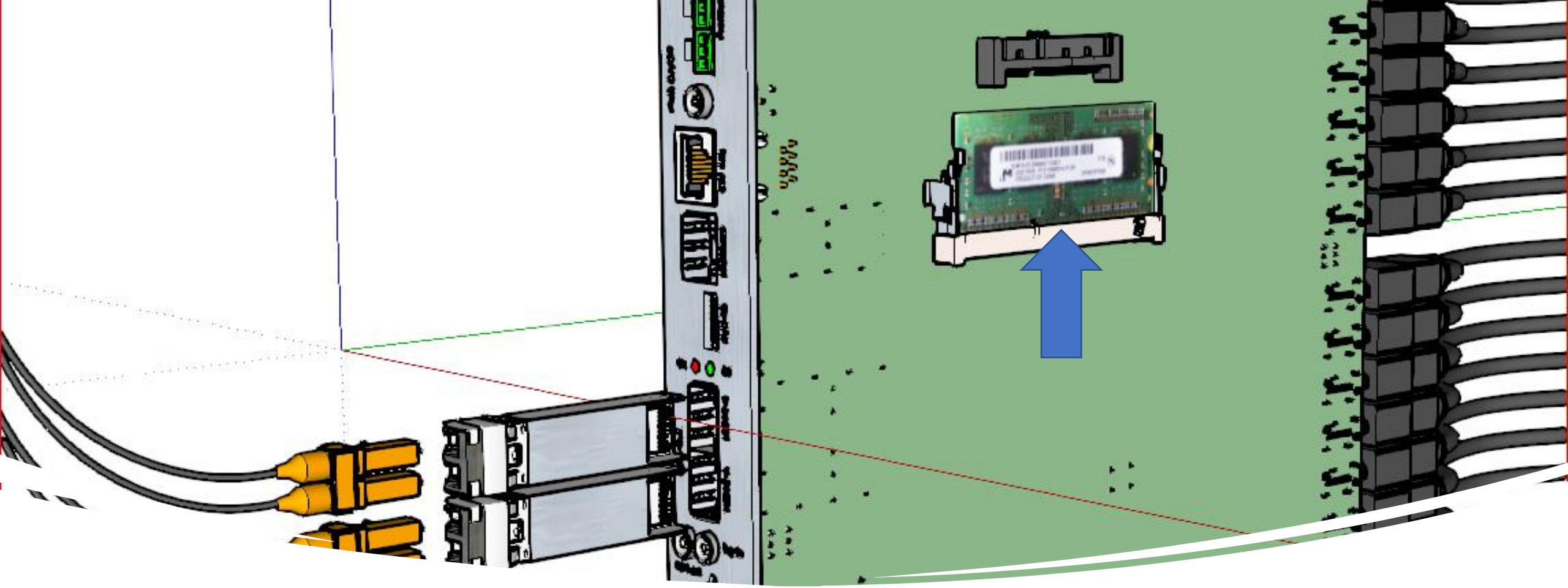


Connected to all I2C bus and Voltage resources of the eFEC



Example: uPython development on RP :

Chip resources programming via I2C bus



eFEC backside

- Plugin DDR4 memory up 64 MB
  for RT Linux option on dual ARM FPGA core

Small detector readout with dFECs

dFEC with 2 HDM links

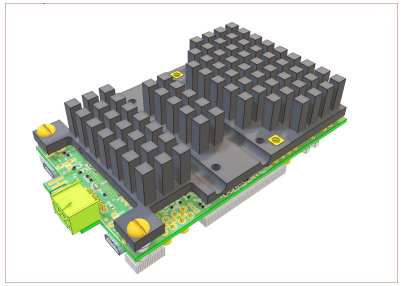
RO link:
copper/fiber SFP
to Laptop

ST optical link
option for clock
sharing

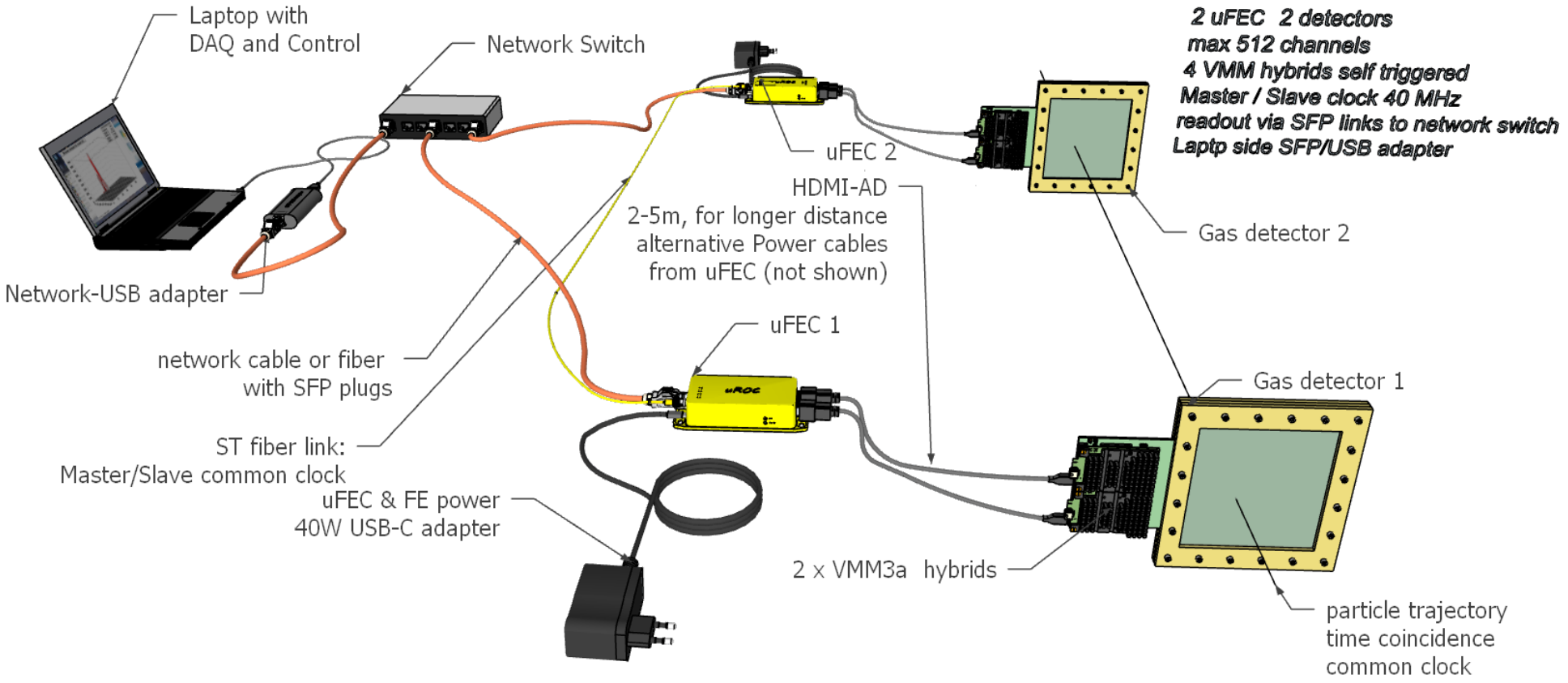
USB-C power (incl. VMMs)

Power via HDMI

Plugged ASIC carriers



Readout systems without eFEC backend
dFECs direct DAQ via ethernet & clock ring



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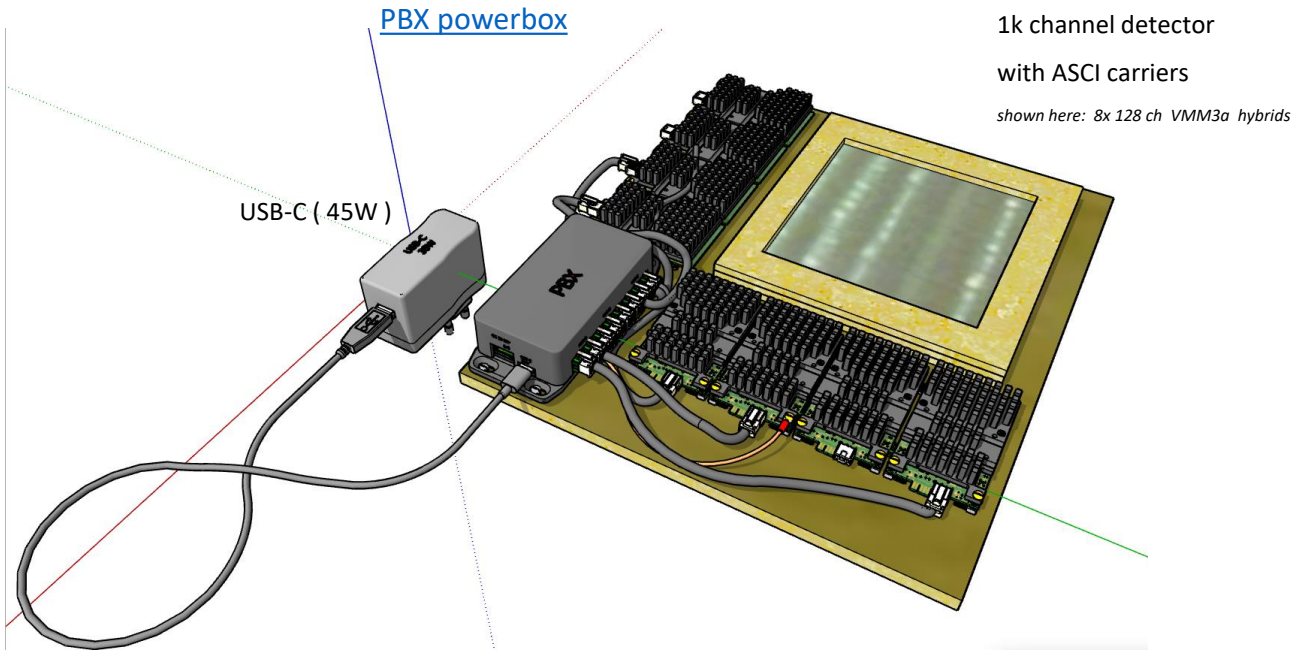
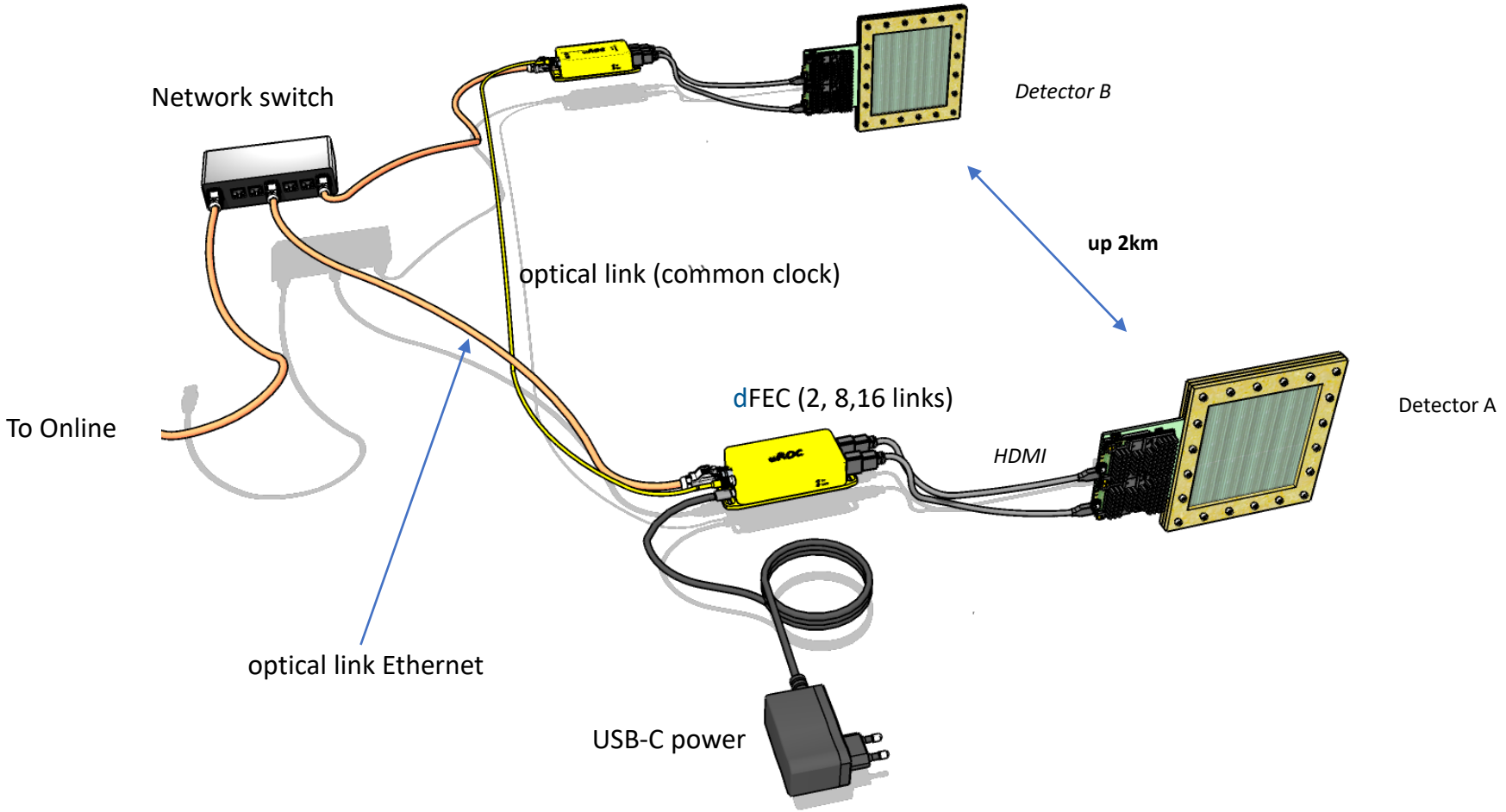
Frontend power

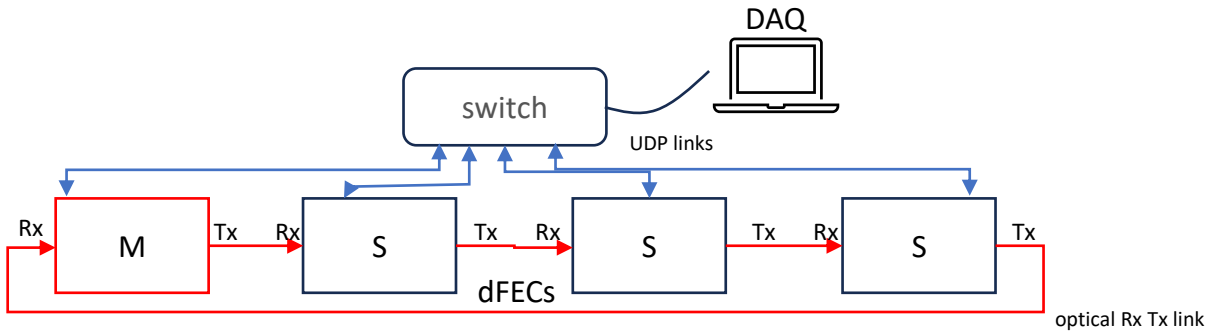


Distributed detectors



Common clock for dFECs w.out backend

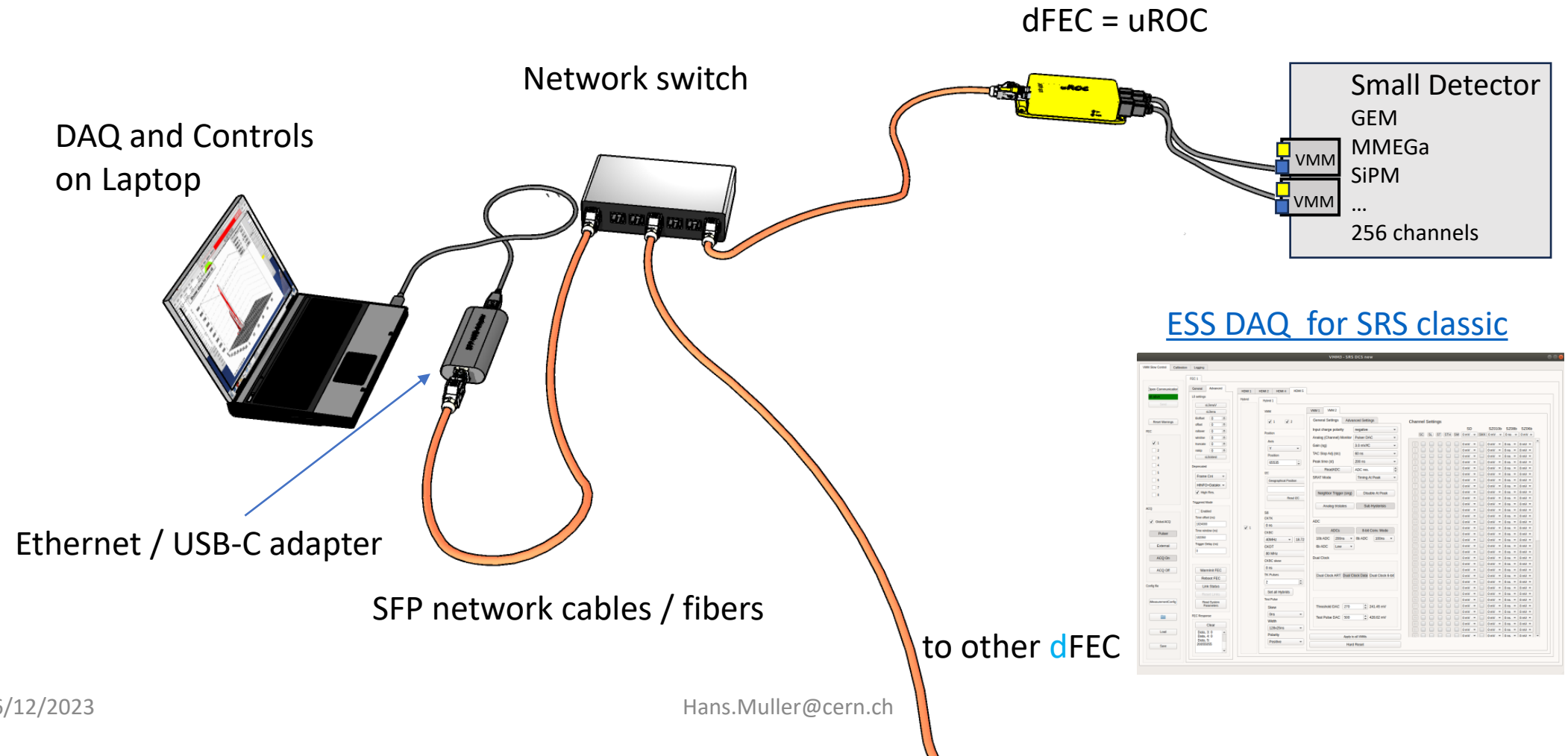
dFECs can be equipped with a Rx / Tx mezzanine with ST fiber connectors for multimode fibers transmitting at 820 nm and up to 2km. This allows connecting dFECs in a clock ring, allowing to determine the phase shift relative each other



Common clock for small systems w.out backend

Small system DAQ on Laptop

dFEC FW will be adapted to work with same ESS- DAQ as classic FEC



[ESS DAQ for SRS classic]

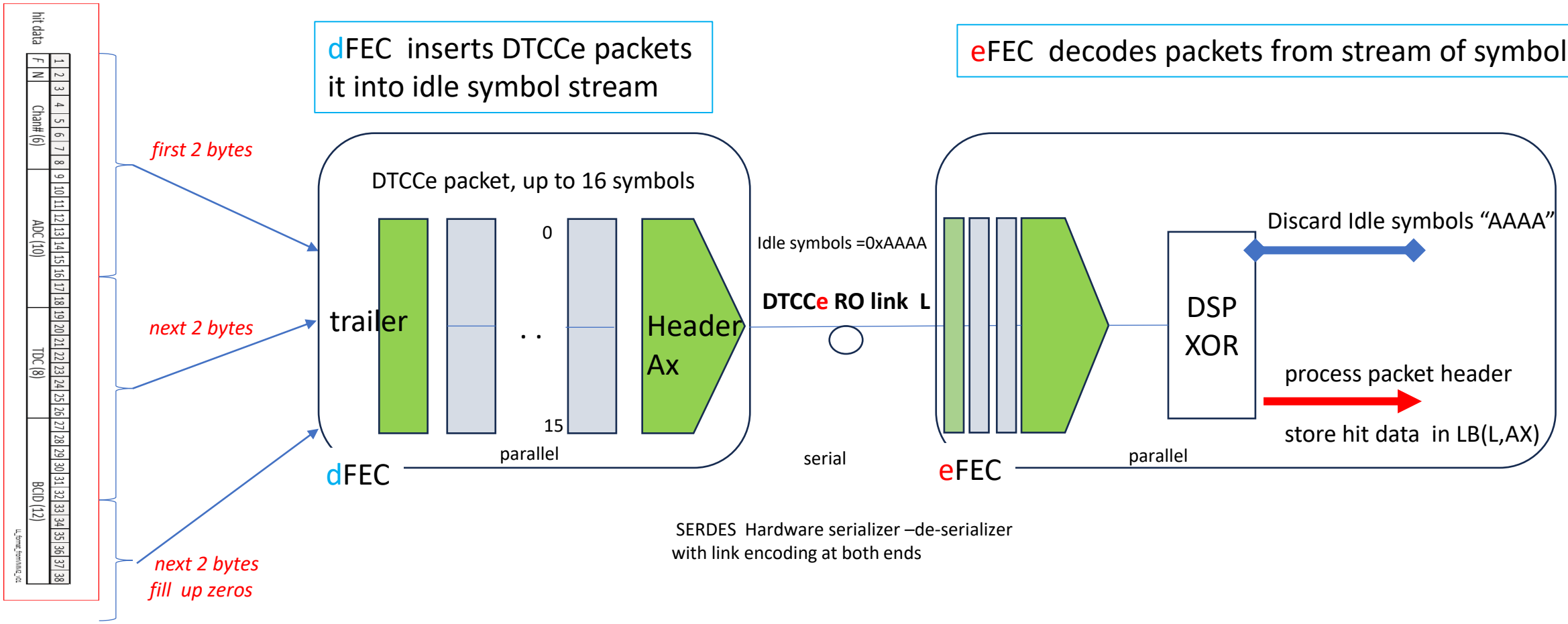
New DTCCe protocol

*DTCC =Data Trigger Clock Control

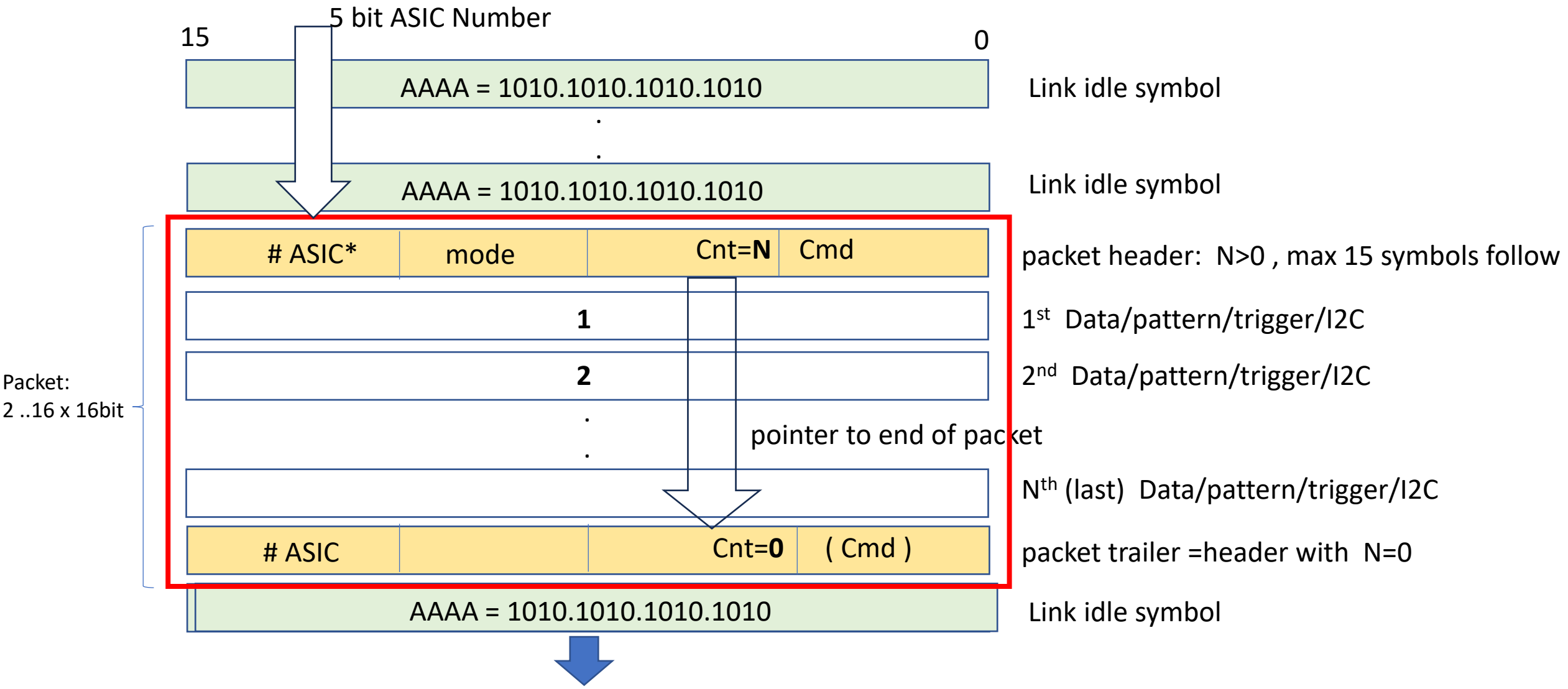
A. packet-based RO –link protocol over serial SFP links eFEC <-> dFEC
B. ASIC index and data type identifier included in packet headers
C. Optional safe mode with roundtrip packet Ack and Retry
D. Optical SFP+ up 12.5 Gbps and up 20km
E. Common clock transmitted over DTCCe from eFEC to all dFECs
F. Bi-di command messages including error codes
G. ASICs can transmit self-triggered hits to eFEC
H. Remote I2C write over DTCCe to I2C resources on dFEC (or ASIC carrier)
I. Remote I2C read (buffered) from frontend I2C /SPI resources

DTCCe packets: 16 bit symbols

hit data from ASIC



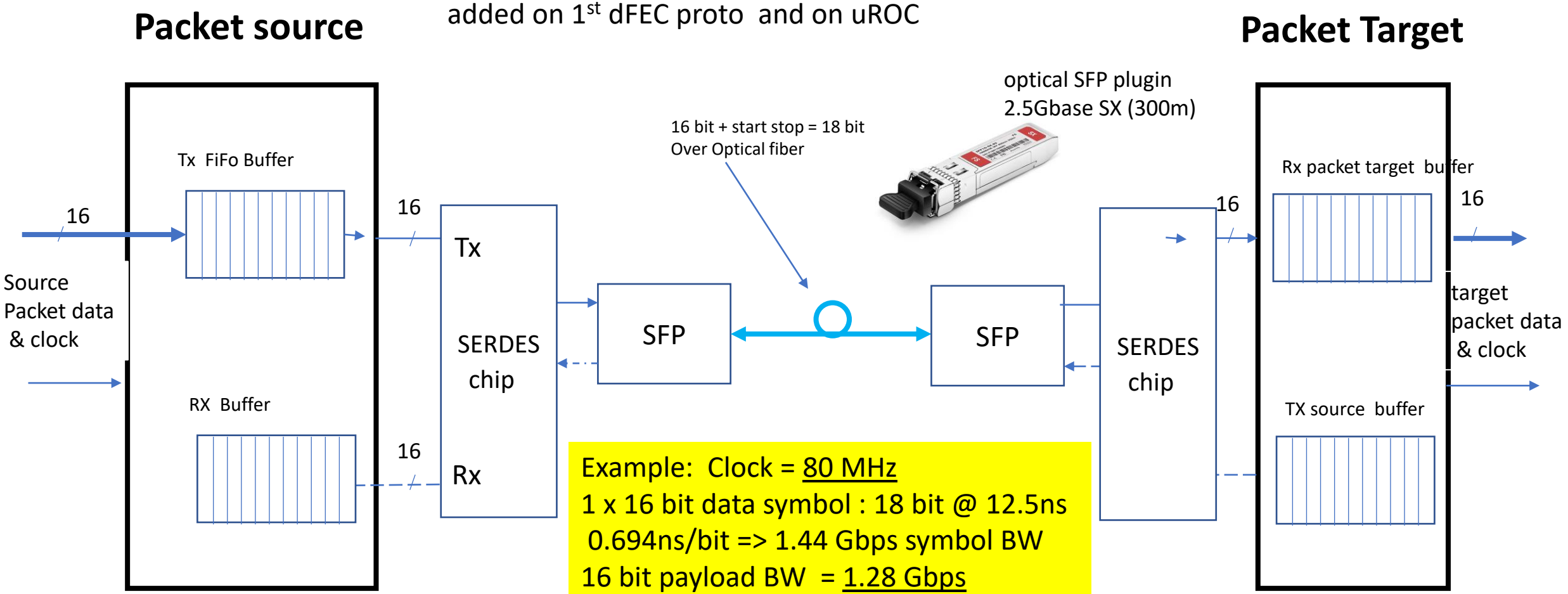
DTCCe link packets format (draft)



* max 32 ASICs

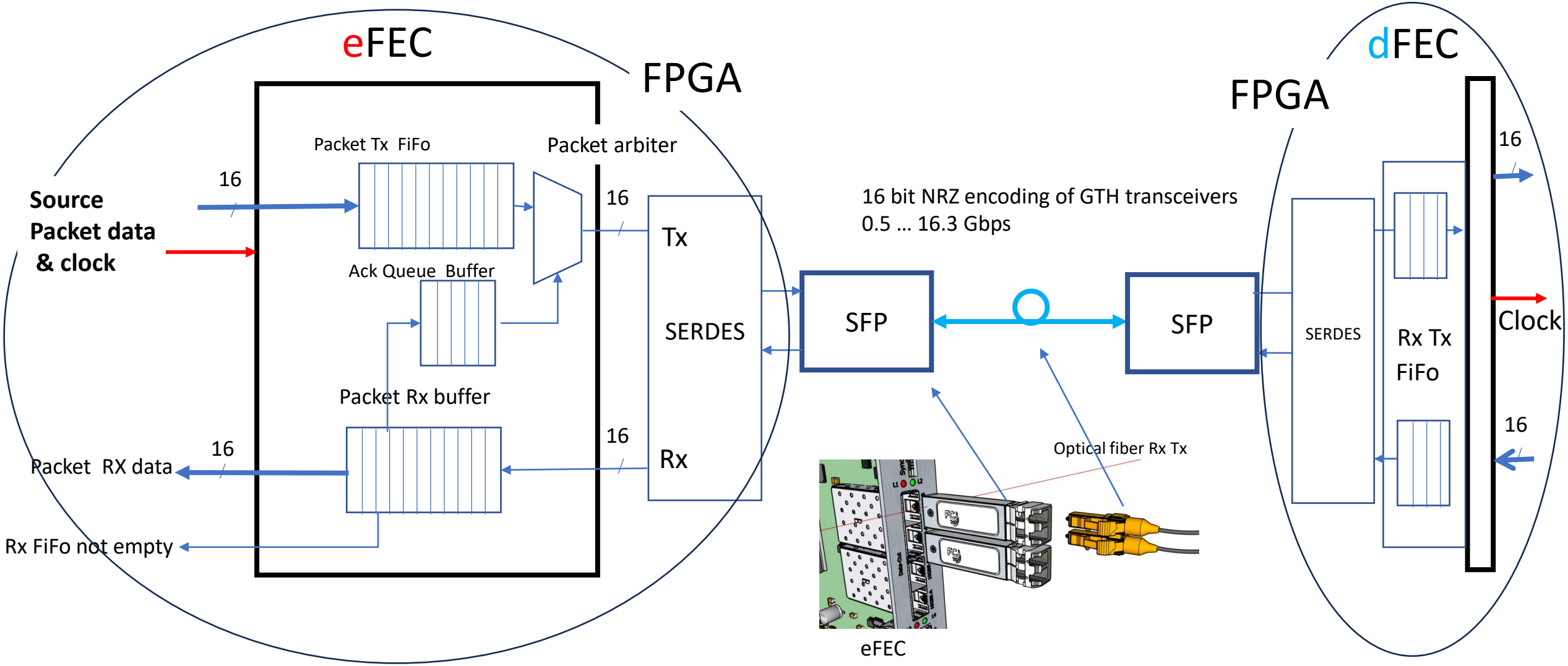
packet Serializer/Deserializer

initial DTCCe development with 1.4 Gbps Serdes chip
added on 1st dFEC proto and on uROC

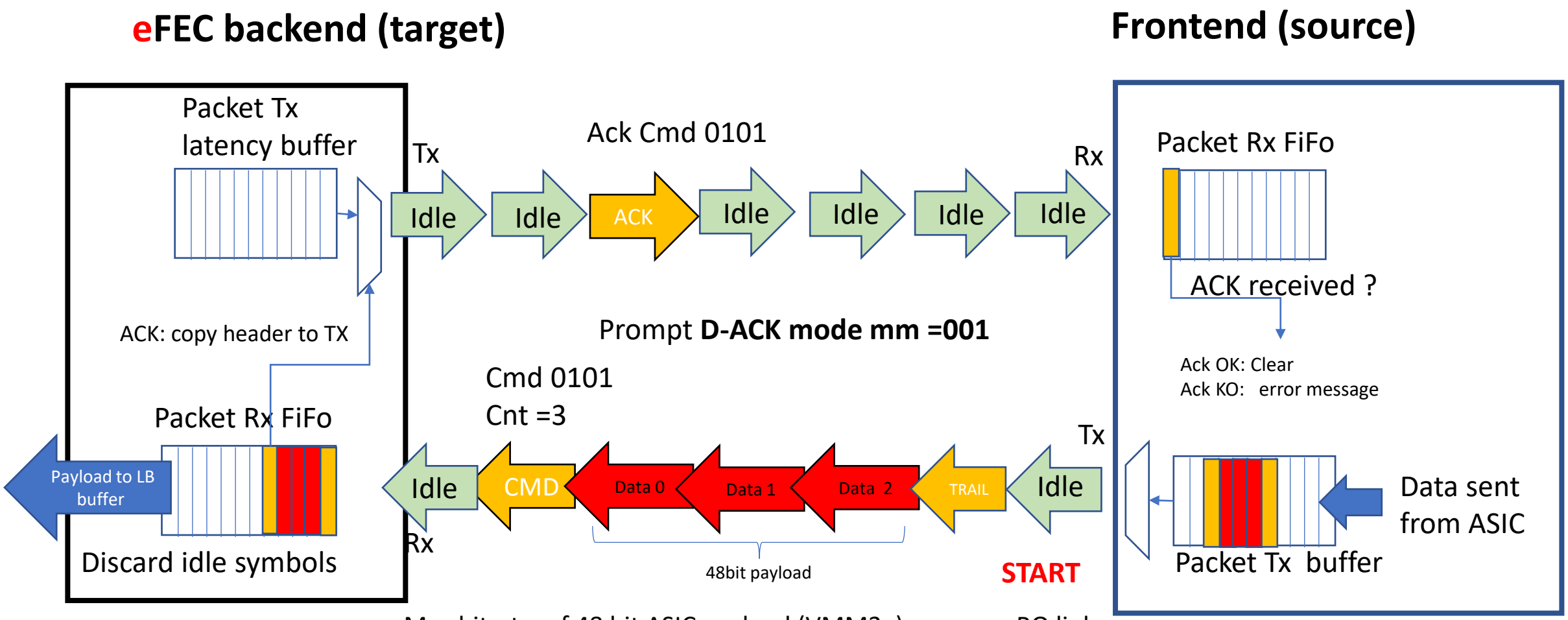


Example: Clock = 80 MHz
1 x 16 bit data symbol : 18 bit @ 12.5ns
0.694ns/bit => 1.44 Gbps symbol BW
16 bit payload BW = 1.28 Gbps

High-BW DTCCe implementation: FPGA



Triggerless 48 bit frontend ASIC hit data



Max hitrate of 48 bit ASIC payload (VMM3a) over one RO link
1.4 Gbps=> ~ 17.5 MHz, 10 Gbps => ~ 125 MHz

SRSe project tasks (-> DRD1 teams)

HARDWARE

eFEC prototypes

- design concept finalized as pre-schematics
- component purchase 2 protos 90% finalized
- commercial PCB routing planned 2nd Q 24
- PCB production & assembly planned 3rd Q24
- 2 prototypes planned 3rd Q 24

eFEC production

- revisions final production files
- Commissioning with frontend in testbeam
- tbd.

Powerbox PBX

- ready for immediate commercial production

dFEC prototypes

- uROC (2 hybrids incl. power) proto 1Q 24
- maxiROC (8/16 hybrids , needs PBX) proto 2Q 24

VMM3a hybrids

- V 5 in production, 600 expected 3Q 24

New ASIC-x hybrids (VMM4, Salsa, …)

- tbd

FIRMWARE / SOFTWARE

DTCCe link protocol (eFEC⇔ dFEC)

- Vacancy !

udp readout link (dFEC ⇔ Laptop)

- bootstrap from ESS DAQ

VMM3a hybrid Firmware (Spartan 7)

- ready

eFEC min. Firmware for DAQ compliance

- Vacancies (team) !

eFEC 10 GBE MAC integration

- Vacanciy !

eFEC SoC diagnostics (C-lang, uPython)

- Vacancy !

eFEC Realtime Core Linux / DDR4

- Vacancy !

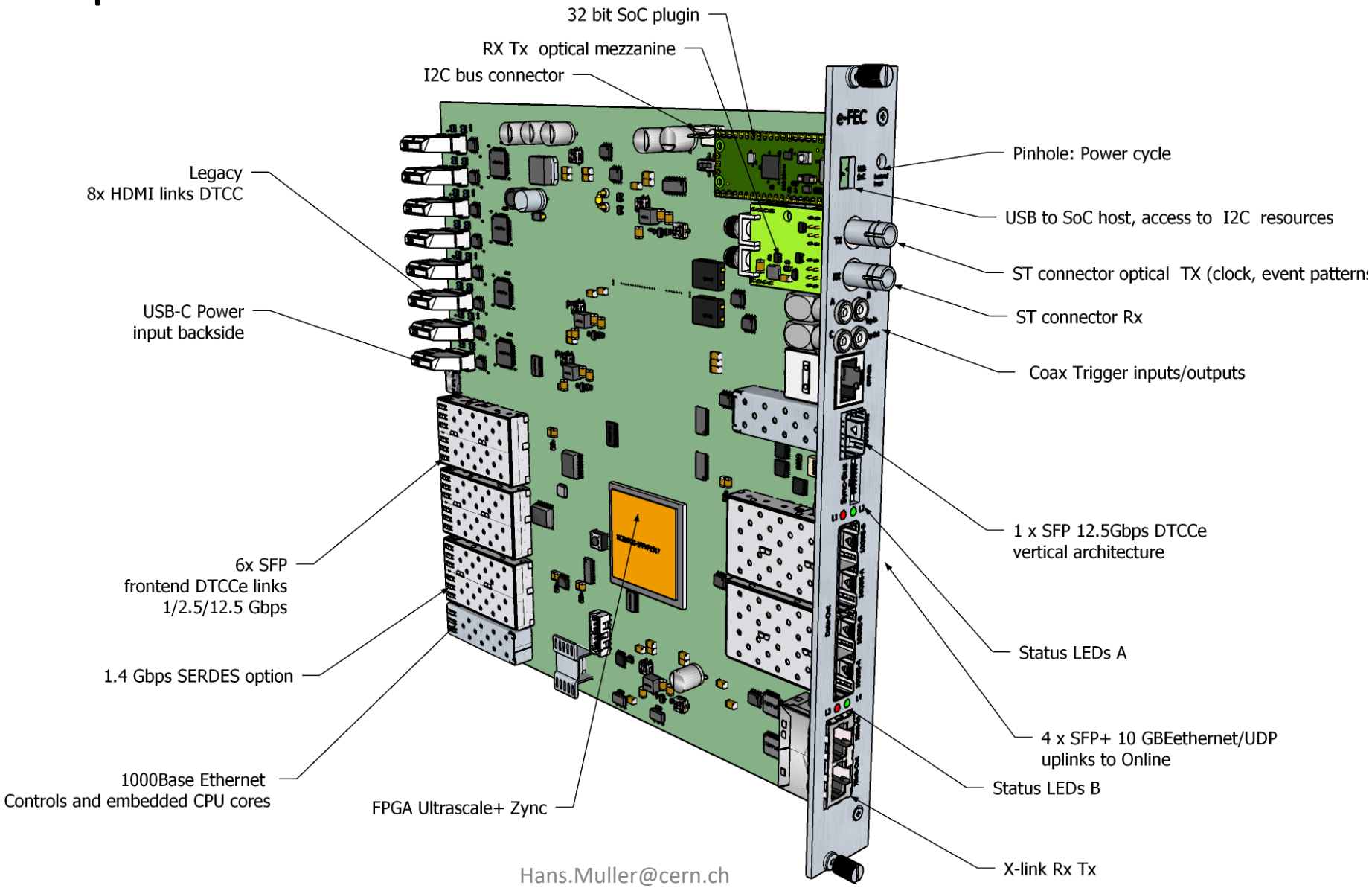
eFEC Triggers

- user tasks !

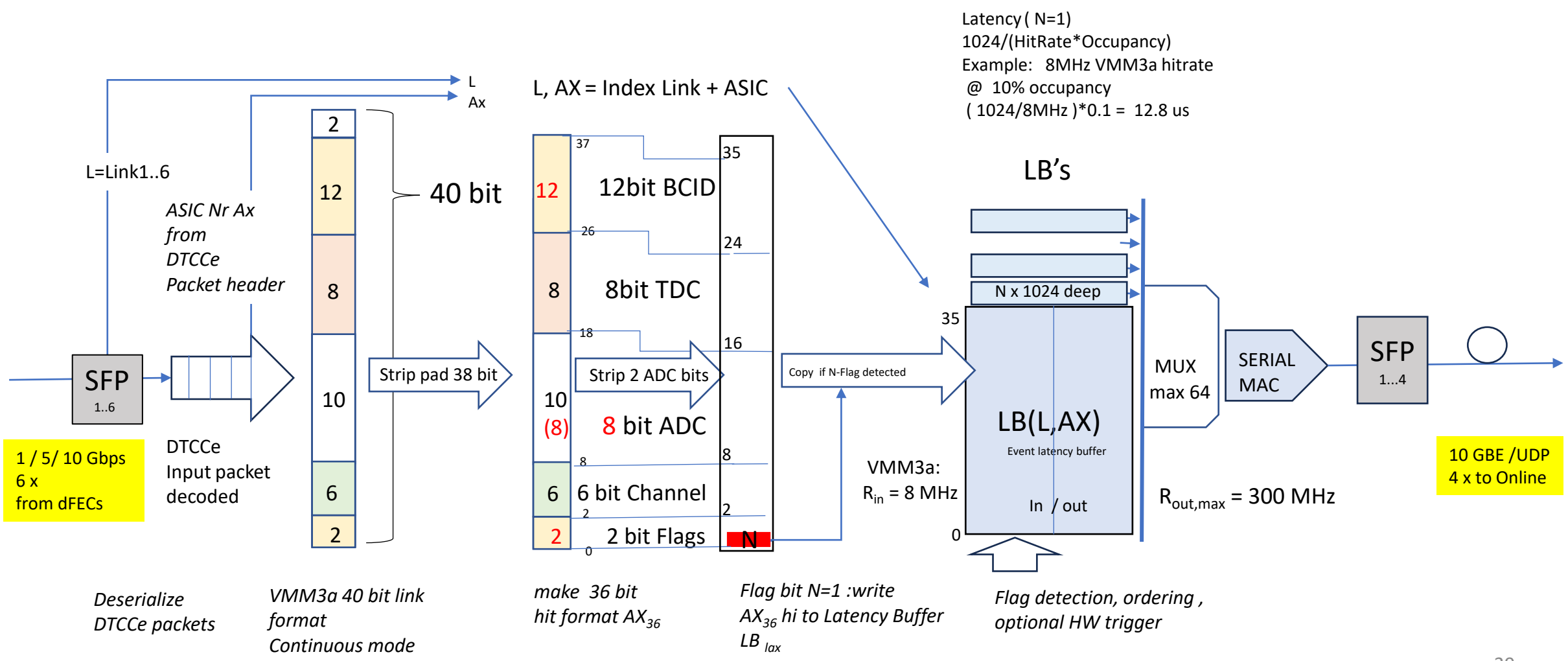
Interested teams: SRSe meeting to discuss tasks and resources planned for Jan 2024

Backup material

eFEC explained

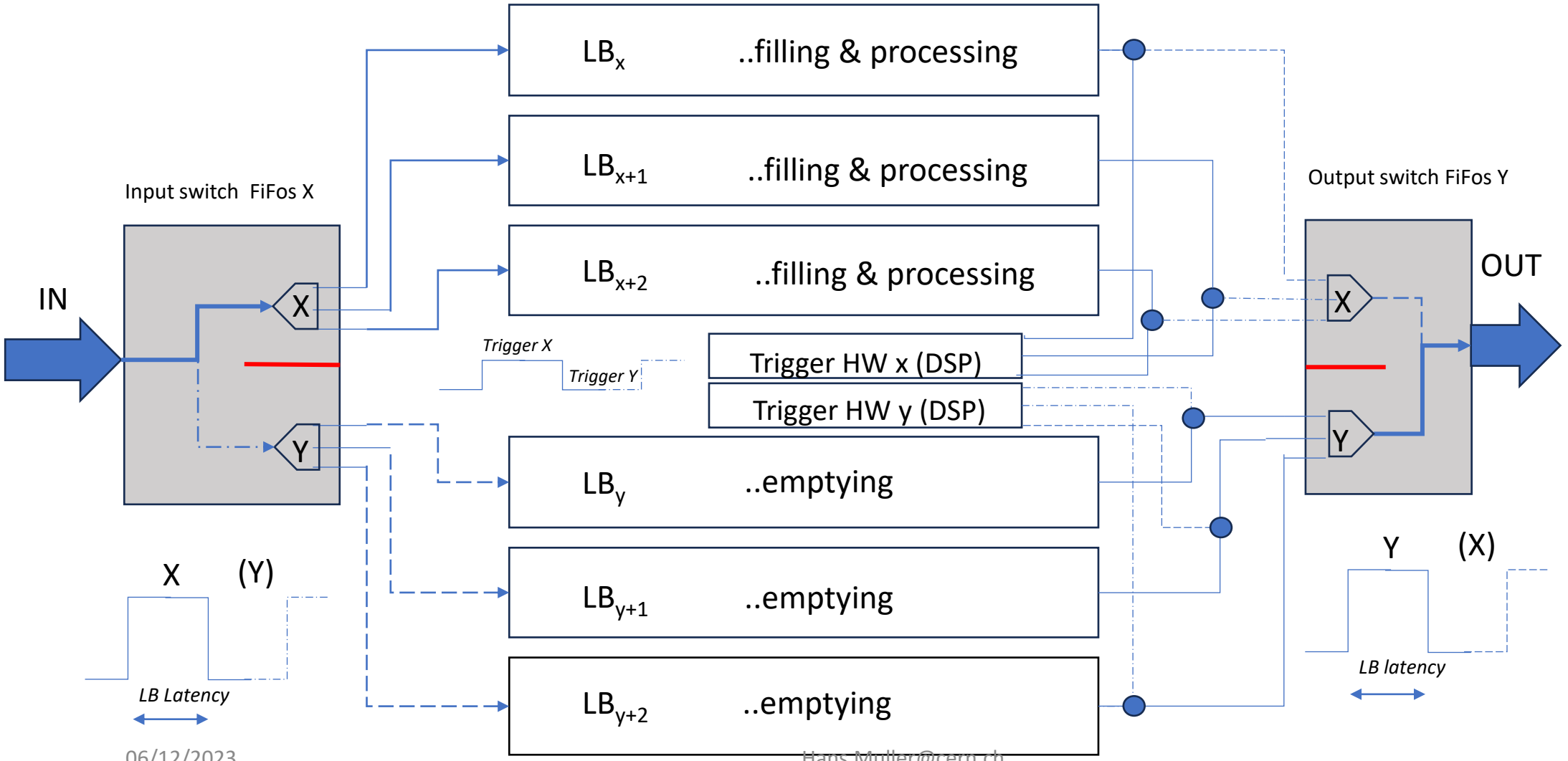


VMM3a ASIC mapping to LB buffer



In/Out ping-pong with LB buffers

“Ping Pong” In/Out with 2 LBs per ASIC



DTCCe packet headers (draft)

15 … 11	7 … 3	0
ASIC Index 0-31	**mode**	**Cnt/PCnt***	**Cmd**
xxxxx	mmm	0000	0000
xxxxx	mmm	0000 … 0001	0001
xxxxx	mmm	0000 … 1000	0010
xxxxx	mmm	0000 … 1000	0011
xxxxx	mmm	1111 * Cnt	0100
xxxxx	mmm	0011 , 1001	0101
xxxxx	mmm	0010, 1000	0110
xxxxx	mmm	0001	1000
xxxxx	mmm	0000 … 1000	1001
1010	1010	1010	1010
xxxxx	mmm .	0001	1011
xxxxx	mmm	0001	1100

4 more headers reserved

Msg. Power cycle Reset (-> frontend)

Msg Reload from Flash (-> frontend) + page select

I2C write (-> frontend) up 30 byte

I2C read (-> frontend->b.end) up 32 byte

Config data (-> frontend) (VMM 108 x16 bit)

frontend Hit Data (-> backend) ex. 40/80bit VMM

Msg. Evt. Count pattern (-> frontend) 16…64 bit

Msg. ext Trigger pattern (-> frontend) 16 bit

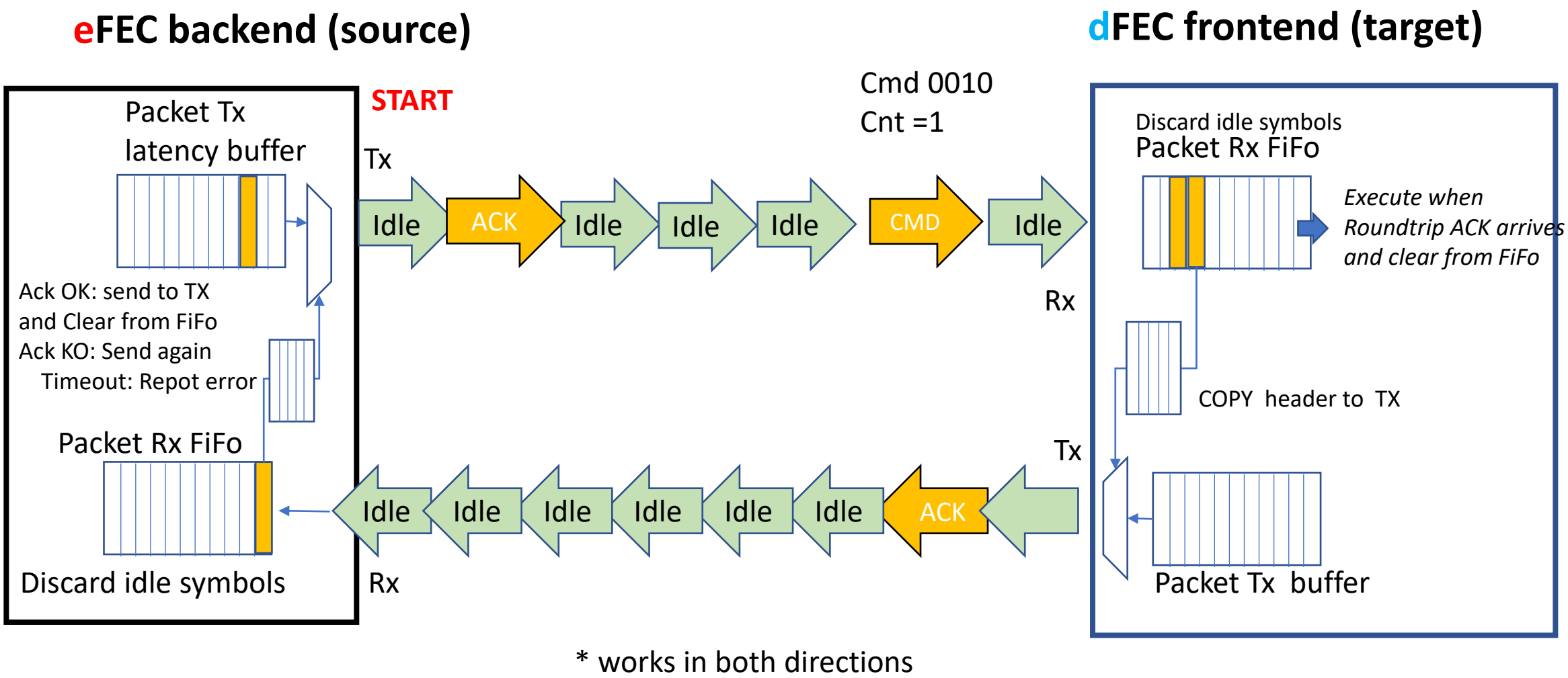
Msg. Time pattern (-> frontend) 16…64 bit

Unique IDLE symbol DTCCe

Msg. Error report (-> backend) 16 bit

Meg. FOR /ART Triggers (-> backend) 16 bit

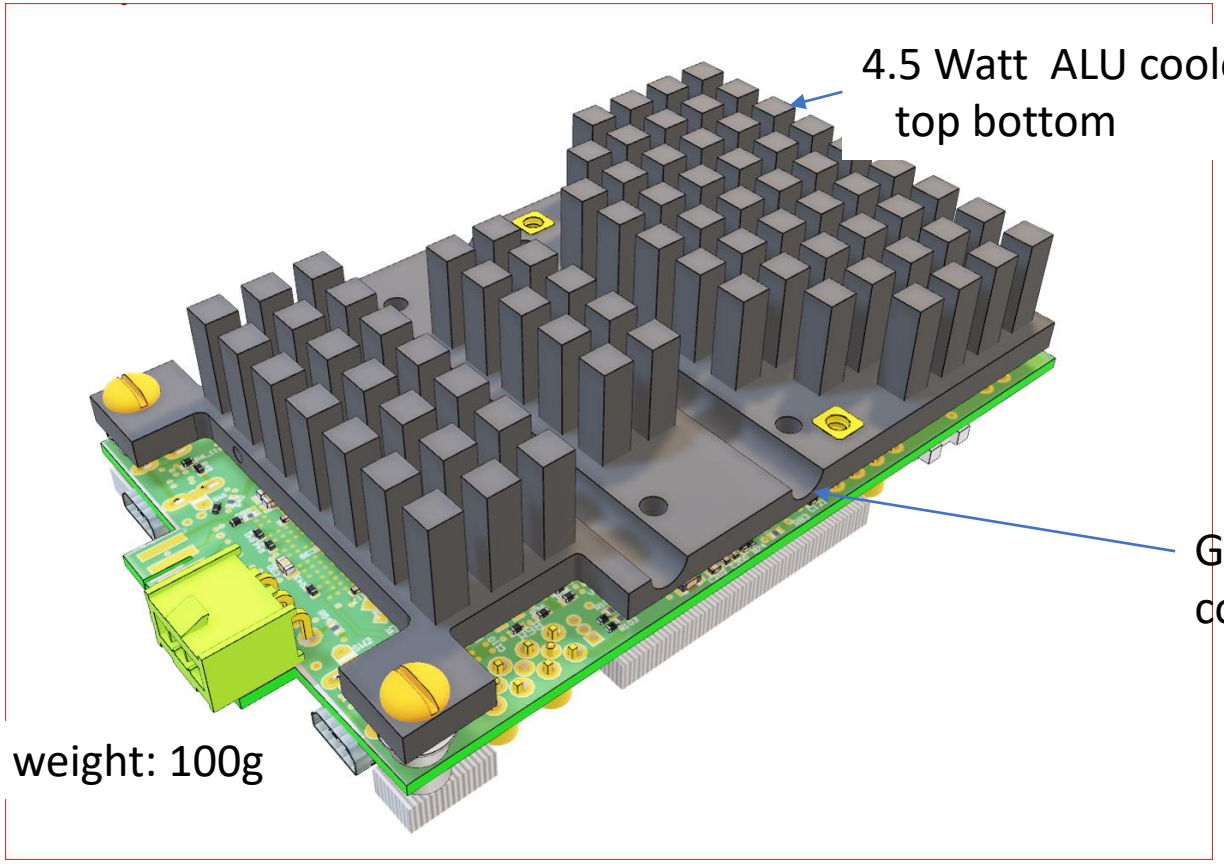
Messages over DTCCe*



* works in both directions

ASIC carriers with cooler

VMM hybrid for SRS* , 128 channels, 2 VMM3a ASICs, 100g, 4Watt, plugs directly to a MPGD gas or photon detector with 140 pin HRS connector. Multipurpose ALU cooler (convection / water pipe) to keep die temperatures below 55 C for long lifetime and low noise. HDMI readout link to DVMM card via micro HDMI-AD cable. 3-Pin AUX power connector for P1 (+3.3V) and P2 (+1.8V). PCB Edge connector for Jtag and I2C. Two 3 pin connectors access to analogue VMM signals (shaper , baseline etc)



* latest revision V5, 2022+