12bit Dynamic range SiPM readout with VMM3a at Focal test beam – Hardware Presentation

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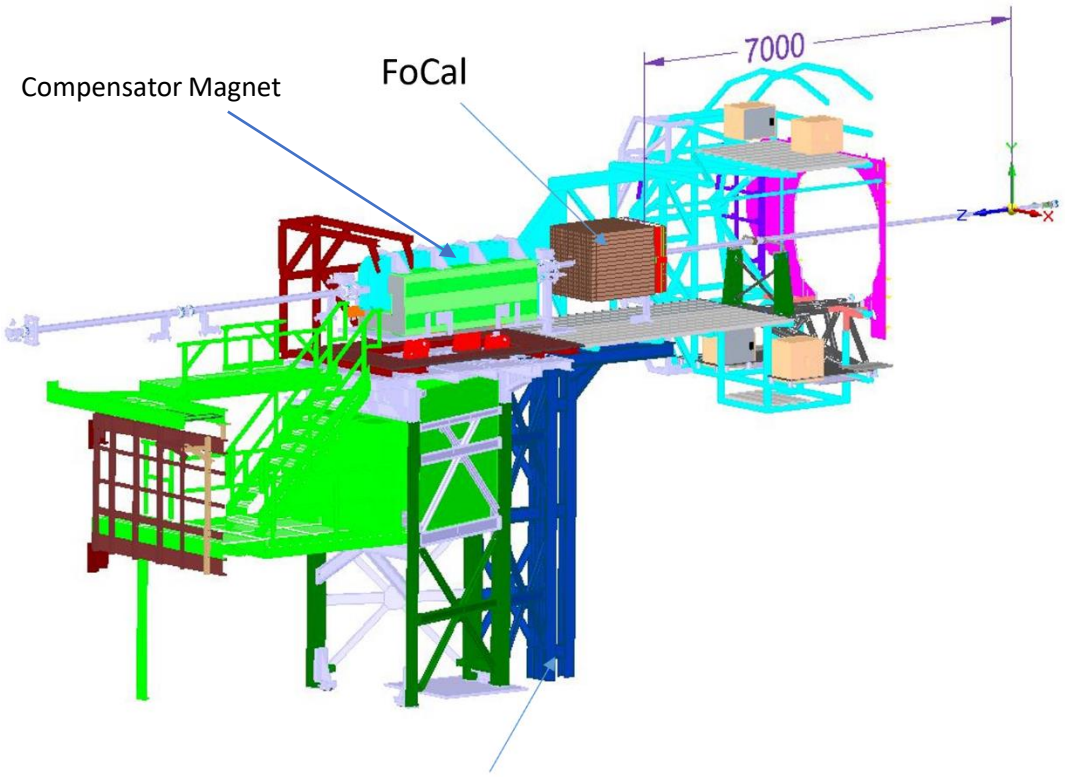
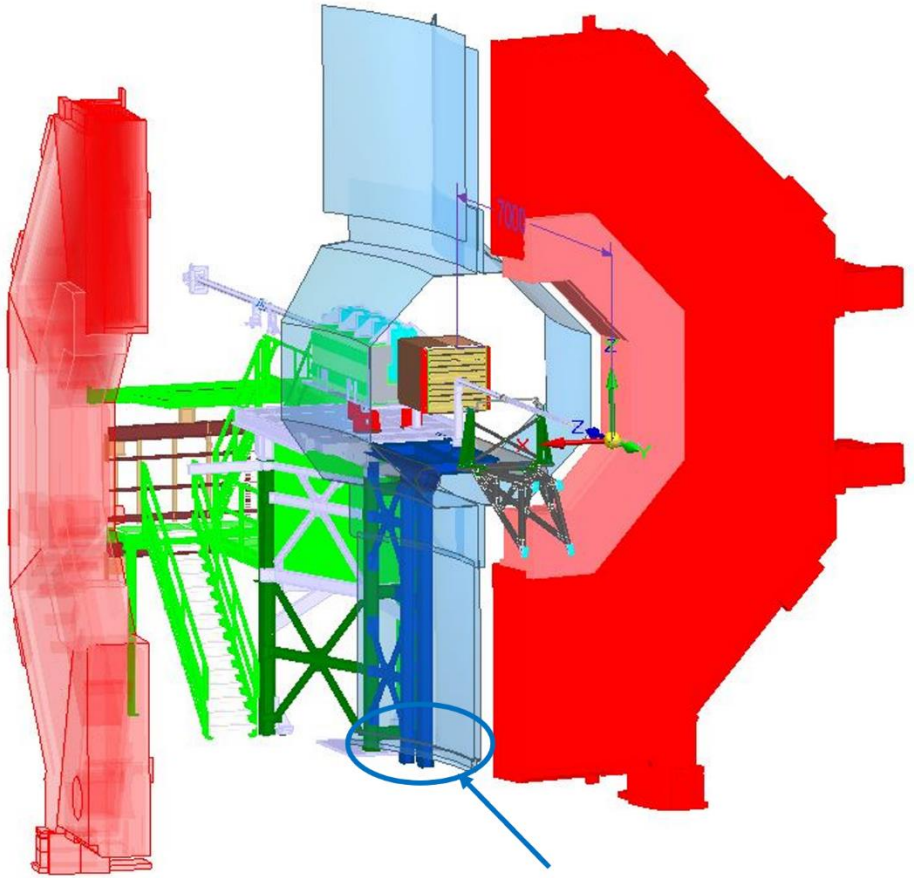
RD51 Collaboration meeting WG5
06/12/2023

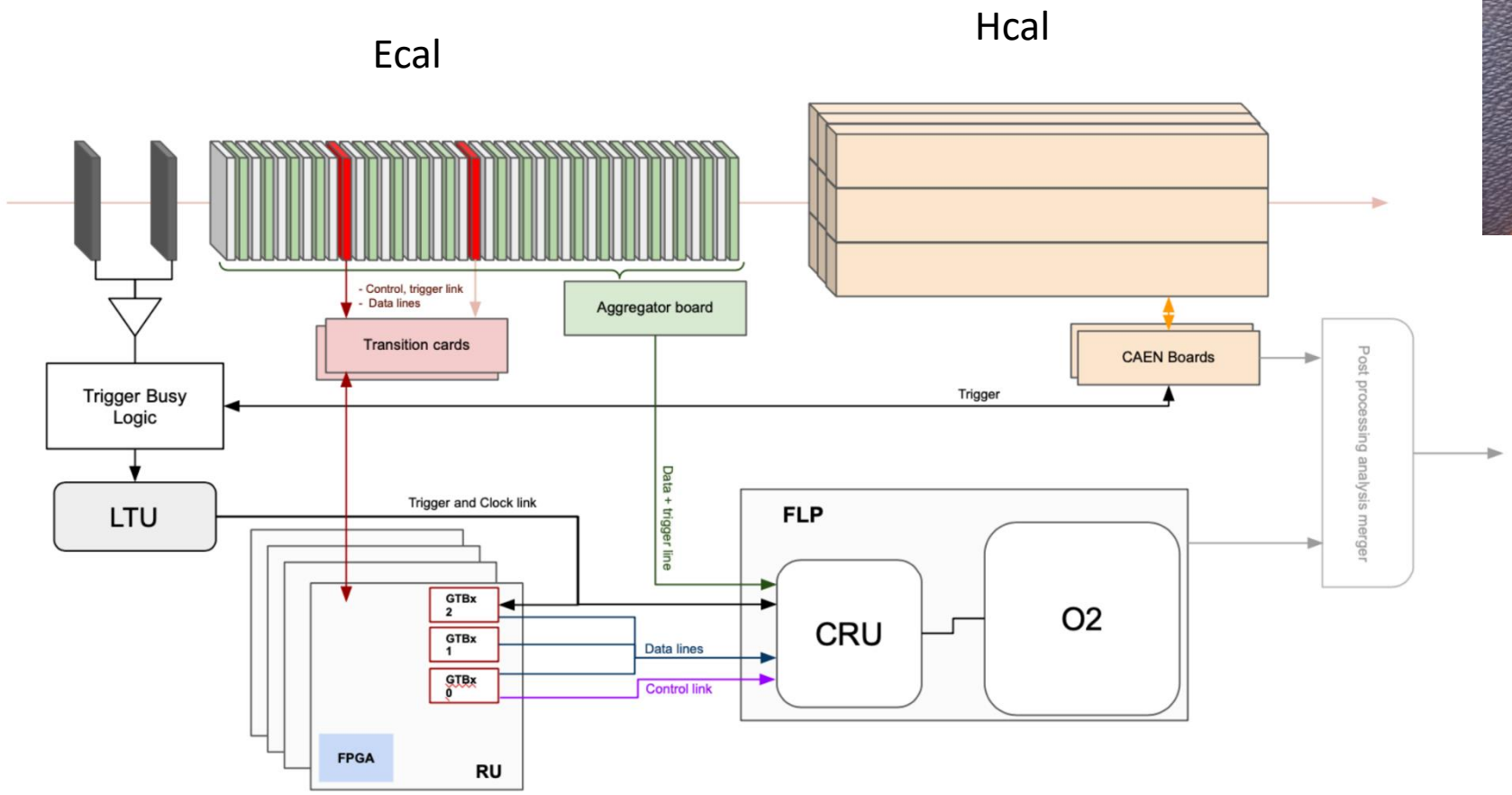
Installation of the Focal outside the ALICE L3 Magnet

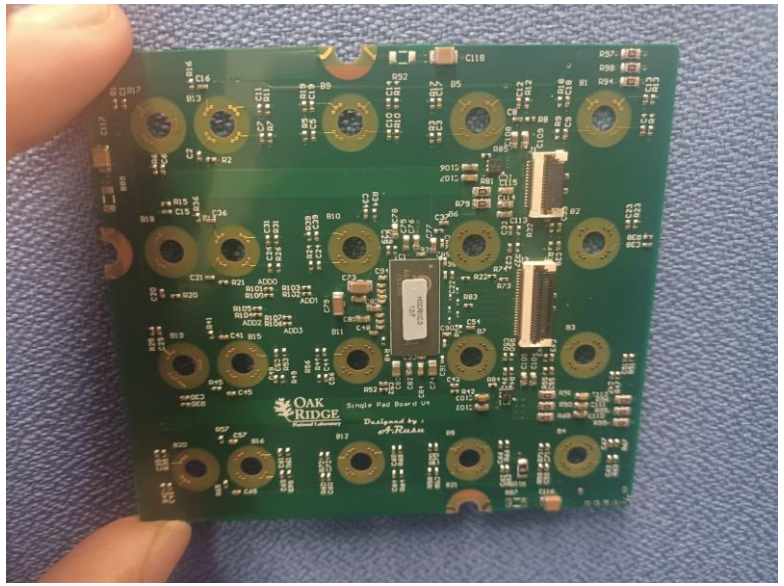


FP-10001



Test beam setup for 2023





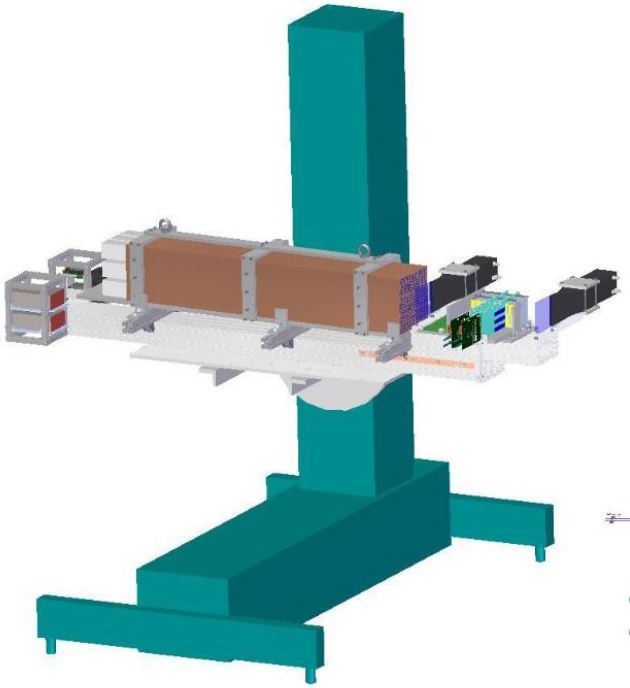
Ecal Pad detector Front End Card V4 based on HGCROC V3 HD chip. 0.5mm Thickness PCB

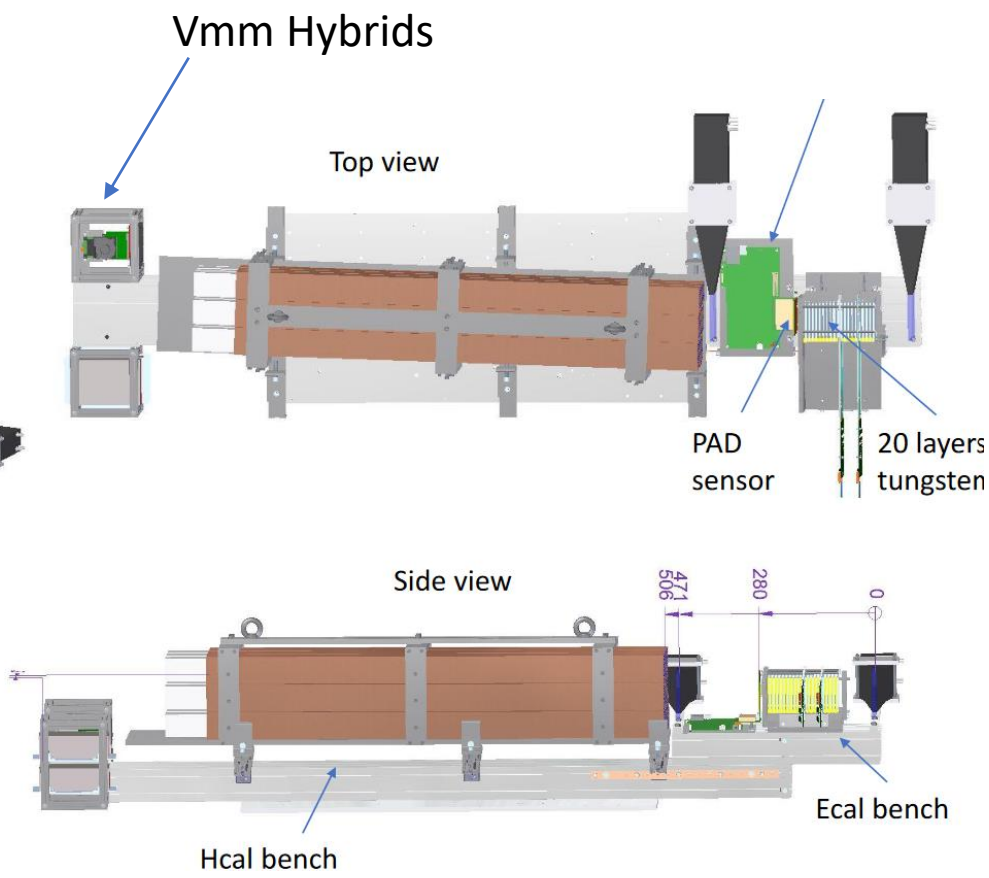
Ecal module consist of 20 converter/detection layers.

18 layers consist of 5 pad sensors 9x8 cm2 each

2 layers the 5th and the 10th are replaced by MAPS layer each consisting of 15x6 Alpide pixel sensor chips.

Hcal – 3D Representation with VMM Set-up at the test beam





Thanks to Ton for the 3D

Focal H

Each module is 6.5x6.5 cm2
Consist of 668 Cu 110 cm capillary tubes.
Each tube has 1mm BC412 fiber.

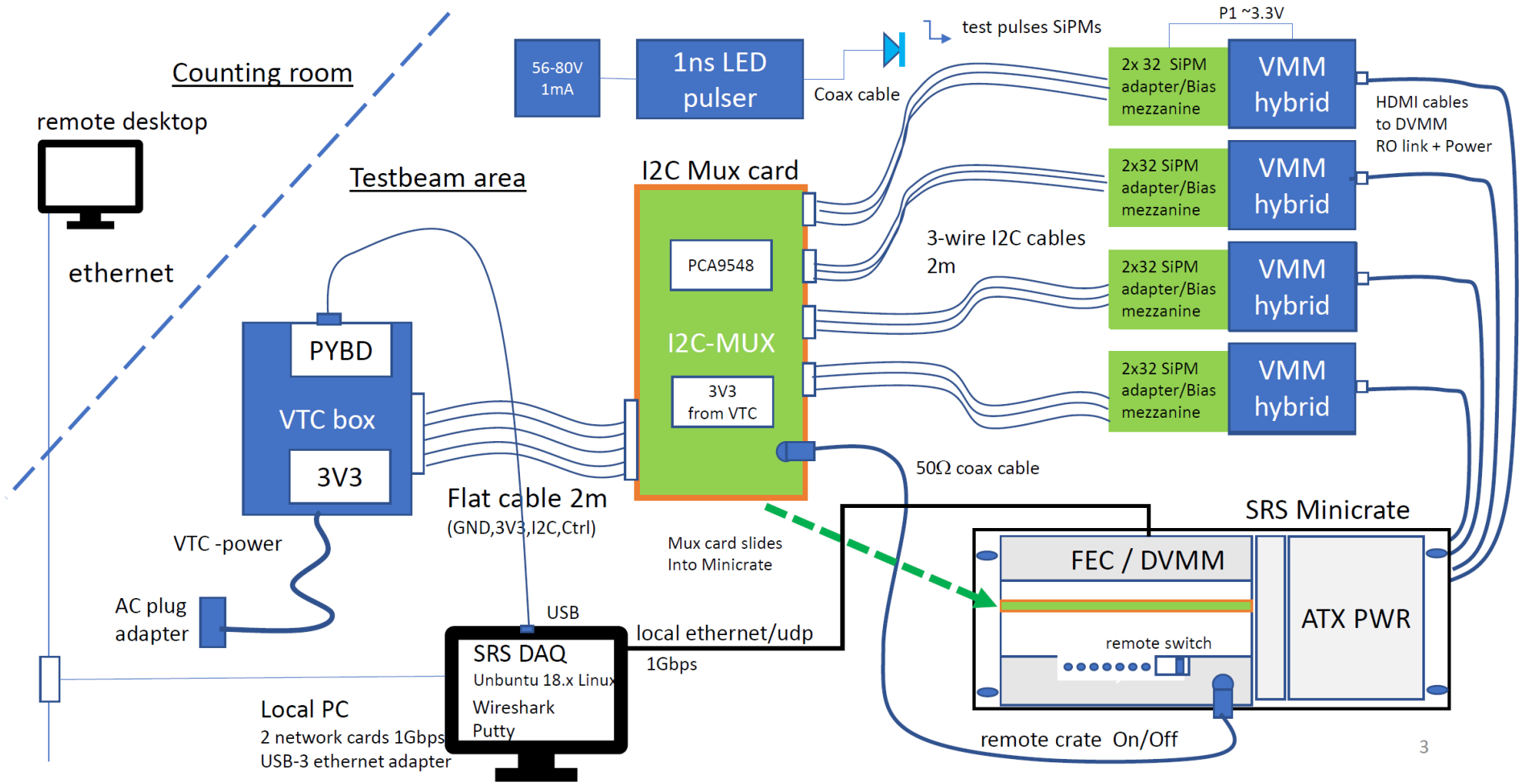
9 modules
Inner module 7x7 SIPM array
Outer module 5x5 SiPM array

192 pieces of Hamamatsu SIPM's (S13360-6025)

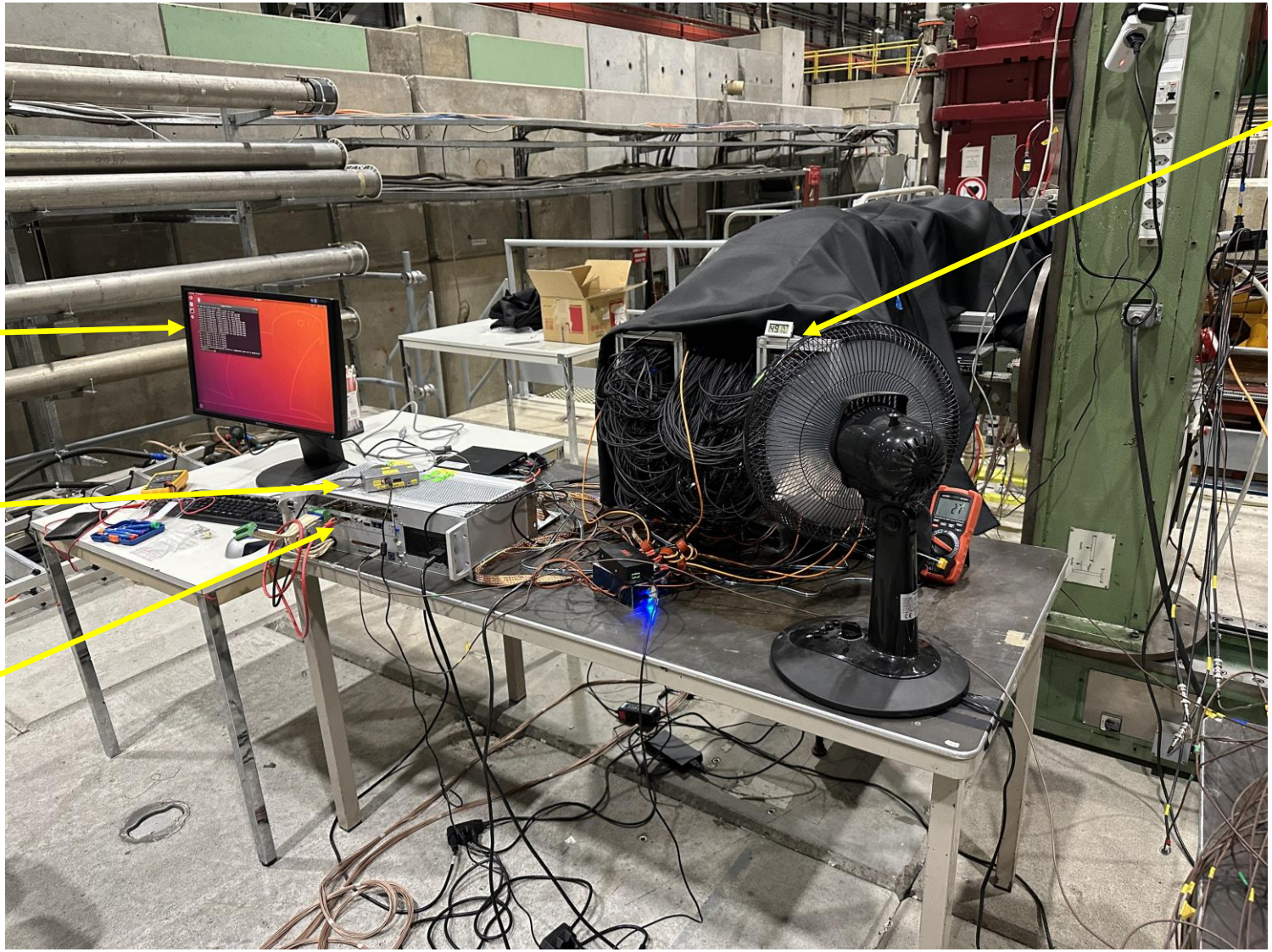
Every time the detector is moved the SIPM's are removed to avoid damage since they are not permanently fixed.

SRS set up at the test beam at CERN SPS

Remote DAQ + SiPM Bias / Crate control



SRS set up at the test beam at CERN SPS



VMM SIPM Adaptor V1

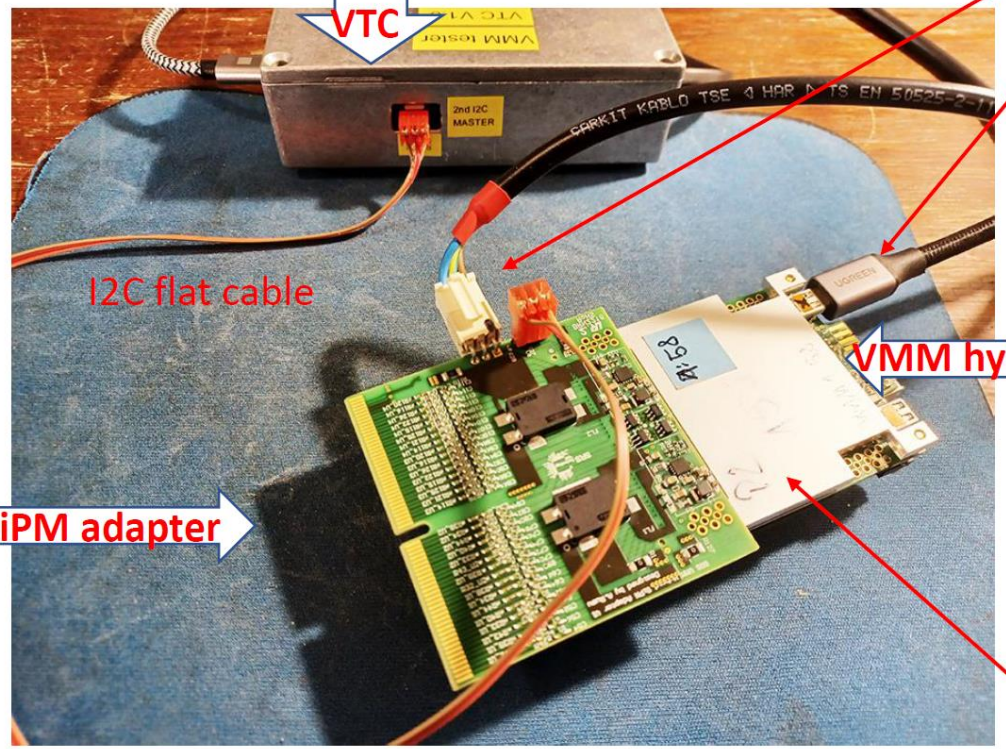
SiPM Adapter V1 (2022) 64 channel High Gain

+3.5V from P1 VMM

edge connector to Focal-embedded SiPMs

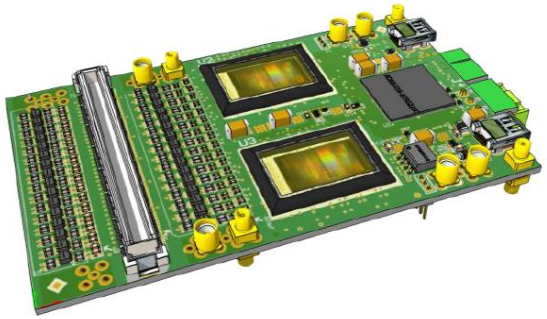
2x 32 SiPM adapter
HRS connector VMM (below)
I2C controlled Bias Voltages 0-75V via 2 x DACs

I2C master (VTC test box with USB and uPython SoC)



3.5V adapter supply cable from VMM

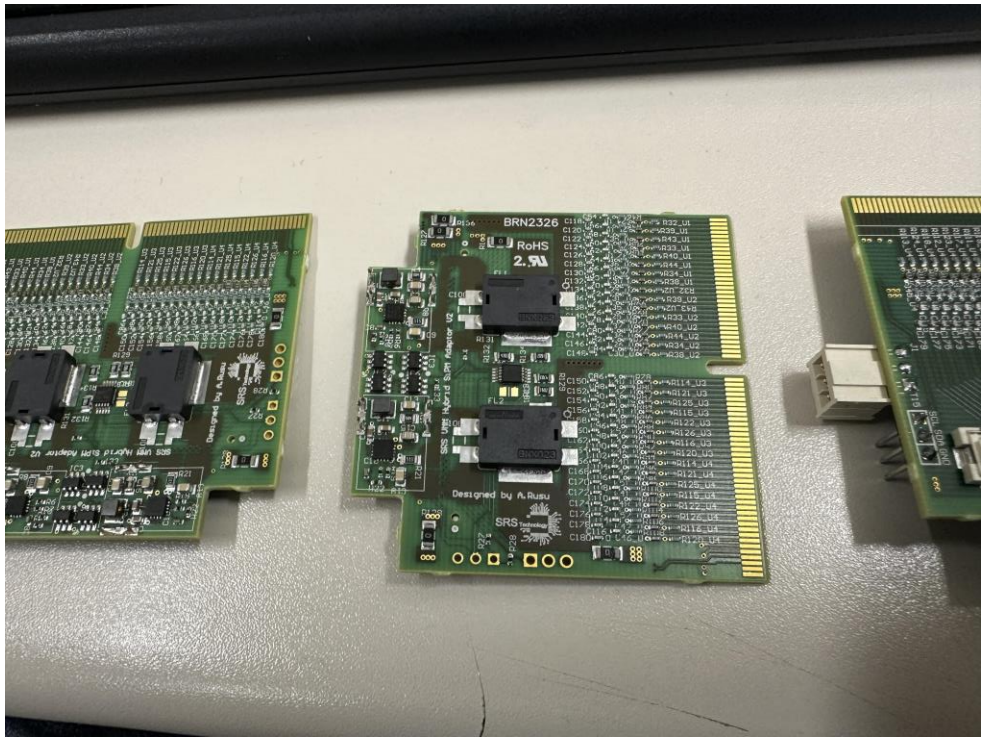
HDMI cable to SRS backend crate



SRS VMM hybrid
140 pin HRS connector
HDMI RO link, AUX power
2x VMM3a ASICs 64 ch.

bottom VMM cooler plate

VMM hybrid Sipm Adaptor V2

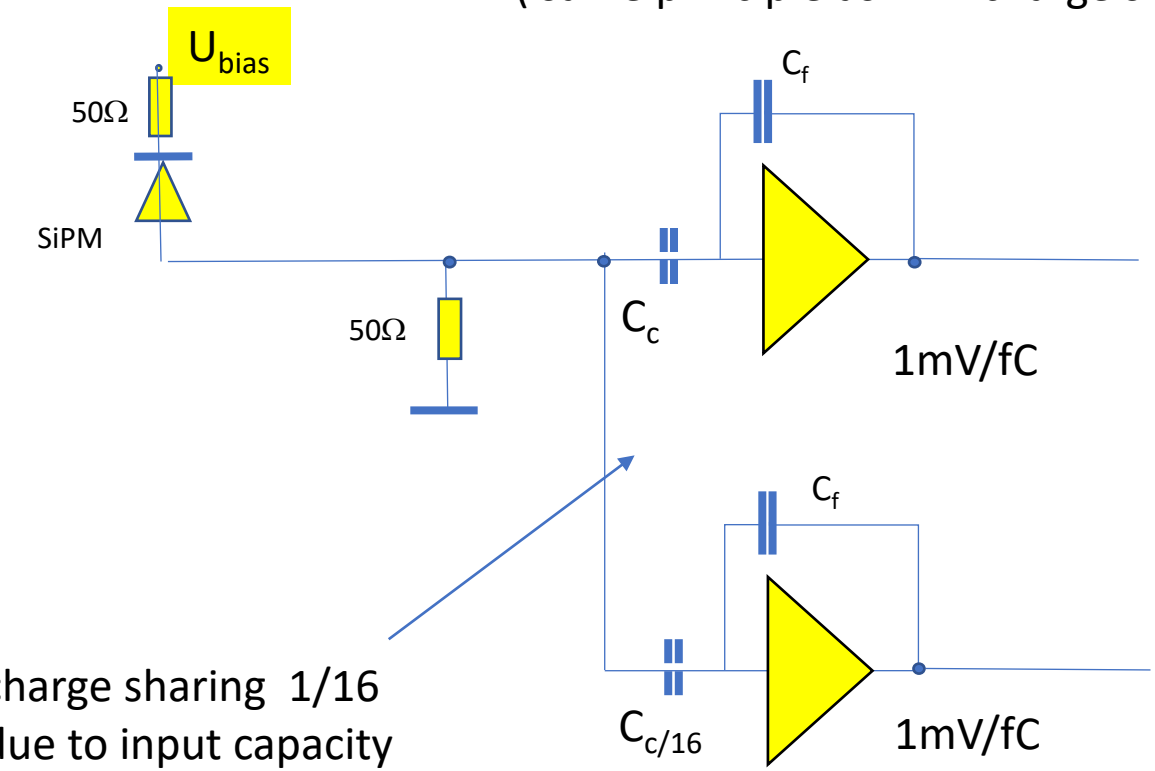


- The adaptor was designed and produced during summer and made ready for the fall 2023 SPS test beam.
- Implemented an ADC to read the voltages and current consumption of the Bias Voltage.
- Added power and I2C on the Hirose connector.
- Implemented the HG and LG by connecting all 128 channels to the VMM hybrid inputs.

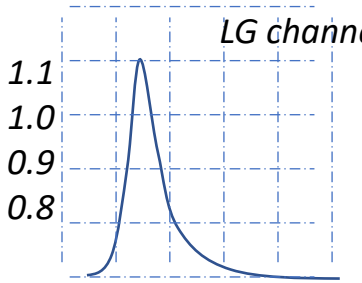
Dynamic range extension (factor 16) with VMM

Dual gain charge amplification: one SiPM channel C-coupled to 2 VMM channels with charge sharing 1/16

(same principle as APD charge sharing in EMCal)



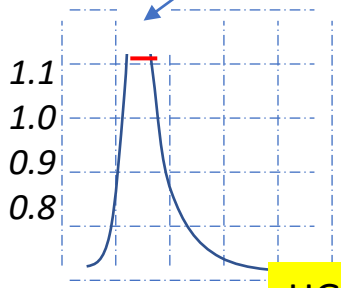
charge sharing 1/16
due to input capacity
ratio 1:16 on same input
Impedance



LG channel non saturated until ~ 1.1V

Low gain

HG channel saturated ~ 1.1V

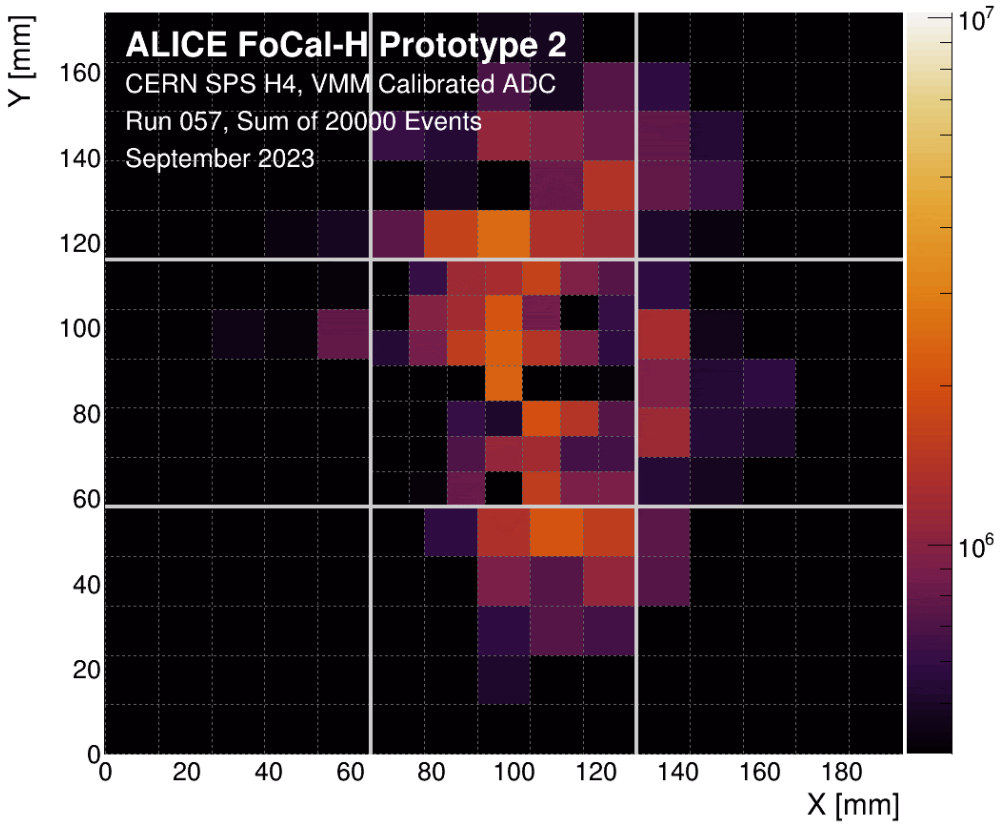


High gain

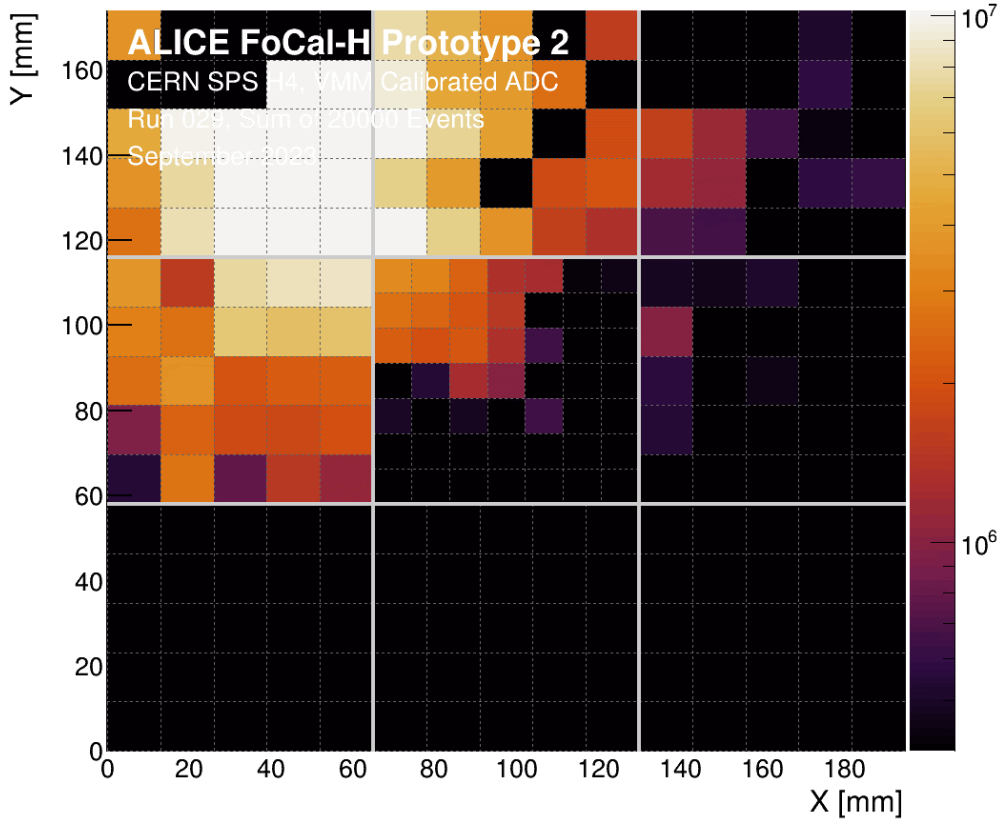
HG reaches dynamic range limit @ ca 1.1V
LG channel factor 16 more headroom
effectively increased dynamic range +4 bits

Thanks to Shihai for the gifs

60 to 350 GeV



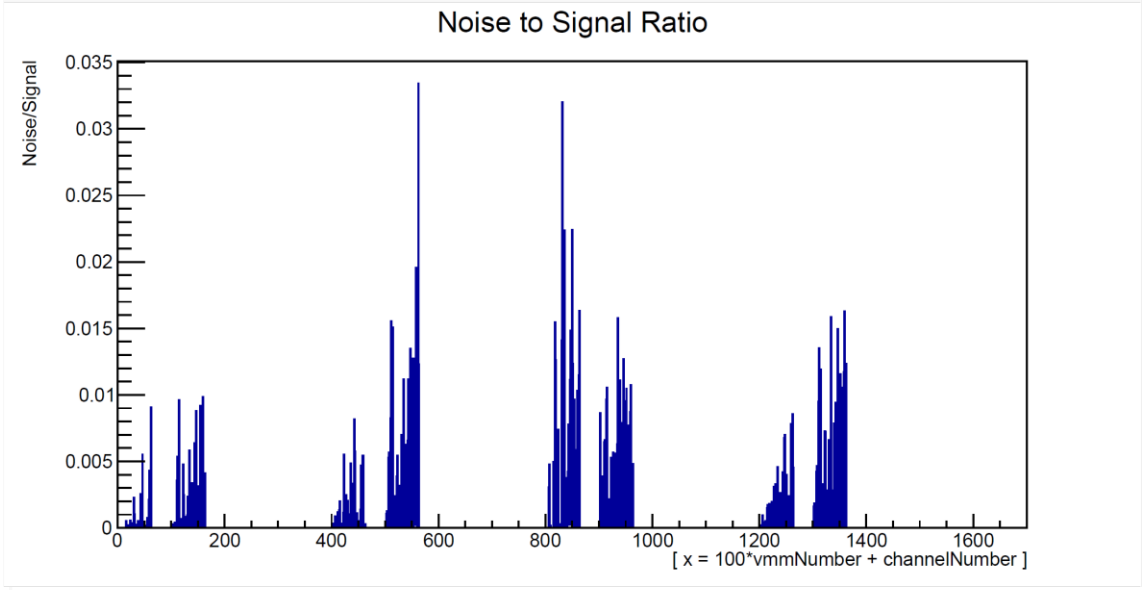
Energy Scan

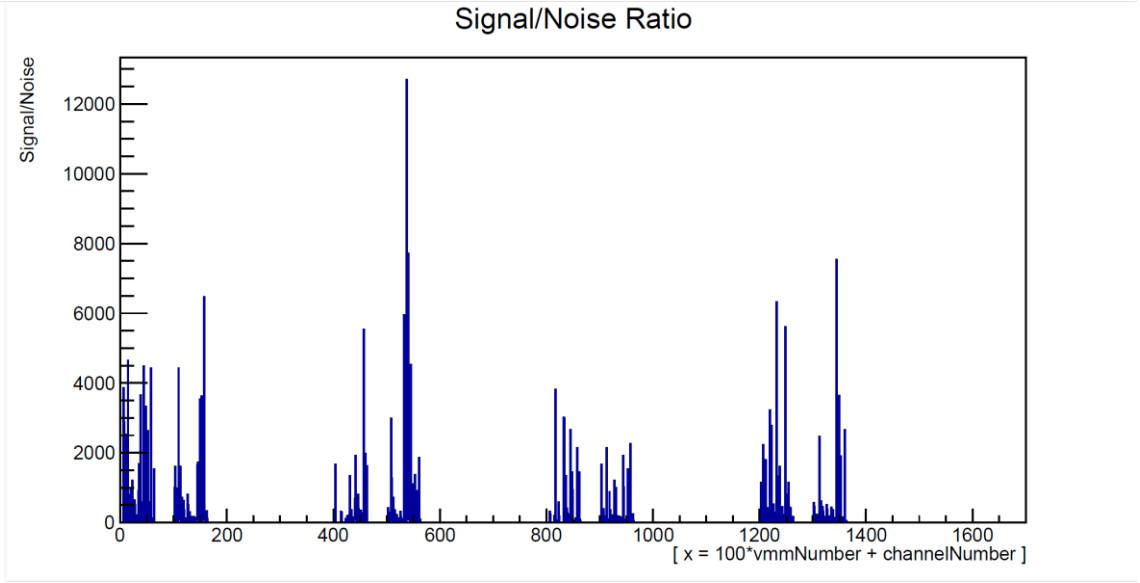


Position Scan

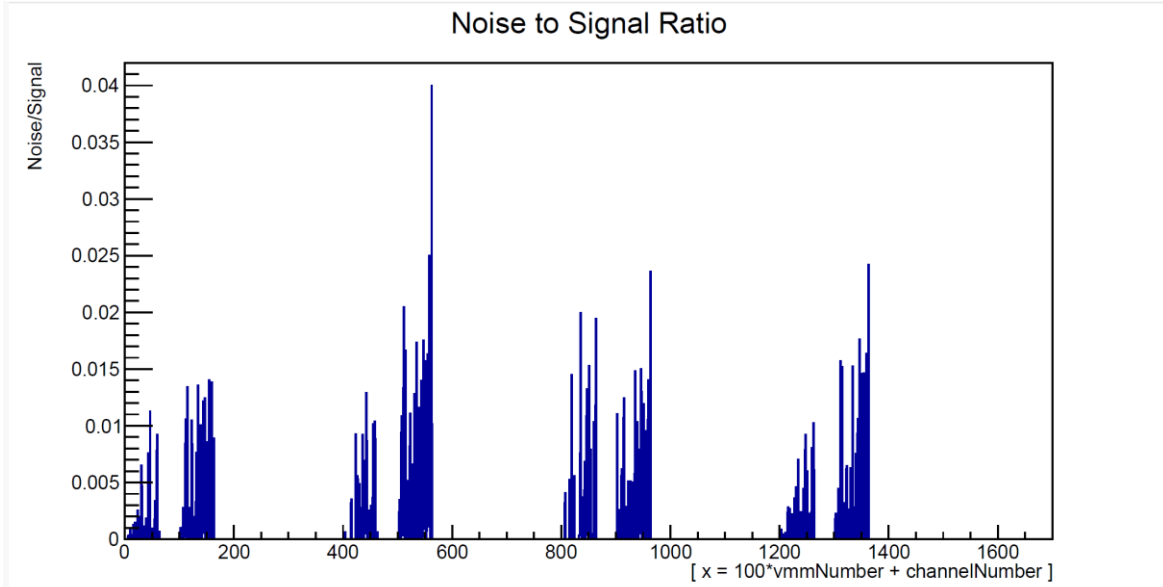
Dark spots within the Beam are from masked channels due to noisy SiPM's

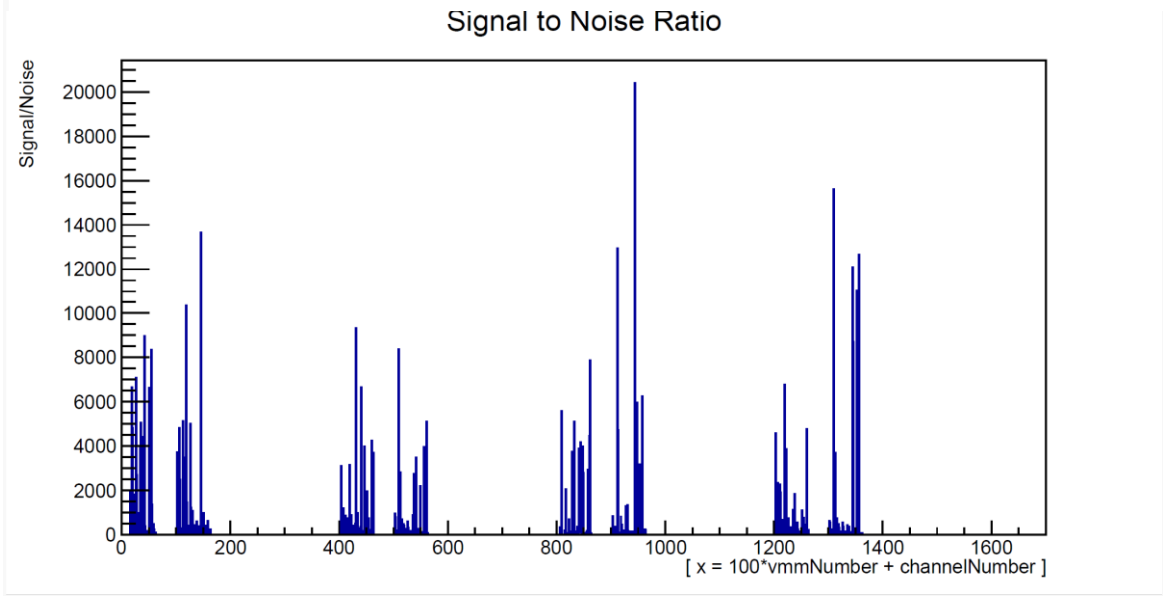
60Gev Power to VMM Hybrids from DVMM with bias 56.7V



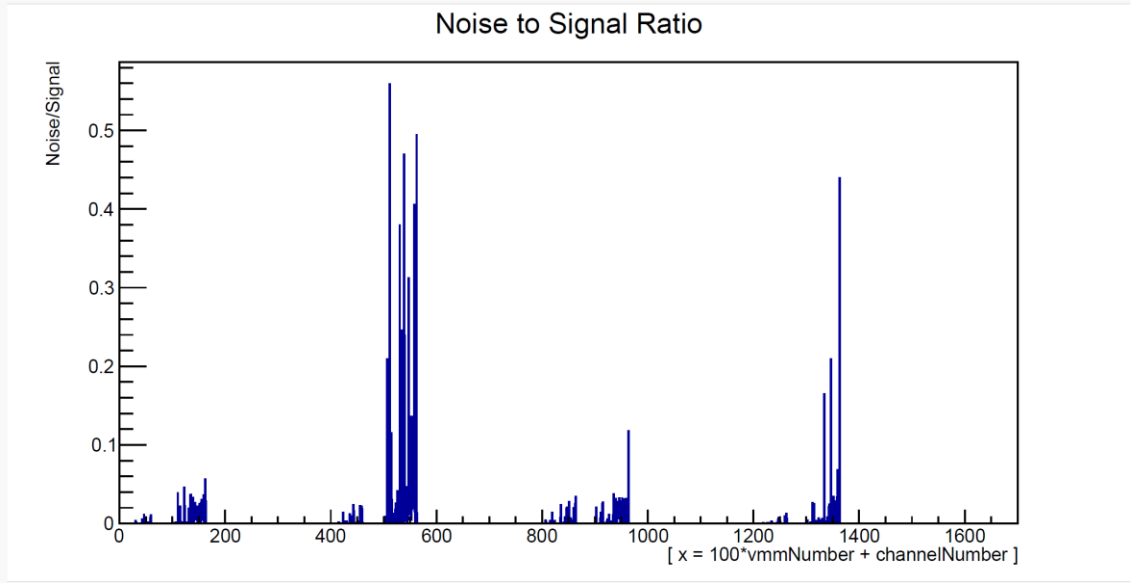


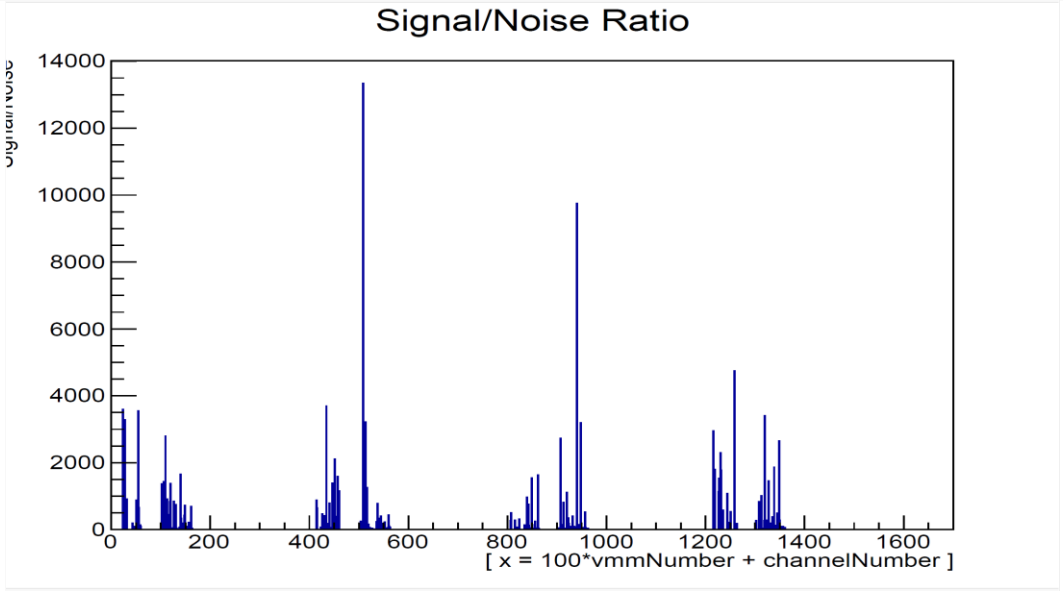
60Gev Power to VMM Hybrids from PBX with bias 55.4V



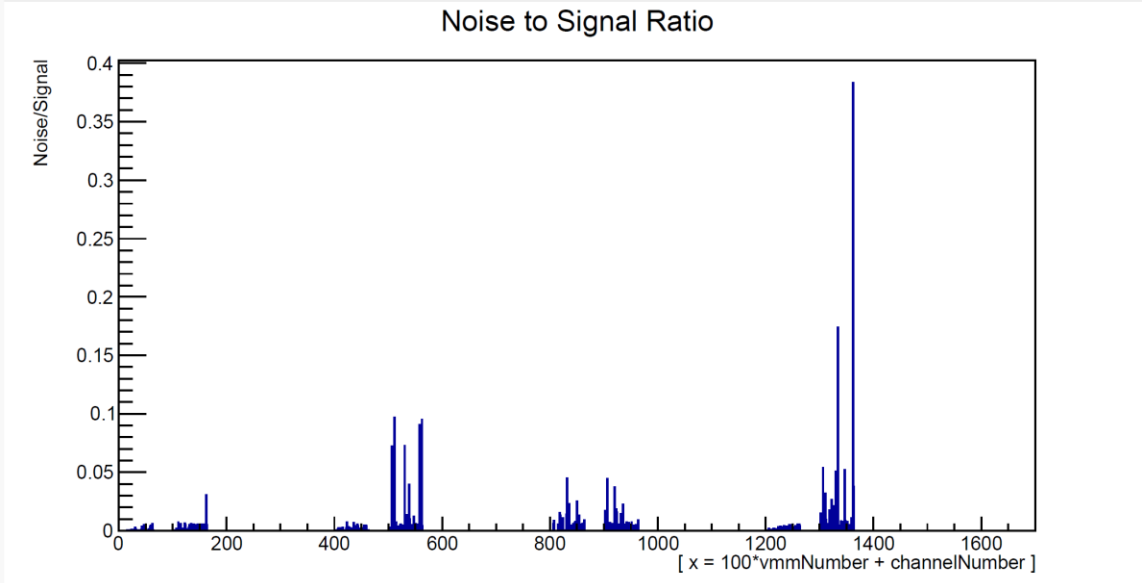


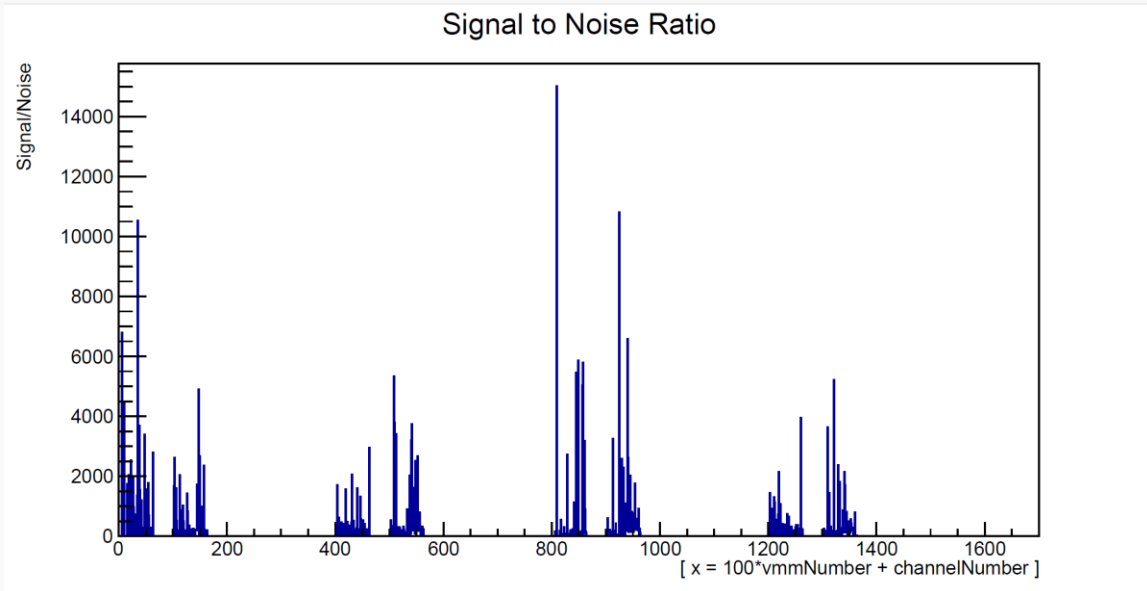
350Gev Power to VMM Hybrids from DVMM with bias 56.7V





350GeV Power to VMM Hybrids from PBX with bias 55.4V





Thanks to Valentin!

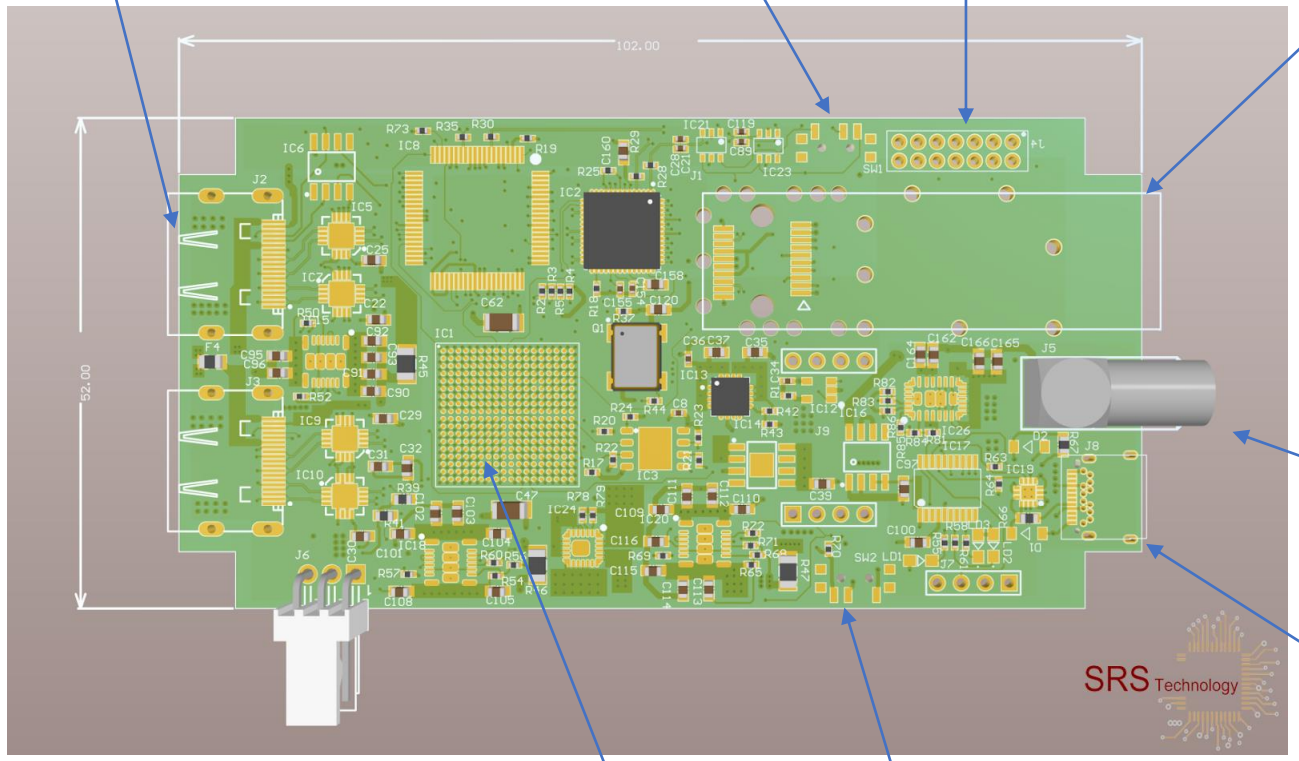
µRoc V1

2 Hybrids inputs plus power trough cable

Switch for Ethernet or SERDES protocol

Jtag

SFP for 1GBE fiber or copper



- After transporting mounting and unmounting the Mini-crate with all the cables at the test beam several times plus switching quickly between readout systems I was thinking how can one make life easier if for low channel detectors one could use a simplified readout architecture that is more portable.
- µRoc is a mini concentrator for the VMM hybrids very small 110x60 mm almost the size of the hybrids that can fit in the VTC box.
- The µRoc would be capable to read 2 VMM hybrids with the same HDMI connectivity and also provide LV power and Bias Voltage for the SIPM's.
- The output of the µRoc is done with Fiber SFP or Ethernet SFP at 1GBE.
- For several µRoc's one board will become the master and will distribute optically to the others the clock.
- Possibility to switch On/Off µRoc's and VMM's via Lemo connector by inserting a 50 ohm termination or via command in the slow control (needs to be implemented in the firmware)
- The power consumption for the uRoc and 2 hybrids is around 15W.

USB C Power

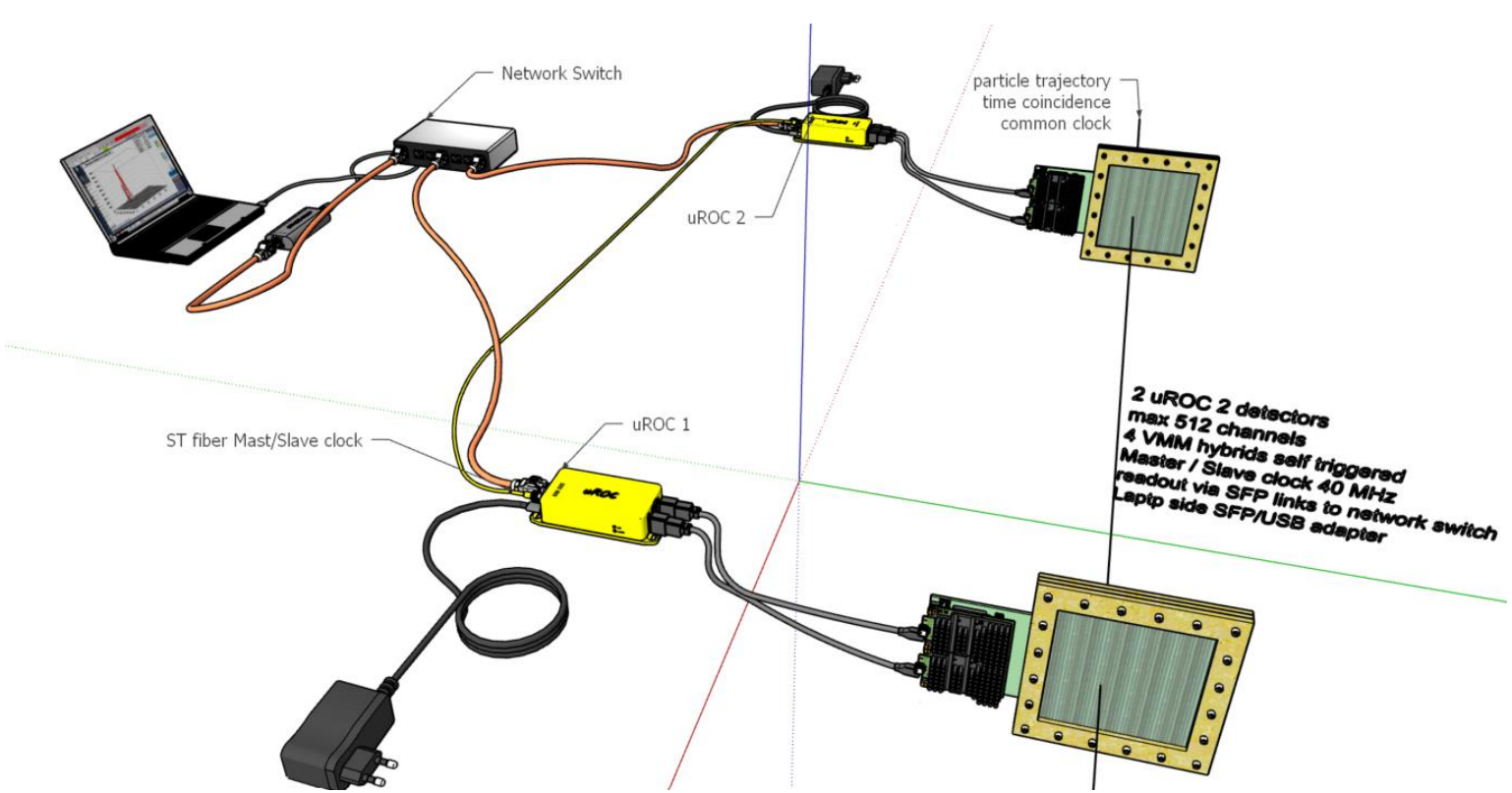
Output for the bias voltage

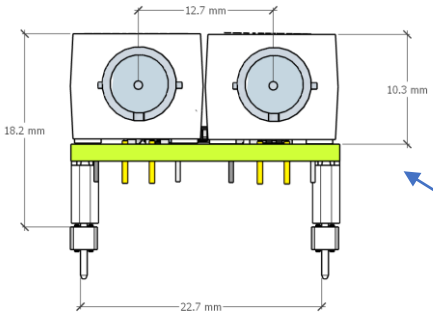
Artix 7 FPGA

Switch for online reset or manual with 50ohm termination

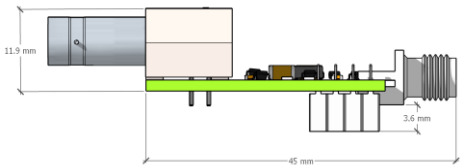
µRoc common clock distribution

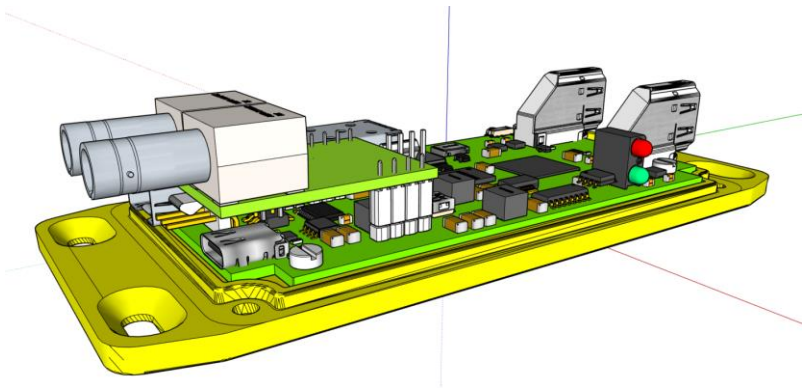
- The circuit was defined and design is ongoing





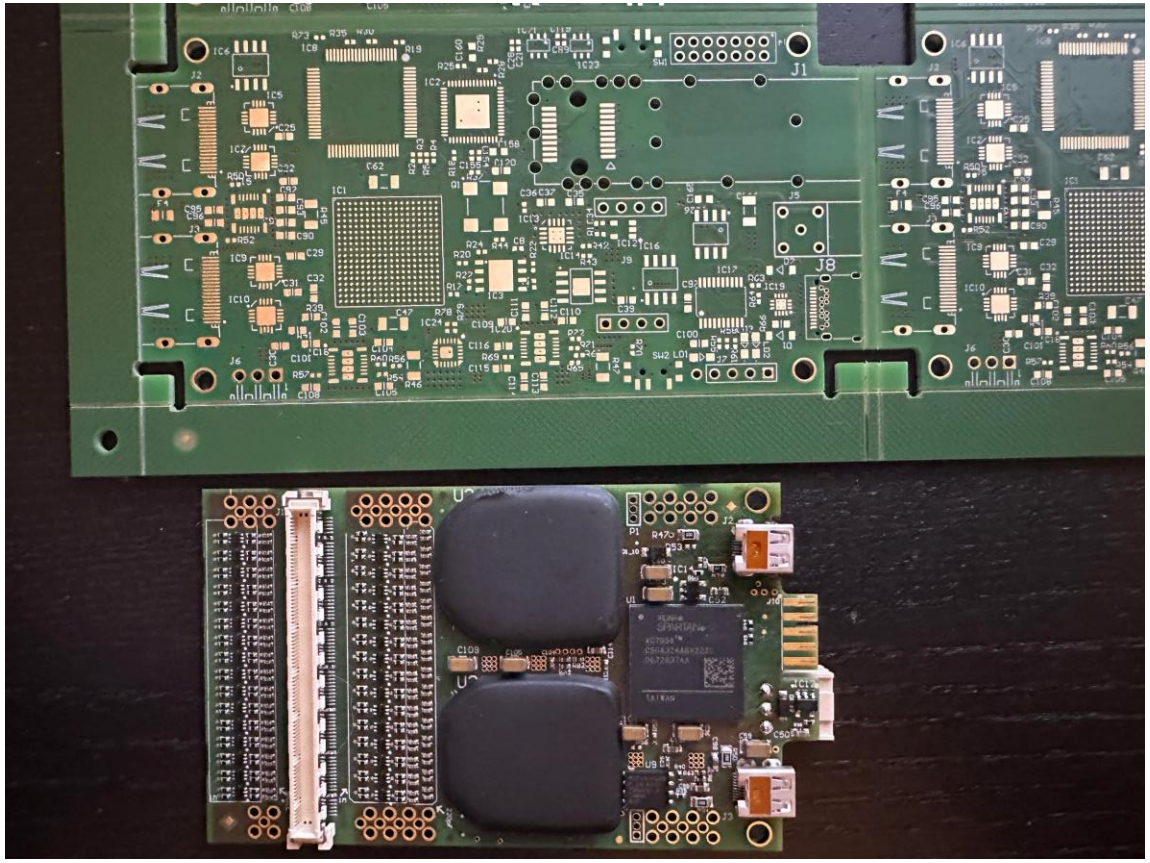
Roc Ck Mezzanine





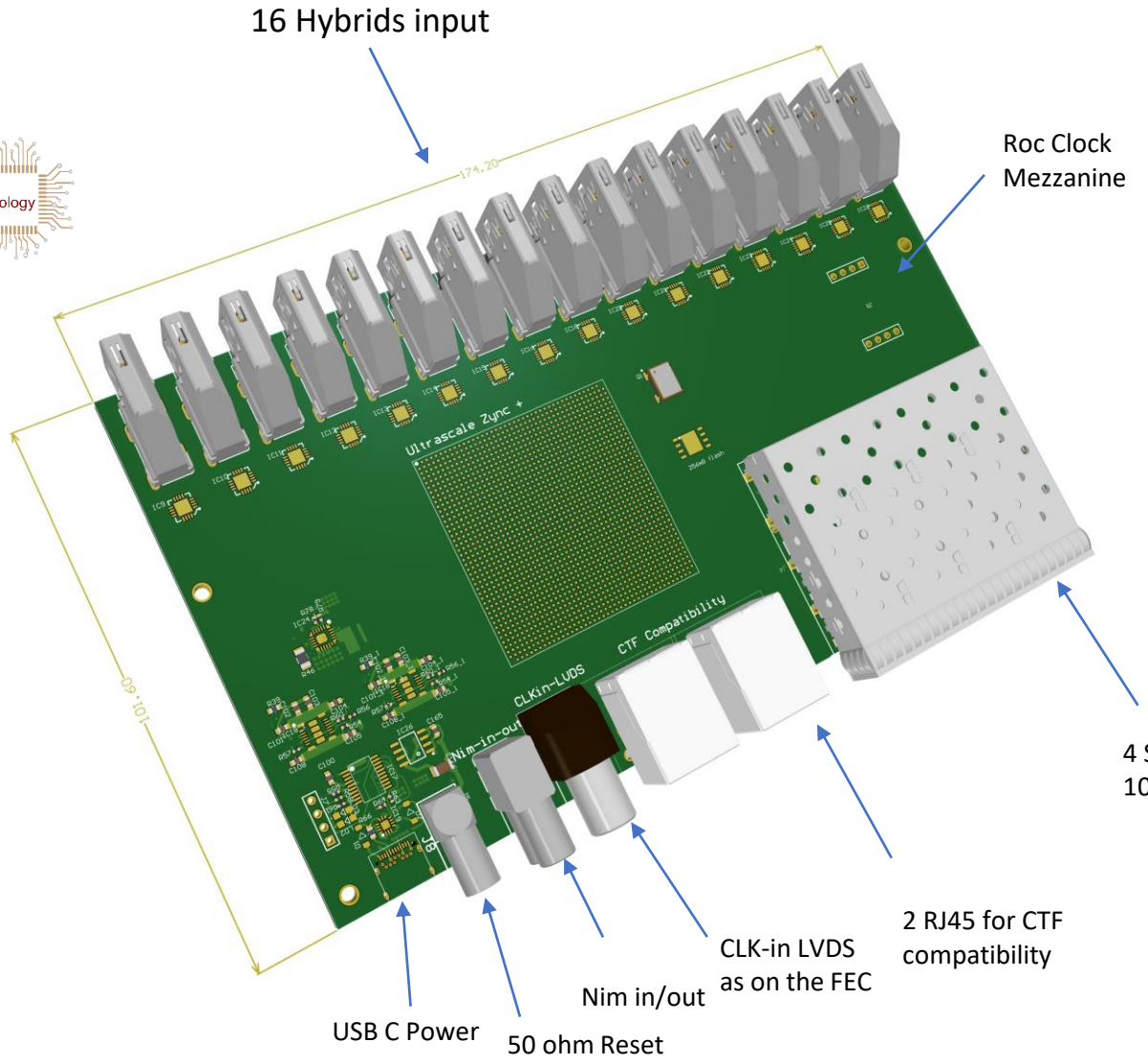
Thanks to Hans for the 3D representation

µRoc V1 Status



- In the photo one can see a size comparison between the VMM Hybrid V5.1 and the µRoc V1
- The 8 layer PCB has been produced and is currently in assembly process.
- The first 2 prototypes are expected by the end of the year 2023.

maxiRoc V1



- Similar to the uRoc the maxiRoc is a compact concentrator with higher number of channels.
- The maxiRoc features the powerful Ultrascale + ZU17EG that has 32 Transceivers of 16.3 Gb/s and 16 of 32.75 Gb/s much faster than the current FEC with Virtex 6 130T at 6.6Gb/s.
- For reading 16 Hybrids at 10 GBE it requires around 70k Slices (thanks to Doro Simulation) and the Ultrascale + has 423000 LUTs (1 slice à 8 LUTs)
- 926k Logic cells and 796 Block Rams.
- The board will be in smaller size 174x101 mm and it can be fitted in a box.
- The power comes from the USB-C.
- The maxiRoc will not power the 16 Hybrids. Power should be used from the PBX or external.
- The Roc Mezzanine can be plugged in for common clock.
- The CTF can be used for common clock.
- The design has started.
- First prototypes are expected in Spring 2024.

Thank You !